

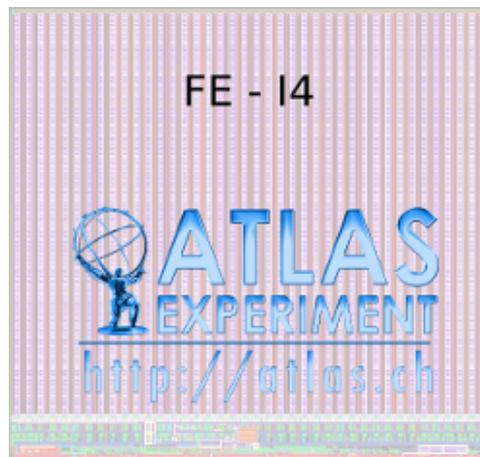
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The FE-I4A Integrated Circuit Guide

FE-I4 Collaboration

ABSTRACT: Detailed reference of the FE-I4 integrated circuit

KEYWORDS: ATLAS, LHC, sLHC, Upgrade, Pixel detector, Insertable B layer, CERN.



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1. Introduction

The FE-I4 integrated circuit contains readout circuitry for 26 880 hybrid pixels arranged in 80 columns on 250 μm pitch by 336 rows on 50 μm pitch. It is designed in a 130 nm feature size bulk CMOS process. The letter “A” in FE-I4A refers to the first fabrication run and will be generally omitted unless describing a specific feature peculiar to this run. Sensors must be DC coupled to FE-I4 with negative charge collection. Each FE-I4 pixel contains an independent, free running amplification stage with adjustable shaping, followed by a discriminator with independently adjustable threshold. The chip keeps track of the firing time of each discriminator as well as the time over threshold (ToT) with 4-bit resolution, in counts of an externally supplied clock, nominally 40 MHz. Information from all discriminator firings is kept in the chip for a latency interval, programmable up to 255 cycles of the external clock. Within this latency interval, the information can be retrieved by supplying a trigger. The data output is serial over a current-balanced pair (similar to LVDS). The primary output mode is 8b/10b encoded with 160 Mb/s rate. The FE-I4 is controlled by a serial LVDS input synchronized by the external clock. No further I/O connections are required for regular operation, but several others are supported for testing.

The many details behind the simple introduction given above are collected in this document. Many of the specifications and features of FE-I4 have been derived from the FE-I3 chip used in the ATLAS pixel detector [4] and a familiarity with FE-I3 will be a useful point of reference to complement this document. This note is intended to both document the chip design and serve as a users’ guide for operation. The reader interesting in learning about the design should focus on sections 2–5 and 11, while the reader trying to operate the chip should focus on 3, 6–10, and the appendices.

2. Specifications and Ratings

125 The ratings given in this section are separated into power supply, temperature and radiation. These are not recognized commercial or military ratings, but rather the results of ad-hoc tests, simulations, or estimates carried out to validate compatibility with design goals. It is assumed that further testing will be carried out to validate the use in each specific application, as needed.

Item	Value	Units
Pixel size	50×250	μm^2
Bump pad opening diameter	12	μm
Input	DC-coupled -ve polarity	
Maximum charge	100,000	e^-
DC leakage current tolerance	100	nA
Pixel array size	80×336	Col \times Row
Last bump to physical chip edge on 3 sides	≤ 100	μm
Last bump to physical edge on bottom	≤ 2.0	mm
Normal pixel input capacitance range	100-500	fF
Edge pixels input capacitance range	150-700	fF
In-time threshold with 20 ns gate (400 pF) ¹	≤ 4000	e^-
Hit-trigger association resolution	25	ns
Same pixel two-hit discrimination (time)	400	ns
Single channel ENC sigma (400 fF)	< 300	e^-
Tuned threshold dispersion	< 100	e^-
Charge resolution	4	bits
ADC method	ToT	
Radiation tolerance (specs met at this dose)	300	MRad
Operating temperature range	-40 to +60	$^{\circ}\text{C}$
Average hit rate with $< 1\%$ data loss	400	MHz/cm^2
Readout initiation	Trigger command	
Max. number of consecutive triggers	16	
Trigger latency (max)	6.4	μs
Maximum sustained trigger rate	200	kHz
External clock input (nominal) ²	40	MHz
Single serial command input (nominal) ²	40	Mb/s
Single serial data output (nominal) ²	160	Mb/s
Output data encoding	8b/10b	
I/O signals	LVDS	

1: At discriminator output. Digital hit detection in region will reduce sensitivity to time-walk.

2: Nominal operating frequencies. The design includes 20% frequency margin in general and $\approx 100\%$ for the data output.

Table 1: Basic Specifications for FE-I4

2.1 Specifications

130 The specifications are listed in Table 1. In addition to these quantitative specifications, there are functional capabilities listed in Table 2 that “carry over” from FE-I3 to FE-I4. Additional features that represent new functionality are listed in Table 3. Some of the features listed in Tables 2 and 3 have not been included in FE-I4A, as indicated.

Capability	Included in FE-I4A
Internal and external pulse calibration charge injection	Y
Internal generation of all bias voltages and currents	Y
SEU-tolerant, programmable global and pixel registers	Y
Global discriminator OR output (“hitbus”)	Y
Self-triggered operation mode based on hitbus	Y
Analog test outputs for one or more pixels	Y
Voltage regulators compatible with serial power included (but not hard-wired)	Y
Individual pixel leakage current monitoring	Y ¹
Charge injector capacitor value measurement circuit	N
Automatic power-on reset	N

1: A replica of the leakage current of any pixel is brought to a pad, but a planned internal ADC has not been implemented in FE-I4A; the current must be measured with an external instrument.

Table 2: Capabilities “Inherited” from FE-I3

2.2 Power Ratings and Start-up

135 The transistors used in FE-I4, even for I/O, have a 2.2 nm gate oxide normally reserved for core circuitry. The chip voltage specifications, with three exceptions, are derived from the properties of this gate oxide. Two exceptions are the DC-DC converter and the EFUSE programming circuitry, where the thickest gate oxide for this process (5.2 nm) was used in order to operate at higher voltage (radiation ratings for these circuits are covered later). The third exception is the input to the voltage
140 regulators, which does not go directly to any gate.

The maximum safe long-term operating voltage for a given oxide thickness is not simple to derive. It depends on temperature, desired lifetime (in 1000’s of power-on hours or KPOH), gate area, and operating duty cycle. A 1 cm² gate area is rated for 1.6 V operation with a 1 PPM failure rate after 100 KPOH at temperature of 125°C. While this suggests that a large detector could operate
145 10 years at 1.6 V without failures, even before considering the lower operating temperature (which further extends lifetime), this value does not include any potential radiation effects. Therefore, we conservatively chose a 1.5 V maximum long term operation voltage as the FE-I4 rating.

An absolute maximum rating (a voltage never to be exceeded) is even more complex to determine. This is because permanent damage occurs long before a voltage high enough to cause
150 instantaneous gate rupture is reached. A mechanical spring serves as a useful analogy. For a working spring, the thing one should not exceed is the elastic limit, which is reached long before there is any chance of breaking the spring wire. Transistor degradation mechanisms depend on temperature

Capability	Included in FE-I4A
PLL clock multiplier to support high speed output from 40 MHz beam clock	Y
V/2 charge pump DC-DC converter included (but not hard wired)	Y
Prompt radiation detector that automatically disables the chip	Y
Two trigger modes: Continuous (single time-slice) and Stop (all time slices)	Y
Programmable Read Only Memory in the form of e-fuses	Y
Opposite-corner alignment marks for flip-chip pattern recognition	Y
Isolated sensor connection through a chip bonding pad ¹	Y
Internal error logging counters	Y
10-bit ADC for monitoring	N
Temperature measurement circuit (using above ADC)	N
Programmable temperature dependence of global threshold	N
LVDS data MUX to support aggregation of 4 chips on a single serial output	N
Internal histogramming of comparator firing phase for timing-in large systems	N
Programmable event size truncation	N
Suppression of programmably long clusters	N

1: The isolation voltage of this connection is not rated and must be measured

Table 3: New and potential capabilities for FE-I4

and area, but also on time spent at a given voltage. A long time above a relatively low voltage can cause more irreversible degradation than a short time at much higher voltage. In fact, there are recommended procedures for highly accelerated stress testing (HAST) burn-in that involve very high voltages (approaching 2.5 V across 2.2 nm oxide) for times of order 100 ns. Like the long term operating voltage, the FE-I4 absolute maximum ratings and transient voltages have been defined somewhat conservatively, by not relying on the added protection afforded by a low operating temperature.

The voltage ratings for FE-I4 are collected in Table 4. Also included in the table are estimates of the current consumption. A minimum operating voltage is provided to indicate that all chip circuits have been designed to operate correctly down to this level (but this is obviously not a safety limit). In the case of the voltage regulator and DC-DC converter, the minimum voltage indicates that it should be possible to run the chip using this device at that input voltage. In FE-I4A, neither the regulators nor the DC-DC converter are internally hard-wired to the main chip, allowing the user to build whatever power scheme is desired using external connections. Three possible schemes, matching the columns in Table 4 are shown in Figure 1. The FE-I4 does not require especially low noise power supplies, and, start-up permitting, it is designed be able to run from a single external supply. The analog stage gain for power supply ripple has been measured in prototypes and found to be unity for frequencies above 1 MHz, as expected from the single ended design. At lower frequencies, however, a positive gain has been observed in prototypes which led to a re-design of the coupling capacitor between the first and second stages, thought to be responsible for this behavior. Therefore, the low frequency response to power supply ripple must

be re-measured in FE-I4A.

	Internal Nodes	Linear Regulators	DC-DC Converter	Units
Min. operating voltage	1.20	1.30	2.20	V
Max. operating voltage	1.50	1.65	3.40	V
Nominal operating current	0.60	0.60	0.31	A
Max. current at max. voltage	0.90	0.90	0.46	A
Peak transients allowed	1.75	2.00	4.0	V
Max. voltage at power supply ¹	2.10	2.50	4.73	V
Derived R/T drop allowed in cables	0.60	0.85	1.33	V

1: The chip will see this voltage minus the cable voltage drop. This limit is chosen under the worst case assumption that a zero voltage drop in the cables can occur.

Table 4: Voltage Ratings and Current Consumption of FE-I4A

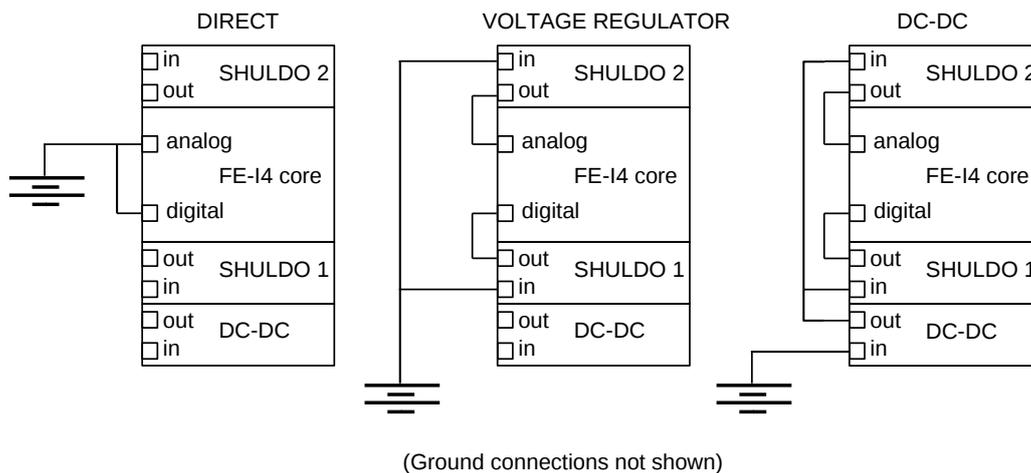


Figure 1: Three Options for Powering FE-I4A

175 FE-I4A contains multiple powering options in order to evaluate the performance of each one and optimize choices for the IBL and future applications (Figure 1). The start-up procedure must be studied and optimized on the physical chip depending on the chosen power option. FE-I4A contains two stand-alone linear-shunt regulators (ShuLDO) that can be externally wired for any purpose, as well as a divide-by-two DC-DC converter. These circuits have no internal power or
 180 ground connections to the rest of the chip. While the linear-shunt regulators permit implementation of serial power, the plan for IBL is to implement direct power as the system is small and there is some flexibility in the size and efficiency of the external services. Direct power also has the advantage of backwards compatibility with existing counting room power supplies and PP2 regulator components. The ShuLDO regulators can be used in shunt mode even for parallel (not serial)

185 power, in order to make the FE-I4 appear as a constant load regardless of activity or configuration, or they can be used in pure linear mode.

Net Name	Reset	Internal Blocks Powered
VDDD1	RD1bar_P(88)	ESD protection for pads on this net RD2bar circuit Input LVDS receivers (with their own bias circuit) Command decoder IOMux bypass and test I/O block
VDDDT3_Pad ¹		T3 isolation wells
VDDA1	RA1bar_P(45) RA2bar_P(56)	ESD protection for pads on this net Current reference Radiation burst detectors Global configuration memory Bypass configuration memory Global bias DACs (but not bias mirrors)
VDD_PLL	-	Clock multiplier core ESD protection for this pad
VDDEfuse(42)	-	Core voltage EFUSE circuitry ESD protection for this pad
VDDD2	RD2bar_P(89)	ESD protection for pads on this net Digital columns and end of column logic Clock multiplier interface LVDS output End of chip logic All other digital circuits
VDDA2	-	ESD protection for pads on this net Bias generator mirrors Analog pixel array Pixel array shift register Pixel configuration latches all other analog circuits

1: The VDDDT3_Pad net does not have added ESD protection because it consists entirely of substrate diodes, which are self-protecting.

Table 5: Power nets in the nominal order they should be turned on. Reset lines shown must be externally controlled, either by logic or and R-C circuit, to implement power-on resets.

Controlling the transient behavior of a chip as large as FE-I4 requires some care. The possibility exists for very large transient currents from an improper power-up sequence. In FE-I4, four internal power nets have been defined in order to permit a controlled transition from power off to on, and anticipating that flexibility in powering parts of the chip independently will be useful to understand the behavior. Each net has separate wire bond pads for supply and for ground. For a

production chip, it is expected that power will be internally distributed to these nets using regulators per the final power configuration chosen. In addition, the T3 isolation wells, the clock multiplier core, the EFUSE block, and the EFUSE programming voltage have dedicated power supply pins
 195 (but not separate ground). Table 5 lists expected order that nets should be powered, indicates what internal circuit blocks each net serves, and lists the relevant reset-bar pins. All resets use negative logic. There is no internal power-on reset generation in FE-I4A. Instead, pins are provided so that power-on resets can be implemented and tested as needed.

2.3 Temperature Range

200 The FE-I4 has been designed to operate at low temperatures achievable with CO₂ cooling, as well as high temperatures for potential applications beyond silicon pixels. The recommended range where all specifications are met is -30°C to +30°C. However, the chip is designed to operate normally in the extended range -40°C to +60°C, but some specifications may not be met. Simulations to verify compliance with specifications have been carried out at -30°C, 0°C, and +30°C.

205 While operation anywhere in the allowed range is supported, some small temperature variation is present. On the digital side, power consumption is expected to vary over the given range. On the analog side, power consumption will remain constant, because it is tied to the current reference. No variation of the current reference has been observed in test devices with an accuracy of 0.02%/°C.

A significant temperature variation exists in the discriminator threshold setting within the analog pixel, which is the sum of adding contributions from the DC level of the second stage and the replication of the global threshold voltage within the pixel. Each of these effects has been measured in prototypes to be approximately 1 mV/°C, but the exact values are expected to be process dependent. Making these circuits passively temperature compensated within the pixel would have brought a significant area penalty and possibly also a significant power penalty. Instead, some degree of temperature compensation was introduced in the global threshold voltage generated in
 210 the bottom of chip (this is a single voltage distributed to all pixels). A temperature varying global threshold voltage output is available on a dedicated bond pad. The variation on this voltage should be such as to mostly compensate the pixel change in threshold with temperature. The user must either connect this output to a global threshold input pad, or must supply an external resistor in
 215 order to generate a “traditional” threshold voltage that does not have temperature variation (except through the resistor used). Alternatively, a purely external threshold voltage can be supplied.

2.4 Radiation Tolerance

The 130 nm feature size process used for FE-I4 enjoys an inherently high total dose radiation tolerance of the core (2.2 nm gate oxide) transistors. Design principles that take advantage of
 225 this benefit have been followed in order to exceed the 300 Mrad specification. Vulnerability to single event upsets has been controlled by using custom layout, triple-redundant memory cells for storing configuration, triplicating digital logic blocs, and hamming coding data buses and storage. However, the FE-I4A is explicitly not robust against exposure to a very high dose rate source (note that high dose rate tolerance is not required for operation at particle colliders, where the integrated
 230 dose can be very high, but the rate at which the dose is delivered is always low). Dedicated radiation burst detection circuitry has been included in FE-I4A that will automatically reset the configuration

memory in the presence of a dose rate exceeding 10^8 Rad/s. Such a rate must be present for 20 ns or longer in order to activate the reset. This was done to ensure that FE-I4A is not classified for export control under ITAR.

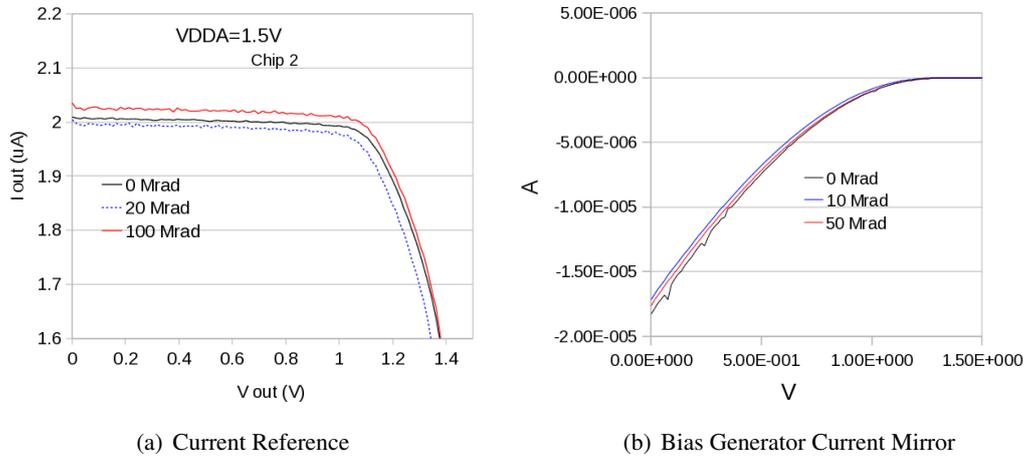


Figure 2: Radiation Effects on Prototype Circuits

235 On small prototypes, no change in the operation of simple digital circuits has been observed up to total dose of 400 Mrad delivered with protons. Analog circuits have small, but measurable changes with dose. The current reference variation is about 2% over 200 Mrad (Figure 2(a)). The current mirrors used to generate bias voltages vary by about 5% (Figure 2(b)), but the same transistor configuration is used to turn the bias voltages into currents within each pixel, compensating
 240 for the change. Thus only small adjustment of the bias settings should be required after irradiation. A lack of compensation was discovered in prototypes for the feedback current of the second stage amplifier. The design has been corrected for FE-I4A such that all bias mirrors are properly compensating.

245 The single pixel noise increase with radiation could not be properly measured in prototypes, because the capacitive test load included in a few channels is not radiation hard (a diode load was used as a large enough metal capacitance could not fit in the available space). We take the observed change in noise as an upper limit, with the expectation it is in fact due mostly to the diode load and not the amplifier. Thus the single pixel noise is expected to increase less than 10% every 100 Mrad.

250 One circuit shows a significant change with radiation. The DC-DC converter is built using the thickest available gate oxide in order to operate with 3.3 V input voltage. The on-resistance of the switches increases approximately 10% per 100 Mrad. Note that this only affects the efficiency, and not the functionality, of the circuit. Thus one must size the DC-DC converter switches for desired efficiency after irradiation.

3. Layout and Organization

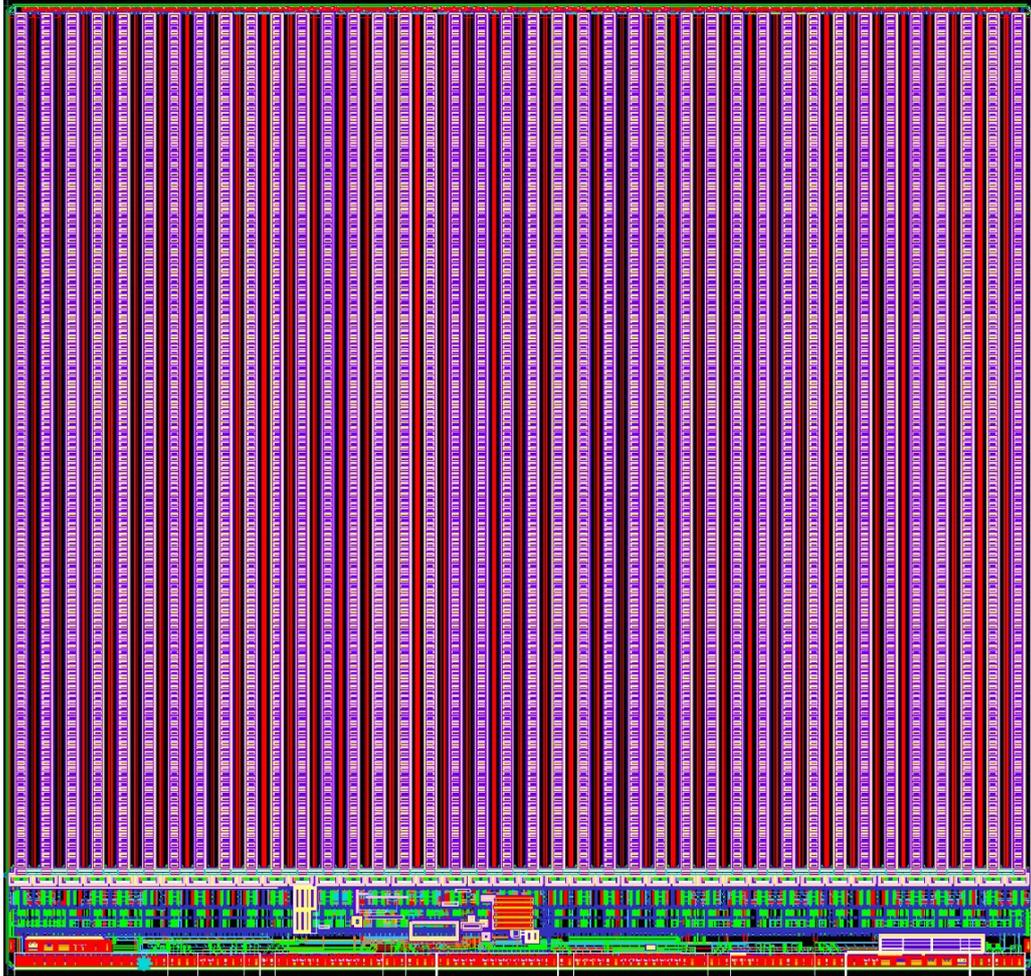


Figure 3: FE-I4 chip layout looking down onto the bump pads. The coordinate origin is at the bottom left corner, with x increasing to the right and y increasing upwards.

255 The FE-I4 layout is shown in Figure 3. References to the “top”, “bottom”, “left”, “right” of the chip are relative to this figure. The FE-I4A has no special identifying feature (logo). The pixel array has bump bond pads with $12\ \mu\text{m}$ width octagonal openings on a $50\ \mu\text{m}$ vertical pitch. In the horizontal direction there is one single column of bump pads along the left and right edges, with 39 pairs of columns in between, spaced $500\ \mu\text{m}$ pair-to-pair, and $50\ \mu\text{m}$ within each pair. The pads are aluminum. There are wire bonding pads along the bottom and top of FE-I4A. The pads at the top are specific to FE-I4A characterization and will not be present in a production version. The pads at the bottom come in three sizes, wide ($250\ \mu\text{m}$ wide bonding area), normal ($100\ \mu\text{m}$ wide bonding area), and narrow ($75\ \mu\text{m}$ wide bonding area). Wide pads are exclusively for high current inputs and outputs and are intended for multiple wire bonds. Normal pads are for all other I/O that may be
 260 required for normal operation or that must be contacted during wafer probing. Narrow pads are for
 265 diagnostic only: they do not need to be contacted in wafer probing and will only be wire bonded

on an as needed basis to diagnose or correct problems or perform special measurements of chip internal voltages or currents. There is a short second row of pads on the left bottom of the chip, corresponding to a stand-alone linear-shunt voltage regulator. There are two normal pads further
 270 inset from the chip bottom, one each on the left and right edges, that make contact to isolated bump bond pads $50\ \mu\text{m}$ below the leftmost and rightmost full double columns of regular bump pads. Pads at the top of the chip are narrow pads oriented sideways. Note that the chip power nets all use multiple normal pads, instead of fewer wide pads, because power must be supplied uniformly along the width of the chip, and therefore the current in each power pad is small. Finally, the chip
 275 contains metal crosses for alignment during flip-chip assembly. There is one cross near each of the four corners, plus a half-cross near each of the lower left and right bump bond pads. Coordinates of wire bond pads and alignment marks are given in appendix D.

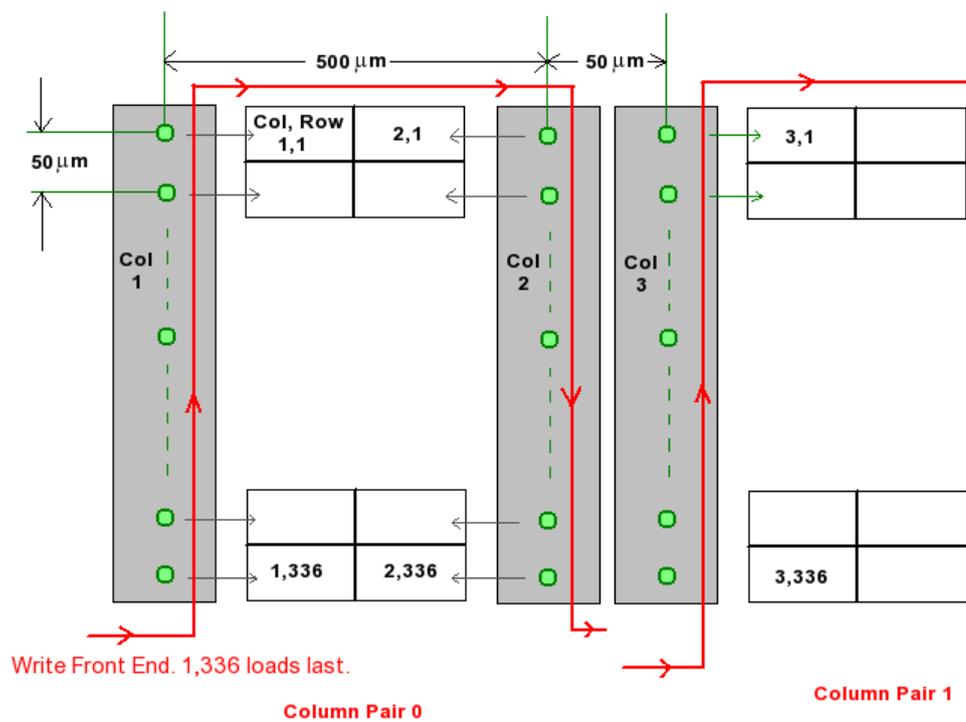


Figure 4: Pixel and column numbering scheme. The red line shows the pixel configuration shift register flow. Each double-column has an independent shift register. To program the pixels in columns 1 and 2 one must select double-column 0 for shift register programming, etc.

The FE-I4 pixel array is organized in column pairs numbered 0 (leftmost) to 39. A column pair consists of two analog columns, 336 pixels tall, on either side of a digital double column. The
 280 digital double column is actually a single column of 4-pixel regions, but it is called double column because it serves two columns of analog pixels. Single analog columns are numbered 1 to 80 (not 0 to 79). Thus column pair 0 contains columns 1 and 2. This can sometimes lead to confusion, but there is logic behind the choice. The pixel addressing scheme used for the output data is based on

single columns, and purposely avoided having a column address of 0 in order to exclude a unique
285 all-0 data pattern. On the other hand, control of the chip is based on column pairs, not single
columns, and in this case 0 was a desirable first address for simple decoding. The column pair,
column, and row numbering convention is illustrated in Figure 4. The analog columns are shown
in gray, with green circles representing the bump bonds to the sensor. The 4-pixel digital regions at
the top and bottom of the digital double column are also shown. The pixel numbering is indicated
290 as (column, row). Column 1 is along the left edge of the chip (recall there is no column 0). Row
1 is at the top (there is similarly no row 0), and the first pixel (1, 1) is at the top left corner. Row
and column addresses using this convention are always reported in the readout, along with the ToT
value for the specified pixel *and* the pixel immediately below it in Figure 4. If there is only a hit in
row 336 and not row 335 of a given column, the ToT for the “bottom” pixel is reported as “1111”,
295 which is the ToT code for no hit. See Section 7 for more details on data output. See Section 8.2.2
for details on how to select specific column pairs for control, calibration injection, etc. Pairing
of columns for analog charge injection is anomalous due to layout constraints. Column “pair” 0
controls charge injection only in column 1, column pair 1 injects into 2 and 3, column pair 2 into 4
and 5, etc., and finally column “pair” 39 injects into the last 3 columns (see Section 8.2.2). This is
300 the only addressing anomaly. All other operations that affect column pairs do so according to the
standard convention of Fig. 4.

4. Circuit Core Description

4.1 Top Level Overview

A top level diagram of FE-I4 is shown in Figure 5. The FE-I4 pixel array is organized in double-columns like the present detector's FE-I3 chip, but the readout architecture is very different. Instead of moving all hits from the pixel array to a global shared memory structure for later trigger processing, the FE-I4 double-columns are further divided into 2×2 pixel regions. Each region contains 4 identical analog pixels, ending in a discriminator, and one shared memory and logic block called Pixel Digital Region (PDR). The PDR can store up to 5 "events". For each event, a counter clocked at 40 MHz keeps track of the time elapsed since the event took place with 25 ns resolution. Clearly this requires distributing the 40 MHz clock to all the regions. The maximum skew of the clock distribution network is 2 ns. When an external trigger arrives, it is also distributed to all the regions simultaneously within 2 ns. The trigger selects any events for which the time counter matches the programmed trigger latency value. When the counter exceeds the latency without a trigger, the event is erased to make room for more. The events selected by a trigger remain in the region until it is their turn to be sent off chip via the serial LVDS output. The events are read out sequentially, ordered by time. All regions can be read out if they are all selected. A "stop" readout mode is also provided where the time counter is stopped and all events stored in every region are read out. This is useful for testing and debugging.

The individual discriminator outputs are synchronized with the 40MHz clock as they feed into the region logic, and all region operations are synchronous. Each synchronized discriminator output is further processed by applying a digital cut on the time over threshold (ToT). Hits smaller than a certain ToT (programmable between 1 and 3 clock periods) are classified as "small hits" and those larger as "large hits". The next available time counter in a given region starts whenever there is at least one large hit in the region. Small hits do not start a counter. Once a counter starts, a ToT code of all 4 pixels is always recorded (which is 1111 for a comparator that did not fire). This automatically stores small hits in the same time bin as large hits from the same cluster. This relaxes the time-walk requirements on the analog circuitry, allowing lower current operation. As clusters will often straddle a region boundary, in addition to storing all 4 pixels within the region, 4 neighbor bits are stored to flag the presence of small hits in the pixels adjacent to the region in the ϕ direction. An association window of two clock cycles is used to capture small hits both within the region and in the 4 neighbor pixels. This scheme is equivalent to the hit duplication function of the FE-I3 chip, where all hits below a certain ToT value are copied to the preceding time bin, but it is more efficient in terms of memory and latency counter usage. Note that by setting the programmable digital ToT threshold to the minimum, one recovers traditional hit discrimination, in which all comparator firings are considered equal and recorded in the time bin that they occurred (which, due to time-walk, tends to be the wrong bin for hits just above the analog discriminator threshold).

All the above data driven information is stored locally in the 4-pixel digital region and only moved further if selected by a trigger. The raw hit rate that this architecture can accommodate with high efficiency is a function of the amount of memory in the region, and how quickly this memory is emptied (given by the programmed trigger latency). Events selected by a trigger potentially remain in the region much longer than the latency (until they are read out), and therefore a higher

trigger rate contributes to filling up the region memory, but because the trigger rate is low relative to the raw hit rate this is not a dominant effect. Figure 6 shows the simulated inefficiency for charge deposits in $250\ \mu\text{m}$ planar unirradiated silicon at 3.7 cm radius of the FE-I4 as a function of the number of minimum bias interactions per 25 ns beam crossing, assuming a $3750\ e^-$ discriminator threshold, 120 crossing latency, and 100 kHz trigger rate. The simulated performance of the present FE-I3 chip under the same conditions is also shown for comparison.

The FE-I4 inefficiency is dominated by single pixel pile-up, and not by the readout architecture, until well beyond the 75 interactions per crossing projected for IBL. The result can be applied to slightly different layer radius, the hit rate scales approximately as $1/r^2$ [3]. In this simulation the rate of discriminator firing at 75 interactions per crossing was $400\ \text{MHz}/\text{cm}^2$. Single pixel pile-up, the main source of inefficiency, occurs when a pixel is hit while the discriminator is still high from a previous hit. This source of inefficiency scales linearly with the average ToT for a hit pixel and with the pixel area. The requirement to keep the total inefficiency below 1% was the driving reason for reducing the FE-I4 pixel area (relative to FE-I3) as well as the ToT dynamic range to 4 bits instead of 8.

The FE-I4 circuitry is divided into functional blocks with well-defined interfaces. This facilitated the design process carried out by a geographically distributed collaboration. Figure 7 shows a simplified schematic of the data path in a typical data acquisition configuration, while Figure 8 shows the simplified command and configuration path for single chip operation.

It may be appreciated from these figures that the output path is common for data and configuration, which both use a common fixed format record as detailed in Section 7. In terms of physical area, 89% is taken up by the 40 double-columns, each consisting of two analog columns and a Digital Double-Column (DDC). These are interfaced to the global control and logic on the chip periphery by a “horizontal” circuit layer running along the bottom of all columns and containing the end of digital column logic (EODCL in Figure 7) and the distribution of analog column configuration, bias, and calibration signals (Figure 8). All the periphery circuit blocks are single double-column oriented, with data, clocks, biases, etc. distributed to/from one or more double-columns in parallel as programmed into the global configuration. Many functions of the periphery logic blocks are programmable, and the global configuration is implemented as a random access memory of 16-bit words. For example, the clock source used to serialize output data can be selected to be any of the PLL outputs (40 MHz, 80 MHz, 160 MHz, or 320 MHz), the raw 40 MHz input clock, or an auxiliary input. The data output block can be configured to implement 8b/10b encoding or not, or to loop back the input clock, and so on. The configuration memory is implemented with triple-redundant SEU hard custom cells, while the digital logic blocks are either triplicated with majority voting or Hamming coded, always synthesized from standard cell libraries.

The main circuit block acronyms are summarized in Table 6. They are described in the following sections highlighting design and performance features. Practical details for operation (what value to program into which register, what wire bond pad to connect, etc.) are not given circuit-by-circuit in this chapter, but are collected for the chip as a whole in the appendix.

4.2 Analog Pixel

A 2-stage amplifier configuration is used to implement the analog front end, shown schematically in Fig. 9. The “Preamp” (first stage) is a cascode amplifier with an NMOS as input device. The

Acronym	Name	Contained in
FEND	analog pixel (Front END)	analog column
BIASDACS	BIAS generator using Digital to Analog Converters	
PDR	Pixel Digital Region	DDC
DDC	Digital Double Column	
EODCL	End Of Double Column Logic	
CMD	Command Decoder	
EOCHL	End Of Chip Logic	
DOB	Data Output Block	
PLL	Phase Locked Loop clock multiplier	CLKGEN
CLKGEN	CLocK GENerator	
CNFGMEM	CoNFiGuration MEMory	
EFUSE	PROM configuration using E-fuses	
PULSGEN	PULSe GENerator (for calibration)	

Table 6: List of Main Circuit Blocks

second stage (“Amp2”), AC coupled to the preamp, is a folded cascode PMOS input amplifier. The main motivation of this 2-stage system is to provide enough gain in front of the discriminator while permitting optimization in the choice of the preamp feedback capacitor (C_{f1}). The discriminator is built with a 2-input voltage comparator and a threshold voltage generator. Signal shaping is only
390 done by the preamp with an adjustable return to baseline, while the second stage provides only voltage gain (given by C_c/C_{f2}). The return to baseline and discriminator threshold are individually adjustable in each pixel, with globally determined range and offset. Altogether 13 bits are available for the configuration of the analog pixel which are stored locally in custom-made SEU-tolerant latches. Two selectable capacitors are provided for analog calibration injection. The preamp feed-
395 back has a low frequency active filter for DC leakage current compensation, and the amount of DC leakage is mirrored to a column-parallel output. The comparator output is fed to the digital pixel region through logic gates which allow to gate it off or combine (logic OR) with a digital test signal. Additionally the comparator output is fed to column-parallel wired-OR circuit. This "HitOR" function can be disabled and should be off for normal operation to avoid parasitic crosstalk.

400 When a negative charge (electrons) Q_{in} is deposited at the input, a positive going pulse appears at the output of the preamp. In an ideal system, the amplitude of this pulse would be Q_{in}/C_{f1} , but because a fast shaping (return to baseline) is required and the amplifier is non-ideal in practice, the actual amplitude will be less. The shorter the (adjustable) shaping, the smaller the pulse amplitude for the same input charge. The return to baseline is implemented by a feedback system very similar
405 to that of the FE-I3, discharging C_{f1} with a quasi-constant current source. The negative going pulse at the output of the second stage feeds the negative input of the comparator, with a threshold voltage at the positive input.

The schematic of the leakage current compensated preamp is shown in Fig. 10. It is a regulated telescopic cascode with the NMOS input transistor M1. The availability of triple-well structures

410 allows to exploit the higher transconductance of NMOS transistors with respect to PMOS and still be shielded from substrate noise. In addition, the NMOS input transistor gives a low DC output potential that introduces a high dynamic range for the expected positive going output signals. Due to the regulated cascode formed by the cascode transistor M2 and the amplifier composed of transistors M5, M6 and M7 the preamplifier has a high output impedance and hence a high gain.

415 Since the biasing voltage of the cascode transistor M2 is generated locally the amount of potential crosstalk paths are reduced and global routing is simplified. Transistor M4 provides additional current to the input transistor M1, to increase its transconductance. The telescopic structure has the advantage that the highest current in the amplifier flows through the input transistor and not through any biasing transistor which reduces the noise contribution from the biasing. The source-

420 follower formed by transistors M8 and M9 decreases the output impedance in order to drive the load presented by the coupling capacitor to the second stage without reducing the bandwidth.

*** ABDER: can you modify/add some explanation of what is it that allows operation down to very low current? *****

The NMOS feedback transistor M18 providing continuous reset is biased in a current mirror topology.

425 ***** ABDER, CAN YOU REWRITE THIS NEXT BIT? IT IS NOT CLEAR. IT SHOULD MENTION M20 *****

The bias current flows into the source-follower at the preamp output, but this does not affect the operating point because it is much smaller than the bias current of the source-follower. The feedback bias current is defined by a global PMOS biasing voltage. The feedback bias current can be tuned at pixel level by a local DAC which steers a current into the gate-drain biasing transistor M19.

430 For high output signals, the NMOS feedback transistor M18 gets saturated and drains a constant current. A nearly linear return to baseline and as a result a pulse width proportional to the input charge is obtained. During the response to an electron signal, the potential at the preamp output is higher than the potential at the input. As a result the terminal of transistor M18 which is connected to the preamp input becomes the source which stays at constant potential. On the contrary, the source of the gate-drain connected feedback bias transistor M19 is located at the output and the source potential follows the output signal. To avoid that the feedback current changes with the preamp output voltage the gate potential of the feedback transistor is stabilized by means of capacitor C_1 .

440

A differential amplifier (transistors M11-M15) tracks the DC shift between input and output of the preamplifier, which is caused by detector leakage current. The dedicated PMOS transistor M15 connected to the preamp input is steered to compensate for DC leakage current. The bandwidth of the differential amplifier has been limited by the addition of the capacitor C2 connected to the gate of M15. As a result the differential amplifier reacts very slowly to voltage variations at the output and so is insensitive to AC signals. The leakage current is mirrored to transistor M16 and can be monitored when transistor M17 is switched on.

445

The second stage is shown in Fig. 11 together with the com- discriminator. A PMOS input transistor has been chosen for the cascode to give a large dynamic range for the expected negative going output signal. The bias voltage of the cascode transistor M3 is generated locally to ease routing. The feedback time constant of the second stage has been chosen to be significantly larger than the feedback time constant of the first stage. In this way a signal undershoot below the DC

potential at the output of the second stage is avoided. The PMOS feedback transistor M10 is only used to set the DC operating point at the second stage input. During signal processing almost no discharge of the feedback capacitor happens through the PMOS feedback transistor. The feedback capacitance is charged and discharged only through the coupling capacitor C_C which connects the output of the first stage to the input of the second stage.

The comparator uses a classical two-stage differential amplifier, where the inverting input corresponding to the gate of transistor M12 is connected to the second stage output and the non-inverting input corresponding to the gate of transistor M13 is connected to a trimmed DC voltage which is provided by the local threshold tuning system. The second comparator stage is powered by the digital supply voltage to avoid that the current transients which are generated by the comparator switching couple to one of the amplification stages through the supply lines. The global threshold $V_{thGlobal}$ is applied to the input of a source-follower which is formed by transistors M18, M19 and M20. A local voltage offset is added by the threshold tuning DAC (TDAC) formed by the resistor ladder and the current source M19. In addition to the TDAC offset, the source-follower adds a natural voltage-offset to $V_{thGlobal}$ which corresponds to the source-gate voltage of transistor M18 and is defined by the current provided by transistors M19 and M20. Since the current provided by M19 is adjustable to define the LSB of the TDAC, most of the current should be provided by M20 to make the source follower offset independent of TDAC LSB. M20 has been biased with the second stage bias V_{bp} in order to save a bias line, as the exact value of the M20 current is not important. This source follower is TDAC circuit is very compact but has a known temperature dependence coming mostly from the has a known temperature dependence in the natural offset of the source follower. The approach taken to correct this temperature dependence is to introduce a compensating temperature dependence into the generation of $V_{thGlobal}$.

4.3 Analog Array and Biases

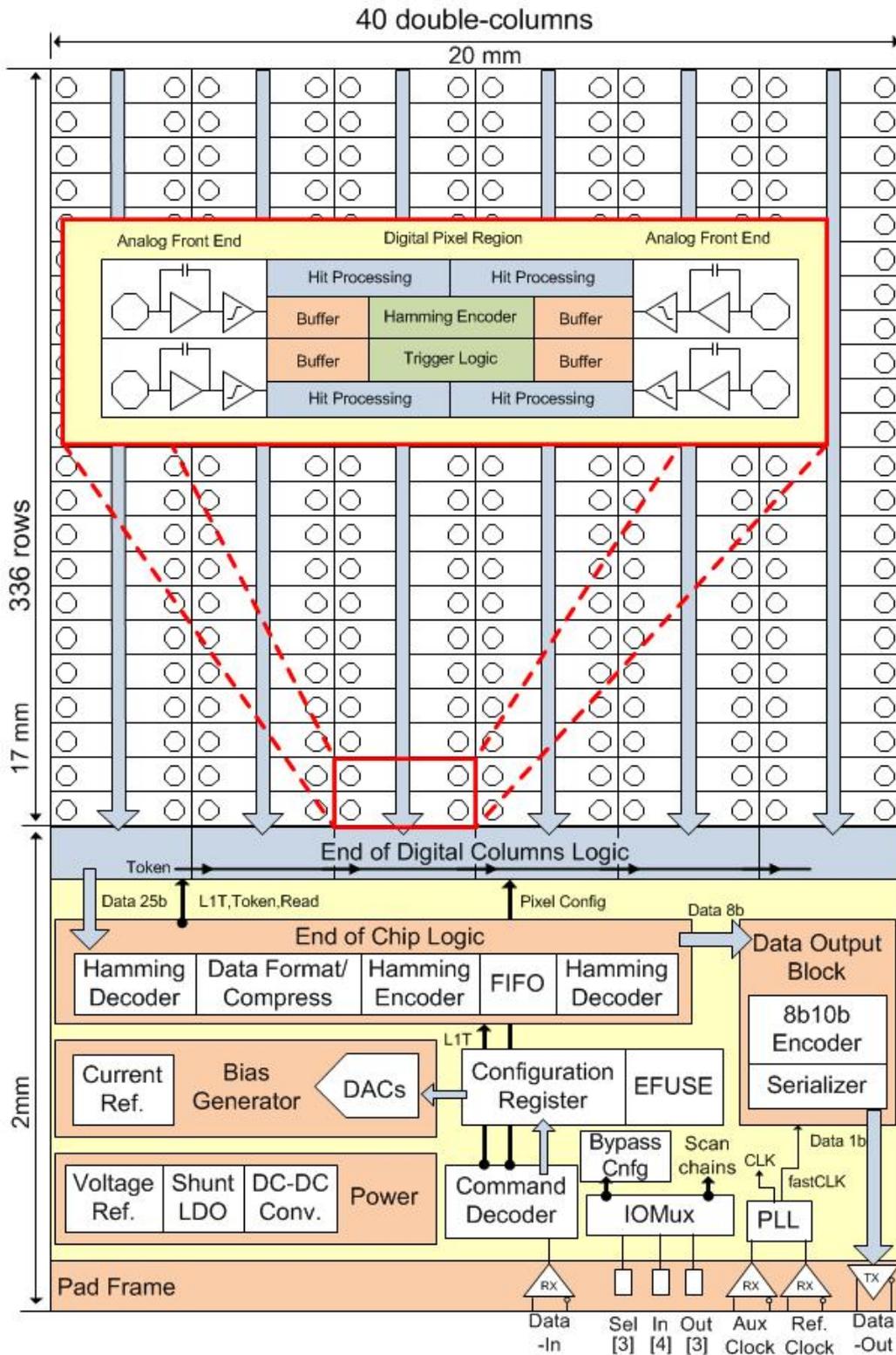


Figure 5: FE-I4 chip diagram, not to scale. The coordinate origin is at the bottom left corner, with x increasing to the right and y increasing upwards.

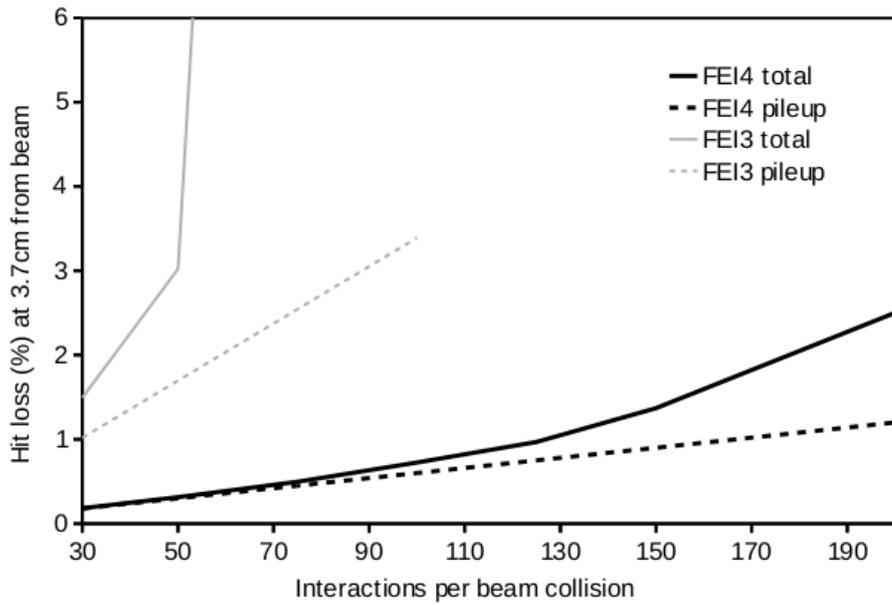


Figure 6: Simulated data losses for FE-I4 and FE-I3 chips placed at 3.7 cm from proton-proton beam collisions at 14 TeV. The expected number of interactions per beam crossings during IBL operation is 75.

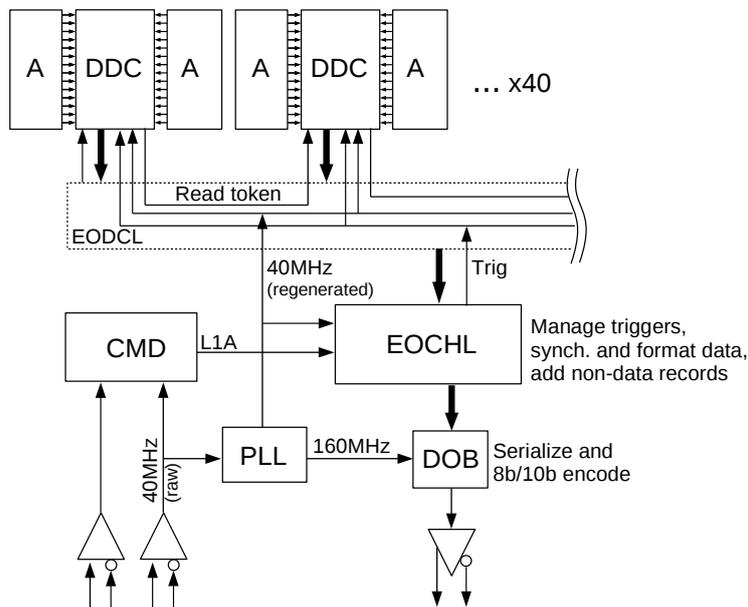


Figure 7: Simplified schematic of the output data path in a typical data acquisition configuration. Circuit blocks shown are analog column (A), digital double column (DDC), end of digital column logic (EODCL), command decoder (CMD), phase locked loop clock multiplier (PLL), end of chip logic (EOCHL), and data output block (DOB).

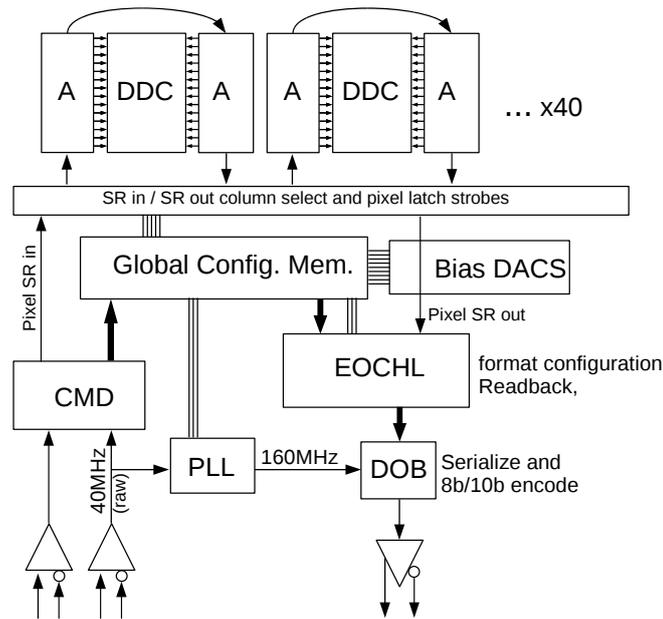


Figure 8: Simplified schematic of the configuration path for typical single-chip operation. Circuit blocks shown are analog column (A), digital double column (DDC), global configuration memory, analog bias digital to analog converters (DACs), command decoder (CMD), phase locked loop clock multiplier (PLL), end of chip logic (EOCHL), and data output block (DOB).

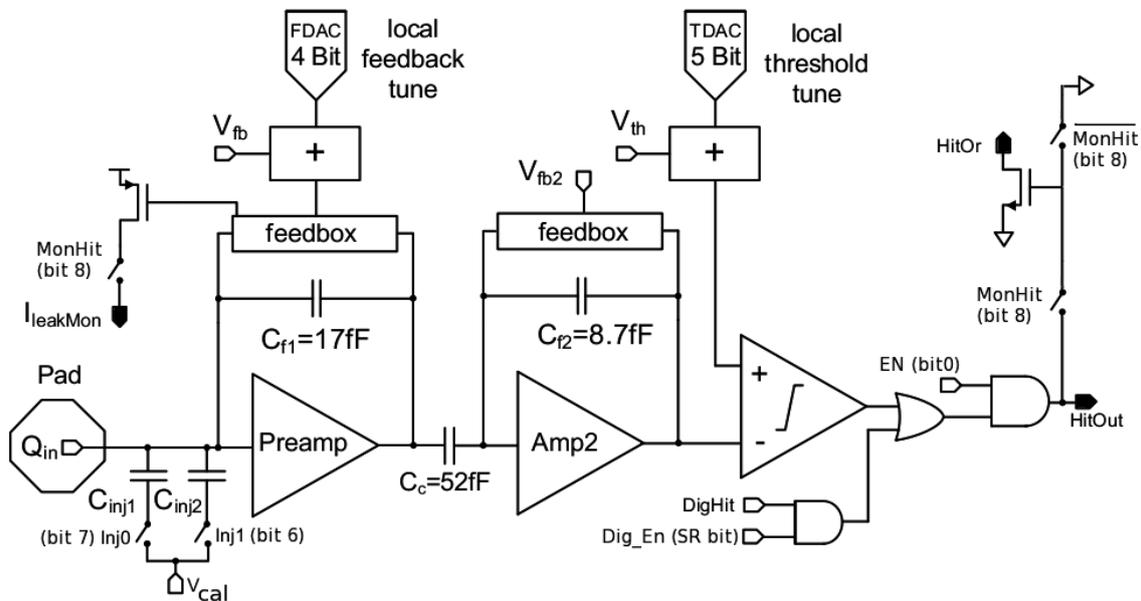


Figure 9: Analog pixel schematic diagram. Output pins are solid, input pins are open.

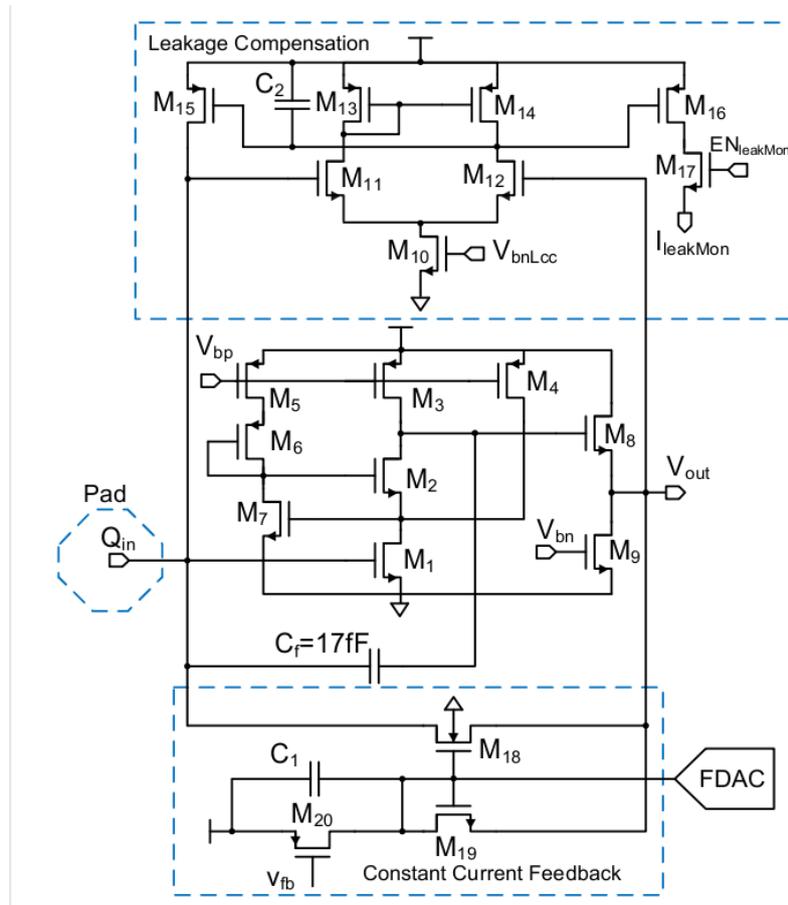


Figure 10: Analog front end preamp circuit schematic.

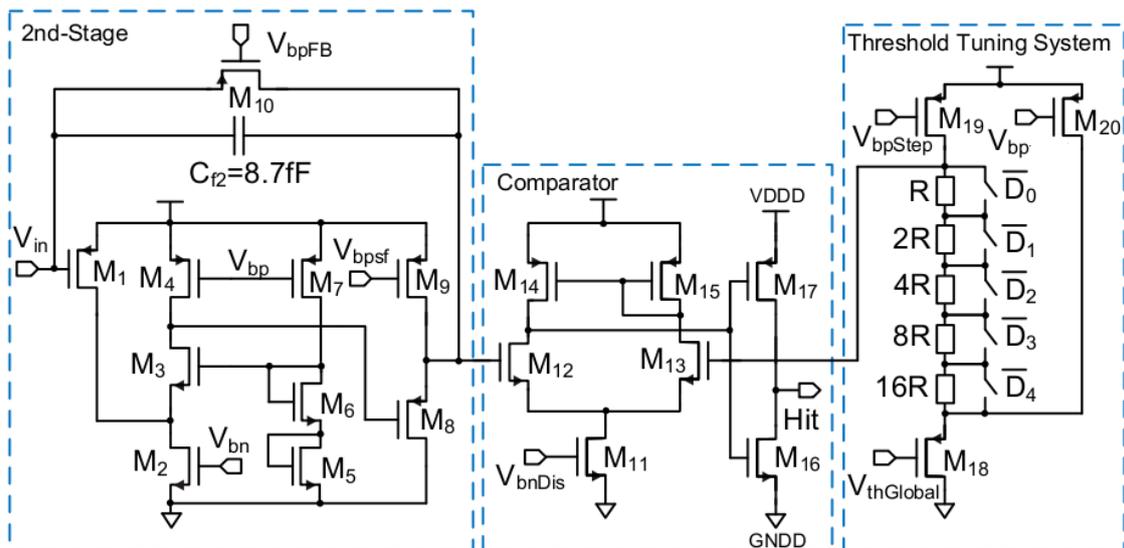


Figure 11: Second stage and discriminator circuit schematic.

4.4 DDC, PDR, and EODCL

The FE-I4 contains 40 Digital Double Columns (DDC) connected together via the End of Double Column Logic (EODCL). Each DDC contains 168 Pixel Digital Regions (PDR) grouped into 7 units of 24 PDRs each. Each PDR processes the data from 4 pixel discriminators (2 rows by 2 columns). The PDR is designed and synthesized as a single logic block: it cannot be subdivided into 4 “pixel” blocks (see Figure 12). The PDR contains 5 latency calculation and triggering units

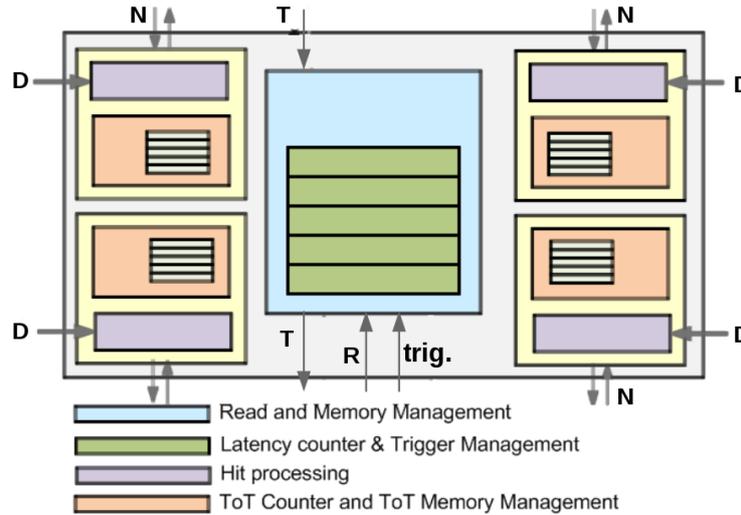


Figure 12: Diagram of the Pixel Digital Region circuit. The selected connections shown are: trigger input, analog discriminator inputs (D), neighbor logic inputs and outputs (N), read token in and out (T), and read signal input (R).

that are PDR-specific, not pixel specific. The time stamping of a hit is hence common information to the region. However, pulse-height information (ToT) is independently counted for each pixel. The PDR contains 4 groups of 5 pixel memories, where each memory stores 4 bits of ToT plus a 1 bit neighbor flag. The digital threshold is applied to the discriminator output of each pixel prior to starting a dedicated 4-bit binary counter for ToT. This is done with a shift register adjustable between 1 and 3 cells (1 cell for digital threshold 0 to 3 for digital threshold 2). If the input and output of the shift register are both high, then the hit has passed the digital threshold and is considered a “big hit”. The reset value of the ToT counter is 1111, and for pixels whose analog discriminator did not fire, this is the value that will remain as the ToT code meaning “no hit”. Whenever the analog discriminator does fire, the counter is decremented to 1110, which means “small hit”, but does not automatically continue to count until the digital threshold shift register has finished shifting. If the digital threshold is passed (big hit), the counter is cleared to 0000 and starts to count. Otherwise it remains at the 1110 code for small hit. The counter stops either when the analog discriminator falls or when it reaches 1101. The resulting ToT counter values vs. actual analog discriminator pulse width and digital threshold setting are listed in Table 7.

Whenever the digital threshold is passed by any of the 4 pixels (indicating the presence of a

"True" ToT (clocks)	HitDiscCnfg			
	00	01	10	11
Below tresh	F	F	F	x
1	0	E	E	x
2	1	0	E	x
3	2	1	0	x
4	3	2	1	x
5	4	3	2	x
6	5	4	3	x
7	6	5	4	x
8	7	6	5	x
9	8	7	6	x
10	9	8	7	x
11	A	9	8	x
12	B	A	9	x
13	C	B	A	x
14	D	C	B	x
15	D	D	C	x
≥16	D	D	D	x

Table 7: ToT 4-bit code values (hex) for actual time over threshold values (left column) and hit discrimination configuration settings. Setting "11" is not valid and will result in hit output being completely disabled. The values above the dividing line in the central 3 columns will only be read out if they are next to a "big hit" – all values below the line are "big hits".

big hit), the next available latency counter is started and a busy flag is set for that counter. The
500 next available counter is calculated by combinatorial logic from the busy flags of the 5 counters,
in order to avoid having a register based pointer that could be vulnerable to SEU. Each latency
counter is mapped one to one with four ToT memories, one per pixel, avoiding the need for a
pointer mechanism which would be vulnerable to SEU. One clock after a latency counter starts,
the PDR will be ready to start another counter, should another big hit occur. Thus the fact that
505 timing is common to the whole region does not result in any dead time penalty. The "pile-up" dead
time (a new hit arriving while a given discriminator is still high from a previous one) affects only
single analog pixels and not the whole PDR as if it were one big pixel. Furthermore, a new big hit
in the PDR does not truncate or otherwise affect the ToT values of the previous hits, even if there
are ToT counters still counting when the new big hit arrives. ToT counters are always allowed to
510 finish counting and their values stored in the ToT memory associated to the time of arrival of the
hit. This does not add any dead time, because the 4 ToT counters are independent. Any dead-time
is already present at the analog discriminator: there is no advantage to not counting ToT as long
as the analog discriminator is high. Of course, for a hit to be possible there must be at least one
analog discriminator that is low and therefore at least one ToT counter that is idle. While the "big
515 hit status" of each pixel is allowed to persist for only one clock cycle, a "small hit status" persists

for 2 clock cycles. Thus the ToT code for small hit will be recorded if it was present either at the same time as a big hit or in the clock after. Each pixel has one neighbor: above (below) in the same column for the pixels at the top (bottom) of the PDR. If the neighbor's status shows a small hit during at the time a big hit occurs or in the clock after, the neighbor bit is latched, if it shows a big hit or no hit then it is not latched.

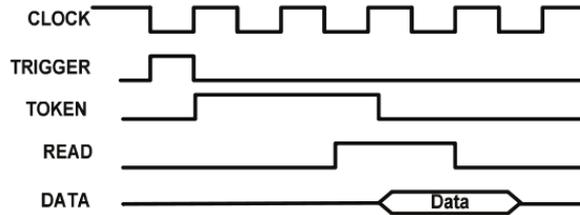


Figure 13: Example of PDR readout timing.

While the DDC contains 168 PDRs it also contains additional elements for signal distribution and is thus a single circuit with inputs from 336 discriminators plus 336 enable signals, half from each left and right sides. The readout of hit data is on two common buses (data and address) and is prioritized by a token organized as a chain of OR gates, triplicated for redundancy with majority voting in every region. The token moves from the DDC top (row 1) to the bottom (row 336). A readout signal causes the PDR with the token to output its data and advance the token (Figure 13). The output data bus consists of 25 bits (16 ToT + 4 neighbor bits + 5 Hamming error protection codes) implemented also with daisy-chained OR gates to avoid the need to drive large wire loads. The 11 bit address bus (8 address + 4 protection bits) is organized as a thermal Gray encoder (Figure 14). This minimizes the number of gates used to generate and transmit the address. Minimum number of gates in turn minimizes area and power, and maximizes yield. A Gray code address bus for N regions needs only N gates for the entire bus. Hamming code protection increases the number to just over 3N. The readout operation is controlled by the read signal in each PDR that holds the token and enables the data transfer of the requested triggered event. Any region with the read signal set holds the token temporarily while placing its data on the bus. Otherwise the token passes through each region in a time given by one OR gate delay.

Need to explain how the trigger ID, trigger ID request and latency comparison are done.

Every PDR needs the 40 MHz system clock. A simple regeneration scenario with balancing is used to distribute the clock with small skew (Figure 15). Some level of mismatch is purposely left uncorrected to preserve a clock skew of about 2 ns, since a perfectly unskewed clock distribution may lead to very sharp power spikes. The trigger signal is distributed in the same way. All other global signals needed by the PDR do not have critical timing and therefore use a simpler distribution scheme as shown in Figure 16.

The DDC power distribution is done with full custom layout in the low resistance top metal layers. This achieves a calculated DDC voltage drop of 10 mV assuming 40 mA per PDR average current consumption (this is the total digital current budget for the chip divided by the number of PDRs). The DDC circuitry is designed entirely using high level description and synthesized with standard cell libraries. However, Each PDR is placed over its own substrate isolation implant, as are all remaining DDC buffers and delays. Finally, each PDR contains a full custom decoupling

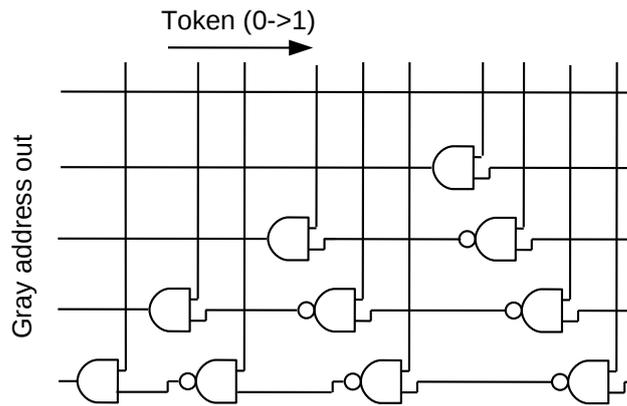


Figure 14: Example of Gray address thermal encoder. The encoder inputs are along the top and are initially all 0. As the token advances from left to right each successive input switches from 0 to 1. This causes the encoder output to present 00000, 00001, 00011, 00010, 00110, etc., where the rightmost bit is at the bottom of the figure. There is one gate per input.

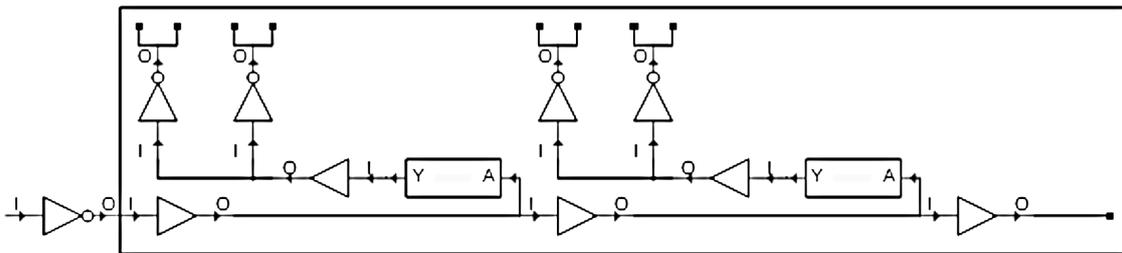


Figure 15: Simplified schematic of clock and trigger distribution in the DDC. The rectangles are delay elements.

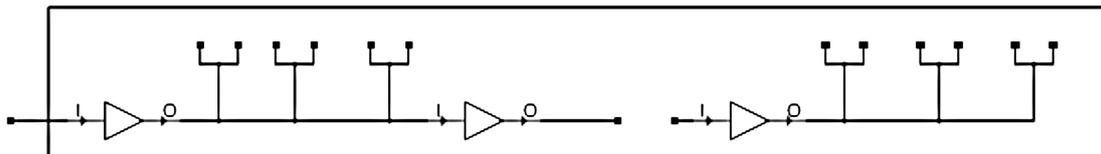


Figure 16: Simplified schematic of distribution non-critical timing signals in the DDC.

550 capacitance of ?? pF. The actual PDR power consumption after physical implementation was simulated to be $6.6 \mu\text{W}/\text{pixel}$ (average) in the typical process corner at 25°C and 1.2 V, with hit rate corresponding to 75 interactions per beam crossing at 3.7 cm radius, and 100 kHz trigger rate with latency of 120 crossings.

The EODCL distributes the read token, control signals, and data among the 40 DDCs. There is only one read token for the entire array. All 40 columns are controlled in parallel and read out
 555 sequentially. Despite the large size of the FE-I4, parallel readout was not needed to meet the trigger rate specifications. The EODCL contains simple logic to select each column for readout as shown

in Figure 17. A token similar to the DDC token runs along the EODCL and generates the column address based on its position.

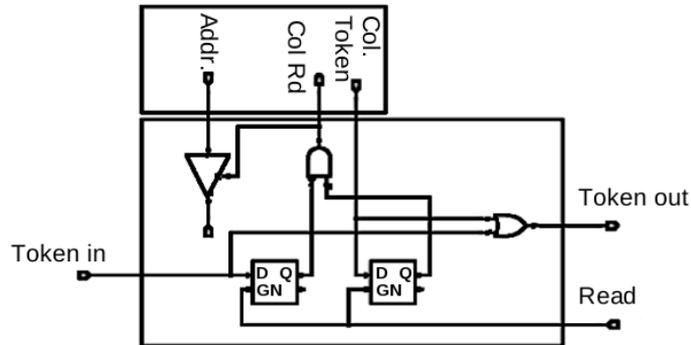


Figure 17: Simplified schematic end of column signal routing in EODCL

560 4.5 End of Chip Logic

The End Of Chip Logic is responsible for several tasks:

- Receive data from the columns,
- Unpack data, arrange into pixel pairs and re-pack for output,
- Temporarily store output data in a asynchronous Fifo,
- 565 • Generate the Bunch Counter value (BCID),
- Generate the Trigger Id,
- Generate multiple triggers,
- Merge service records into the data stream,
- Merge configuration read back records in the data stream,
- 570 • Receive bits from the pixel shift register, pack them and merge into the data stream.

All logic for these tasks is triplicated with majority voting at the output, to make it SEU safe. All data in this block are stored in Hamming Code for the same reason. All counters are triple redundant, with the value of each bit updated from the majority output on every clock.

575 A schematic of the EOCHL is shown in Figure 18. It is made up of the following circuit blocks, each one represented by a box in the figure: Read Out Controller, Error Handler, Reset Deglitcher, Data Formatter, and Shift Register. The Read Out Controller generates all the signals needed to read data from the pixel array using a state machine, receives all data, and prepares it for output to the data output block. Hit data are received from the EODCL and fed through the Data Formatter to first unpack them into single pixel values and then combine two pixels into one data

580 record as efficiently as possible. This is called dynamic phi pairing, explained by the following algorithm: (1) take all hits in the same column, including neighbor hits; (2) list them in ascending row; (3) use the first hit column and row address for the first data record, and place the ToT value in the first ToT field; (4) if the next hit has a row number greater by exactly 1, then place its ToT code in the second ToT field and advance to the following hit; (5) otherwise place the “no hit”
 585 code in second ToT field and process the next hit as a new record; (6) repeat until there are no more hits in the column. The Data Formatter also adds a header in front of the data, containing the BCID, the trigger ID, and a flag to indicate if any service records are ready to be read out. The data format including headers and all record types is described in detail in Section 7. The Error Handler receives error pulses from the rest of the chip, counts them in 32 separate categories (given in the
 590 Appendix), and produces service records to report errors off chip. The Shift Register is not actually a shift register, but rather the block that processes the output of the column shift registers and packs it into address and value records. The data from global configuration registers for read-back is also received by this circuit.

4.5.1 Readout Controller

595 Figure 19 shows a schematic of the Readout Controller. Data records are received from the Data Formatter, Shift Register, or Error Handler via the Data Concentrator. Each record is then Hamming coded and written into the FIFO via the Data Switch. The FIFO is 8 bits deep by 36 bits wide, including the Hamming code bits. The FIFO is written with the same system clock as used by the pixel array, but it is read out with the FIFO Read signal generated by the DOB. This allows using an
 600 asynchronous clock for data output. The output of the FIFO is Hamming decoded before sending to the DOB.

The data flow through the FIFO proceeds via the Input multiplexer to select data source, the Hamming Encoding, the Data switch, the FIFO proper, and finally the Hamming Decoder. The Input multiplexer has 3 data sources: hit data via the Data Formatter, Configuration Register Data
 605 (both value and address), and Service Records from the Error Handler. Additionally, the FIFO has a 4th input source which is the Bunch Counter and contains the data header fixed bits. The data flow through this block is combinatorial. The header bits are already Hamming Coded, while the Hamming code for all other data is calculated prior to writing into the FIFO.

The Data Switch has two inputs and one output. The inputs are Hamming encoded data or
 610 Header. The output is controlled by a register needed to avoid timing errors: when the fifo is full the register is frozen until the “full” signal is removed. The FIFO provides buffering between Data Formatter and the DOB. The write and read sides of the FIFO work in their own clock domain with double clock synchronization blocks for the addresses in between. This synchronization generates the Fifo_Full and Fifo_Empty signals. The Hamming decoder converts the 36-bit wide FIFO con-
 615 tents to the 3-byte wide (24 bits) data stream. The decoders can correct up to one error in each 8-bit output data word. Additionally, if an error is detected an error signal is sent to the Error Handler.

The Readout Controller has the following counters: trigger multiplication counter, level-1 trigger ID counter (L1_Trig_Id), bunch crossing counter (BC), L1 trigger input to EODCL counter (L1In), trigger request to EODCL counter (L1Req), and skipped trigger counter. Each counter is
 620 triplicated with majority voting logic on the output. Every clock cycle a new value is loaded into the counter from the output of the majority vote, so a SEU will be automatically corrected. Two

registers are used to keep track of triggers sent to the EODCL and pending for readout: the L1 register and the BC register. The L1 register is 16 bits (each triple redundant) and keeps track of the 16 possible trigger slots. For each trigger pulse sent to the EODCL the corresponding bit in the L1 register is set. The position of the bit for each trigger pulse is given by the L1In counter value. When event data for a given trigger have been read out, the corresponding bit is cleared. The position of the bit for the event being read out is given by the L1Req counter value. The BC register contains 16 Hamming coded words. Each word contains an 8-bit (plus Hamming code) bunch crossing ID (given by the BC counter value) and a 7-bit (plus Hamming code) level-1 trigger ID (given by the L1_Trig_Id counter value). There is a one to one correspondence between L1 counter bits and BC counter words. The values stored in the BC register are sent out as part of the Data Header. An “event” is labeled by these values.

When L1 trigger command is received by the chip, the Trigger Generator produces a burst of trigger pulses given by the the value programmed in the Trig_Cnt global register (see Appendix C). This is done by presetting a the 4-bit trigger multiplication counter to the Trig_Cnt value and, when a trigger command arrives, counting down to zero. During this time trigger pulses are sent to the EODCL (one per clock) and counted by the L1In counter. Each trigger pulse is half a period long and high during the low phase of the clock. All pulses in the burst are marked with the same Trigger ID in the BC register, which is the value of the L1_Trig_Id counter. This is a 7-bit counter incremented when trigger commands are received by the chip. The bunch crossing ID, on the other hand, is different on each pulse, given by the BC counter. This is an 8-bit counter of the 40 MHz clock. The BC counter is zeroed by the RD2bar reset and also by the bunch counter reset command.

The L1In is a 4 bit counter which serves as a write pointer for the L1 and BC registers, and its value is also sent to the EODCL to be used as an internal trigger identifier in the pixel array. The L1In counter is incremented for every L1 pulse sent to the EODCL. Note this is more frequently than every L1 trigger command sent to the chip when the trigger multiplier is set different to a value other than 1 (the value 0 results in 16 pulses). The L1Req is a separate 4-bit counter which serves as a read pointer for the L1 and BC registers, and is also sent to the EODCL in order to select all the data from this specific trigger. This counter is increased by the Readout State machine after an event is finished reading out. Both the L1In and L1Req values are only used internally and not copied to the output data stream.

The skipped counter counts trigger pulses not sent to the columns because the L1 register is full. These triggers are ignored. The counter is 8 bits. The read out of the counter is done by the command decoder. Reading the counter also clears its content.

4.5.2 Readout Processor

The Readout Processor is the state machine that organizes the readout cycle activities. Figure 20 shows a flow chart of the state machine. This orders the processing of hit data, configuration data, and service records. The first test point in the state machine checks if the data acquisition is enabled and if there has been a trigger for the given L1Req number. When both conditions are met a readout cycle will start. Once a readout cycle starts the event is always finished completely before any other action. Note that in FE-I4A there is no event timeout and it is possible for all pixels to have a hit at the same time, in which case the readout cycle will last a long time. The Read Out cycle has the following steps:

1. Wait 3 clocks for the token to arrive from the EODCL.
- 665 2. If Token is through, send Read pulse to the EODCL.
3. Wait 3 clocks for hit data and new token.
4. Place data in the Data Formatter and check token for more data.
5. If more data, repeat the steps 3 and 4 until token is false.
6. Check if a service word has to be sent (see below).
- 670 7. Go back to the starting point.

In case of no hit data the state machine will check if Configuration Address and Value words are pending. The Configuration Address is optional and can be disabled by a configuration register bit. When the Data Acquisition is disabled, multiple Configuration Address and Value words can be sent out in one block. This must be the case in order to process data from the column shift registers. A Service Request command always sends out 32 service words and a null word. A single Service Record will also be sent automatically at the end of each hit data event hit data, in case Service Records are pending. Note that even if error pulses have been received by the Error Handler, Service Records will not come out automatically unless there are triggers given to the chip which result in hit data output.

680 4.5.3 Error Handler

Logging of error signals is accomplished by 32 identical Error loggers in the Error Handler block. Each Error logger has a synchronous rising edge detector followed by a 10-bit counter. When a rising edge is detected, the Error output is set, and the counter is incremented. The counter stops at the maximum value of all 1's. The counter is reset during the read cycle. All 32 Error output signals are connected to an Error Control module. If any Error logger has detected an error, the module Error Control will send a Write_Service_Record signal to the Readout Controller. In the data stream, a service record will be added after the data header and a flag is set in the Data Header. The service record contains 16 bits of payload, consisting of the address of the Error logger and the value of the counter. This automatic service record generation can be masked off with the Error Mask register. Sending a ReadErrorReq signal will output 32 service records (regardless of the error mask bits) and will reset all the error counters (this signal is generated with the Global Pulse command).

4.6 Data Output Block

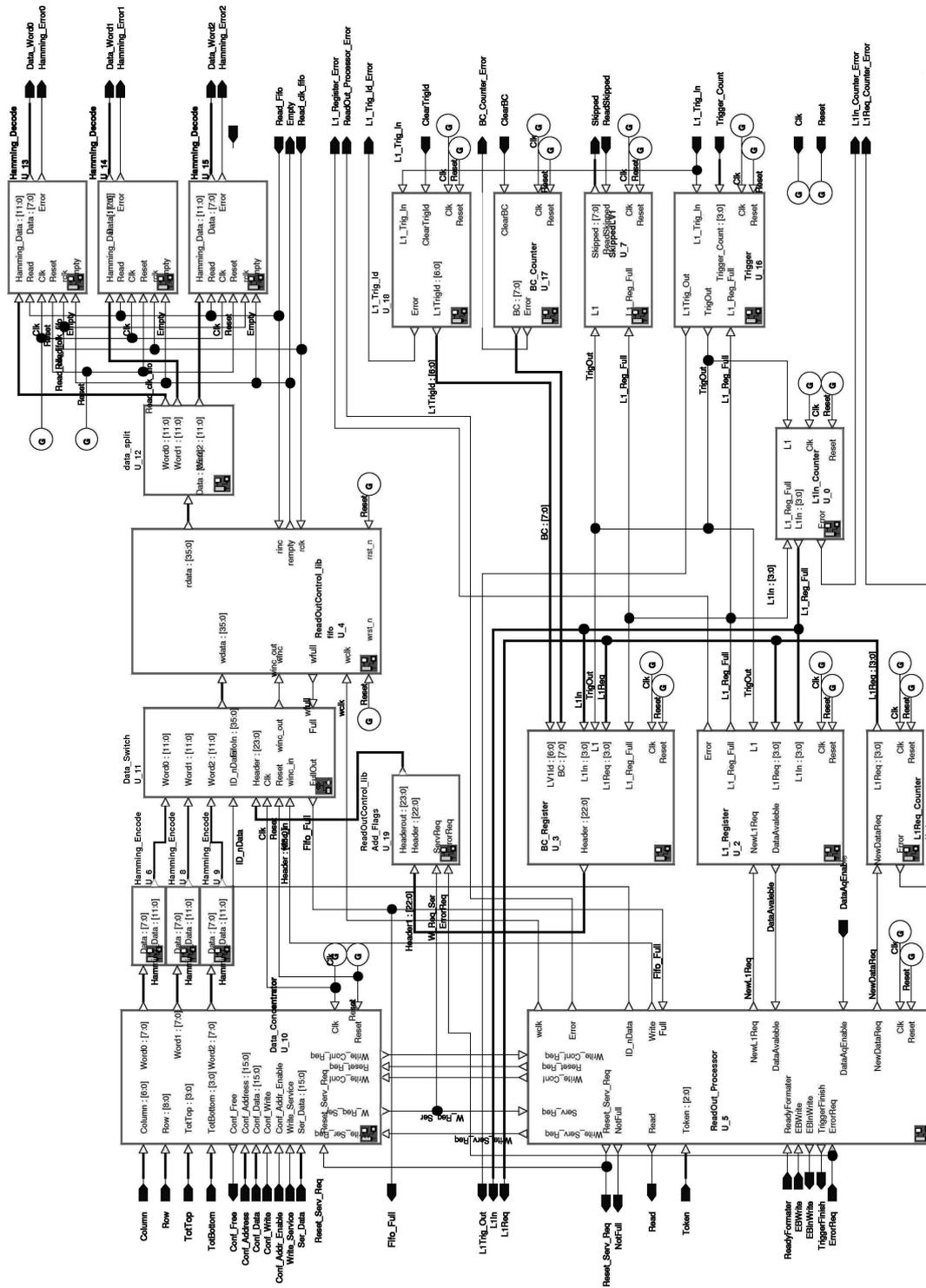


Figure 19: High level schematic of the End Of Chip Logic block

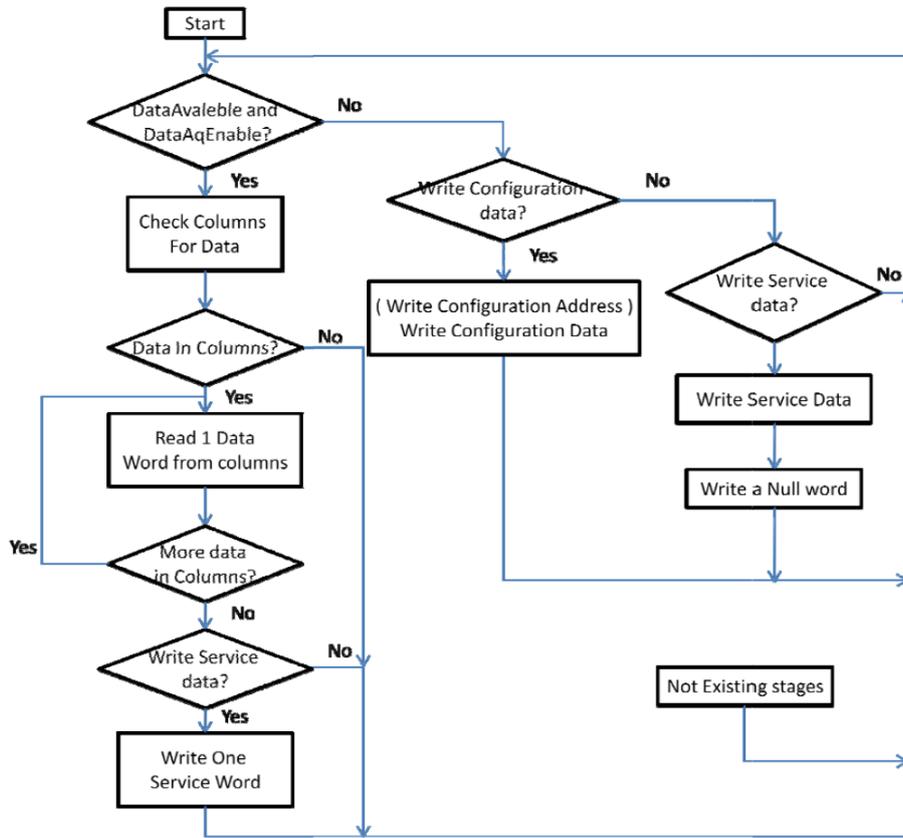


Figure 20: Flow chart of Readout Processor state machine.

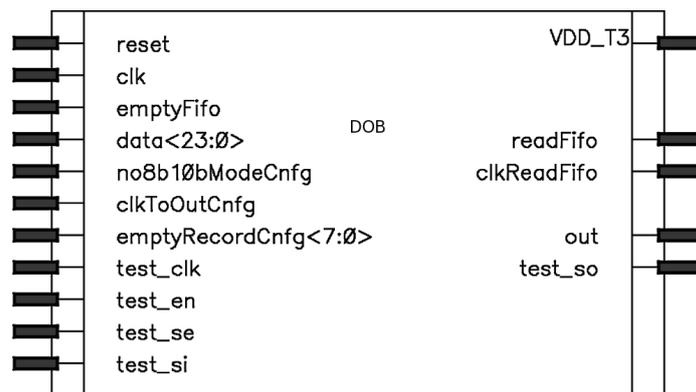


Figure 21: Data Output Block Symbol

4.7 Clock Generator

695 The clock generator block contains two parts: a Phase Locked Loop (PLL) core that generates different clock frequencies, and a multiplexer (MUX) output stage that selects what signal to send to each of two outputs going to the rest of the FE-I4 chip. The PLL core has a dedicated power pin at the chip level, as well as an enable signal in the chip global configuration— both must be present for operation. Figure 22 shows the circuit schematic. The PLL is a classical (type II) architecture with
700 a Phase Frequency Detector (PFD), a Charge Pump (CP), a Loop Filter (LF), a Voltage Controlled Oscillator (VCO) and Dividers (DIVs). The nominal oscillating frequency of the VCO in the PLL is $f_{VCO} = 640$ MHz. The multiplication factor of the PLL is $N = f_{VCO}/f_{REF} = 16$.

Internally dividing down a high frequency naturally leads to output clocks with a 50% duty cycle even for an unbalanced reference clock. In addition, a higher output frequency of the VCO
705 results in smaller capacitance values in the LF. The capacitances of the LF take up about one third of the area of the PLL core. The capacitors are of vertical natural capacitors (VNCAP) type from metal layers 1 to 3. The LP consists of three capacitors with capacitance values of 319 fF, 710 fF and 7.43 pF plus one additional 710 fF capacitor that decouples the supply voltages. The block uses standard library cells for all digital logic, placed in a common T3 deep implant for substrate
710 isolation. The custom circuits (PFD, CP, and LF) use triple well transistors for regular V_t and RF types.

The CLKGEN signals are single-ended CMOS (nominal 1.2 V). The nominal input reference clock is $f_{REF} = 40$ MHz. The PLL generates $\times 8$, $\times 4$, $\times 2$, and $\times 1$ clocks waveforms with 50%
715 duty, with a constant phase relationship to the input reference (the exact phase difference will be process and temperature dependent). Each multiplication ratio has an independent enable so that switching noise can be minimized by disabling buffers for unwanted ratios. The $\times 16$ f_{VCO} is used to synchronize all lower frequency outputs, and so is slightly ahead in phase. The two CLKGEN outputs (CLK0_OUT and CLK1_OUT) can each provide any of the internally generated clocks (40M_se, 80M_se, 160M_se, 320M_se, but not the 640 MHz clock signal), the input reference
720 clock (RefCLK) or an auxiliary clock (AuxCLK) that is an external input for the CLKGEN block. The output selection is controlled by a global configuration register (6 bits total, 3 for each output). The independent power makes it possible to completely disable the PLL and still operate the MUX to provide either RefCLK or AuxCLK to the rest of the chip.

CLK0_OUT feeds the data output block and thus controls the output data rate, while CLK1_OUT
725 feeds the end of chip logic and the digital array, which nominally run at 40 MHz. The $\times 1$ ratio is desirable for CLK1_OUT, because it will have 50% cycle and low jitter even if the reference clock is of poor quality. Note that the generated clocks are multiples of the input reference clock, thus, for example, the name 80M_se really means $f_{REF} \times 2$ and not exactly 80 MHz.

Two outputs (Fb2Fast and Ref2Fast) provide error flags if the PLL does not acquire a stable
730 lock on the input reference clock. Internally the CP of the PLL is controlled by a signal called UP and a signal called DN. When the PLL has acquired a lock, both UP and DN signal lines will stay high only for a very small fraction of the time of the reference clock period. If one of the signals is high for a longer time, that indicates that the control loop senses a need to adjust the VCO oscillation frequency. This corresponds to a loss of lock. If the VCO oscillates too fast with
735 respect to the multiplied reference clock ($N \cdot f_{REF}$), the signal Fb2Fast will be high. If the VCO

oscillates too slow with respect to the multiplied reference clock, the signal Ref2Fast will be high. During start-up, one or both will be high until lock is established- typically less than $5 \mu s$. These lines are monitored within the chip and rising edges counted as errors and reported (see Section 10). If Fb2Fast or Ref2Fast are permanently high this might indicate that the PLL is out of locking range (see Table 8), which may be due to the reference clock input or the PLL supply voltage level - a higher supply voltage will result in faster oscillation of the VCO.

740

The performance specifications of the CLKGEN block, based on simulations and on measurements done on a demonstrator chip are listed in Table 8. The two bias currents shown in the table are provided by the BIASDACS block and programmed with global configuration registers. They can also be overridden by providing the bias current directly to the corresponding pads. Both currents flow into NMOS current sinks. The CLK0_OUT output of the CLKGEN block can be directly monitored on the chip LVDS output by putting the DOB block into clock loop back mode, and one can make use of this feature for standalone operation. The required contacts and settings for operating the CLKGEN block as a standalone circuit are summarized in Table 9.

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The measurements on a demonstrator chip are limited by available instruments to input reference clock jitter RMS of 2 ps and output frequency of 160 MHz. However, since the lower frequency clocks are internally generated from the higher frequency clocks, the encouraging results

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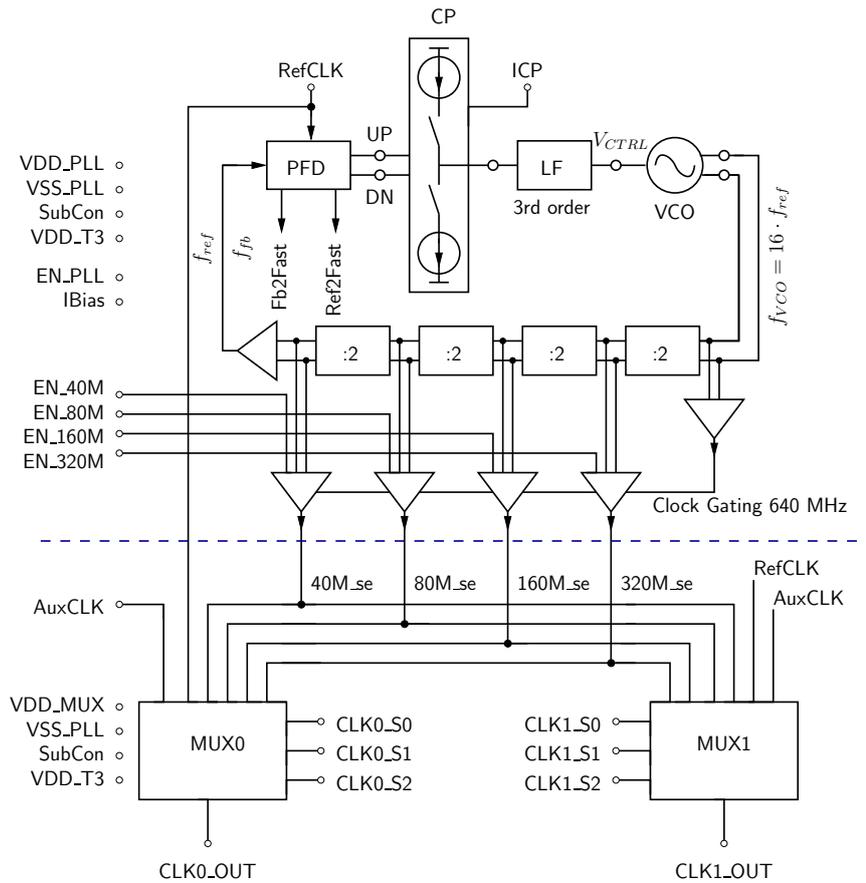


Figure 22: Clock Generator Schematic

indicate proper functioning of the (unobserved) higher frequency clocks. These measurements also include the performance characteristics of the LVDS drivers integrated into the output pads of the demonstrator. The results are summarized in Table 10.

The CLKGEN single event transient (SET) cross-section is unknown as it could not be simulated. The cross-section will strongly depend on the layout. None of the CLKGEN sub-blocks has been designed with special SET-hardened architecture. However, in case of a loss of lock due to SET, the PLL core will reacquire lock in the same way as it does during normal settling. SET recovery was simulated by charge injections of 3 pC in 1.5 ns at various nodes of the PLL core circuit. In all cases lock was reacquired in times of order 1 μ s.

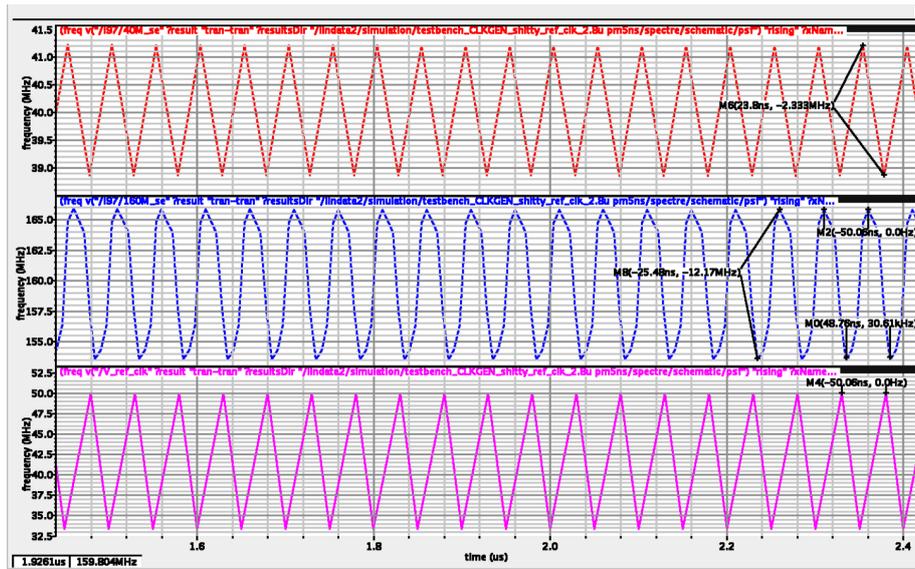


Figure 23: CLKGEN output frequency (top: $\times 1$, middle: $\times 4$) for bottom input reference clock having a variation of ± 5 ns

In the IBL application of FE-I4 the 40 MHz input reference clock will be delivered from a

Specification	Unit	min	nom	max
Supply Voltage (V_{DD_PLL} , V_{DD_MUX})	V	N/A	1.2	1.5
Clock Multiplier N	-	-	16	-
General Bias I_{BIAS}	μ A	60	80	250
Charge Pump Reference current I_{CP}	μ A	N/A	10	N/A
Input Reference Clock Frequency f_{REF}	MHz	21	40	61
VCO Oscillation Frequency f_{OSC}	MHz	336	640	976
Peak Current Consumption I_{PEAK}	mA	4.6	5.3	5.7
Average Current Consumption I_{DC}	mA	2.7	3.4	3.7
Settling Time (2% accuracy) t_{SETTLE}	μ s	0.9	0.9	1.1

Table 8: Performance Specifications for the CLKGEN Block

custom optical to electrical converter called DORIC. The DORIC generated clock behaves like a superposition of two 20 MHz clock signal that do not have a fixed alignment in time but rather vary by ± 5 ns upon start-up and by ± 0.5 ns after parameter tuning. The ± 5 ns (± 0.5 ns) variation of the period length between two consecutive edges corresponds to a input reference clock of the PLL varying between 33 MHz (39.2 MHz) and 50 MHz (40.8 MHz) in contrast to the ideal 40 MHz. Simulation results for the worst case are depicted in Figure 23. It can be seen that the PLL smooths out the frequency variation of the input reference clock by about a factor of 7.

4.8 Command Decoder

The command decoder (CMD) is responsible for interpreting the serial commands to control the chip. All valid commands can be found in Section 6.3. The CMD circuit is completely synchronous using the input clock provided externally with no option to use a different clock. The serial input is sampled on the rising edge of the clock and each sample is interpreted as a bit. The input bit stream is continuously parsed searching for valid command patterns. Patterns not corresponding to a command sequence are ignored. Once a command is found the full number of bits expected for that command are recorded before searching for a new command. The processing is done by a state machine. The CMD control generates internal logic signals that control the various blocks of the chip. All internal signals going to other blocks are synchronized with the rising edge of the clock. The CMD symbol is shown in Figure 24.

Internal net	Wire bond Pad(s)	Configuration register
VDD_PLL	VDD_PLL	–
VDD_T3	VDDT3_Shield	–
VDD_MUX	VDDD2	–
VSS_PLL	GND_PLL	–
SubCon	VSS	–
IBias	PIIbias_P	PIIbias or SRAB 24-31
ICP	PIIcp_P	PIIcp or SRAB 32-39
EN_PLL	–	EN_PLL
EN_320M, EN_160M	–	EN_320M, EN_160M or SRAB 80-81
EN_80M, EN_40M	–	EN_80M, EN_40M or SRAB 88-89
CLK0_S2 - CLK0_S0	–	CLK0 or SRAB 82-84
–	–	clk2OutCnfg
RefCLK	Ref_Clk_N	–
	Ref_Clk_P	–
CLK0_OUT	DOB_OUT_N	lvdsDrvEN
	DOB_OUT_P	lvdsDrvEN

Table 9: Summary of required connections and settings for standalone operation of the clock generator block. Internal nets refer to the schematic. See the appendix for the specific number of each wire bond pad or configuration register.

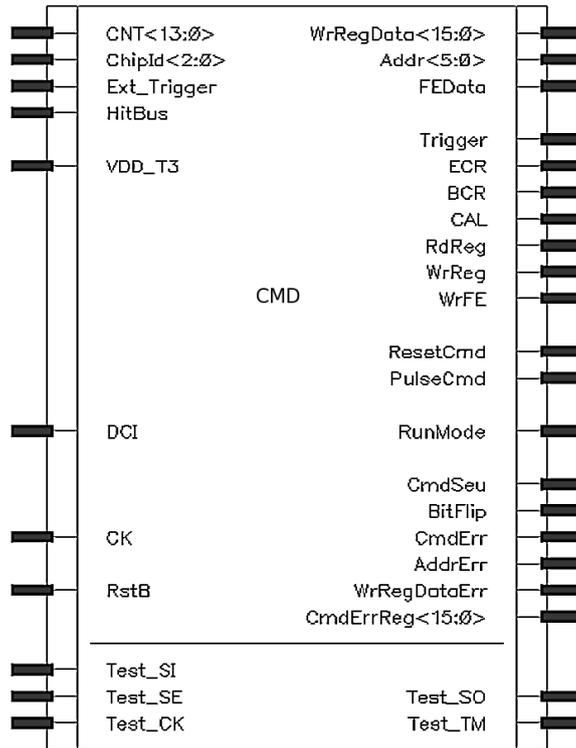


Figure 24: Command Decoder Symbol

The CMD state machine is triplicated, so that there are actually three distinct copies inside the FE-14 and all CMD outputs are selected with a majority voting circuit. Each copy processes the input serial stream independently and in parallel. Because each state machine returns to its idle state after a finite amount of time (usually after a small number of clock cycles), there is a very small probability that bit-flips in any state machine will cause the majority voting circuit to be incorrect. Errors can happen only if SEU bit-flips occur in two different state machine status registers within the time it takes either one to return to the idle state. Even in such a case, as soon as the first of the two affected state machines returns to its idle state, the majority voting output would again be correct. In addition to the majority voting circuit there is an XOR tree of all triplicated outputs

	Reference in	CLKGEN out				
Frequency [MHz]	40	40	80	160	320	640
Jitter pk-pk [ps]	44	82	74	94	70	106
σ -Frequency [kHz]	6.5	19	79	258	1710	8100
σ -Period [ps]	4.1	12	12	11	17	20
Duty Cycle Deviation [%]	–	0.24	0.33	0.1	n.m. ¹	n.m.

1: n.m. stands for not measured

Table 10: Measurements of CLKGEN Signal Integrity

790 in order to calculate, once every clock cycle, if there has been a detection of a SEU anywhere inside the Command Decoder. Whenever this happens a 5-bit counter is incremented and its non-overflowing value is stored inside the CMD in register CmdErrReg[15:10]. Additionally, a pulse on the CmdSeu internal net is sent to the End of Chip Logic (EOCHL), which will independently count the errors and produce a service record.

795 The command communication protocol is designed to allow single bit flips on the input serial stream without generating errors. If such a BitFlip is detected when there are no commands recognized, a non-overflowing, internal counter is incremented and its value is stored in CmdErrReg[9:5]. If the BitFlip occurs during a Trigger command the Command Decoder will detect it and increment a 3-bit, non-overflowing counter stored in CmdErrReg[4:2], but still decode the corresponding trigger correctly. In addition to that there is the ability to detect a BitFlip during the Fast or Slow header. The occurrence of these events is flagged (but not counted) in the CmdErrReg[1:0]. In addition to that the logical OR of these three errors (Trigger, Fast header, Slow header) will generate a CmdErr error signal sent to the EOCHL.

805 Internally, the CMD controls the 6-bit global register address bus and the 16-bit register write value. The Address and the WrRegister storage inside the CMD are also triplicated or SEU protected. This triplication includes error correction whenever triple redundant mismatch is detected. If an error is detected the AddrErr and WrRegDataErr signals are generated and sent to the EOCHL in order to allow the counting of these types of errors.

810 The whole CMD can be reset using the external RD1bar, negative logic signal. However, since the CMD is completely synchronous, the clock must be running in order for to reset to operate. No serial command exists for resetting the CMD state machine. The global reset command produces BCR and ECR signals that are sent to the EOCHL and also causes a reset of the internal CMD error counters described earlier. The ECR command does not clear the CMD error counters.

815 To allow quality assurance testing that is sensitive even to failures that would be masked by the triple redundant design, a Scan Chain has been implemented. There are four dedicated Scan Ports that can be accessed via the IOMUX block.

- Test_SE: Scan Enable port. Scan circuitry is active when it is high.
- Test_CK: Scan test clock.
- Test_SI: Input of the scan chain circuitry.
- 820 • Test_SO: Output of the scan chain circuitry.

All flip-flops in the CMD circuit are included in the scan chain when in test mode. There are 246 D flip-flops and 224 of them are implemented as multiplexed scan flip-flops, while the remaining 22 are already connected as shift registers inside the design.

4.9 Global Configuration Memory

825 4.10 EFUSE

4.11 Pulse Generator

The PULSGEN block can be thought of as a pulse generator instrument, with a digital and an analog output that can be routed to the pixel array. The input capacitance of the full array has

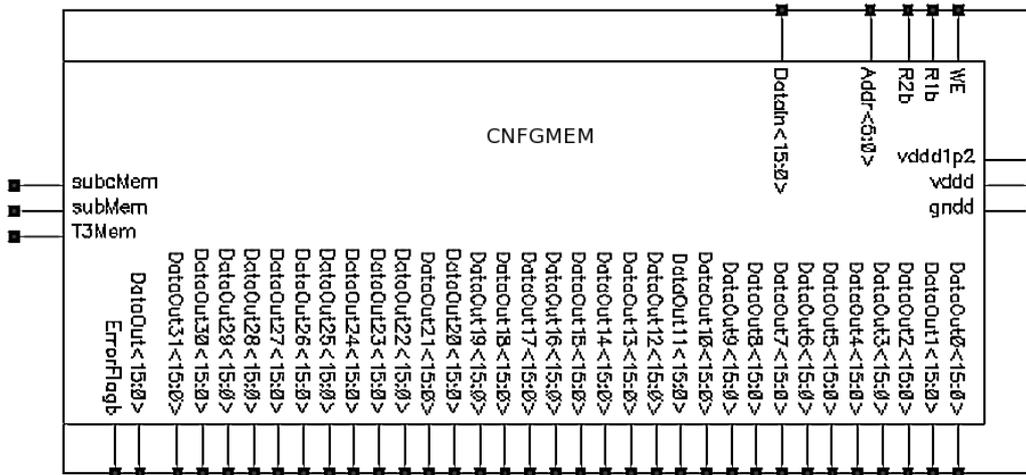


Figure 25: Configuration Memory Symbol

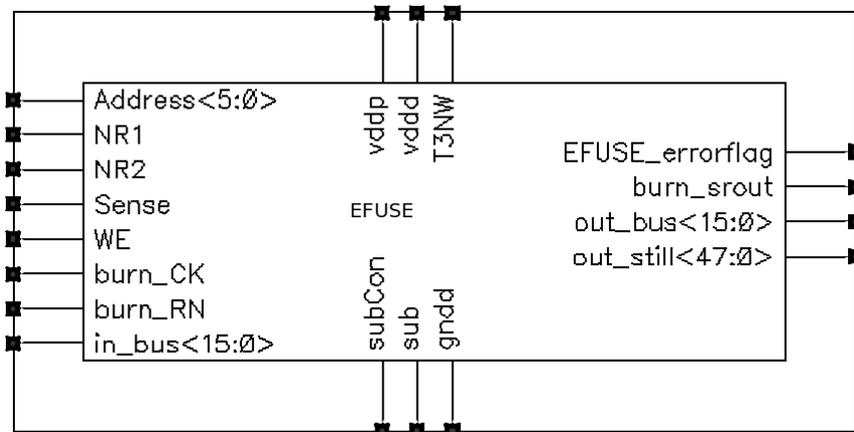


Figure 26: EFUSE Symbol

830 been estimated from 40 pF to 80 pF. The analog pulse fall time must be faster than 10 ns to avoid any ballistic deficit (charge injection happens on the falling edge) and the rise time must be hundreds of microseconds to avoid any baseline due to reverse charge injection. The PULSEGEN has a programmable delay line with range of 50 ns and 1 ns or better resolution. In practice the PULSEGEN generates a DC voltage and a gate signal (with programmable delay) that controls 41 end-of-double-column choppers in parallel. This results in a fast fall time. The slow rising back to quiescent DC is ensured by a very weak PMOS transistor in triode mode. The rise time is adjusted by varying the size of the PMOS transistor (implemented as an array). The programmable delay is generated by a voltage ramp and a comparator. The discriminator threshold is fixed and the ramp rate is adjustable. The ramp uses a current supply from the bias generator and can be disabled by setting this current to zero. Varying the ramp current results in the delay changing non-linearly (as the inverse of current). Instead, the current can be fixed and a divider in the ramp generator can be varied, resulting in a linear delay change with divider setting. Setting the divider to its maximum value disables it. The entire pulse generator can also be bypassed, allowing external injection. For

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840

external injection a digital pulse and DC voltage, or an external analog pulse, have to be supplied. A block diagram of the PULSEGEN block is shown in Fig. 27. The distribution of signals to columns is illustrated in Fig. 28. Note that the same digital pulse output can be used for digital injection or to control the chopper circuits for analog injection. While the delay is adjustable, the width of the digital pulse is simple equal to the width of the pulse used to trigger the PULSEGEN, which can be produced by the CMD CAL command or by a global pulse command (either CMD or external).

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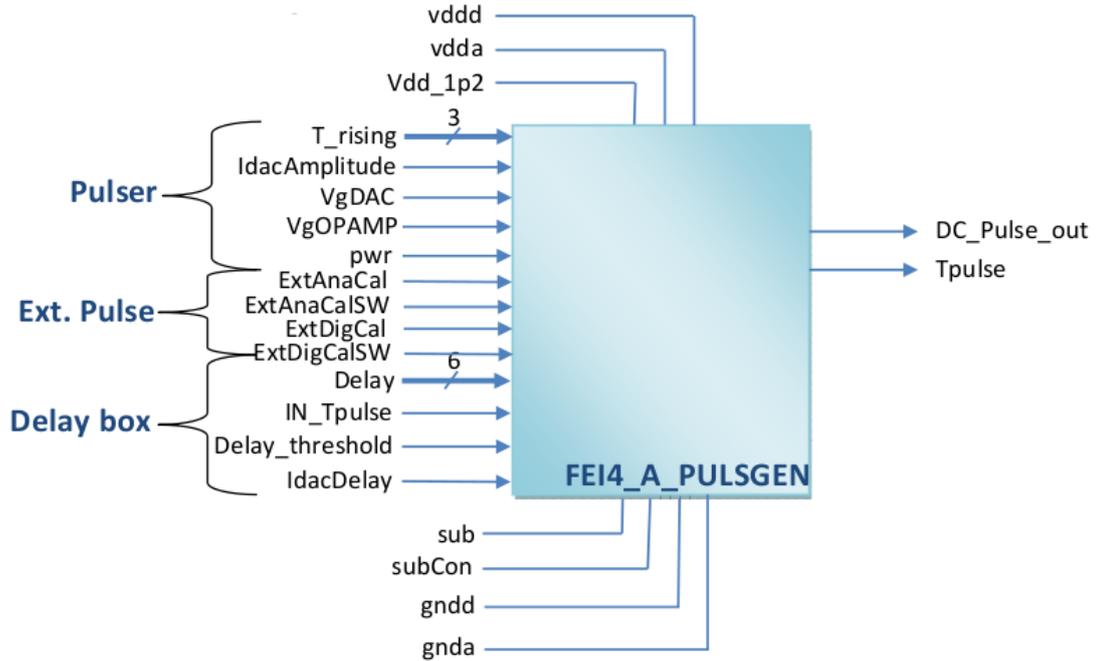


Figure 27: Block diagram of the PULSEGEN block.

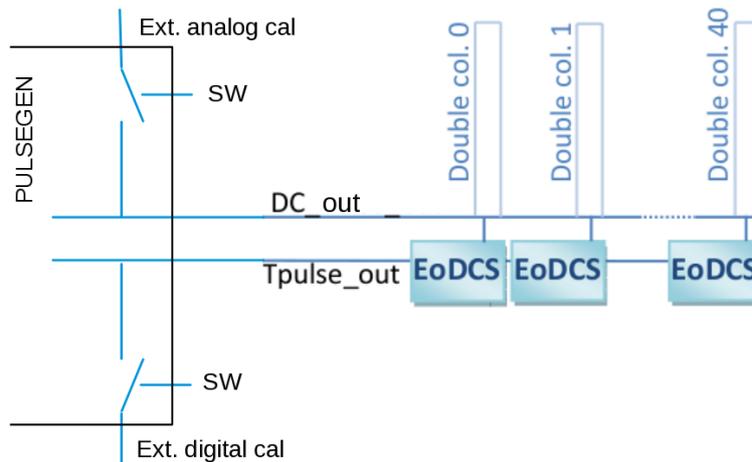


Figure 28: Distribution of the PULSEGEN signals to the columns.

A diagram of the delay generator is shown in Fig. 29. It shows the current divider, ramp gen-

erator and discriminator. The threshold voltage is tied to the voltage reference, which is internally set to $V_{DDA}/2$ in FE-I4A. The current divider uses a NMOS mirror followed by a programmable, unbalanced PMOS mirror to divide the input current depending of the value programmed. The output current is given by eq. 4.1,

$$I_{out} = \left(1 + \frac{1}{10N}\right)I_{in} \quad (4.1)$$

where N is the input code (6 bit), I_{in} is the input current supplied by the bias generator block, and I_{out} is the output current. Setting N to its maximum value will actually bypass the divider entirely, making $I_{out} \equiv I_{in}$.

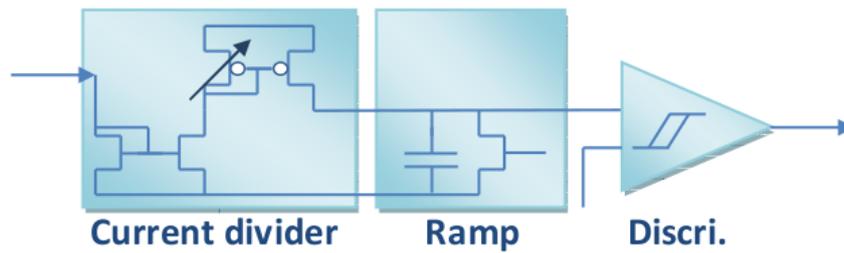


Figure 29: Diagram of the delay generator in the PULSEGEN block.

The ramp generator is a simple capacitance C with a charge-compensated injection switch. When the T_{pulse} signal is low, the capacitance is shorted by the switch and the output ramp signal is tied to ground. When T_{pulse} goes high, the input current charges the capacitance giving a ramp slope I_{out}/C . When the current divider is used to set the delay, the input current I_{in} defines the step size, and the delay is simply equal the the divider setting times the step size (with small nonlinearities shown below), plus a constant offset predicted to be 18 ns. The simulated value of step size vs. input current is shown in Fig. 30, while the differential and integral nonlinearity simulation predictions are shown in Fig. 31. When the divider is bypassed (by programming the maximum value), the simulated delay vs. input current is shown in Fig. 32.

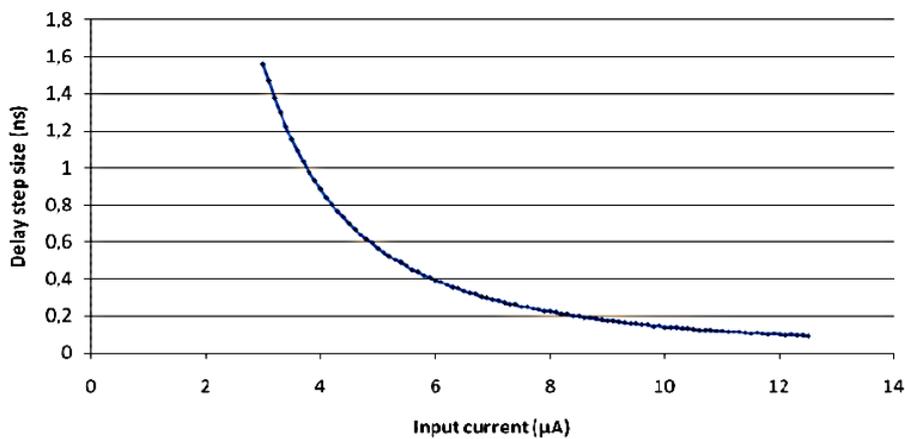


Figure 30: Simulated delay step size vs. input current.

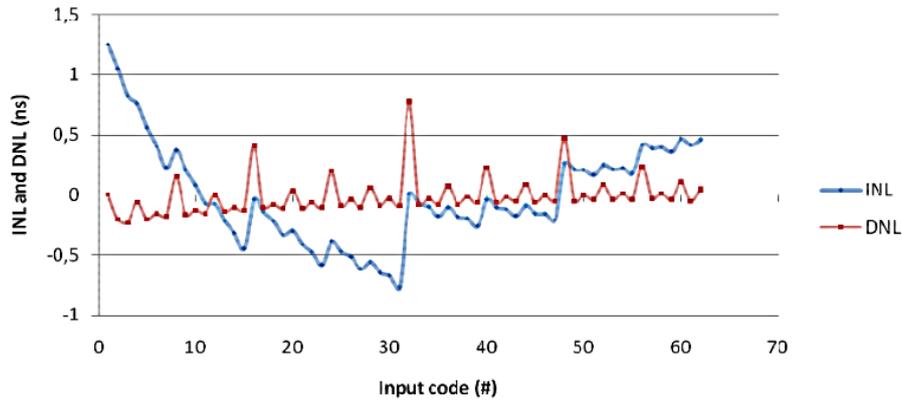


Figure 31: Simulated differential and integral nonlinearities of the delay generator when using the current divider.

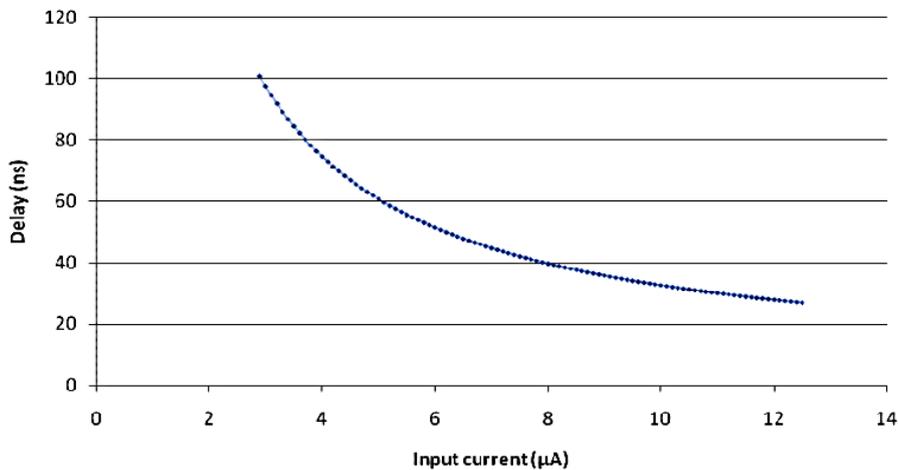


Figure 32: Simulated delay as a function of input current when the current divider is bypassed.

The DC voltage output is generated in two stages: a current to voltage converter to transform an input current to a rail to rail output voltage, followed by a sense circuit to correct the voltage for an expected offset due to the leakage current of the pixel matrix. The sense circuit also serves as a high impedance output leading to the required long rise time of the injection pulse at the pixel inputs.

870 The input current is provided by a 10-bit DAC in the bias generator (not part of the PULSEGEN block). The current to voltage converter is based on the generic FEIA_A_OPAMP block, described separately. The circuit is a resistor, chosen to produce 750 mV at maximum current, followed by a non-inverting gain 2 amplifier, to achieve rail-to-rail output (Fig. 33(a)). The cascade transistor is there to present a constant voltage to the output of the DAC supplying the current. The deviation

875 of the output from a linear ($V=I_{in} \cdot VDD/I_{max}$) at different temperatures, from simulation, is shown in Fig. 34.

The output voltage must have high impedance to produce a long rise time to DC quiescent after each falling edge. This high impedance leads to an offset due to leakage current in the large matrix

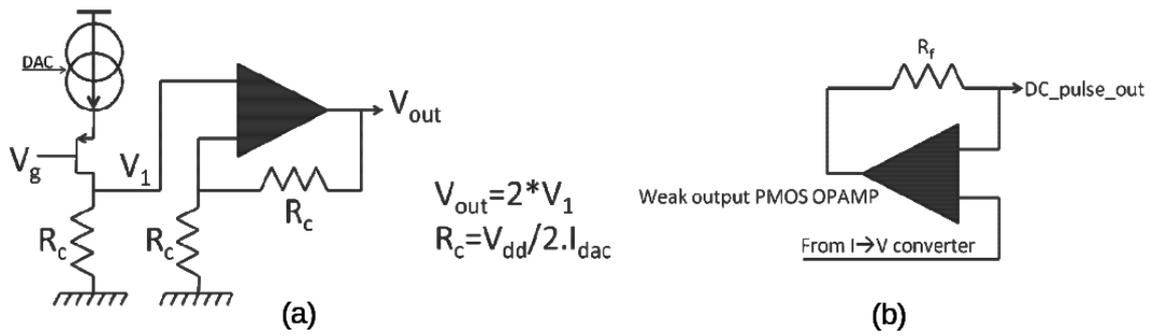


Figure 33: Schematic of (a) the current to voltage converter, and (b) the output sense circuit.

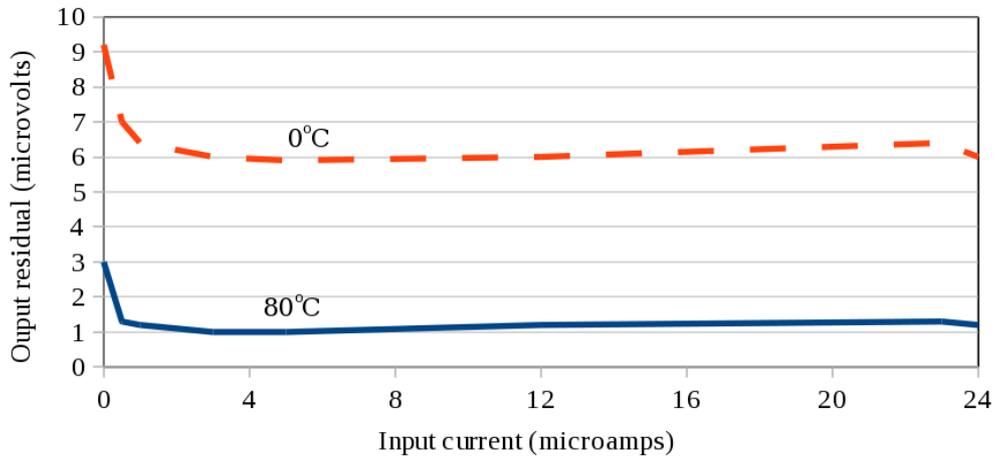


Figure 34: Simulated output voltage residual of current to voltage converter.

of pixels. A passive high impedance output would have an offset of over 100 mV due to pixel
 880 leakage. Therefore, an active feedback system senses the leakage current and compensates for the
 offset. The compensation uses a modified version of the FEI4_A_OPAMP with a weak output
 connected as shown in Fig 33(b). A row of 8 switchable PMOS is used to allow 3-bit control rising
 edge slope. A 100 k feedback resistor increases the output impedance. The rise time from 0 to 1 V
 varies from 25 μ s for 000 setting to 750 μ s for 111. A simulation of the fall time when driving the
 885 full array, as seen by one arbitrary pixel, is shown in Fig. 35. Four process corners are overlaid in
 the same plot.

4.12 Other Circuitry

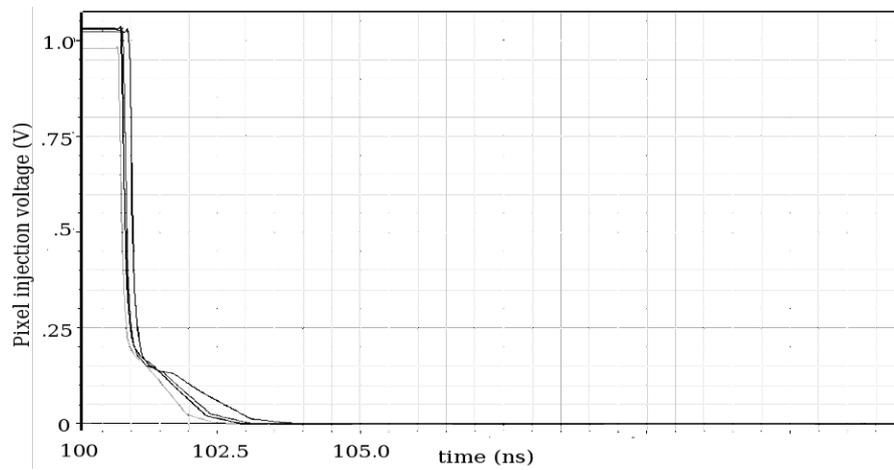


Figure 35: Simulated fall time in 4 process corners, when driving the full pixel array. An arbitrary delay value is shown, with the PULSEGEN triggered at $t=0$.

5. Peripheral Circuits

5.1 ESD Protection

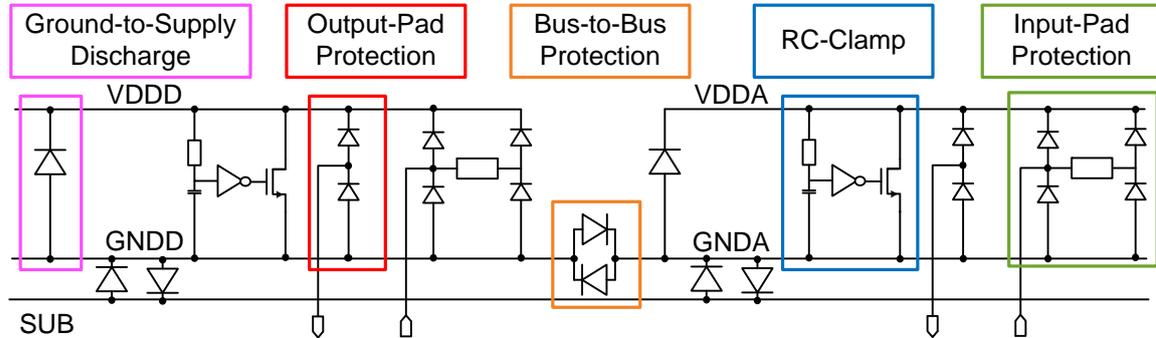


Figure 36: ESD strategy applied to the FE-I4 pad frame

890 An ESD event is the abrupt discharge of static charge which is induced by human handling or contact with machines. An IC might get exposed to an ESD event during all phases of life-time starting with chip fabrication and extending to the various stages of assembly at system level and daily usage. In a typical work environment, a charged human body can lead to an electrostatic potential of up to 4000 V which during contact with a grounded object like an IC pin results in a discharge for about 100 ns with peak currents in the ampere range. Since the voltage levels that arise during an ESD event exceed the breakdown voltages of transistors and other components integrated on the chip, the implementation of a protection strategy is mandatory to avoid device destruction. The protection objective is to provide a discharge path of least impedance to ground through devices which have been designed to withstand large currents. During the discharge process the appearance of high voltage drops on the wires of the ESD network has to be avoided. High voltage drops would cause an ESD current flow into the sensitive internal circuits which would then be harmed.

900 The ESD protection strategy for the FE-I4 readout chip shown in Fig. 36 is based on recommendations of the process vendor. The applied strategy follows a non-self protecting approach which means that additional ESD devices are added in parallel to the I/O circuits. In case of the FE-I4 chip, the added ESD circuitry is formed by a double-diode network which connects the I/O pin to the supply rails by reverse biased diodes. During an ESD event of positive voltage the upper diode conducts a current to the positive supply rail while during an ESD event of negative voltage the current flows through the lower diode and originates from the ground bus. Due to the fact that the diode junction capacitance increases the capacitive load at the I/O pins, the diode dimensions have to be balanced between the demands for robust ESD protection and for high I/O circuit bandwidth. Input pads which provide connection to transistor gate electrodes are equipped with additional ESD structures to avoid the breakdown of the transistor gate-oxide during an ESD event. A series resistor and an additional secondary diode pair of smaller diode area is added to the primary double-diode network. The series resistor and the on resistance of the second diode pair form a voltage divider. Hence the voltage across the conducting diode of the primary diode network is reduced if the series resistor is higher than the on-resistance of the secondary diode pair.

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To provide an ESD current path from the positive supply voltage to the ground bus, an RC-triggered power clamp is connected between the supply rails. During normal operation the NMOS transistor of the RC-clamp circuit is switched-off whereas the NMOS transistor is switched-on during the transient pulse of an ESD event. ESD events can also induce a current flow into the ground pin. To avoid the current flow through parasitic diodes of the internal circuitry, dedicated ground-to-supply discharge diodes are added in parallel to the RC-clamp circuit. Since the diode junction capacitance is not harmful to the power supply bus, the diodes can be large without an impact on the chip performance.

The supply voltages of the FE-I4 chip are organized in several supply domains. In addition a dedicated ground rail is used for the definition of the substrate potential. Since an ESD discharge might cross the supply domain boundaries, it has to be avoided that the discharge happens through the connections which the internal sensitive circuitry has across the supply domains. For this reason a bus-to-bus protection circuit composed of an antiparallel connected diode pair is placed between the ground busses of the different supply domains and between the ground busses and the substrate rail which provides a discharge path of low impedance in both directions. Amongst others, the separation of the supply voltage into an analog and a digital domain is motivated by concerns related to crosstalk and noise. Due to the fact that the junction capacitance of the antiparallel connected diodes re-couples the supply rails to some degree, the choice of the diode dimensions is a trade-off between ESD reliability and isolation efficiency.

5.2 LVDS Driver

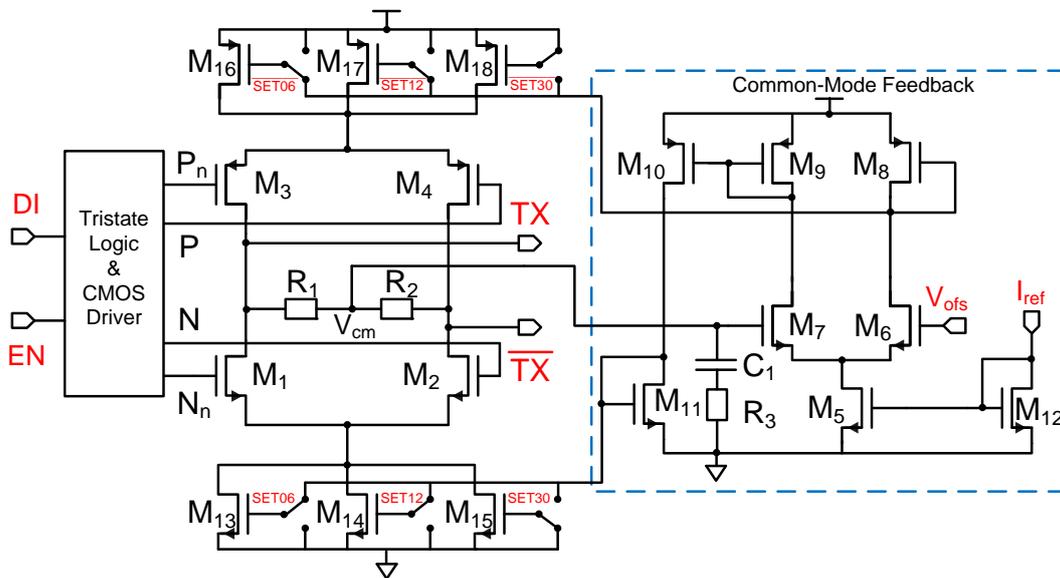


Figure 37: Schematic of the LVDS driver with common-mode feedback and adjustable signal current

The LVDS driver shown in Fig. 37, has a standard circuit architecture adapted to lower supply voltages with the possibility of signal current magnitude adjustment. The driver implementation is based on the common four transistor switch scheme arranged in a bridge configuration. When

Ports	Type	Nominal Value	Description
vddLvds	Power	1.2 - 1.5 V	
vddT3	Power		T3 Well Isolation Voltage
gndLvds	Ground		
gndSub	Ground		Substrate Voltage
sub	Ground		Substrate
I_{ref}	Analog	60 μA	Bias Current
V_{os}	Analog	vddLvds/2	Defined Offset Voltage
V_{cm}	Analog		Derived Common-Mode Voltage
TX		$I_{out} = \pm I_{06} + I_{12} + I_{30}$	Non-Inverted Signal Output
TXn		$I_{out} = \mp I_{06} + I_{12} + I_{30}$	Inverted Signal Output
DI	Digital		Data Input
EN	Digital		Enable Output Signal
SET06	Digital		Output Current Setting ($I_{06} = I_{ref} * 10$)
SET12	Digital		Output Current Setting ($I_{12} = I_{ref} * 10$)
SET30	Digital		Output Current Setting ($I_{30} = I_{ref} * 30$)

Table 11: LVDS driver Ports

DI	EN	N	Nn	P	Pn	Out
0	0	0	0	1	1	Z
1	0	0	0	1	1	Z
0	1	0	1	0	1	0
1	1	1	0	1	0	1

Table 12: Tristate-logic truth table

940 transistors M1 and M4 are switched-off and transistors M2 and M3 are switched-on, the polarity of the output current and in turn the polarity of the differential voltage is positive. In the inverted case, M1 and M4 are switched-on and transistors M2 and M3 are switched-off and the polarity of the output current is reversed. The choice of the dimensions of the switch transistors M1 - M4 corresponds to a trade-off between on-resistance and capacitive load for the CMOS drivers which generate the switch signals. A small on-resistance is desired to get a small voltage-drop across the switch transistors. This is important especially for small supply voltages due to the fact that the switch transistor voltage drop decreases the dynamic range of the differential and the common-mode signal. On the contrary, a small on-resistance is reached for wide transistor geometry which gives rise to larger capacitive load and increased power consumption. The transistor on-resistance has been chosen to generate a voltage drop of 50 mV for a signal current of 3 mA.

950 The common-mode voltage is sensed by means of a high ohmic voltage divider which is formed by resistors R1 and R2 of 100 k Ω each. The common-mode voltage is fed to the common-mode feedback circuit which compares the common-mode voltage with the applied offset voltage V_{os} by means of a NMOS differential pair. The biasing voltages of the NMOS transistors M13, M14, and M15 and the PMOS transistors M16, M17, and M18 are steered by the common-mode

feedback such that the applied offset voltage V_{os} is enforced. The common-mode feedback loop has been stabilized by a pole-zero compensation network formed by R3 and C1. For short-distance communication, functionality has been added to decrease the magnitude of the signal current. By setting configuration SET06, SET12 and SET30 bits, the gates of transistors M12-M14 can be switched between the biasing voltage provided by transistor M11 and the ground potential while the gates of transistors M15-M17 can be switched between the biasing voltage provided by transistor M8 and the supply voltage. For a bias current $I_{ref} = 60\mu A$, the output current is adjustable from 600 μA to 3 mA.

A third high-ohmic state at the LVDS output is reached by opening all switching transistors M1 - M4 at the same time. The gates of transistors M1 - M4 are controlled independently by dedicated signals P,Pn, N and Nn. A tristate logic block sets the signals at the gates of the switching transistors according to the truth table shown in Table 12 depending on the logic level of the enable (EN) and the data input (DI) signal. The third high-ohmic state allows to multiplex data of several LVDS drivers onto the same transmission line.

970 **5.3 LVDS Receiver**

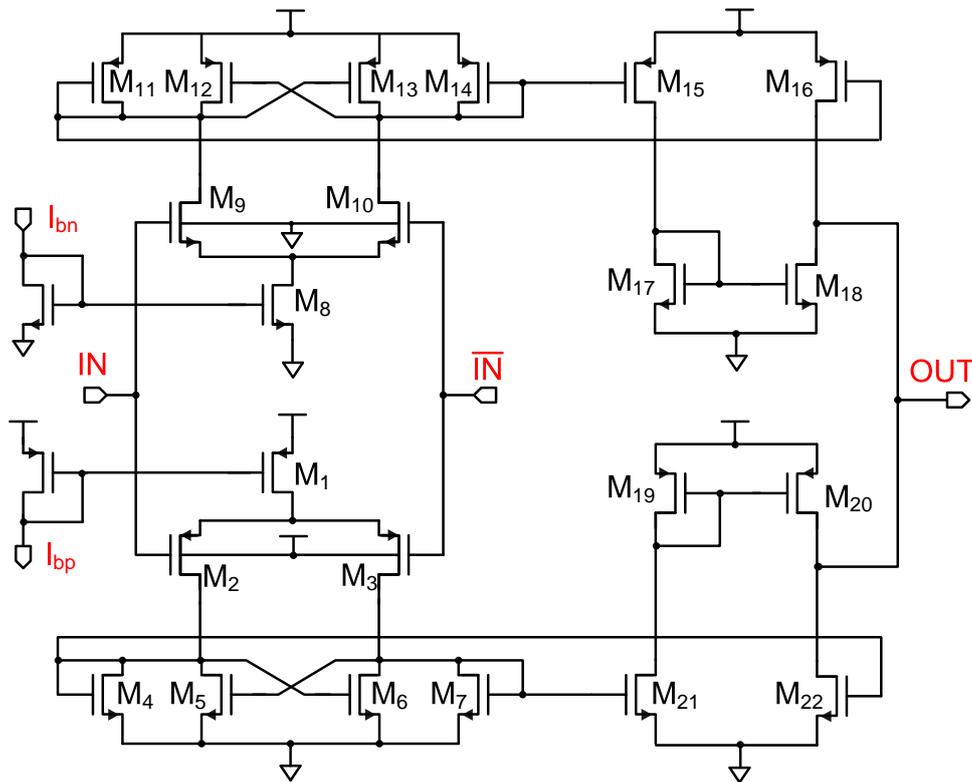


Figure 38: LVDS receiver with low voltage rail-to-rail input stage

The LVDS receiver implementation is shown in Fig. 38. An NMOS differential input stage and a PMOS differential input stage are connected in parallel to reach a wide range of input signal common-mode voltages in which the LVDS receiver is capable to operate. For high input signal common-mode voltages, the NMOS input stage is processing the input signal whereas the PMOS

975 input stage stops operating since the differential pair formed by transistor M2 and M3 drives the bias transistor M1 out of saturation. For low input signal common-mode voltages the PMOS input stage processes the input signal whereas the NMOS input stage stops operating since the bias transistor M8 is driven out of saturation. Both stages are equipped with a positive feedback decision circuit formed by transistors M4 to M7 and M11 and M14 which increases the switching speed and
 980 also allows the introduction of hysteresis. A high-gain second stage amplifier combines the two signal paths and converts the output signal to full-swing CMOS.

To reach a the wide input common-mode range, special care has been given to the choice of the threshold voltages of the differential input pair formed by transistors M2, M3 and M9, M10. The higher the threshold voltage of the NMOS differential pair transistors is, the smaller the
 985 input signal common-mode voltage region becomes in which the biasing transistor M1 remains in saturation. However, the smaller the threshold voltage of the NMOS differential pair transistors is, the smaller the region becomes in which the differential pair transistors M9 and M10 themselves stay in saturation. The process vendor provides transistor types with different threshold voltages which allows to have an optimal choice on the transistor threshold voltage. Due to the reverse short
 990 channel effect, the threshold voltage also varies with the channel length which has to be taken into account during transistor dimensioning. The smaller the channel length, the higher the effective threshold voltage becomes.

An additional degree of freedom is introduced by the bulk-effect. In case the bulk and the source of a transistor are not connected to the same potential, the transistor threshold varies with
 995 the potential difference V_{SB} between source and bulk. The higher the potential difference becomes, the more the threshold voltage increases. As is shown in Fig. 38, the transistors of the differential input pairs have their bulk contact connected to the respective supply rail and not shorted to the source. As a result, the input transistors are subject to the bulk-effect. The source potential of the input transistors follows the voltage potential which is applied to the transistor gate and the
 1000 threshold voltage is adapted dynamically to the common-mode voltage of the input signal. For example, in case of the NMOS input transistors, the threshold voltage decreases with decreasing input common-mode voltage which helps to keep the biasing transistor M8 in saturation. Furthermore,

Ports	Type	Nominal Value	Description
vddLvds	Power	1.2 - 1.5 V	
vddT3	Power		T3 Well Isolation Voltage
gndLvds	Ground		
gndSub	Ground		Substrate Voltage
sub	Ground		Substrate
I_{bn}	Analog	24 μA	Bias Current flows into NMOS
I_{bp}	Analog	-24 μA	Bias Current flows out of PMOS
RX			Non-Inverted Signal Input
RXn			Inverted Signal Input
Out	Digital		Data Output

Table 13: LVDS receiver ports

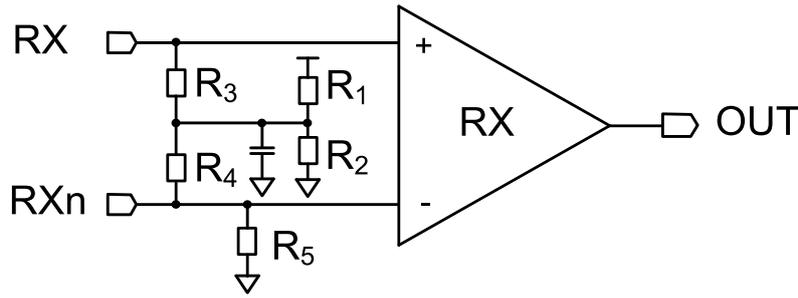


Figure 39: Fail-safe biasing circuit connected to the LVDS receiver input

the threshold voltage increases with increasing input common-mode voltage which is beneficial to keep the NMOS input transistors M9 and M10 in saturation.

1005 Special attention has also been given to the propagation delay through the two signals paths corresponding to the NMOS and PMOS input stage. For a constant propagation delay independent of the input common-mode voltage, the propagation delays of both signal paths have to be equal. The propagation delay results from the time-constants defined by the transistor transconductance and the parasitic transistor capacitances. Due to the fact that NMOS transistors have an approx-
1010 imately four times higher mobility than PMOS transistors in this process, the W_P/L_P ratio of the PMOS transistors M11-M14 in the decision circuit has to be chosen four times higher than the W_N/L_N ratio of the NMOS transistors M4-M7 to reach the same transistor transconductance.

$$\frac{W_P}{L_P} = 4 \frac{W_N}{L_N} \quad (5.1)$$

Moreover, since the oxide capacitance is equal for NMOS and PMOS transistors, the transistor area has to be equal so that an equal capacitive load results.

$$W_P L_P = W_N L_N \quad (5.2)$$

1015 The conditions defined by 5.1 and 5.2 are met both by the following choice of transistor dimensions:

$$W_P = 2W_N \quad (5.3)$$

$$L_P = \frac{L_N}{2} \quad (5.4)$$

Hence an equal signal propagation delay through both input stages results when the PMOS transistor width W_P is chosen twice the NMOS transistor width W_N and the PMOS transistor length L_P is chosen half the NMOS transistor length L_N .

1020 5.3.1 Fail-Safe Circuitry

Under certain conditions, the CMOS output of the LVDS receiver might be undefined and reach an intermediate state of increased current consumption or even start oscillating. Such a condition can for example arise, if the LVDS receiver inputs are left open and are unused, if the LVDS driver is powered off, if the transmission line is broken or if the LVDS receiver inputs are shorted. To avoid

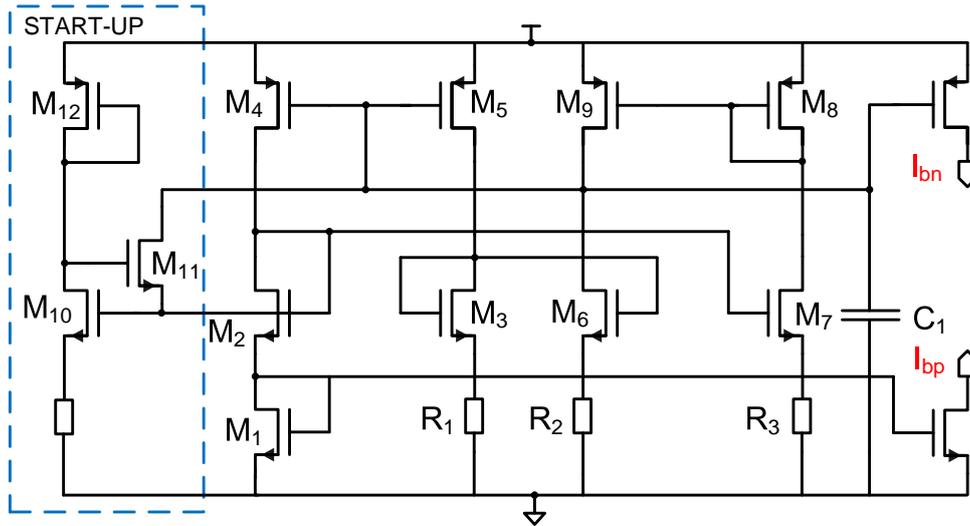


Figure 40: Low voltage biasing circuit with first order temperature compensation

1025 that in any circumstance the LVDS receiver output settles to a undefined state, the device has to be equipped with a fail-safe circuitry.

The fail-safe circuit of the FE-I4 LVDS receiver is depicted in Fig. 39. A common-mode voltage of half of the supply voltage is generated by the voltage divider formed by the equally sized resistors R1 and R2. This voltage is fed to the LVDS receiver inputs by the two resistors R3 and R4 which are also of equal size. The differential voltage is generated by the pulldown resistor R5 which is connected to the inverting LVDS receiver input. The voltage difference between the two inputs is defined by:

$$V_d = \frac{R_4}{R_1 + R_4 + R_5} V_{Supply} \quad (5.5)$$

1035 The fails-safe circuit integrated on the FE-I4 readout chip generates a nominal differential voltage V_d of 60 mV. The chosen fail-safe scheme is far more robust to resistor mismatch with respect to traditional fail-safe circuits consisting of two resistive voltage dividers connected to each LVDS receiver input. In addition the used fail-safe architecture also addresses the scenario in which the LVDS receiver input pins are shorted. In case of a short, resistor R3 and R4 are connected in parallel which leads to a differential voltage which in fact is smaller than the voltage defined by equation 5.5 but still is high enough to enforce a defined output state.

1040 5.3.2 LVDS Receiver Biasing

The biasing circuit of the FE-I4 LVDS receiver is shown in Fig. 40. The transistors M6, M7, M8 and M9 form a differential amplifier which senses the gate potential of the gate-drain connected transistors M2 and M3 and biases the transistors M4 and M5. The transistor M1 is introduced to reach a first order temperature compensation while resistors R2 and R3 are added to improve matching. The amplification loop enforces the same current through transistors M2, M3, M4 and M5 and resistor R1 and equalizes the gate potential of transistors M2 and M3. Kirchoff's voltage law gives:

$$V_{gs1} + V_{gs2} - V_{gs3} - IR_1 = 0 \quad (5.6)$$

Assuming that transistors M1, M2 and M3 are operating in strong inversion and applying a simplified square-law transistor model, equation can be written as:

$$\sqrt{\frac{2}{\mu C_{ox}} \frac{L_1}{W_1} I} + V_{th} - IR_1 = 0 \quad (5.7)$$

The temperature coefficient of the current I defined in equation 5.7 can be set to zero when the resistor R_1 is chosen to be:

$$R_1 = \frac{V_{th} k_{\mu} + 2k_{th}}{I k_{\mu} + 2k_{R1}} \quad (5.8)$$

where k_{μ} , k_{th} and k_{R1} are the temperature coefficients related to the charge carrier mobility, the threshold voltage and the resistor R_1 , respectively. Both transistors M2 and M3 are gate-drain connected which gives a circuit configuration with a single high impedance node and simplifies stabilization. For stabilization, the capacitor C_1 has been added to the V_{bias} port. The capacitance of C_1 has been chosen such that a phase margin greater than 60° is attained.

To ensure that the biasing circuit reaches its nominal operating point when power is switched-on, the startup circuit composed of transistors M10, M11, M12 has been added. When no current flows through the transistors of the biasing circuit, the source potential of transistor M11 is close to ground and gate potential is close to the positive supply rail. The transistor M11 then enforces a current flow from transistor M9 through transistor M11 into transistors M2 and M1. When the nominal current point is reached, the source potential of transistor M11 increases whereas the gate potential decreases. As a result the transistor M11 is switched-off and does not influence the operation of the biasing circuit.

As is seen from Fig. 41a, the biasing current settles at supply voltages higher than 1 V to a value of approximately 24 μA . For supply voltages greater than 1 V, the biasing circuit has an output impedance of 4 M Ω . As is shown in Fig. 41b, the maximum variation of the biasing current in the temperature region of $\pm 50^\circ\text{C}$ is about 140 nA which corresponds to approximately 0.5 % of the nominal current value. Monte-Carlo simulations give a standard deviation of 1.3 μA when process variation and component mismatch are taken into account which corresponds to 5 % of the nominal current value.

5.4 Shunt-LDO Regulators

The Shunt-LDO regulator is a combination of a low-drop linear voltage regulator and a shunt regulator. The Shunt-LDO regulator can be configured as a pure linear voltage regulator for usage in a conventional voltage based supply scheme. In addition, the regulator provides dedicated shunt circuitry which can be enabled for application in a current based serially powered supply scheme.

A simplified circuit of the Shunt-LDO regulator is shown in Fig. 42. The LDO regulator part is formed by the error amplifier A1, the PMOS pass transistor M1 and the voltage divider formed by the resistors R_1 and R_2 . In a voltage based supply scheme, the unregulated input voltage is applied to the REG_IN port while REG_OUT corresponds to local ground. The regulator generates an output voltage $\text{REG_OUT} = 2V_{ref}$ where V_{ref} is the reference voltage which is provided to the inverting input of the error amplifier A1.

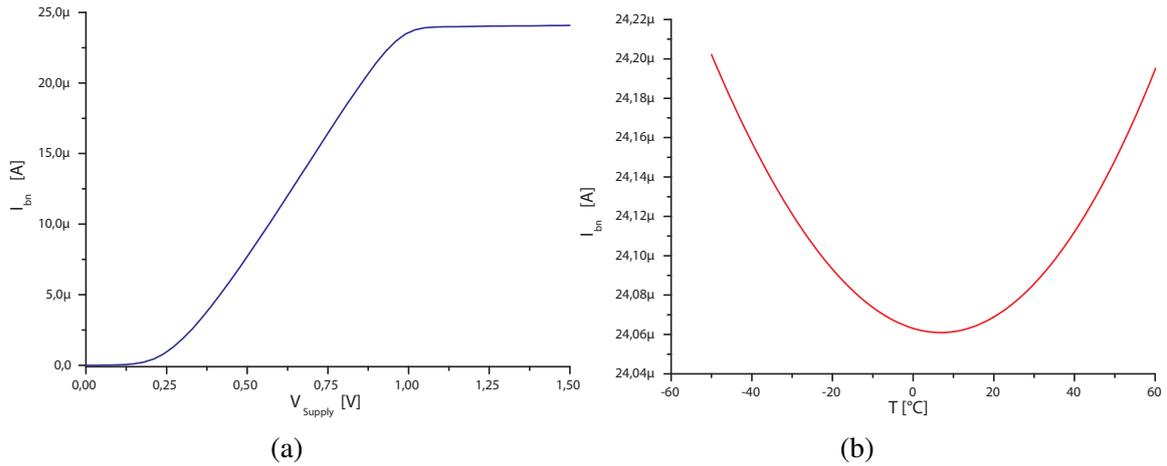


Figure 41: Simulated current variation a) as a function of the supply voltage and b) as a function of the temperature

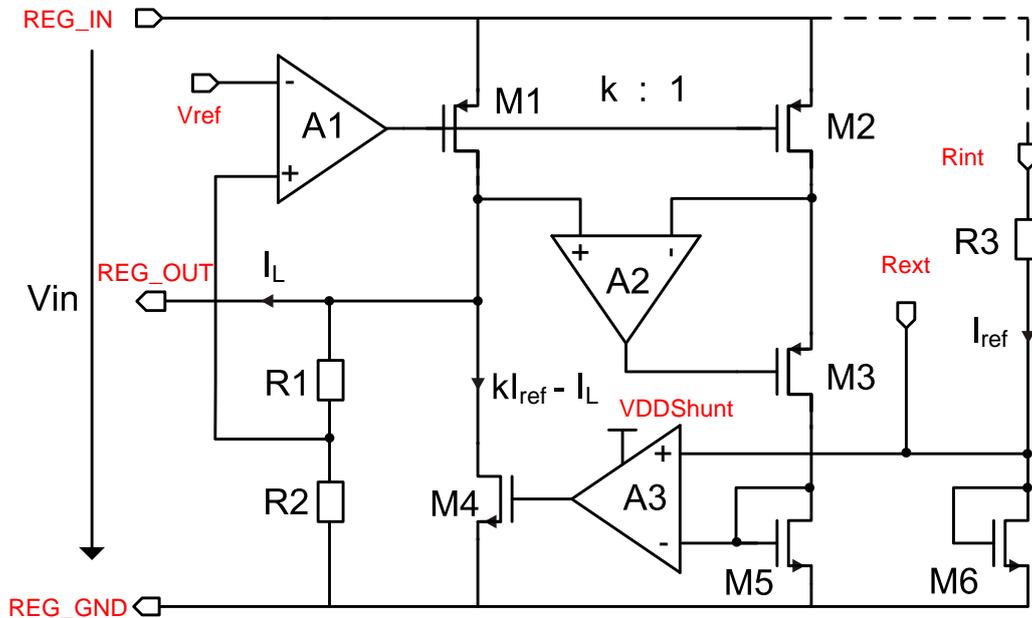


Figure 42: LDO regulator with shunt capability (Shunt-LDO)

In a current based supply scheme the supply current is flowing into the REG_IN port. The pass transistor M1 is steered to create a voltage drop V_{DS} between regulator input REG_IN and the output voltage terminal REG_OUT such that the wanted output voltage is generated with respect to local ground. For shunt operation, the transistor M4 is added to provide an additional current path to REG_OUT. Transistor M4 is controlled to drain all current which is not drawn by the load connected to REG_OUT. For this purpose the current flow through transistor M1 is compared with a reference current which is defined by resistor R3. A fraction of the current flowing through transistor M1 given by the aspect ratio k of the current mirror formed by transistor M1 and M2, is

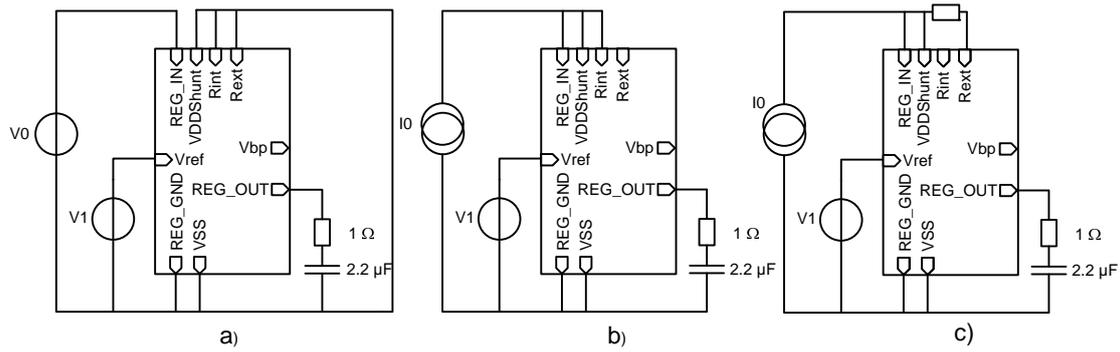


Figure 43: Connection scheme of the regulator for usage as a a) conventional LDO regulator, b) Shunt-LDO regulator with internal reference resistor c) Shunt-LDO regulator with external reference resistor

drained into the gate-drain connected transistor M5. The amplifier A2 and the cascode transistor M3 are added to improve the mirroring accuracy. The reference current which depends on the input potential REG_IN is drained into the gate-drain connected transistor M6. The reference current is compared to the fraction of current flowing through transistor M1 by use of the differential amplifier A3. If the current drained to transistor M6 is smaller than the reference current, the shunt transistor M4 is steered to draw more current and vice versa. By this means, a constant current independent of the regulator load is flowing through transistor M1 with a value defined by:

$$I_{in} \approx k \frac{V_{in} - V_{thM6}}{R3} \quad (5.9)$$

where V_{thM6} is the threshold voltage of transistor M6. The resistor R3 is integrated internally and has a resistance of 2 k Ω . With the internal resistance a maximum shunt current of 500 mA is reached at a voltage drop of 1.7 V between REG_IN and REG_OUT. Resistor R3 is used for the reference current definition if the Rint port is connected externally to the REG_IN port. However the reference current can also be defined by an external resistor. In this case, the Rint port is left floating. One electrode of the external resistor is then connected to the Rext port while the other electrode of the external resistor is connected to the REG_IN port. To enable shunt operation the supply voltage of amplifier A3 which is provided by the VDDShunt port has to be externally connected to the REG_IN port. Shunt operation is disabled by shorting the Rint, Rext and VDDShunt ports to the local ground port REG_OUT. In Fig. 43 the three different possible configurations of the Shunt-LDO regulator are shown.

Since the Shunt-LDO regulator has no integrated voltage reference circuit, the reference voltage which defines the REG_OUT voltage has to be provided externally. However biasing currents are generated by an internal biasing circuit. The generated biasing voltage can be measured on the Vbp port. The Shunt-LDO regulator requires an external capacitor of 2.2 μ F connected to the REG_OUT port for stable operation. The usage of ceramic capacitors should be avoided. Instead capacitors with an ESR¹ of about 1 Ω have to be used to reach stable regulation. On the FE-I4 two Shunt-LDO regulators are integrated which are located at the far right (regulator 1) and the far left

¹Equivalent Series Resistance

(regulator 2) at the chip periphery. The REG_IN port of regulator 1 is hard wired to the output port of the DCDC converter which is located next to the regulator at the far right of the chip periphery. In addition the VDDT3 potential of the Shunt-LDO regulator and the DCDC converter is provided for both circuits by the DCDC_IN port. Hence even if regulator 1 is operated stand-alone without usage of the DCDC converter, the DCDC_IN port should not be left floating. The DCDC_IN port should be shorted to the REG_IN port.

Ports	Type	Nominal Value	Description
REG_IN	Power	1.4 - 2.5 V / 500 - 600 mA	regulator voltage/current input
VDDShunt	Power	1.4 - 2.5 V	supply voltage of shunt circuitry
REG_GND	Ground		local ground / shunt current output
REG_OUT	Power	1.2 - 1.5 V	regulator voltage output
Vref	Analog	600 - 750 mV	reference Voltage (REG_OUT=2Vref)
Vbp	Analog		bias voltage for PMOS transistor
Rint	Analog		port for internal reference resistor
Rext	Analog		port for external reference resistor

5.5 DC-DC Converter

1125 5.6 Analog Output Buffers

6. Connection and Control

The primary method of communication with the FE-I4 chip is via a differential serial command input and a differential serial data output. An external differential clock, nominally 40 MHz, is required. The serial input is sampled on the rising edge of the clock. Alternate control paths through dedicated CMOS pins are also provided for test purposes. Prior to operating the FE-I4, certain physical connections must be made as described below.

6.1 Connection

The FE-I4A has functionality that must be enabled by making physical connections. This was done to have maximum testing flexibility in case of failures. This section describes only the connections needed for basic operation. A full pinout description is provided in the appendix. Only pads at the bottom of the chip are needed for basic operation. All power, ground and substrate pads at the bottom should be connected, as the horizontal power distribution within the chip is poor. In addition, the following connections can or must be made:

- Chip ID (Cmd_ChipId_P<0>(67), Cmd_ChipId_P<1>(68), Cmd_ChipId_P<2>(69)): three wire bonds can be made to set the chip ID to something other than 000. This is not necessary for single chip operation, as there are internal pull-down resistors to default to 000 if the pads are left floating.
- Current Reference (Iref_out_P(33), VbbnIn_P(34)): this is the master current from which all other chip internal currents are derived. The chip outputs this current on pad Iref_out_P(33) which must be externally connected to pad VbbnIn_P(34). By looping this critical current externally it is possible to substitute an external current source in case of problems and also to characterize the current reference as a standalone circuit.
- Global Threshold (vthin_P(16), VthinC_P(24)): Vthin_P(16) is both a current output and a voltage input. The output current is controlled by the Vthin register, and by loading a 45 k Ω external resistor it can be used to produce a global threshold voltage. No other connections are needed in this configuration. Since this current is normalized by the temperature-stable current reference, the global threshold voltage generated this way will also be temperature stable (assuming the resistor is stable). Unfortunately, the pixel threshold itself has a known temperature dependence, and a different configuration must be used to have a temperature stable threshold. VthinC_P(24) is an output voltage with a temperature dependence intended to cancel out the pixel threshold temperature dependence. This voltage can therefore be looped back to Vthin_P(16) to achieve a temperature compensated threshold (this compensation is not expected to be perfect). When this is done the Vthin register should be set to zero and no external resistor should be present. The VthinC_P(24) voltage is controlled by the Vthin_Alt register. Finally, an external voltage can simply be supplied to Vthin_P(16) to force any desired global threshold.
- Resets (RA1bar_P(45), RA2bar_P(56), RD1bar_P(88), RD2bar_P(89)): all the resets are negative logic (i.e. ground means reset) and have internal pull-up resistors. Thus if left unbonded the chip should be functional. However, reset actions may be required, particularly

1165 upon applying power. RA1bar_P(45) and RA2bar_P(56) can be tied together to a common
negative logic external signal, but RD1bar_P(88) and RD2bar_P(89) should remain separate.
Alternatively, one can add an RC circuit, with pull-up to VDDA1, VDDD1, and VDDD2, re-
spectively, to implement an automatic power-on reset. However, in the case of RD2bar_P(88)
1170 this needs a second resistor to GROUND, to overcome the internal pull-up (200 k), which is
to VDDD1, not VDDD2. See Table 5.

- LVDS pads: Please see Section 6.2.
- Bypass control: all bypass control functions are internally pulled up or down to be normally
off, thus ignoring all other pads should not interfere with operation. However, if once wishes
1175 to make use of alternate control pads and therefore wire bonds the SelCmd_P(85) pad, care
should be taken to hold this pin high for normal operation.
- E-fuses: the programmable read only memory in the form of e-fuses is design to have some
standalone capability so that the chip serial number can be retrieved even in the case of a
damaged chip. It therefore has a separate power supply: VDDEfuse(42). This pad should
be connected to the same supply as VDDD1 for normal operation. Burning-in e-fuse value
1180 requires 3.3 V power as well as a dedicated low frequency clock and should only be done
during wafer probing. Thus the pad VDD33(41) should never be wire bonded (it is a normal
width pad because it must be contacted during wafer probing).

6.2 LVDS Pads

The FE-I4 differential inputs and outputs are compatible with the LVDS standard, but are not ex-
1185 actly conforming because they operate on a 1.2 V supply. These pads (listed below) are nevertheless
referred to as LVDS. The LVDS driver and receiver circuits have been described in the circuit sec-
tion. The LVDS receivers are self biased and will immediately work upon application of VDDD1.
The LVDS output, on the other hand, must be enabled by writing the configuration memory.

- * Aux_Clk_N(90) & Aux_Clk_P(91)
1190 An auxiliary clock input which can be selected for use by appropriate bit settings in the
configuration memory. Not needed for normal operation.
- * Ref_Clk_N(92) & Ref_Clk_P(93)
The external clock input (normally 40 MHz). Required.
- * CMD_DCI_N(94) & CMD_DCI_P(95)
1195 The serial command input. Required.
- * DOB_OUT_N(104) & DOB_OUT_P(103)
The serial output. Must be enabled before producing any output.

6.3 Commands

All configuration data between the ROD and the FE-I4 follow a simple serial command protocol.
1200 This protocol is subdivided in three major command classes, “Trigger”, “Fast”, and “Slow” com-
mands. Due to the fact that we have a 40 MHz link between the ROD and the FE chip and trigger

commands have to be passed to the chip without waiting, the FE-I4A has a Run Mode during which it will accept trigger and fast commands only and send back the corresponding hit data. If a slow command is received while the chip is in Run Mode the state machine will decode it but the CMD will send no internal control signals to the rest of the chip, and therefore slow commands other than “RunMode” will have no effect. In contrast, while in Configuration Mode the FE-I4A will process only slow commands (i.e. reset and configuration commands) but will not react to trigger or fast commands, as is the case with the present pixel detector modules. The chip can be placed in either Run Mode or Configuration Mode by issuing the “RunMode” slow command with the appropriate argument. Upon power-up or reset the chip will be in Configuration Mode.

In the Trigger command group the only command is “LV1”, in the Fast group there are three commands and in the Slow group there are six commands. Commands can have up to six different fields (numbered 1-6). All fields have fixed length with the exception of Field 6.

The possible values for the first two fields are listed in Table 14. Trigger and Fast commands have no further fields. Table 15 shows Fields 3-6 for Slow commands. A “-” for a field entry in the tables indicates that the field (and subsequent command fields) are ignored.

6.3.1 Trigger & Fast Commands

Name	Field 1	Field 2	Description
size (bits):	5	4	
LV1	11101 ¹	-	Level 1 Trigger
BCR	10110	0001	Bunch Counter Reset
ECR	10110	0010	Event Counter Reset
CAL	10110	0100	Calibration Pulse
Slow	10110	1000	Slow command header

1: A single bit flip in the LV1 command will still result in a LV1 being decoded

Table 14: Trigger and Fast Commands

LV1 (Trigger): The LV1 command triggers the acquisition of a new event from the chip. This command simply generates a one clock wide pulse that is sent to the end of chip logic trigger input. Two or more consecutive trigger commands can be issued and will be decoded correctly. The minimum distance between two consecutive trigger *commands* is therefore five clock cycles. This is not to say that there can be no triggers on consecutive clock pulses, as the trigger count is multiplied in the EOCHL after receiving the command from the CMD. Any bit pattern resulting from flipping a single bit in the nominal pattern will still be interpreted as the original LV1 command with the correct timing. In addition to the LV1 command, a CMOS input to the chip permits supplying trigger pulses directly to the end of chip logic from an external source. This external trigger input is ORed with any trigger pulses generated from LV1 commands.

1230 **BCR** (Bunch Counter Reset): The bunch crossing counter inside the FE is set to zero in response to this command. It has no effect on any other internal structure. This command produces an output pulse of 1 clock cycle.

1235 **ECR** (Event Counter Reset): The ECR command is meant to completely clear the FE data path without touching the configuration of the chip. It can therefore be issued in order to synchronize events across the detector in case problems with data alignment are detected. This command resets and clears all memory pointers and data structures. This command produces an output pulse of 16 clock cycles.

1240 **CAL** (Calibration Pulse): In response to a CAL command a control pulse is sent to the internal Pulse Generator circuit. The Pulse Generator circuit then generates digital or analog calibration pulses and distributes them to the pixel array. This control pulse is user controllable by means of the 14 bits named CMDcnt stored in the configuration memory.

CMDcnt[13:8] sets the delay, in clock cycle units, between the command detection and the beginning of the pulse. All values between 0 and 63 are allowed. Note that this is a digital coarse delay. A fine analog delay can be added by the Pulse Generator circuit, described separately.

1245 CMDcnt[7:0] instead sets the width, always in clock cycles, of the calibration pulse that will be generated. The possible range is any value between 0 and 255; corresponding to pulse widths of one and 256, respectively.

6.3.2 Slow Commands

1250 The slow command is detected once the appropriate slow command header (10110 1000) has been found in the data stream. the fields following the header are interpreted according to Table 15. These fields are as follows:

- * Field 3: This 4-bit field always exists and it defines the particular slow command.
- * Field 4: This 4-bit field always exists and is the chip ID. The three least significant bits define the chip address and are compared with the geographical address of the chip (selected via wire bonding), while the most significant one, if set, means that the command is broadcasted to all FE chips receiving the data stream. If the chip ID does not match the geographical address of the FE or it is not a broadcast command, the command itself will be decoded but simply ignored.
- 1260 * Field 5: This is the 6-bit address field. It holds the value of the address to be used with WrRegister or RdRegister commands. For the WrFrontEnd command this field is present but is ignored. Any value is fine but it is advisable to fill this field with 000000. In case of a GlobalPulse command the value written in this field is used to compute the width of the GlobalPulse pulse, which ranges from one to 64 clock cycles. In case of a RunMode command this field is used to toggle between RunMode (111000) and ConfMode (000111).
- 1265 * Field 6: This is the “payload” data for all write operations. Only the commands WrRegister (16-bit payload) and WrFrontEnd (672-bit payload) use this field.

1295 concisely, the command decoder always processes the commands you send it, but depending on its mode it either does or does not produce output. This command toggles the FE between RunMode and ConfMode. In order to set the FE in RunMode one has to write 111000 in Field 5. A value of 000111 puts the chip in ConfMode. Any other combination of Field 5 does not change the RunMode status of the chip.

6.4 Test Pads

6.4.1 External Injection and Triggering

1300 There are two test pads, ExtAnaInjectIn_P(46) and ExtDigInjectIn_P(50) which can be used for external analog and digital injection, respectively. Injection with either of these pads must be enabled by setting the configuration bits ExtAnaCalSW or ExtDigCalSW; these bits are located in global register 31.

1305 Cmd_ExtTrigger_P(66) is a test pad capable of external triggering. Pulsing this high for 25ns will have exactly the same result as issuing a LV1 command through the command decoder. Sending the trigger in this method works regardless of the RunMode status of the command decoder itself; but no events or data will be sent to the user in response to the trigger if not in RunMode.

6.5 I/O Mux

1310 The IOMUX block is a bank of multiplexed CMOS inputs and outputs provided for testing purposes. It has a 3-bit select field available as wire bond pads, which determines where the inputs and outputs are routed within the chip. There are four input pads (see Table 16) and three output pads (see Table 17).

Selected Block	IoMxSel_P [2:0] 71,72,73	IoMxIn_P				← bits ← pads
		[0] 74	[1] 75	[2] 76	[3] 77	
IoMx	000	LpBack	_1	-	-	
DOBT	001	DOBT_clk	DOBT_en	DOBT_se	DOBT_si	
EOCHLT	010	EOCHLT_tm	EOCHLT_si	EOCHLT_se	EOCHLT_ck	
Effuse	011	Effuse_RN	Effuse_CK	-	-	
SR	100	SRIN_FrmIoMx	SRCK_FrmIoMx	-	-	
CMDT	101	CMDT_SI	CMDT_CK	CMDT_SE	CMD_TM	
cReg	110	cRegSRClr	cRegLd	cRegClk	cRegDin	
abReg	111	abRegCKin	abRegDacLthClr	abRegSrclr	abRegDin	

1: Fields with “-” are not routed anywhere

Table 16: IOMUX Input

6.6 Programming the Shadow Registers

1315 The shadow registers are alternate memory registers which are available to the user to bypass the normal configuration memory. However, only a selected subset of the global memory registers

are shadowed (see Appendices B and C). The shadow registers are split into two independent structures, the abReg and the cReg. They consist of their own shift register and set of latches. Both can only be written to using bond pads, no commands are necessary. The abReg and cReg are implemented with slightly different features, although programming them is very similar. Most of the programming is done through the IOMUX, but there are some other dedicated pads required.

SelAltBus_P(53) is a bond pad which determines if the chip should use the configuration memory or the shadow registers for configuration. Pulling SelAltBus_P(53) high will give control of the chip to both these shadow registers; there is no option to only use one or the other. Pulling it low will give control of the chip to the configuration memory. SelAltBus_P(53) is internally pulled low, but wire bonding to ground is recommended for normal detector operation. Toggling SelAltBus_P(53) does not effect the elements of the configuration memory or shadow register. One can make use of this feature for rapid switching between two different configurations, for example to create power transients.

6.6.1 cReg

The cReg is 144 cells long. The user is able to clear its associated shift register, but not to clear the latches. Latches would need to be cleared by first having all zeros in the shift register, either by clearing or filling it explicitly with zeros, and then loading the latches. To fill the shift register, supply data at Din and feed it to the shift register with a clock provided at Clk. While you are supplying this clock, the old data will also be shifted out and can be viewed at SrOut. To load the latches from the shift register, pulse the Ld line high.

6.6.2 abReg

The abReg is 288 cells long. It has the functionality to both clear the latches (DacLthClr) and its shift register (Srclr); to do either simply pulse the appropriate IOMUX input lines high. To fill the shift register, supply data at Din and feed it to the shift register with a clock provided at CKin. While you supply this clock the old data will also be shifted out and can be viewed at SRout.

Selected Block	IoMxSel_P [2:0] 71,72,73	IoMxOut_P			
		[0] 82	[1] 83	[2] 84	← bits ← pads
IoMx	000	IoMxLpBack	1'b0 ¹	1'b0	
DOBT	001	DOBT_so	ErrorinBus[22]	ErrorinBus[23]	
EOCHLT	010	EOCHLT_so	EOCHLErrorOut1	CLK input to EOCHL	
Effuse	011	Effuse_srout	1'b0	1'b0	
SR	100	SRCK_OUTIoMx	SR_OUTIoMx	HitOr	
CMDT	101	CMDT_SO	1'b0	1'b0	
cReg	110	cRegSrOut	cRegOut143	cRegClkOut	
abReg	111	abRegSRout	bRegOut0	abRegCKout	

1: Fields with "1'b0" always return logical low

Table 17: IOMUX Output

Once the shift register has been filled you then must load the latches. There are two bond pads regABstbld_P(51) and regABDaclld_P(52), which must be pulsed to load latches corresponding to the memories. The abReg actually controls two different subsets of global memory but shares a common shift register. Both of these pads control the latch loading for a different subset of latches in the abReg.

1345

7. Output Data Format

The FE-I4 runs from an externally supplied clock, nominally 40MHz. A clock multiplier inside the chip is used to be able to output data at the required rate of 160Mb/s. The default output mode is 8b/10b encoded, but this encoding can be switched off. 8b/10b encoding allows recovery of the 160 MHz clock from the data stream in the BOC/ROD in the control room and provides data framing and phase alignment. The data stream before encoding follows a few guidelines to facilitate data recognition when 8b/10b coding is turned off for testing purposes. The FE-I4 output is always sending out bits, which will be codes for idle output when there is no other output.

7.1 8b/10b

Code Group	kin/kout	8-bit data	10-bit data	10-bit data
		HGF EDCBA	(RD-) abcdei fghj	(RD+) abcdei fghj
K28.0	1	000 11100	001111 0100	110000 1011
K28.1	1	001 11100	001111 1001	110000 0110
K28.2	1	010 11100	001111 0101	110000 1010
K28.3	1	011 11100	001111 0011	110000 1100
K28.4	1	100 11100	001111 0010	110000 1101
K28.5	1	101 11100	001111 1010	110000 0101
K28.6	1	110 11100	001111 0110	110000 1001
K28.7	1	111 11100	001111 1000	110000 0111
K23.7	1	111 10111	111010 1000	000101 0111
K27.7	1	111 11011	110110 1000	001001 0111
K29.7	1	111 11101	101110 1000	010001 0111
K30.7	1	111 11110	011110 1000	100001 0111

Table 18: The 12 commands, “K”-Code Group. On the two right columns, the two versions of actual 10b streams.

Many introductions to 8b/10b coding can be found in the literature [5, 2, 1]. An 8b/10b coder maps the 256 possible “symbols” of an 8-bit word into a specific subset of the 1024 symbols possible for a 10-bit word. The circuit that performs the mapping is called the coder. The selected 10b symbols have some favorable engineering properties:

- Each 10b word is either perfectly DC-balanced, or has a disparity of +2 or -2. The disparity of a word is defined as the number of 1’s minus the number of 0’s.
- There is always perfect DC balance over 20 bits. The coder keeps track of DC balance by evaluating a running disparity and compensates for positive or negative disparity with the next word sent.

- 1365 - The coder can also generate 12 symbols which have a special meaning, in that they are decoded as commands. These commands are shown in Table 18. These symbols do not have an 8b representation, they only are possible after the 10b encoding.

Of particular interest are the three commands K.28.1, K.28.5 and K.28.7. These three commands contain the unique stream 00.11111 (or the complementary stream 11.00000). This pattern can then be used for frame alignment, and these three commands are consequently called commas. The K.28.7 command cannot be generated from any single bit flip in the data stream. Conversely, a single bit flip in K.28.7 will result in K.28.1, K.28.5, or an undefined symbol. This is the only command which satisfies these single bit flip tolerance properties. However, no two K.28.7 can be used in a row or false codes can result in case of wrong synchronization.

7.2 FE-I4 Protocol

1375 The format used is based on a Start of Frame (SOF) using K.28.7, followed by 30 bit word(s) and an End of Frame (EOF) using K.28.5. Each 30-bit word corresponds to a 24-bit record before encoding. the protocol also has an Idle State based on K.28.1. the 24-bit records can be Data Header, Data Record, Address Record, Value Record, or Service Record. Detailed information about the various records is given later. When 8b/10b encoding is turned off, there is also a 24-bit Empty Record, which is transmitted whenever there is no other data (since the Idle State only exists after encoding).

Idle State When no records are pending to be transmitted, the Data Output Block takes care of keeping the output line busy with an Idle State consisting of K.28.1 commas. When 8b/10b is turned off for test purposes, Empty Records are transmitted instead.

1385 **SOF** The Start of Frame is K.28.7. The purpose of K.28.7 is to provide a unique 1-bit flip tolerant stream that marks the beginning of the transmission of an event, and can be used for frame synchronization (see below). After a SOF, valid record words are Data Header, Address Record, Value Record, or Service Record. Data Record word(s) might only be present after a Data Header word. A triggered empty event is recognized by the absence of any Data Records after a Data Header. Value Record word(s) might be present after an Address Record word or also directly after an SOF (a read back mode where no address is read back).

EOF The End of Frame consists of one K.28.5 comma. The main purpose of the EOF is to provide some uniqueness in the stream between 2 events, which can then be used for frame synchronization during heavy data transmission when there may be no Idle States.

1395 **Frame synchronization** Synchronization at the receiving hardware can be done by searching for a combination of two successive commas. The useful combinations for alignment are EOF followed by SOF, Idle State followed by SOF, or two consecutive Idle States (a total of six unique bit patterns when including code changes due to running disparity value).

7.3 Records

1400 Records are always described *unformatted*, meaning *before* 8b/10b encoding. All records are 24 bits long, divided into three 8-bit fields. All records except the Data Record and the Empty Record

start with the pattern 11101, to ease the recognition of the start of transmission when 8b/10b is turned off. The six record types are summarized in Table 19) and a more detailed description follows, with bit order notation [MSB:LSB] and bit 0 comes out of the chip last in the serial stream.

1405 **Data Header (DH)** | 11101 | 001 | Flag | [6:0]LV1ID | [7:0]bcID |

The header for transmission of pixel data

- 11101: Eases the recognition of the start of transmission; tolerant to 1-bit flips.
- 001: Unique code for Data Header; 1-bit flip gives invalid code.
- Flag to indicate that errors have been logged.

1410 6:0 LV1ID: Value of a counter of trigger commands received, in Gray code. The counter wraps around.

1415 7:0 BCID: Value of a counter of clock cycles received at the time of the trigger pulse for the given event. The counter wraps around. Note that for a single trigger command received, up to 16 consecutive internal trigger pulses might be generated depending on the configuration. Each of these trigger pulses will result in a data header with the same LV1ID, but different BCID.

Data Record (DR) | [6:0]Column | [8:0]Row | [3:0]ToT(1) | [3:0]ToT(2) |

The pixel data

6:0 Column: Column ID in binary. Numbering goes from 0000001 to 1010000.

1420 8:0 Row: Row ID in binary. Numbering goes from 000000001 to 101010000.

3:0 ToT(1): ToT value for pixel (col,row).

3:0 ToT(2): ToT value for pixel (col,row+1).

1425 The pixel data sent out will be formatted using dynamic ϕ -pairing, where a single Data Record is used to send information from two neighbor pixels adjacent inside the same column. The ToT value is itself a code and not exactly a ToT number. The meaning of the ToT code is given by Table 7. Whenever pixel 336 is hit but 335 is not, then dynamic ϕ -pairing will assign row number 336, and the ToT(2) value (normally corresponding to row+1) will be 1111 (the code for no hit). See Figure 4. In general, when a record contains data for only one pixel, it will always be in the ToT(1) field with ToT(2)=1111. The ToT(1) field can never
1430 be 1111 (except due to an SEU upset): the combination ToT(1)=1111, ToT(2)=xxxx is not valid. After Data Record of a group the chip will send an Empty Record if 8b/10b is turned off.

Address Record (AR) | 11101 | 010 | Type | [14:0]Address |

The address of a global register, or the position of the shift register

- 1435
- 11101: Eases the recognition of the start of transmission; tolerant to 1-bit flips.
 - 010: Flags the Address Record; 1-bit flip gives invalid code.
 - Type: 1-bit information. 0 identifies Global Register; 1 identifies Shift Register.

14:0 Address: If Type is Global Register, address gives the Global Register ID. If Type is Shift Register, address gives the Shift Register position.

1440 **Value Record (VR)** | 11101 | 100 | [15:0]Value |
The value of a global register, or the value contained in the shift register

- 11101: Eases the recognition of the start of transmission; tolerant to 1-bit flips.
- 100: Flags the Value Record; 1-bit flip gives invalid code.

15:0 Value: Configuration read-back value.

1445 Note that the use of 11101 followed by 100 for a Value Record allows also for sending Value Records with no Address Record in front.

Service Record (SR) | 11101 | 111 | [5:0]Code, [9:0]Counter |
A service message (e.g. error message)

- 11101: Eases the recognition of the start of transmission; tolerant to 1-bit flips.
- 111: Flags the Service Record; 1-bit flip gives invalid code.

1450

5:0 Code: Error code (0-31).

9:0 Counter: Number of times this error occurred since last counter reset.

Note that when belonging to a data stream, only a single Service Record is allowed.

Empty Record (ER) | abcdefgh abcdefgh abcdefgh |

1455 When 8b/10b coding is turned off, to ease the recognition of the end of a data stream and to control the data output when nothing is pending to be sent out, 24-bit long Empty Records are constantly produced. The 8-bit pattern abcdefgh is programmable (normally it will simply be left at the default value of 00000000). One Empty Record will be sent after every group of Data Records belonging to the same Data Header. In 8b/10b mode the idle state is the K.28.1 comma the abcdefgh pattern is not used.

1460

Precedence: A Data Header, potentially followed by Data Record(s) and a single Service Record, has precedence over Configuration Read-Back (Address Record followed by Value Record(s) or directly Value Record(s)) which has precedence over Service Record(s). As long as no Data / Configuration / Service message needs to be transmitted, the Data Output Block will take care of transmitting Idle States (or Empty Records if 8b/10b is off). From the Idle State, as soon as Data or Configuration or Service message needs transmission, the Data Output Block will finish the transmission of the current K.28.1 comma (or Empty Record) and proceed with the transmission of relevant information. Note that Service Records are never transmitted by themselves unless there is a command requesting them. Spontaneous chip errors will result in an unrequested Service Record only after the next Data Header.

1465

1470

24-bit Record Word	Field 1	Field 2	Field 3	Field 4	Field 5
Data Header DH	11101	001	Flag	LV1ID [6:0]	bcID [0:7]
Data Record DR	Column [6:0]	Row [8:0]	ToT(1) [3:0]	TOT(2) [3:0]	
Address Record AR	11101	010	Type	Address [14:0]	
Value Record VR	11101	100	Value [15:0]		
Service Record SR	11101	111	Code [5:0]	Number [9:0]	
Empty Record ER	abcdefgh	abcdefgh	abcdefgh		

Table 19: The Six 24-bit Record Words. The AR type is 0 to indicate that it is a Global Register address or 1 to indicate Shift Register position.

7.4 Valid Record Sequences

There are only five valid sequences that records can follow. They are shown below both before (raw mode) and after 8b/10b encoding (framed) using the acronyms of Table 19:

- 1475 1. Pixel Data:
raw: $(1) \times \text{DH}, (0/n) \times \text{DR}, (0/1) \times \text{SR}, (1) \times \text{ER}$
framed: SOF, $(1) \times \text{DH}, (0/n) \times \text{DR}, (0/1) \times \text{SR}, \text{EOF}$
2. Configuration with address read back:
raw: $(1/n) \times (\text{AR}, \text{VR})$
framed: SOF, $(1/n) \times (\text{AR}, \text{VR}), \text{EOF}$
- 1480 3. Configuration with no address read back:
raw: $(1/n) \times \text{VR}$
framed: SOF, $(1/n) \times \text{VR}, \text{EOF}$
- 1485 4. Service message:
raw: $(1/n) \times \text{SR}$
framed: SOF, $(1/n) \times \text{SR}, \text{EOF}$
5. Idle:
raw: $(1/n) \times \text{ER}$
framed: $(1/n) \times \text{Idle}$

8. Programming

1490 The FE-I4 has wide functionality but a minimal command set. A sequence of several commands is typically needed to accomplish some meaningful action. This allows maximum flexibility, which means that the same action can typically be accomplished in several different ways. The best sequence to perform some action is given by the user needs and constraints, and by the performance to be measured. Some sequences may run “more smoothly” than others, and some, while logically possible, may not run at all. For example it will be logically possible to write all pixel registers in the entire chip at the same time, but because the chip is so large and writing a register produces a power transient, this may not work in practice.

8.1 Global Configuration

1500 The FE-I4 functionality is configurable by programming a master memory bank referred to as global registers (GR). It is necessary to program the GR in order to do anything meaningful. The GR also serves to retrieve non-hit information from the chip. The GR is organized as a random access memory of 16-bit words. Individual words are identified by 6-bit addresses. However, not all 64 possible addresses are used. Attempting to write an unused address will return an error message (but nothing bad will happen). The GR is accessed one register at-a-time via the WrRegister and RdRegister commands. There is no clear command that will reset all registers to zero. However, such a reset does take place on power-up via an automatic power-on reset on the VDDA1 power supply, and it can be forced externally by pulling to ground both the RA1bar_P(45) and RA2bar_P(56) bond pads. Tables 20 and 21 summarize the register address allocation.

Address	Register Type	Function
0 - 31	Read/Write	Configuration of biases and operating settings
32 - 35	Read/Write with E-fuse PROM	Chip serial number and pixel SR repair

Table 20: Read/Write Registers

Address	Expected Return [15:0]
36-39	0000000000000000
40	0010101010101010
41	EOCHLSkipped[0:7] + 10101010
42	CMDErrReg[15:0]
43-63	0000000000000000

Table 21: Read-only Registers

1510 In addition to the read and write register commands, the functionality of 27 out of the registers in the 0-31 range can be carried out by a completely separate, parallel structure, called the “bypass control”. The 432 bypass control bits are loaded as a stand-alone serial shift register, with the bits corresponding to GR 5 loading last and then transferred from this shift register to a shadow register that can not be accessed in any other way. This bypass shadow register is completely independent

from the GR. Reading GR registers can not be used to find out what is in the bypass shadow register.
 1515 Control of the chip can be given to the bypass register by pulling high the SelAltBus_P(53) bond pad (if this pad is left floating it will be internally pulled low). Note that because the bypass register and the GR are completely independent, one may for test purposes have a different configuration in each one, and instantly switch between them by toggling the bypass control bond pad. This could for example be used to modulate current consumption for noise or power supply tests.

1520 The E-fuse PROM allows burning in a unique serial number into each chip (see Appendix E) as well as a non-default selection bit for use of alternate pixel shift registers in selected double-columns, which can be useful to recover yield losses or failures. The GR registers with E-fuse PROM behave like normal registers, except that they “boot up” with the PROM values on power-up. They will also automatically reload the PROM values in case of an SEU (detected as a triple-redundant mismatch), or a re-load can be forced by issuing a “read E-fuse” pulse (using the GlobalPulse command). Burning of the PROM cannot be performed via commands, but only by applying a voltage of 3.3V and special control signals to dedicated bond pads. The value that is in the relevant global registers will be burned in when such special signals are applied. Thus one must first load the desired values into the global register, read them back to verify that they were correctly stored, and only then apply the special signals to perform the burn-in. The default value of all E-fuses is 0, and burning a 1 is not reversible. Note, however, that the PROM values are not used for anything other than initializing the relevant GR registers, but the registers can be then changed with the WrRegister command like any other global register. In order to be certain of reading the PROM values (for example to retrieve the chip serial number) one should always issue a “read
 1530 E-fuse” pulse before the RdRegister command. The PROM values can also be retrieved using a dedicated stand-alone shift register completely independent from the GR. This shift register has an independent power pin so that it should be readable even on a non-working chip as long as VDDD1 can be applied. VDDD1 is needed because direct access to the Efuse block is via the IOMUX pins (see Section 6.5), which are powered by VDDD1.

1540 8.2 Pixel Configuration

8.2.1 Pixel shift register

The pixel configuration is single column-pair oriented. One can think of the chip as having only one 672-pixel double-column: this is the length of the pixel shift register. The pixel shift register is written by the WrFrontEnd command, and at the same time 672 bits are sent to the chip output,
 1545 which are typically the bits that were previously in the shift register. There is no separate read shift register command. The pixel registers themselves are not affected by the WrFrontEnd command. To program the pixel registers, data must be copied from the shift register to the appropriate latches as explained later. This must be done by the user with a sequence of commands in addition to WrFrontEnd (or even without the WrFrontEnd command in case of special cases such as writing
 1550 the same value into all pixels of a double-column).

In reality the chip has 40 double-column’s, each one with an identical 672-bit shift register. The WrFrontEnd command writes to none, one, or several of these 40 double-column’s in parallel, as determined by the “PxSRSel” global register. This contains a 2-bit mode and a 6-bit address

that can be 0-39 for the double-column number. Values higher than 39 are also supported. Table 22 indicates which double-column's are selected depending on the mode and address.

Colpr_Mode	Action
00	Write only the addressed double-column
01	Write every 4 th double-column with such phase as to include addressed double-column
10	Write every 8 th double-column with such phase as to include addressed double-column
11	Write all double-columns

Table 22: Selection Modes of the Double-columns

Values	Action
0-39	Read the given double-column
40, 48-55	Grounded
41-47, 56-63	Loop-back(Read the input to the shift register instead of the output). Normally no need to use these values.

Table 23: Read-back action depending on column address values

The double-column selection not only affects the shift register, but also other analog column operations such as transfer of bits from shift register to pixel registers and vice-versa, or HitOR output enable. It does not affect the digital column enabling, for which there is a dedicated mask. For all modes the SR of the addressed double-column is read back during the write operation. If the address >39 then the input bit stream may be looped back or a fixed value sent to the readout as shown in Table 23. Thus, for example, address=18 (decimal) and mode=10 (binary) will write double-column's 2, 10, 18, 26, and 34 and at the same time read back double-column 18, while address=42 and mode=10 will write the same group of 5 double-column's but will copy the input bit stream directly to the output instead of reading back any of them.

Finally, the WrFrontEnd command will not unconditionally transfer a 672-bit stream to the selected pixel shift registers, because the shift register has several operating modes, controlled by the global configuration bits S0, S1, and HitLd (Table 24). It is up to the user to ensure that the shift register is in shift mode (S0=S1=HitLd=0) before issuing the WrFrontEnd command.

The WrFrontEnd command for a given double-column will fill the pixel shift register such that the last row of the lower-numbered column is filled last, see Figure 4. For example, in double-column 0 (columns 1 and 2), the last pixel filled is 1, 336. For double-column 20 (columns 41 and 42), the last pixel filled is 41, 336.

8.2.2 Calibration Pulse Injection

The "PxSRSel" global register mentioned earlier has a 2-bit mode (Table 22) and a 6-bit address (Table 23). The selection of the double-column for calibration pulse injection is different for analog injection and digital injection.

Digital Injection

The digital injection is straightforward. The 6-bit address which can be 0-39 corresponds to double-

column indicated by this formula -

1580 If the column pair address is n , the columns selected will be $2n + 1$, and $2n + 2$.
 Thus address 0 corresponds to columns 1 and 2. Address 5 corresponds to columns 11 and 12
 and address 39 corresponds to columns 79 and 80. Recall that while column pair numbering
 starts at 0, column numbering starts at 1 (see Section 3). In addition, to perform digital injection
 DIGHITIN_SEL (which is in the global register 21) must be set high.

1585 **Analog Injection**

For analog injection, the 6-bit column pair address (values 0-39) is translated into single column
 selection as follows :

Address 0 corresponds to single column 1 only. Address 39 corresponds to the triplet of columns
 78, 79 and 80. For all other addresses, the two columns selected are:

1590 if address in n , then the columns selected are $2n$, and $2n + 1$.

Thus Address 1 corresponds to columns 2 and 3; address 5 corresponds to columns 10 and 11,

The modes described in Table 24 work in the same way as described earlier. For example,
 address=10 and mode=01 will select column pairs 2, 10, 18, 26, and 34 and thus the columns
 which correspond to those double-columns based on the respective formulas for digital and analog
 1595 injection.

8.2.3 Pixel SEU hard registers

Each pixel has 13 SEU hard transparent latches. These can be set to either latched or transparent
 for a whole double-column at once. Thus, in a given double-column, all bit 0 latches can be either
 latched or transparent at the same time. For a latch to be transparent three things have to happen:
 1600 (1) the corresponding pixel strobe bit must be set in the “PxStrobes” global register, (2) the double-
 column in question must be selected (see previous section), and (3) an internal signal called “Latch
 Enable” must be high. The Latch Enable signal can not be set to static high. It can only be pulsed
 high using the Global Pulse command with the Latch Enable bit in the GlobalPulse global register
 set to 1. This seemingly complex scheme was designed to be very tolerant of SEUs not only in the

S0, S1, HitLd ¹	Description
0,0,0	Normal shift mode; shifts in on clock rising edge and out on falling edge
1,0,0	Clock rising edge loads “1” in parallel into all cells
0,1,0	Clock rising edge loads “0” in parallel into all cells
1,1,0	Clock rising edge loads selected ² pixel register value into all cells in parallel
0,0,1	Shifts in on clock rising edge and out on falling edge
1,0,1	Clock has no effect. Comparator rising edge sets bit for each pixel
0,1,1	Clock rising edge loads “0” in parallel into all cells
1,1,1	Clock has no effect

1: Effects of HitLd = 1 modes are not well understood and are best to be avoided except when used
 for hit flagging (see Section 9.6).

2: For how pixel register cells are selected see Section 8.2.3

Table 24: Shift Register Modes

1605 latches themselves but also in the logic that controls the programming of the latches. There is no reset or clear command for the pixel latches - they can only be cleared by writing the value zero.

Unlike the Latch Enable signal, any combination of pixel strobe bits can be set to static high as desired. The pixel strobe bits control not only which latches can be written, but also which ones can be read back. To read back a given latch, the inverse of the value in the latch must first be transferred to the shift register cell of every pixel in the double-column (using S0=S1=1), and then shifted out using the WtFrontEnd command. It is important to note that read-back has negative logic: what is read back is the negative of what is stored! This was done because the layout turned out to be slightly more compact than for positive logic. Since the shift register has only one bit per pixel, only the inverted value from one of the 13 latches can be transferred to the shift register at a time. This will be the lowest order pixel latch that is set. Thus if the pixel latch for bit 0 is set, then bit 0 inverse will be read out regardless of what other latches are set.

PxStrobes	Latch controlled in the pixel
[0]	Output enable. Must be set to 1 to see hits through the normal readout path.
[1:5]	TDAC value [1]=MSB
[6]	Large injection capacitor. Must be 1 to inject charge through this cap.
[7]	Small injection cap. Must be 1 to inject. In parallel with large cap.
[8]	Imon and hitbus out. Active low. Must be 0 to monitor leakage current or include pixel in hit bus.
[9:12]	FDAC value [12]=MSB
SR ¹	Enable digital injection

1: The shift register (SR) bit in each pixel is “overloaded” with the function to enable digital injection, in addition to its primary function of being the data input to the latches

Table 25: Pixel Latch Assignments

8.3 Examples

This section provides command sequences to perform some common pixel register operations. It may be possible to achieve the same result with different command sequences. Specific GR registers or bits within registers are identified by functional names rather than register numbers. 1620 The name-to-number assignment will be provided in a look-up table.

8.3.1 Clear the pixel shift register

Table 26 provides the command sequence needed to clear the shift register (set all bits to 0).

8.3.2 Set all pixel shift register bits to 1

1625 The pixel shift register cells have a clear function but not a set function. However, all the bits can

	Issue command	To do what	Comments
1	WrRegister (22)	Select double-column(s) for operations	TBD how many can be cleared in parallel
2	WrRegister (13, 21)	Set S0=S1=HitLd=0	Set SR in normal mode
3	WrRegister (27)	Select SR_clr=1	De-select all others
4	GlobalPulse	Pulse SR clear line	Clears the SR of the double-column's selected in 1

Table 26: Commands to Clear the Shift Register

be set to 1 simultaneously by changing the operating mode from normal shift to parallel input. This is done with GR bit S0 and issuing a single clock pulse to the SR (see Table 27).

	Issue command	To do what	Comments
1	WrRegister (22)	Select double-column(s) for operations	TBD how many can be set in parallel
2	WrRegister (13, 21)	Set S0=1, S1=HitLd=0	Sets the SR in parallel high input mode
3	WrRegister (27)	Set FE_clk_pulse=1	De-select all others
4	GlobalPulse	Pulse SR clock line	Clocks the SR to latch in a "1" in parallel
5	WrRegister (13, 21)	Set S0=S1=HitLd=0	Return SR to normal mode

Table 27: Commands to Set all the Shift Register Bits to 1

8.3.3 Load arbitrary bit stream into pixel shift register (and read back previous contents)

There is a direct command to do this, but recall that the command structure is single double-column oriented: the write command thinks there is only one shift register 672 bits long. The full chip is accessed by repeating the same operation on different sets of double-column's by changing the PxSrSel register. The same sequence is used to put a new bit stream into the SR and to read back what was there before, but note that writing can happen to multiple double-column's in parallel (per PxSrSel mode), but only 1 of those double-column's is read back. Table 28 shows the commands.

	Issue command	To do what	Comments
1	WrRegister (22)	Select double-column(s) for operations	TBD how many can be loaded in parallel
2	WrRegister (13, 21)	Set S0=S1=HitLd=0	Sets the SR in normal mode
3	WrFrontEnd	Clocks 672 bits in	672 bits also come out of 1 double-column per PxSrSel

Table 28: Commands to Load an Arbitrary Bit Stream

1635 **8.3.4 Load pixel latches**

The only two possible operations on the pixel latches are load and read. There is no command to reset latches to zero, because such functionality would make the latches vulnerable to SEUs. However, all latches will initialize to zero on power-up, and re-initialization can be forced externally by pulling down both the RA1bar_P(45) and RA2bar_P(56) bond pads simultaneously. Table 29 provides the command sequence needed to copy the shift register contents into 1 or more pixel latches.

	Issue command	To do what	Comments
1	WrRegister (22)	Select double-column(s) for operations	TBD how many can be loaded in parallel
2	WrRegister (13, 21)	Set S0=S1=HitLd=0 and select latch bits to load	TBD how many latch bits (1 to 13) can be loaded at the same time
3	WrRegister (27)	Set Latch_En=1	De-select all others
4	GlobalPulse	Pulse LoadLatches line	Copies SR bits to selected latch bits
6	WrRegister (13)	Set all bits to 0	It's bad for SEU to leave strobe bits high

Table 29: Commands to Load the Pixel Latches**8.3.5 Copy inverse of pixel latch contents to pixel shift register**

This is the only way to read back pixel latches. First the latch contents must be copied into the SR, and then the SR must be read out. Note that the latch contents are inverted when transferred back to the SR. The necessary command sequence is given in Table 30.

	Issue command	To do what	Comments
1	WrRegister (22)	Select double-column(s) for operations	TBD how many can be copied in parallel
2	WrRegister (13, 21)	Set S0=S1=1, HitLd=0 and set the bit to copy	Sets the SR in parallel input mode and which latch (0-12) to present to the input
3	WrRegister (27)	Set FE_clk_pulse=1	De-select all others
4	GlobalPulse	Pulse SR clock line	Clocks the SR to copy the selected latch
5	WrRegister (13, 21)	Set S0=S1=HitLd=0	Return SR to normal mode

Table 30: Commands to copy pixel latch contents to pixel shift register

8.4 Scan Chain

All the scan chains are accessed in the IOMUX interface (See Section 6.5) and are implemented for the data output block, end of chip logic, and command decoder. All of the scan chains for a given block are the same length:

- 1650 · DOB - 72 bits
- EOCHL - 3192 bits
- CMD - 262 bits

9. Data Acquisition

After the FE-I4 has been configured (see Section 8) it should be put into RunMode for data acquisition. Four types of RunMode data acquisition are possible: external trigger, calibration, self trigger, and stop mode. Only fast commands are possible when in RunMode: trigger (LV1), calibration pulse (CAL), bunch counter reset (BCR), and event counter reset (ECR). Additional “slow” data acquisition modes are possible using alternate output pads. The HitOr_P(105) pad is a wired OR of all selected pixels, and thus can be used to detect hits in real time without knowing which pixel they came from (unless only one pixel is enabled. Additionally, by setting the HitLD configuration bit, the pixel configuration shift register can be used as data output buffer to record whether each discriminator fired or not (without knowing how many times it fired).

9.1 External Triggering

This acquisition mode is appropriate for reading hit data from a detector with an external trigger system. It is the mode that will be used in the running experiment and in beam tests. All enabled pixel regions will automatically store events upon detection of a big hit without any user intervention (recall that a big hit is a discriminator pulse exceeding the programmed HitDiscCnfg. See Table 7). The leading edge of a big hit pulse starts an 8-bit latency counter within the hit region. The counter starts at 11111111 (decimal 255) and counts down with the system clock, until it reaches the Trig_Lat value programmed in the chip configuration memory. Note Trig_Lat is *not* the actual value of the trigger latency, but its 8-bit complement. Thus if a trigger latency of 120 clocks is desired ($120 \times 0.025 = 3 \mu\text{s}$), one must program a Trig_Lat value of $255 - 120 = 135$.

When the chip recognizes a trigger command, a burst of trigger pulses is sent in parallel to all the regions. The length of this burst is given by the programmed trigger multiplier value TrigCnt, which can be 0 to 15. The value 0 produces a 16 pulse burst. The pulses in the burst are spaced by one clock. A LV1 trigger (positive pulse) can also be supplied directly on the Cmd_ExtTrigger_P(66) input pad. Internally a burst will be produced exactly as before. Note that the LV1ID should be disregarded when using external injection as the counters are not reliable when using external triggering. Issue an ECR command to reset the LV1ID counter when returning to command oriented triggering (if necessary). External triggering also works regardless of the RunMode status of the chip.

For a hit region to be selected for read out, a trigger pulse must reach the region while one of the region’s five latency counters is equal to Trig_Lat. For each latency counter, if no trigger pulse arrives while this condition is true, the next clock cycle both resets the counter to 255 and clears the corresponding ToT data within the region. A Trig_Lat value of 255 is not supported and the user should not expect for the triggering to function properly.

An example timing diagram is given in Figure 44. In this example the trigger latency is set to 244, the trigger multiplier is set to one, and HitDiscCnfg is set to 2. The first pulse on HitOr_P(105) is from a hit which is smaller than HitDiscCnfg and is thus not saved; no latency counter is enabled and the trigger does nothing. The second and third injections are considered big hits and therefore you can see a latency counter begin for each injection. The second trigger does not land on Trig_Lat and thus has no effect. You can then see the latency counter count down to Trig_Lat and eventually reset itself. The third trigger is a successful one (hit data comes out from the chip) as it occurs

exactly at Trig_Lat. Please note that this diagram is from a real simulation using external injection to inject the hits and commands for everything else.

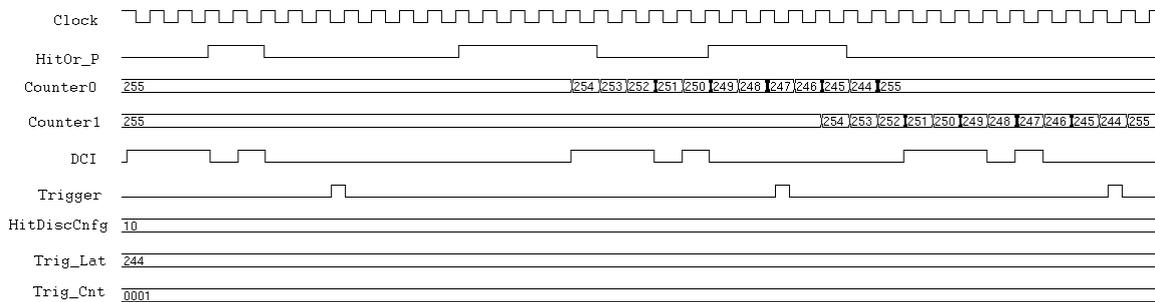


Figure 44: Proper Latency and Trigger Timing Example

The chip can queue a maximum of 16 triggers for readout at any given time. Commands that overflow this buffer will result in skipped triggers (see Section 10.2). The chip must be in RunMode the entire time that trigger pulses are being generated. It is not enough that the LV1 command itself was issued while in RunMode. For example, if the trigger multiplier is set to 15 and the user exits RunMode immediately after issuing a LV1 command, only a fraction of the expected 15 triggers will actually be sent to the columns.

9.2 Calibration

Even without a sensor connected, hits can be produced in pixel regions by either digital or analog injection. There are many different ways to produce injection pulses, but generally can be classified as using the internal pulse generator block, or not.

The internal pulse generator block can be thought of as a typical benchtop pulse generator instrument, with a trigger input, a programmable delay, and both analog and digital output pulses. The term “start input” will be used here instead of “trigger input” to avoid confusion with the chip trigger function. Not only the leading edge, but also the width of pulses provided to the start input have meaning. Start pulses can be generated by issuing a CAL command if in RunMode, by issuing a control pulse command if not in RunMode, or by directly supplying to the Cmd_AltPls_P input pad with the appropriate configuration regardless of RunMode. The latter two methods require the chip to have been configured to route the command pulse to the pulse generator (see Section 8). The relationship between the start input and the digital and analog outputs is shown in Figure 45. The delay and analog output level are programmable. The return to programmed level of the analog output uses a slow ramp (also programmable) to avoid wrong polarity charge injection. The falling edge of the analog output produced negative charge injection (the correct polarity for pixel amplifier input).

Analog or digital injection can also be accomplished without using the pulser. An external positive digital pulse can be supplied to pad ExtDigInjectIn_P(50) for digital injection (note that the ExtDigCalSW bit must be set for this to work). An external negative edge (voltage should always be between ground and VDDA1) can be supplied to pad ExtAnaInjectIn_P(50) for analog charge injection (note that ExtAnaCalSW bit must be set for this to work).

The digital injection pulse can be routed in parallel to any set of pixels by (1) enabling digital injection by setting the DIGITIN_SEL configuration bit, (2) selecting the column pairs for injection using the Colpr_Mode and Colpr_Addr registers, and (3) loading a 1 into the shift register for all desired pixels (zero for all not desired pixels) of the enabled columns. All three conditions are required. See Section 8.2.2 for column selection details. The digital injection pulse is ORed with the comparator output. Therefore, the analog state must be “below threshold”, or the discriminator must be off (bias current set to zero) for digital injection to work. For example, setting a very low discriminator threshold with the comparator active will prevent digital injection from working, because the discriminator will be always high. The width of the digital injection pulse will simulate the time over threshold response.

The analog injection pulse can be routed in parallel to any set of pixels by (1) selecting the column pairs for injection using the Colpr_Mode and Colpr_Addr registers, and (2) setting the injection capacitor pixel configuration bits of the desired pixels in the enabled columns. See Section 8.2.2 for column selection details. There are two switchable injection capacitors, one much larger than the other, that can be used in any combination (see Section 4.2).

The injection techniques described above allow the user to populate pixel regions with hits at will. The external trigger methods can then be used to produce output in the usual way. It is up to the user to determine the correct timing of LV1 commands or other triggers relative to CAL commands or other injection methods.

If the user is injecting a hit, and the injection pulse width is sufficiently large such that a trigger

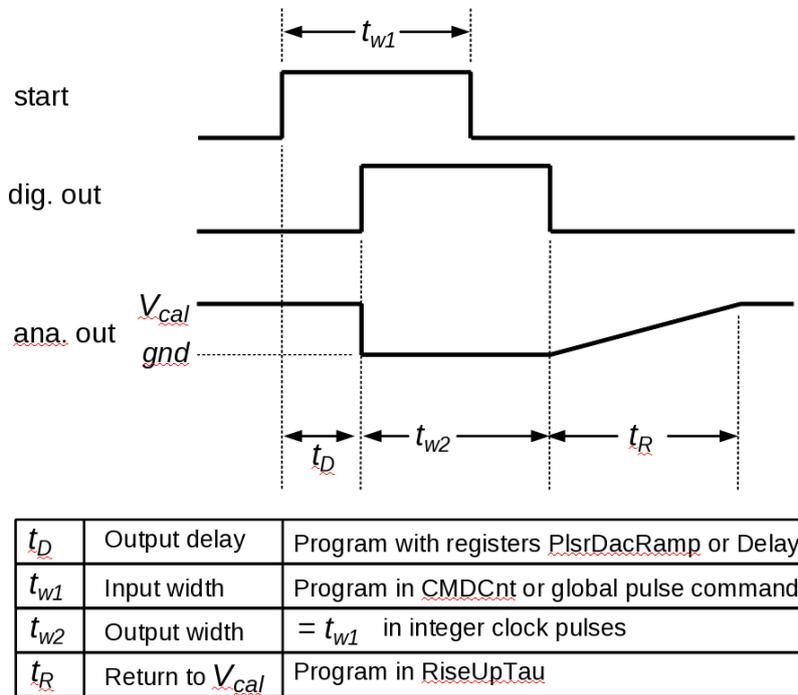


Figure 45: Outputs of pulse generator circuit block relative to start input. The analog output level, V_{cal} , can be programmed with register PlsrDAC.

1745 pulse is sent to the columns while still injecting the trigger will be ignored. For example, if there is an injection lasting 20 clock cycles using a CAL command but the user only waits 10 clock cycles before issuing the trigger then the trigger will not be accepted by the PDR. This is because the trigger would occur 10(user wait) + 5(clock cycles needed to issue LV1 command) after the end of the CAL command but the injection is still occurring.

9.2.1 Pulser Configuration

1750 The parameters of the pulser are configurable for maximum flexibility, but this also means they must be properly programmed before the pulser can be used. Referring to Fig. 45, the Vcal DC voltage level, the t_D delay, and the t_R rise time must be programmed. The Vcal voltage generation requires a bias to be programmed as well as the voltage itself. The delay is programmed with a combination of a current and a ratio (2 registers). The required registers are shown in Table 31.

1755 There is also an op-amp that must be biased. More details can be found in Section 4.11. The DC voltage level buffered by 2 op-amps can be observed on the external analog injection input pad. To do this, enable External analog injection, and Disable External digital injection.

Function	Register number	Register field	N. bits	Value
Vcal DAC bias	19	plsrDacBias	8	96
Vcal DAC setting	21	plsrDAC	10	0-1024
Current to voltage converter bias	14	BonnDAC	9	237
Delay current	17	PlsrIdacRamp	8	180
Delay value	31	PlsrDelay	6	0-63
Rise time	31	PlsrRiseUpTau	3	7
Enable	31	PlsrPwr	1	1
External digital	31	ExtDigCalSW	1	0
External analog	31	ExtAnaCalSW	1	0
Op-Amp bias	18	PlsrVgOPamp	8	255

Table 31: Configuration settings for internal pulser operation.

9.3 Stop Mode

9.4 HitOr_P(105)

1760 HitOr_P(105) is a convenient signal, available at the pad level, which is high whenever a pixel comparator is high. The comparator of each pixel in a column is ORed together to form a HitBus. The HitBus for a column is then ORed together with its column pair to form a double-column HitBus. Finally, each double-column HitBus is ORed together to form HitOr_P(105). Inclusion of a given pixel in HitOr_P(105) is controlled by an enable bit in latch 8 of of the 13 pixel latches (Table 25).

1765

9.5 Self Trigger

The user is also able to allow the HitBus signal to act as an input to the command decoder for “automatic” triggering. This is achieved by an enable bit called GateHitOr in global memory

1770 register 27 (Appendix C). When this functionality is enabled, the HitBus signal going high will tell the command decoder to issue a trigger pulse.

9.6 HitLd

1775 HitLd is a configuration bit which the user is able to control in Global Register 21. When this is enabled, a hit (small or big) will load a 1 into the shift register cell corresponding to that pixel. First clear all the shift registers in the chip before enabling this function. To read out the data for a particular double-column first place the shift register in normal operating mode ($S0=S1=HitLd=0$) and issue a WrFrontEnd command to shift out the data. After processing the data the only information which is received is whether or not a hit was registered in each pixel.

10. FE-I4A Exceptions, Variants, and Error Messages

10.1 Pixel Variants

1780 The FE-I4A array is not completely uniform; circuit variants have been included for testing. These are listed in Table 32. Every column listed has only one thing different from nominal, either the front end feedback capacitor flavor, the discriminator design, or the design of the SEU-tolerant latches. A Vertical Natural Capacitor (VNCAP) is used in special columns as a reference for the preamp feedback. The value of this capacitor determines the gain and therefore affects the threshold and the calibration of the channel. VNCAP could not be used in the whole array due to design 1785 rules against such widespread use. A low standby current discriminator (CPPM discriminator) was included to test possible power reduction, while a different design for the pixel latches (CPPM latch) was included to compare SEU performance.

Column pairs (0-39)	Columns (readout)	Variant
1	3-4	VNCAP
6	13-14	VNCAP
11	23-24	VNCAP
13	27-28	VNCAP
15	31-32	VNCAP
17	35-36	VNCAP
22-25	45-52	VNCAP
30-37	61-76	CPPM latch
39	79-80	CPPM discriminator

Table 32: Column pair variants. Column pairs not listed are nominal. The column pairs are identified by their control address, 0-39. For convenience the affected column values in the readout data are also listed.

10.2 Skipped Trigger Counter

1790 The trigger counter (LV1ID) corresponds to trigger commands from the command decoder, and not individual trigger pulses which may result from trigger multiplication. For example, if the trigger issues three trigger commands while Trig_Cnt is set to 4, the final LV1ID will be 2 and not 11 (start counting at 0).

1795 Regardless of the value of Trig_Cnt the user should not be able to generate any skipped triggers by simply issuing many LV1 commands in a row. In this case the LV1ID keeps up with the number of trigger commands which have been sent from the command decoder, but the EOCHL begins to limit the number of trigger pulses which are sent as a result (it limits the cluster size). See Figure 46 for an example.

10.3 Long Command Decoder Commands

1800 Two outputs of the command decoder, resulting from the CAL and GlobalPulse commands, have the capability of staying high for many clock cycles after the command itself has been decoded.

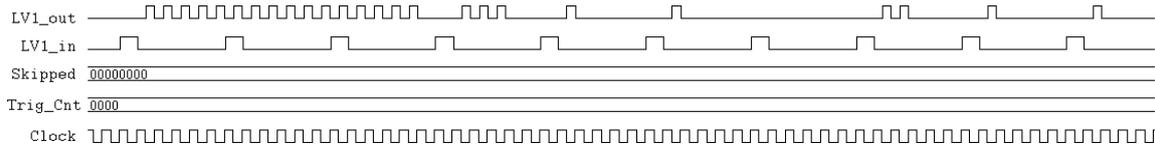


Figure 46: Result of Sending Many Trigger Commands

The command decoder only allows for one input line to be active at a time so if a command has been sent (and had enough time to be decoded) while an output is active, the command will not be processed. Furthermore, if the command is sent towards the falling edge of the active output, a BitFlip error may be produced. For example, a CAL command can be programmed to produce a pulse as long as 256 clock cycles. If the user issues a CAL command (with such a long width) and immediately issues an ECR, the CAL output pulse will not be affected, but the ECR will not be decoded because the output of CAL is still high.

10.4 Service Record Error Codes

Error Code	Signal Name	Block Name
31	EFUSE_errorflag	EFUSE
30	AddrErr	DatabusMux
29	CmdSeu	CMD
28	BitFlip	CMD
27	CmdErr	CMD
26	AddrErr	CMD
25	WrRegDataErr	CMD
24	ErrorFlagb	CNFGMEM
23	Ref2Fast	CLKGEN
22	Fb2Fast	CLKGEN
21	RA2b	Pad, PRD ¹
	... ²	
10	HitOr	Array
9	Fifo_Full	EOCHL
8	ReadOut_Processor_Error	EOCHL
7	L1_Trig_Id_Error	EOCHL
6	L1_Register_Error	EOCHL
5	L1Req_Counter_Error	EOCHL
4	L1In_Counter_Error	EOCHL
3	Hamming_Error2	EOCHL
2	Hamming_Error1	EOCHL
1	Hamming_Error0	EOCHL
0	BC_Counter_Error	EOCHL

1: Prompt Radiation Detector

2: 20-11 will never be sent out - these lines are internally pulled low.

Table 33: Service Record Codes

1810 **11. Simulation and Performance**

References

- [1] Actel Corporation. Implementing an 8b/10b encoder/decoder for gigabit ethernet in the actel sx fpga family. Actel Application Note AC135, Actel Corporation, October 1998.
- [2] Lattice Semiconductor Corporation. 8b/10b encoder / decoder. Reference Design RD1012, Lattice Semiconductor Corporation, November 2002.
- [3] Ian Dawson. Updated ibl radiation estimates.
<http://indico.cern.ch/conferenceOtherViews.py?view=standard&confId=52704>, February 2009.
- [4] Kevin Einsweiler. http://pixdata.lbl.gov/html/docs/ATLASPixelFEChip_v3_0.pdf, December 2003.
- [5] Albert X. Widmer and Peter A. Franaszek. A dc-balanced, partitioned-block, 8b/10b transmission code. *IBM Journal of Research and Development*, 27(5):440–451, 1983.

A. Troubleshooting

This section lists some tips and tricks for troubleshooting FEI4_A. No new information is presented here; only examples of practical methods to utilize functionality of the chip for debugging purposes. It is in general possible to test individual blocks without reliance on others in order to determine what is working and what is not. Scan chains are one useful method of testing the individual blocks, these scan chains do rely on the IOMUX to interface the data from the respective block.

The first step in troubleshooting is to eliminate mistakes in operating or configuring the chip. The following is a list of quick checks.

1. Power nets require multiple redundant connections. Use all or almost all the pads for each power net.
2. The LVDS output will not work until properly configured.
3. Readback of the pixel latches (13 per pixel) is the complement of their contents.
4. LSB/MSB order is not the same for all variables in the global memory registers.
5. The ToT values from hit data are encoded and not a straight number (see Table 7).
6. The latency counters count *down* from 255 to the Trig_Lat, not up from 0 (see Section 9.1). Thus Trig_Lat is not the actual latency.
7. Check that SelCmd_P(85) is pulled high for normal chip operation.
8. The CLKGEN block must be configured properly (see Section 4.7 and Table 37).

A.1 IOMUX

To check that a test system is working correctly, make use of the loopback mode of the IOMUX. This test will only depend on the IOMUX itself. By selecting the correct block (see Section 6.5) and providing a stimulus to the correct bond pad, the output is a slightly delayed copy of the input.

Another simple test using the IOMUX is to see if data is shifted properly through the abReg and cReg (as explained in Section 6.6)

A.2 Command Decoder Operation

To check if the CMD is properly decoding commands look at IOMux outputs that directly originate in the CMD.

A.3 Testing Downstream of the Command Decoder

To bypass the CMD, pulse Cmd_ExtTrigger_P(66) high for one clock cycle. External triggering is ORed together with the trigger output line of the command decoder, so pulsing this line has exactly the same effect as a successful trigger command. Furthermore this does not depend on the RunMode status of the chip. After the trigger the chip should output a data header (LVIID and BCID) regardless if there was a hit or not. This test does rely on a large number of other blocks such as the DOB, EOCHL and CLKGEN.

1855 A.4 Alternate Configuration Register**A.5 Analog Outputs****A.6 Data Output Block and/or Clock Generator**

Setting clk2OutCnfg to 1 should present the DOB clock to its output. In order to avoid dependence on the CMD and configuration memory one program this bit using the alternative configuration register (see SelAltBus_P(53)). The DOB scan chain output (DOBT_so) will have the clock divided by 8 (10) for 8b/10b mode off (on), even while not running a scan chain test. This permits assessing indirectly at the CLKGEN and DOB operation even if the LVDS output is not functioning.

1860

B. Table of Registers

1865 Tables 34-36 list all used global registers. The same information is repeated in Section C, but ordered by field name, divided into initialization, options and functions, masks and values, and analog biases. As of right now, the shadow register locations in Section C are most reliable/accurate than listed here.

#	Name	Variables (<0> loads last)	Shadow Register	Shadow Location	Default (decimal)
2	TrigModes	Trigger_Count<15:12> Conf_Addr_Enable<11> CFGspare2<0:10>	N/A	N/A	
3	ErrMask0	ErrorMask(15:0)<15:0>	N/A	N/A	128, 0
4	ErrMask1	ErrorMask(31:16)<15:0> ErrorMask(22)===configBit	N/A	N/A	??, 66
5	PrmpVbp_R + Vthin	PrmpVbp_R<8:15> Vthin<0:7>	AB	SRAB<152:159> SRAB<144:151>	+ 50, 64
6	DisVbn_CPPM + PrmpVbp	DisVbn_CPPM<8:15> PrmpVbp<0:7>	AB	SRAB<168:175> SRAB<160:167>	+ 64, 32
7	TdacVbp + DisVbn	TdacVbp<8:15> DisVbn<0:7>	AB	SRAB<184:191> SRAB<176:183>	+ 0
8	Amp2Vbn + Amp2VbpFol	Amp2Vbn<8:15> Amp2VbpFol<0:7>	AB	SRAB<200:207> SRAB<192:199>	+ 69, 26
9	PrmpVbp_T + Amp2Vbp	PrmpVbp_T<8:15> Amp2Vbp<0:7>	AB	SRAB<216:223> SRAB<208:215>	+ 66, 64
10	FdacVbn + Amp2VbpFif	FdacVbn<8:15> Amp2VbpFif<0:7>	AB	SRAB<232:239> SRAB<224:231>	+ 66, 175
11	PrmpVbnFol + PrmpVbp_L	PrmpVbnFol<8:15> PrmpVbp_L<0:7>	AB	SRAB<248:255> SRAB<240:247>	+ 64, 66
12	PrmpVbpF + PrmpVbnLcc	PrmpVbpF<8:15> PrmpVbnLcc<0:7>	AB	SRAB<264:271> SRAB<256:263>	+ 16, 0
13	FEND array config signals	S1<15> S0<14> PixelStrobes<1:13> spare<0>	AB	SRAB<272:287>	255
14	LvdsDrvIref + BonnDac	LvdsDrvIref<8:15> BonnDac<0:7>	AB	SRAB<8:15> + SRAB<0:7>	

Table 34: Global Registers (1 of 3)

#	Name	Variables (<0> loads last)	Shadow Register	Shadow Location	Default (decimal)
15	Plllbias + LvdsDrv Vos	Plllbias<8:15> LvdsDrv Vos<0:7>	AB	SRAB<24:31> SRAB<16:23>	+
16	TempSenslbias + Plllcp	TempSenslbias<8:15> Plllcp<0:7>	AB	SRAB<40:47> SRAB<32:39>	+
17	DAC8SPARE1 PlsrldacRamp	spare<15:8> PlsrldacRamp<0:7>	AB	SRAB<56:63> SRAB<48:55>	+
18	DAC8SPARE2 PlsrVgOPamp	spare<15:8> PlsrVgOPamp<7:0>	AB	SRAB<72:79> SRAB<64:71>	+
19	PlsrDacBias DAC8SPARE5	PlsrDacBias<15:8> spare<7:0>	AB	SRAB<88:95> SRAB<80:87>	+
20	Vthin_Alt	vthin_AltCoarse<8:15> vthin_AltFine<0:7>	AB	SRAB<104:111> SRAB<96:103>	+
21	FEND array config signals + PlsrDAC	spare<15:13> HITLD_IN<12> DINI_OVERRIDE<11> DIGHTIN_SEL<10> PlsrDAC<0:9>	AB	SRAB<138:143> SRAB<112:121>	+
22	FEND array config signals	spare<15:10> Colpr_Mode<8:9> Colpr_Addr<2:7> spare<1:0>	AB	SRAB<122:137>	
23	ColMask0	DisableColumnCnfg(15:0)<15:0>	C	SRC<0:15>	128
24	ColMask1	DisableColumnCnfg(31:16)<15:0>	C	SRC<16:31>	
25	ColMask2 + Trigger Latency	LatCnfg<15:8> DisableColumnCnfg(39:32)<7:0>	C	SRC<32:39> + SRC<40:47>	
26	HitDiscCnfg + StopMode + CMDent12	CNT(12:0)<15:3> StopModeCnfg<2> HitDiscCnfg<1:0>	C	SRC<48:49> + SRC<50> + SRC<51:63>	+

Table 35: Global Registers (2 of 3)

#	Name	Variables (<0> loads last)	Shadow Register	Shadow Location	Default (decimal)
27	PIIEn + GlobalPulse + CMDent13	PIIEn<15> Efuse_Sense<14> StopClkPulse<13> ReadErrorReq<12> ReadSkipped<11> spare<10:6> GateHitOr<5> CalEn<4> SrClr<3> LatchEn<2> SR_Clock<1> CNT(13)<0>	C	SRC<79> + SRC<78:65> + SRC<64>	
28	PLL_CNFG	lvdsDrvSet06<15> spare<14:10> EN_40M<9> EN_80M<8> CLK1_S0<7> CLK1_S1<6> CLK1_S2<5> CLK0_S0<4> CLK0_S1<3> CLK0_S2<2> EN_160M<1> EN_320M<0>	C	SRC<80:95>	
29	LVDSDrv	spare<15:14> no8b10bModeCnfg<13> clkToOutCnfg<12> EmptyRecordCnfg<4:11> spare<3> lvdsDrvEN<2> lvdsDrvSet30<1> lvdsDrvSet12<0>	C	SRC<96:111>	
31	Pulser config	PlsrRiseUpTau<15:13> PlsrPwr<12> PlsrDelay<6:11> ExtDigCalSW<5> ExtAnaCalSW<4> spare<3:0>	C	SRC<128:143>	
32	Efuse1	SELB(0:15)<15:0>	N/A	N/A	
33	Efuse2	SELB(16:31)<15:0>	N/A	N/A	
34	Efuse3	SELB(32:39)<15:8> spare<7:4> Cref<3:0>	N/A	N/A	
35	Efuse4 (chip serial #)	chip_SN<15:0>	N/A	N/A	

Table 36: Global Registers (3 of 3)

C. Configuration Parameters

This appendix presents a different view of the configuration parameters than the global registers table, but it does not contain independent information. In general this list should be a more convenient place to look for a particular parameter or to have an overview of what parameters are available. This list does not give the internal position of bits within a given register - refer to Appendix B for the internal structure of each register.

C.1 Initialization of the Chip

[2]	[1]	[0]	Selects
0	0	0	RefCLK (input clock to chip)
0	0	1	F320M (320 MHz)
0	1	0	RefCLK (input clock to chip)
0	1	1	F320M (320 MHz)
1	0	0	F160M (160 MHz)
1	0	1	F80M (80 MHz)
1	1	0	F40M (40 MHz regenerated clock)
1	1	1	AuxCLK (auxiliary input to chip)

Table 37: Multiplexer Selection for CLK0 and CLK1 of the CLKGEN Block

1875 EN_PLL

Size: 1-bit Controls: CLKGEN Suggested value: 1

Global Register: 27 Alternate Register: C[79]

Enables the CLKGEN block to produce clock output.

CLK0

1880 Size: 3-bit Controls: CLKGEN Suggested value: 100 (binary)

Global Register: 28 Alternate Register: C[82:84]

Control bit for CLK0 multiplexer output. Clock0 controls the DOB. See Table 37.

CLK1

Size: 3-bit Controls: CLKGEN Suggested value: 000 or 110 (binary)

1885 Global Register: 28 Alternate Register: C[85:87]

Control bit for CLK1 multiplexer output. Clock1 controls everything else except for the CMD and DOB. See Table 37.

EN_320M

Size: 1-bit Controls: CLKGEN Suggested value: 0

1890 Global Register: 28 Alternate Register: C[80]

Enables the 320 MHz clock inside CLKGEN block. Note that the clock still has to be selected in one of the CLKGEN muxes.

EN_160M

Size: 1-bit Controls: CLKGEN Suggested value: 1

1895 Global Register: 28 Alternate Register: C[81]

Enables the 160 MHz clock inside CLKGEN block. Note that the clock still has to be selected in one of the CLKGEN muxes.

EN_80M

Size: 1-bit Controls: CLKGEN Suggested value: 0

1900 Global Register: 28 Alternate Register: C[88]

Enables the 80 MHz clock inside the CLKGEN block. Note that the clock still has to be selected in one of the CLKGEN muxes.

EN_40M

Size: 1-bit Controls: CLKGEN Suggested value: 1

1905 Global Register: 28 Alternate Register: C[89]

Enables the 40 MHz clock inside the CLKGEN block. Note that the clock still has to be selected in one of the CLKGEN muxes.

lvdsDrvEN

Size: 1-bit Controls: IOB Suggested value: 1

1910 Global Register: 29 Alternate Register: C[98]

This switches on the LVDS data output driver. The output will be tri-stated if this bit is off.

GateHitOr

Size: 1-bit Controls: CMD Suggested value: 0

Global Register: 27 Alternate Register: C[69]

1915 HitOr is a signal which is high whenever any enabled pixel comparators in the entire chip are high; all the comparator outputs are “ORed” together with HitOr being the output. When GateHitOr is enabled, this pulse is routed to the CMD to produce a self-trigger. The actual trigger happens 16 clocks after the HitOr pulse to allow for ToT to complete. Note that when this is enabled do not expect the Trigger ID, which is stored inside the data header, to be anything meaningful; make
1920 sure to reset the Trigger ID after turning the self-trigger off to restore meaning to the counter when issuing trigger commands.

DIGITIN_SEL

Size: 1-bit Controls: array Suggested value: 1

Global Register: 21 Alternate Register: AB[143]

1925 In addition to the procedure necessary to create digital hits in pixels with either a GlobalPulse or CAL command, this bit must also be set high since it is ANDed with the input pulse signals. A digital inject scan will not be possible with this bit low.

PlsrPwr

Size: 1-bit Controls: PULSEGEN Suggested value: 1

1930 Global Register: 31 Alternate Register: C[140]

This bit switches on the calibration pulse delay generator. If this bit is set low, one cannot use the calibration injection command to inject hits (analog or digital).

Cref

Size: 4-bit Controls: Trims master reference current Suggested value: x

1935 Global Register: 34 Alternate Register: not shadowed

The setting x must be adjusted for each chip to have a $2\ \mu\text{A}$ master current.

C.2 Options / Functions

Colpr_Mode

Size: 2-bit Controls: array Suggested value: 0

1940 Global Register: 22 Alternate Register: AB[128:129]

When performing operations on the double-columns, these two bits determine what double-columns are affected relative to the addressed Colpr_Addr. See Table 22.

Colpr_Addr

Size: 6-bit Controls: array Suggested value: 0-39

1945 Global Register: 22 Alternate Register: AB[130:135]

The address of the double-column for all double-column operations. Numbers zero through 39 correspond to the 40 double-columns on the chip. Numbers greater than 39 are valid for talking to column pairs in modes other than 00, but have special read-back meaning such as loop-back of the input. See Table 23.

1950 **Conf_AddrEnable**

Size: 1-bit Controls: EOCHL Suggested value: 1

Global Register: 2 Alternate Register: N/A

Enables the sending of an “address record” (in addition to “value record”) in response to a RdRegister command on any of the global memories. When this bit is enabled, the EOCHL places an address record before every value record in the data stream to be passed to the DOB.

1955

no8b10b

Size: 1-bit Controls: DOB Suggested value: 0

Global Register: 29 Alternate Register: C[109]

Disables 8b/10b encoding of the DOB data output.

1960 **clk2OutCnfg**

Size: 1-bit Controls: DOB Suggested value: 0

Global Register: 29 Alternate Register: C[108]

This is a select line for a 2-1 MUX which controls what is presented to the DOB output. If this bit is 0, the normal data is displayed. If this bit is 1, the input clock of the DOB is displayed. This is useful for debugging and for mark space ratio tuning of optical links.

1965

Pixel_strobes

Size: 13-bit Controls: FEND Suggested value: 0

Global Register: 13 Alternate Register: AB[274:286]

1970 Enable line for each of the 13 strobes for the pixel latches. If high, when a GlobalPulse is issued with Latch_En enabled and S0=S1=0, the shift register cell value will be loaded into the corresponding pixel latch(es). The strobes are also used to select which latch to read back into the shift register. See Table 25.

S0

Size: 1-bit Controls: FEND Suggested value: 0

1975 Global Register: 13 Alternate Register: AB[273]

Controls the input to the double-column shift registers. See Table 24.

S1

Size: 1-bit Controls: FEND Suggested value: 0

Global Register: 13 Alternate Register: AB[272]

1980 Controls the input to the double-column shift registers. See Table 24.

HITLD_IN

Size: 1-bit Controls: FEND Suggested value: 0

Global Register: 21 Alternate Register: AB[141]

1985 If this bit is enabled, a pixel hit will load a 1 into the corresponding shift register cell. This could then be read out by setting HITLD_IN=0, ensuring S0=S1=0 and reading out the shift register. See Table 24.

DINJ_OVERRIDE

Size: 1-bit Controls: array Suggested value: 0

Global Register: 21 Alternate Register: AB[142]

1990 This is a way to set the digital injection line to always high. This is provided for testing the pixel digital regions in stop mode. For expert use only.

StopModeCnfg

Size: 1-bit Controls: EODCL Suggested value: 0

Global Register: 26 Alternate Register: C[50]

1995 If this bit is high, stop mode is enabled. Stop mode freezes all the latency counters for any pending hits in the chip. This allows to read out all hits stored in the array for all latency counter values, but no new hits will be stored while in stop mode. This is a very useful mode for testing the digital region.

ExtAnaCalSW

2000 Size: 1-bit Controls: PULSEGEN, IOB Suggested value: 0

Global Register: 31 Alternate Register: C[132]

This enables external analog charge injection from the dedicated input pad.

ExtDigCalSW

Size: 1-bit Controls: PULSEGEN, IOB Suggested value: 0

2005 Global Register: 31 Alternate Register: C[133]

This enables external digital injection from the dedicated input pad.

configBit

Size: 1-bit Controls: SRsync Suggested value: 0

Global Register: 4 Alternate Register: N/A

2010 “Synchronizes” data and clock coming from the analog shift register with the WrFrontEnd command before it is fed to the EOCHL. This helps to fix a problem with the latching of the data from the shift register in the EOCHL. This is for testing purposes. Please note that this bit shares the same location in the global memory as ErrorMask<20>.

C.3 Digital Value Settings and Masks2015 **Trigger_Count**

Size: 4-bit Controls: EOCHL Suggested value: 1

Global Register: 2 Alternate Register: N/A

Number of consecutive triggers to send upon issue of trigger command. After the CMD decodes the command, it is sent to the EOCHL where it is then multiplied. This is useful for trigger scans since the trigger command itself takes 5 clock cycles to issue. If there were no multiplier, the most often you could trigger would be every 5 clock cycles. Value 0000 means 16 consecutive triggers.

2020

Trig_Lat

Size: 8-bit Controls: EODCL Suggested value: 0-254

Global Register: 25 Alternate Register: C[40:47]

2025 8-Bit complement of trigger latency in clock cycles ($\text{Trig_Lat} = 255 - \text{true latency}$). When a hit is registered in a pixel, a latency counter starts counting down from 255 in the corresponding PDR. When the counter decreases past Trig_Lat, the hit will be erased. When a trigger is issued, events which have their latency counter equal to Trig_Lat will be flagged for read out. Do not use a value of $8'b11111111 = 8'd255$.

2030 **CMDent**

Size: 14-bit Controls: CMD Suggested value: 0

Global Register: 26 Alternate Register: C[51:64]

These bits control the CAL pulse for internal analog or digital injection. CAL[13:8] sets the delay, in clock cycle units, between the command detection and the beginning of the pulse. All values 0-63 are allowed.

2035 CAL[7:0] instead sets the width, always in clock cycles, of the CAL pulse that will be generated. The possible range is any value 0-255 resulting in pulse width 1-256 clocks.

HitDiscCnfg

Size: 2-bit Controls: EODCL, PDR Suggested value: 2

2040 Global Register: 26 Alternate Register: C[48:49]

These two bits discriminate between “small” and “big” hits in the PDRs. Pulse widths less than or equal to `HitDiscCnfg` are considered small, while hits larger than it are considered big. Do not use a value of $2'b11 = 2'd3$.

ErrorMask

2045 Size: 32-bit Controls: EOCHL Suggested value: 0

Global Register: 3, 4 Alternate Register: N/A

There are 32 error counters/lines in the chip. When errors in the chip are detected a service request is automatically flagged to be sent out for that particular error code. This service record itself will come out after the next data header is requested/sent and its counter reset. If the corresponding bit is enabled in ErrorMask, the chip will completely neglect sending out the service request automatically for that error. If a `Rd_Errors` pulse is sent to the EOCHL, all the error counters are sent to the user and then reset, regardless of the mask settings. Please note that ErrorMask<20> is overloaded and also controls the `configBit` variable.

2050

SELB

2055 Size: 40-bit Controls: array Suggested value: 0

Global Register: 32, 33, 34 Alternate Register: N/A

Each of the 40 double-columns has a shift register associated with it. If one of these shift registers becomes corrupt the user has the option of using a spare shift register which can be enabled by setting high the corresponding bit in SELB. Note that this configuration can be copied to the E-Fuses so that it is loaded by default upon chip power up. Also note that this B backup shift register does not have latch read back capability - it can only be used to program the pixel latches but not to read them back.

2060

DisableColumnCnfg

Size: 40-bit Controls: EODCL Suggested value: 0

2065 Global Register: 23, 24, 25 Alternate Register: C[0:39]

Setting a particular bit high will completely disable the digital portion of the selected double-column.

Chip_SN

Size: 16-bit Controls: N/A Suggested value: 0-65535

2070 Global Register: 35 Alternate Register: N/A

This is the chip serial number. Note that this configuration can be copied to the E-Fuses to permanently burn in a serial number.

EmptyRecordCnfg

Size: 8-bit Controls: DOB Suggested value: 0

2075 Global Register: 29 Alternate Register: C[100:107]

The DOB sends out empty records when the EOCHL FIFO is empty. If `no8b10b` is enabled (i.e. the DOB does not encode the output data), then the DOB uses this word as its “comma” instead of the 8b/10b K.28.1.

C.4 Control Pulser

2080 All bits in this section are useful only in conjunction with a GlobalPulse command. They simply enable possible destinations for the global pulse. Any of them can be enabled simultaneously.

SR_Clock

Size: 1-bit Controls: CTRLPULSER, EOCHL Suggested value: N/A

Global Register: 27 Alternate Register: C[65]

2085 If this bit is high when a GlobalPulse is issued, a single clock pulse is sent to the SR_Clock input in the EOCHL.

Latch_En

Size: 1-bit Controls: CTRLPULSER Suggested value: N/A

Global Register: 27 Alternate Register: C[66]

2090 If this bit is high when a GlobalPulse is issued, the value in the shift register cell will be copied into the pixel latches which are selected in Pixel_strobes. This applies to the double-columns which are selected via Colpr_Addr and Colpr_Mode.

SR_Clr

Size: 1-bit Controls: CTRLPULSER Suggested value: N/A

2095 Global Register: 27 Alternate Register: C[67]

If this bit is high when a GlobalPulse is issued, the double-column shift registers which are selected (i.e. Colpr_Mode and Colpr_Addr) will be all set to zero.

CalEn

Size: 1-bit Controls: CTRLPULSER Suggested value: N/A

2100 Global Register: 27 Alternate Register: C[68]

Having this bit enabled allows a GlobalPulse command to essentially act as a CalibrationPulse command with digital injection enabled. Please note that DIGITIN_SEL must also be enabled for this to work. The width of the pulse (which affects the ToT values) is adjusted by sending different width GlobalPulse commands.

ReadSkipped

Size: 1-bit Controls: CTRLPULSER, EOCHL Suggested value: N/A

Global Register: 27 Alternate Register: C[75]

2105 If this bit is high when a GlobalPulse is issued, the EOCHL will send out a “service record” with the number of skipped triggers. Upon the sending of this record, the skipped trigger counter is
2110 reset.

ReadErrorReq

Size: 1-bit Controls: CTRLPULSER, EOCHL Suggested value: N/A

Global Register: 27 Alternate Register: C[76]

2115 If this bit is high when a GlobalPulse is issued, the EOCHL will send out a “service record” for all 32 error lines (regardless of the value of ERRORMASK). After the service records are sent out, the counters are also cleared.

StopClkPulse

Size: 1-bit Controls: CTRLPULSER Suggested value: N/A

Global Register: 27 Alternate Register: C[77]

2120 If this bit is high when a GlobalPulse is issued and the chip is in stop mode (i.e StopModeCnfg is enabled), trigger latency counters for pixels which have registered hits will be incremented by one.

Efuse_Sense

Size: 1-bit Controls: CTRLPULSER, EFUSE Suggested value: N/A

Global Register: 27 Alternate Register: C[78]

2125 If this bit is high when a GlobalPulse is issued, the EFUSE registers will be reloaded with their PROM values. Anything the user has written to those registers will be lost.

C.5 Analog Biases

Please note that the global memory register and alternate shift register positions of the analog settings have not been verified in the SystemVerilog test bench.

2130 **PrmpVbp_R**

Size: 8-bit Controls: Column 40 Input transistor current Suggested value: 43

Global Register: 5 Alternate Register: AB[152:159]

This controls only the pixels in column 40 and is provided in case of long pixels.

Vthin

2135 Size: 8-bit Controls: Vthin output current Suggested value: N/A

Global Register: 5 Alternate Register: AB[144:151]

Set to 255 if using the temperature compensated Vthin_C voltage. Full scale is about 25 μ A.

Vthin_Alt

Size: 16-bit Controls: Vthin_C output voltage Suggested value: N/A

2140 Global Register: 20 Alternate Register: AB[96:111]

Two 8 bit values for coarse and fine adjustment. The coarse scale is non-linear. Range is 0 to 1V.

DisVbn_CPPM

Size: 8-bit Controls: Discriminator bias for "CPPM" columns Suggested value:

62

2145 Global Register: 6 Alternate Register: AB[168:175]

See Table 32 for listing of column variants in FE-I4A.

PrmpVbp

Size: 8-bit Controls: Columns 2-39 Input transistor current Suggested value: 43

Global Register: 6 Alternate Register: AB[160:167]

2150 Main preamp bias. This setting will have the greatest impact on the VDDA2 current of the chip. Set to 00 to turn off the preamps and most of the current.

TdacVbp

Size: 8-bit Controls: TDAC LSB size Suggested value: 255

Global Register: 7 Alternate Register: AB[184:191]

2155

DisVbn

Size: 8-bit Controls: Discriminator bias for baseline columns Suggested value: 26

Global Register: 7 Alternate Register: AB[176:183]

2160 See Table 32 for listing of column variants in FE-I4A. This bias affects all columns except “CPPM” type.

Amp2Vbn

Size: 8-bit Controls: Second stage main bias Suggested value: 79

Global Register: 8 Alternate Register: AB[200:207]

2165

Amp2VbpFol

Size: 8-bit Controls: Second stage follower bias Suggested value: 26

Global Register: 8 Alternate Register: AB[192:199]

2170 **PrmpVbp_T**

Size: 8-bit Controls: Not used Suggested value: 0

Global Register: 9 Alternate Register: AB[216:223]

This is not used in FE-I4A. Intended to support ganged pixels in future versions.

Amp2Vbp

2175 Size: 8-bit Controls: Second stage load bias Suggested value: 85

Global Register: 9 Alternate Register: AB[208:215]

FdacVbn

Size: 8-bit Controls: FDAC LSB size Suggested value: 50

2180 Global Register: 10 Alternate Register: AB[232:239]

Amp2Vbpf

Size: 8-bit Controls: Second stage feedback current Suggested value: 13

Global Register: 10 Alternate Register: AB[224:231]

2185

PrmpVbnFol

Size: 8-bit Controls: Preamp follower bias Suggested value: 106

Global Register: 11 Alternate Register: AB[248:255]

2190 Bias to the follower of the first stage. This follower drives the coupling capacitor between first and second stages.

PrmpVbp_L

Size: 8-bit Controls: Column 1 Input transistor current Suggested value: 43

Global Register: 11 Alternate Register: AB[240:247]

This controls only the pixels in column 1 and is provided in case of long pixels.

2195 **PrmpVbpf**

Size: 8-bit Controls: Preamp feedback Suggested value: 20

Global Register: 12 Alternate Register: AB[264:271]

This is the master feedback current of the preamp. It sets the fall time of preamp output which in turn determines the ToT LSB scale. There is a 4-bit trim of this current in each pixel.

2200 **PrmpVbnLcc**

Size: 8-bit Controls: Preamp leakage compensation Suggested value: 0

Global Register: 12 Alternate Register: AB[256:263]

Leakage current compensation circuit bias.

PlsrDacBias

2205 Size: 8-bit Controls: Suggested value: 96

Global Register: 19 Alternate Register: AB[88:95]

Bias for calibration voltage DAC.

PlsrDAC

Size: 10-bit Controls: Suggested value: 0-255

2210 Global Register: 21 Alternate Register: AB[112:121]

Calibration injection voltage value (VCAL).

PlsrDelay

Size: 6-bit Controls: PULSER Suggested value: 2

Global Register: 31 Alternate Register: C[134:139]

2215 Analog fine delay value for the calibration pulse. Applies to both digital and analog injection. This delay is added on top of the CMDcnt delay.

PlsrldacRamp

Size: 8-bit Controls: Suggested value: 180

Global Register: 17 Alternate Register: AB[48:55]

2220 This is the bias current for the analog delay generator above. It controls the delay step size. It can also be used to adjust the delay, but the delay is proportional to the inverse of this current, while the PlsrDelay adjustment is linear. See Fig. 30.

PlsrRiseUpTau

Size: 3-bit Controls: PULSER Suggested value: 7

2225 Global Register: 31 Alternate Register: C[141:143]

2230 Sets the speed of the return to baseline of the analog calibration pulse. The baseline is the VCAL voltage (see PlsrDAC). To inject charge the voltage is switched very fast from baseline to ground and held at ground for the duration of the CAL pulse (see CMDcnt). After this time the voltage linearly ramps back up to VCAL to avoid reverse polarity injection. The speed of this ramp is controlled by this bias.

PlsrVgOPamp

Size: 8-bit Controls: Suggested value: 255

Global Register: 18 Alternate Register: AB[64:71]

Bias for op-amps used in pulse generator.

2235 **LvdsDrvIref**

Size: 8-bit Controls: LVDS driver bias current Suggested value: 171

Global Register: 14 Alternate Register: AB[8:15]

BonnDac

2240 Size: 8-bit Controls: PLSGEN current to voltage converter Suggested value: 237

Global Register: 14 Alternate Register: AB[0:7]

Bias for the current to voltage converter of the PULSGEN.

PlIbias

Size: 8-bit Controls: PLL bias current Suggested value: 88

2245 Global Register: 15 Alternate Register: AB[24:31]

Bias current of PLL oscillator

LvdsDrvVos

Size: 8-bit Controls: LDVS driver offset voltage Suggested value: 105

Global Register: 15 Alternate Register: AB[16:23]

2250

TempSensIbias

Size: 8-bit Controls: Not used Suggested value: 0

Global Register: 16 Alternate Register: AB[40:47]

Not used in FE-I4_A as the temperature sensor is not included.

2255 **PlIcp**

Size: 8-bit Controls: PLL comparator bias Suggested value: 28

Global Register: 16 Alternate Register: AB[32:39]

Bias current of comparator in PLL phase detector

lvdsDrvSet12

2260 Size: 1-bit Controls: LVDS driver strength Suggested value: 1
Global Register: 29 Alternate Register: C[96]
Coarse control of the output current of the LVDS output.

IvdsDrvSet30

2265 Size: 1-bit Controls: LVDS driver strength Suggested value: 1
Global Register: 29 Alternate Register: C[97]
Medium control of the output current of the LVDS output.

IvdsDrvSet06

2270 Size: 1-bit Controls: LVDS driver strength Suggested value: 1
Global Register: 28 Alternate Register: C[95]
Fine control of the output current of the LVDS output.

D. Wire Bond Pads

Figure 47 shows the layout of the wire bond pads for the chip. Table 38 gives the list of the bond pads on the bottom row, Table 39 for the middle row and Table 40 gives the list for the top row of pads.

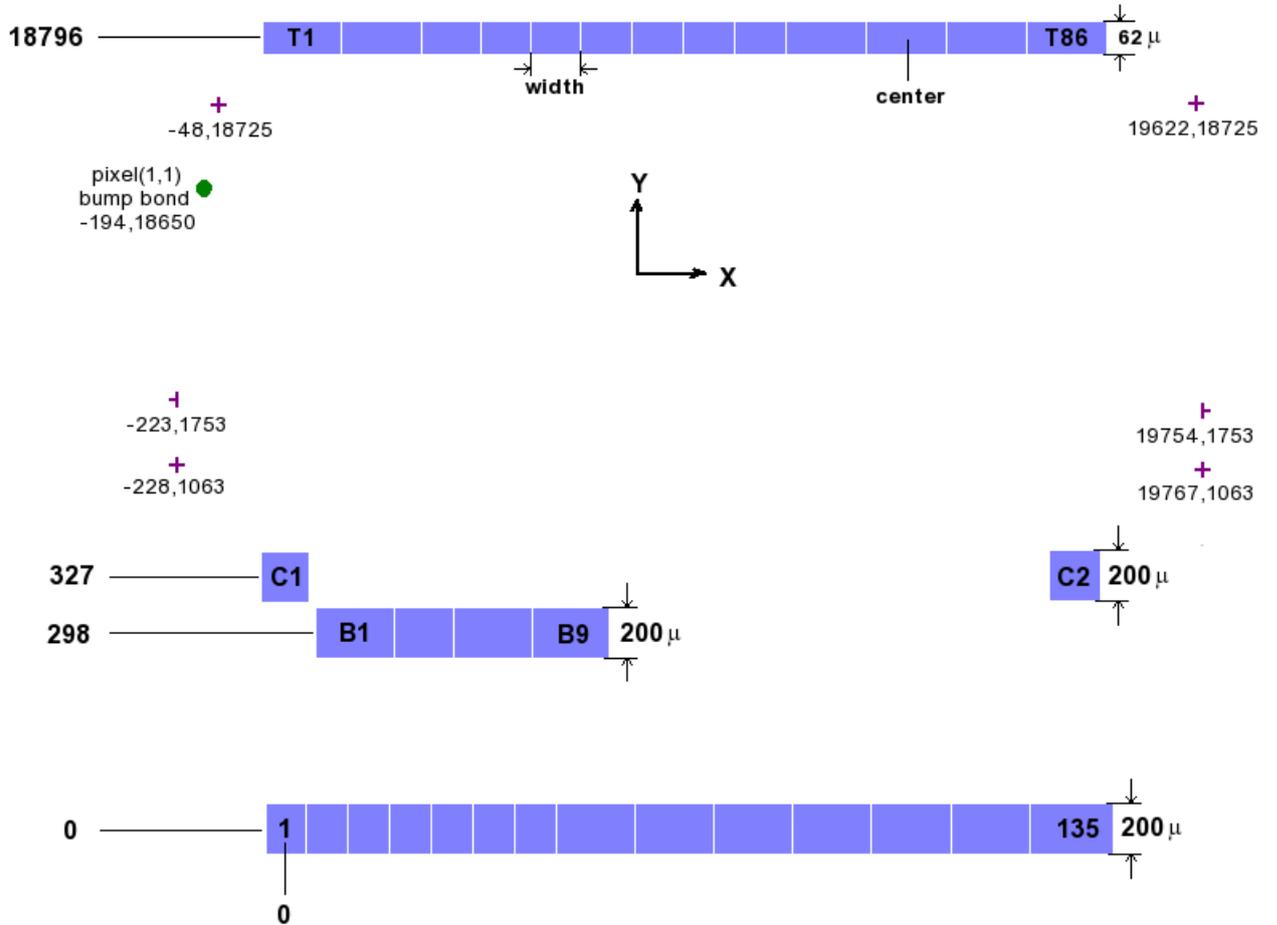


Figure 47: Layout of the wire bond pads. The origin (0,0) is centered on pad 1. The bottom and middle rows of pads are 200 μm high, the top row pads are 62 μm high. The pad widths vary and are given in the tables for each pad. The numbers along the left indicate the ordinates of that row of pads. For example, the coordinates of pad C2 are (19731,327). The (x,y) coordinates of the alignment marks, and of the bump bond for pixel (1,1) are also shown.

D WIRE BOND PADS

Pad Num	Name	Center (μm)	Width (μm)	Description	ESD rail
1	out1_00_P	0	75	Buffered preamp output of pixel 1/336 needs a 1 kΩ resistor to VDDA2	VDDA2
2	PrmpVbpf_P	100	75	Main preamp feedback bias (feedback global control).	VDDA2
3	PrmpVbnLcc_P	200	75	Leakage compensation amp bias.	VDDA2
4	PrmpVbnFol_P	300	75	Preamp follower bias.	VDDA2
5	PrmpVbp_L_P	400	75	Main Preamp bias for column 1 (leftmost)	VDDA2
6	FdacVbn_P	500	75	Controls the LSB of the preamp feedback DAC (feedback local tuning)	VDDA2
7	Amp2Vbpf_P	600	75	Stage 2 Feedback bias.	VDDA2
8	Amp2Vbp_P	700	75	Stage 2 load bias.	VDDA2
9	Amp2Vbn_P	800	75	Stage 2 main bias.	VDDA2
10	Amp2VbpFol_P	900	75	Stage follower main bias.	VDDA2
11	TdacVbp_P	1000	75	Controls the LSB of the local threshold DAC (threshold local tuning)	VDDA2
12	DisVbn_P	1100	75	Discriminator bias.	VDDA2
13	DisVbn_cppm_P	1200	75	CPPM Discriminator bias (col 79 and 80)	VDDA2
14	PrmpVbp_P	1300	75	Main Preamp bias for all columns except the leftmost and rightmost.	VDDA2
15	PrmpVbp_R_P	1400	75	Main Preamp bias for column 80 (rightmost)	VDDA2
16	vthin_P	1500	75	Controls the global threshold instead of vthinC_P if desired. Needs 45kΩ to GROUND if used alone. (see Section 6.1)	VDDA2
17	vref_P	1600	75	A reference voltage (set at 1/2 VDDA2). Used by the pulser.	VDDA2
18	PlsrIdacRamp_P	1700	75	Pulser Ramp control	VDDA2
19	Pllbias_P	1800	75	Provided the PLL Ibias	VDDA2
20	Pllicp_P	1900	75	Provided the PLL charge pump bias	VDDA2
21	LvdsDrvIref_P	2000	75	A bias for the LVDS driver.	VDDA2
22	LvdsDrvVos_P	2100	75	A reference voltage to the LVDS driver (controls the common mode)	VDDA2
23	IleakOut_P	2200	75	Detector leakage monitor	VDDA2
24	VthinC_P	2300	75	Could be used to control the global threshold. Should be connected to vthin_P to be usable.	VDDA2

Continued on next page

Table 38 – continued from previous page

Pad Num	Name	Center (μm)	Width (μm)	Description	ESD rail
25	VDDA2M	2400	75	Connected to measure VDDA2 inside the chip. Should not be connected to VDDA2 off chip.	VDDA2
26	GND A2	2537	100	Ground, return for VDDA2 powered blocs	VDDA2
27	VSS	2687	100	Substrate potential (0V)	VDDA2
28	VDDA2	2837	100	VDDA2 powers the main analog array and the bias DACs (with other blocks). 1.5V nominal	VDDA2
29	VDDD2	2987	100	VDDD2 powers the main digital array and the EOCHL bloc (with other blocks). 1.2V nominal	VDDD2
30	GND D2	3137	100	Ground return for VDDD2 powered blocs	VDDD2
31	VSS	3287	100	Substrate potential (0V)	VDDD2
32	VDDT3_Shield	3437	100	Biases most of the isolation regions (T3). 1.5V nominal	-
33	Iref_out_P	3587	100	Master current reference (to be looped back and connected to VbbnIn_P)	VDDA2
34	VbbnIn_P	3737	100	Master bias for the DACs (nominally provided at Iref_out_P)	VDDA2
35	GND A2	3887	100	Ground, return for VDDA2 powered blocs	VDDA2
36	VDDA2	4037	100	VDDA2 powers the main analog array and the bias DACs (with other blocks). 1.5V nominal	VDDA2
37	GND A2	4187	100	Ground, return for VDDA2 powered blocs	VDDA2
38	VDDA2	4337	100	VDDA2 powers the main analog array and the bias DACs (with other blocks). 1.5V nominal	VDDA2
39	VDDD2	4487	100	Powers the main digital array and the EOCHL bloc (with other blocks). 1.2V nominal	VDDD2
40	GND D2	4637	100	Ground return for VDDD2 powered blocs	VDDD2
41	VDD33	4787	100	3.3V supply for the Efuse programming. Needed only for Efuse programming.	VDD33 /GND A1
42	VDDEfuse	4937	100	Digital supply for the Effuse bloc (1.5 or 1.2 to be determined based on the test). 1.5V nominal	VDDEfuse /GND A1
43	VDDA1	5087	100	Powers configuration memory, registers and related blocs. 1.5V nominal	VDDA1

Continued on next page

Table 38 – continued from previous page

Pad Num	Name	Center (μm)	Width (μm)	Description	ESD rail
44	GNDA1	5237	100	Ground, return for VDDA1 powered blocs	VDDA1
45	RA1bar_P	5387	100	Resets the blocs powered by VDDA1. Active low. Pulled-up on-chip. can be overridden.	VDDA1
46	ExtAnaInjectIn_P	5537	100	Overrides the internal analog charge injection.	VDDA1
47	capMeasure_P	5687	100	Not Connected	VDDA1
48	VDDA1	5837	100	Powers configuration memory, registers and related blocs. 1.5V nominal	VDDA1
49	GNDA1	5987	100	Ground, return for VDDA1 powered blocs	VDDA1
50	ExtDigInjectIn_P	6137	100	External digital hit “emulation”	VDDA1
51	regABstbld_P	6287	100	Loads the control portion of the AB shift register into the effective latches.	VDDA1
52	regABDaclD_P	6437	100	Loads the DAC portion of the AB shift register into the effective latches.	VDDA1
53	SelAltBus_P	6587	100	Determines whether the main memory latches are used or the alternate latches are used to configure the chip.	VDDA1
54	VDDA1	6737	100	Powers configuration memory, registers and related blocs. 1.5V nominal	VDDA1
55	GNDA1	6887	100	Ground, return for VDDA1 powered blocs	VDDA1
56	RA2bar_P	7037	100	Resets the blocs powered by VDDA1. Active low. Pulled-up on-chip. can be overridden.	VDDA1
57	GNDA2	7187	100	Ground, return for VDDA2 powered blocs	VDDA2
58	VSS	7337	100	Substrate potential (0V)	VDDA2
59	VDDA2	7487	100	VDDA2 powers the main analog array and the bias DACs (with other blocks). 1.5V nominal	VDDA2
60	VDDD2	7637	100	Powers the main digital array and the EOCHL bloc (with other blocks). 1.2V nominal	VDDD2
61	GNDD2	7787	100	Ground return for VDDD2 powered blocs	VDDD2
62	VSS	7937	100	Substrate potential (0V)	VDDD2
63	VDDT3_Pad	8087	100	Biases isolation regions (T3) of IO bloc. 1.5V nominal	VDDD2
64	VDDD1	8237	100	Powers Command decoder and other control blocs (i.e. IOMux). 1.2V nominal	VDDD1

Continued on next page

Table 38 – continued from previous page

Pad Num	Name	Center (μm)	Width (μm)	Description	ESD rail
65	GNDD1	8387	100	Ground, return for VDDD1 powered blocs	VDDD1
66	Cmd_ExtTrigger_P	8537	100	External generation of a trigger (usually generated by the command decoder)	VDDD1
67	Cmd_ChipId_P<0>	8687	100	Chip ID bit 0	VDDD1
68	Cmd_ChipId_P<1>	8837	100	Chip ID bit 1	VDDD1
69	Cmd_ChipId_P<2>	8975	75	Chip ID bit 2	VDDD1
70	Cmd_AltPls_P	9112	100	General purpose external digital pulse (usually generated by the command decoder)	VDDD1
71	IoMxSel_P<2>	9262	100	Input/output multiplexer channel(bloc) selection.	VDDD1
72	IoMxSel_P<1>	9412	100	Input/output multiplexer channel(bloc) selection.	VDDD1
73	IoMxSel_P<0>	9562	100	Input/output multiplexer channel(bloc) selection.	VDDD1
74	IoMxIn_P<0>	9712	100	Input of IO multiplexer bit 0.	VDDD1
75	IoMxIn_P<1>	9862	100	Input of IO multiplexer bit 1.	VDDD1
76	IoMxIn_P<2>	10012	100	Input of IO multiplexer bit 2.	VDDD1
77	IoMxIn_P<3>	10162	100	Input of IO multiplexer bit 3.	VDDD1
78	VDDD1	10312	100	Powers Command decoder and other control blocs (i.e. IOMux). 1.2V nominal	VDDD1
79	GNDD1	10462	100	Ground, return for VDDD1 powered blocs	VDDD1
80	VDD_PLL	10612	100	Powers the PLL core.	VDD_PLL
81	GND_PLL	10762	100	Ground, return for PLL core	VDD_PLL
82	IoMxOut_P<0>	10912	100	Output of IO mulShunt circuitry power supply. Should be grounded if in regulation mode. tipleplexer bit 0.	VDDD1
83	IoMxOut_P<1>	11062	100	Output of IO multiplexer bit 1.	VDDD1
84	IoMxOut_P<2>	11212	100	Output of IO multiplexer bit 2.	VDDD1
85	SelCmd_P	11362	100	Enables the command decoder to program the array configuration shift register,	VDDD1
86	VDDD1	11512	100	Powers Command decoder and other control blocs (i.e. IOMux). 1.2V nominal	VDDD1
87	GNDD1	11662	100	Ground, return for VDDD1 powered blocs	VDDD1
88	RD1bar_P	11812	100	Resets the blocs powered by VDDD1. Acrive low. Pulled-up on-chip. can be overridden.	VDDD1

Continued on next page

Table 38 – continued from previous page

Pad Num	Name	Center (μm)	Width (μm)	Description	ESD rail
89	RD2bar_P	11962	100	Resets the blocs powered by VDDD2. Active low. Pulled-up on-chip. can be overridden.	VDDD1
90	Aux_Clk_N	12112	100	Auxillary clock input. LVDS MINUS	VDDD1
91	Aux_Clk_P	12262	100	Auxillary clock input. LVDS PLUS	VDDD1
92	Ref_Clk_N	12412	100	Reference clock input. LVDS MINUS	VDDD1
93	Ref_Clk_P	12562	100	Reference clock input. LVDS PLUS	VDDD1
94	CMD_DCI_N	12712	100	Command Decoder Data Input. LVDS MINUS	VDDD1
95	CMD_DCI_P	12862	100	Command Decoder Data Input. LVDS PLUS	VDDD1
96	VDDD1	13012	100	Powers Command decoder and other control blocs (i.e. IOMux). 1.2V nominal	VDDD1
97	GNDD1	13162	100	Ground, return for VDDD1 powered blocs	VDDD1
98	LvdsRecVbn_P	13300	75	LVDS receiver bias.	VDDD1
99	LvdsRecVbp_P	13400	75	LVDS receiver bias.	VDDD1
100	GNDA2	13537	100	Ground, return for VDDA2 powered blocs	VDDA2
101	VSS	13687	100	Substrate potential (0V)	VDDA2
102	VDDA2	13837	100	VDDA2 powers the main analog array and the bias DACs (with other blocks). 1.5V nominal	VDDA2
103	DOB_OUT_P	13987	100	Data output. LVDS PLUS	VDDD2
104	DOB_OUT_N	14137	100	Data output. LVDS MINUS	VDDD2
105	HitOr_P	14287	100	Buffered chip-wide OR'ed hit (the OR of all hits)	VDDD2
106	VDDD2	14437	100	Powers the main digital array and the EOCHL bloc (with other blocks). 1.2V nominal	VDDD2
107	GNDD2	14587	100	Ground return for VDDD2 powered blocs	VDDD2
108	VSS	14737	100	Substrate potential (0V)	VDDD2
109	VDDT3_Pad	14887	100	Biases isolation regions (T3) of IO bloc. 1.5V nominal	VDDD2
110	VDDD2	15037	100	Powers the main digital array and the EOCHL bloc (with other blocks). 1.2V nominal	VDDD2
111	GNDD2	15187	100	Ground return for VDDD2 powered blocs	VDDD2

Continued on next page

Table 38 – continued from previous page

Pad Num	Name	Center (μm)	Width (μm)	Description	ESD rail
112	VDDD2	15337	100	Powers the main digital array and the EOCHL bloc (with other blocks). 1.2V nominal	VDDD2
113	GNDD2	15487	100	Ground return for VDDD2 powered blocs	VDDD2
114	GNDA2	15637	100	Ground, return for VDDA2 powered blocs	VDDA2
115	VDDA2	15787	100	VDDA2 powers the main analog array and the bias DACs (with other blocks). 1.5V nominal	VDDA2
116	GNDA2	15937	100	Ground, return for VDDA2 powered blocs	VDDA2
117	VDDA2	16087	100	VDDA2 powers the main analog array and the bias DACs (with other blocks). 1.5V nominal	VDDA2
118	Vbp1_P	16224	75	Regulator 1 Bias	DCDC_IN/ REG_GND
119	Vref1_P	16324	75	Regulator 1 Reference	DCDC_IN/ REG_GND
120	Rext1_P	16424	75	Regulator 1 setting	DCDC_IN/ REG_GND
121	Rint1_captionP	16562	100	Regulator 1 setting	DCDC_IN/ REG_GND
122	VddShunt1	16712	100	Power for shunt circuitry. Should ground for pure linear mode.	DCDC_IN/ REG_GND
123	REG1_GND	16937	250	Regulator 1 return (ground)	DCDC_IN/ REG_GND
124	REG1_OUT	17237	250	Regulator 1 ouput	DCDC_IN/ REG_GND
125	REG1_IN	17537	250	Regulator 1 input	DCDC_IN/ REG_GND
126	CAP_BOT_P	17837	250	DC-DC capacitor bottom plate	DCDC_IN/ REG_GND
127	CAP_TOP_P	18137	250	DC-DC capacitor top plate	DCDC_IN/ REG_GND
128	DCDC_IN	18437	250	DC-DC input	DCDC_IN/ REG_GND
129	GNDA2	18662	100	Ground, return for VDDA2 powered blocs	VDDA2
130	VSS	18812	100	Substrate potential (0V)	VDDA2

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Table 38 – continued from previous page

Pad Num	Name	Center (μm)	Width (μm)	Description	ESD rail
131	VDDA2	18962	100	VDDA2 powers the main analog array and the bias DACs (with other blocks). 1.5V nominal	VDDA2
132	VDDD2	19112	100	Powers the main digital array and the EOCHL bloc (with other blocks). 1.2V nominal	VDDD2
133	GNDD2	19262	100	Ground return for VDDD2 powered blocs	VDDD2
134	VSS	19412	100	Substrate potential (0V)	VDDD2
135	VDDT3_Shield	19562	100	Biases most of the isolation regions (T3). 1.5V nominal	VDDD2

Table 38: Bottom Row Pads. Unless explicitly indicated, the ESD rail return is the corresponding GROUND. For example, VDDA2 is paired with GNDA2, and VDD_PLL is paired with GND_PLL.

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Pad Number	Pad Name	Pad Center (μm)	Pad Width (μm)	ESD rail
C1	DetBias_L	-157	100	None
B2	REG2_IN	277	250	REG2_IN
B3	REG2_OUT	577	250	REG2_IN
B4	REG2_GND	877	250	REG2_IN
B5	VDDShunt2	1102	100	REG2_IN
B6	Rint2_P	1252	100	REG2_IN
B7	Rext2_P	1389	75	REG2_IN
B8	Vref2_P	1489	75	REG2_IN
B9	Vbp2_P	1589	75	REG2_IN
B10	VSS	1727	100	REG2_IN
C2	DetBias_R	19731	100	None

Table 39: Middle Row Pads. The GND corresponding to REG2_IN is REG2_GND.

Pad Number	Name	Center (μm)	Width (μm)	Description
T1	Ileakout	151	140	Leakage monitoring output probed at the location of pad (connected to the global IleakOut)

Continued on next page

Table 40 – continued from previous page

Pad Number	Name	Center (μm)	Width (μm)	Description
T2	InjectInL1	377	140	InjectIn (analog inject input) of column 1 (leftmost). For monitoring or override.
T3	GND A2M	603	140	Connected to measure GND A2 inside the chip. Should not be connected to GND A2 off chip.
T4	vthEffL<1>	828	140	Effective threshold setting node. Internal node pixel 1/1
T5	VDD A2M	1054	140	Connected to measure VDD A2 inside the chip. Should not be connected to VDD A2 off chip.
T6	GND D2M	1280	140	Connected to measure GND D2 inside the chip. Should not be connected to GND D2 off chip.
T7	VDD D2M	1505	140	Connected to measure VDD D2 inside the chip. Should not be connected to VDD D2 off chip.
T8	outD2<0>	1731	140	Buffered Hit of Pixel 2/1.
T9	outD1<0>	1957	140	Buffered HitOr of column 2.
T10	outD1<1>	2183	140	Buffered HitOr of column 3.
T11	outD2<1>	2408	140	Buffered Hit of Pixel 3/1.
T12	outD2<2>	2634	140	Buffered Hit of Pixel 4/1.
T13	outD1<2>	2860	140	Buffered HitOr of column 4
T14	vddd_L	3086	140	Power for digital Buffers on left half of chip. 1.2V. connected to VDDD_TOP at the PCB level.
T15	gndd_L	3311	140	ground return for vddd_L
T16	gnda_L	3537	140	ground return for vdda_L
T17	vdda_L	3763	140	Power for simple analog Buffers on left half of chip. 1.5V. connected to VDDA_TOP at the PCB level.
T18	out2<0>	3988	140	Buffered 2nd stage output for pixel 2/1
T19	out1<0>	4214	140	Buffered preamp output for pixel 2/1. Requires a pull-up resistor to VDDA_TOP.
T20	out1<1>	4440	140	Buffered preamp output for pixel 3/1. Requires a pull-up resistor to VDDA_TOP.
T21	out2<1>	4666	140	Buffered 2nd stage output for pixel 3/1

Continued on next page

Table 40 – continued from previous page

Pad Number	Name	Center (μm)	Width (μm)	Description
T22	out2<2>	4891	140	Buffered 2nd stage output for pixel 4/1
T23	out1<2>	5117	140	Buffered preamp output for pixel 4/1. Requires a pull-up resistor to VDDA_TOP.
T24	PwrEnable_L	5277	140	Power Enable for the Analog Buffers Bloc on the Let side of the chip (ABBL)
T25	Sel_L<3>	5503	140	Channel selection bit 3 for ABBL
T26	out_L<3>	5729	140	Output 3 of the ABBL.
T27	Vg_L	5954	140	Bias for the ABBL
T28	out_L<2>	6180	140	Output 2 of the ABBL.
T29	vssaT	6406	140	Substrate. Connected to ground.
T30	out_L<1>	6631	140	Output 1 of the ABBL.
T31	gndaT	6857	140	Analog ground for the Analog Buffers Blocs.
T32	vddaT	7083	140	Analog Power for the Analog Buffers Blocs. 1.5V
T33	out_L<0>	7309	140	Output 0 of the ABBL
T34	Sel_L<2>	7534	140	Channel selection bit 2 for ABBL
T35	Sel_L<1>	7760	140	Channel selection bit 1 for ABBL
T36	Sel_L<0>	7986	140	Channel selection bit 0 for ABBL
T37	PwrEnable	8277	140	Power Enable for the Analog Buffers Bloc at the center of the chip (ABBC)
T38	Sel<3>	8503	140	Channel selection bit 3 for ABBC
T39	out<3>	8729	140	Output 3 of the ABBC.
T40	Vg	8954	140	Bias for the ABBC (should be shorted to Vg_L, pad T27)
T41	out<2>	9180	140	Output 2 of the ABBC.
T42	vssaT	9406	140	Substrate. Connected to ground.
T43	out<1>	9631	140	Output 1 of the ABBC.
T44	gndaT	9857	140	Analog ground for the Analog Buffers Blocs.
T45	vddaT	10083	140	Analog Power for the Analog Buffers Blocs. 1.5V
T46	out<0>	10309	140	Output 0 of the ABBC.
T47	Sel<2>	10534	140	Channel selection bit 2 for ABBC
T48	Sel<1>	10760	140	Channel selection bit 1 for ABBC
T49	Sel<0>	10986	140	Channel selection bit 0 for ABBC

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Table 40 – continued from previous page

Pad Number	Name	Center (μm)	Width (μm)	Description
T50	PwrEnable_R	11277	140	Power Enable for the Analog Buffers Bloc on the right of the chip (ABBR)
T51	Sel_R<3>	11503	140	Channel selection bit 3 for ABBR
T52	out_R<3>	11729	140	Output 3 of the ABBR.
T53	Vg_R	11954	140	Bias for the ABBR (should be shorted to Vg_L, pad T27)
T54	out_R<2>	12180	140	Output 2 of the ABBR.
T55	vssaT	12406	140	Substrate. Connected to ground.
T56	out_R<1>	12631	140	Output 1 of the ABBR.
T57	gndaT	12857	140	Analog ground for the Analog Buffers Blocs.
T58	vddaT	13083	140	Analog Power for the Analog Buffers Blocs. 1.5V
T59	out_R<0>	13309	140	Output 0 of the ABBR.
T60	Sel_R<2>	13534	140	Channel selection bit 2 for ABBR
T61	Sel_R<1>	13760	140	Channel selection bit 1 for ABBR
T62	Sel_R<0>	13986	140	Channel selection bit 0 for ABBR
T63	vbpBuf	14231	140	Bias for the simple analog buffers.
T64	out1_R<2>	14457	140	Buffered preamp output for pixel 77/1. Requires a pull-up resistor to VDDA_TOP.
T65	out2_R<2>	14683	140	Buffered 2nd stage output for pixel 77/1
T66	out2_R<1>	14909	140	Buffered 2nd stage output for pixel 78/1
T67	out1_R<1>	15134	140	Buffered preamp output for pixel 78/1. Requires a pull-up resistor to VDDA_TOP.
T68	out1_R<0>	15360	140	Buffered preamp output for pixel 79/1. Requires a pull-up resistor to VDDA_TOP.
T69	out2_R<0>	15586	140	Buffered 2nd stage output for pixel 79/1
T70	vdda_R	15811	140	Power for simple analog Buffers on right half of chip. 1.5V. connected to VDDA_TOP at the PCB level.
T71	gnda_R	16037	140	ground return for vdda_R
T72	gndd_R	16263	140	ground return for vddd_R

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Table 40 – continued from previous page

Pad Number	Name	Center (μm)	Width (μm)	Description
T73	vddd_R	16489	140	Power for digital Buffers on right half of chip. 1.2V. connected to VDDD_TOP at the PCB level.
T74	outD1_R<2>	16714	140	Buffered HitOr of column 77.
T75	outD2_R<2>	16940	140	Buffered Hit of Pixel 77/1.
T76	outD2_R<1>	17166	140	Buffered Hit of Pixel 78/1.
T77	outD1_R<1>	17392	140	Buffered HitOr of column 78.
T78	outD1_R<0>	17617	140	Buffered HitOr of column 79.
T79	outD2_R<0>	17843	140	Buffered Hit of Pixel 79/1.
T80	VDDD2M	18069	140	Connected to measure VDDD2 inside the chip. Should not be connected to VDDD2 off chip.
T81	GNDD2M	18294	140	Connected to measure GNDD2 inside the chip. Should not be connected to GNDD2 off chip.
T82	VDDA2M	18520	140	Connected to measure VDDA2 inside the chip. Should not be connected to VDDA2 off chip.
T83	vthEffR<40>	18746	140	Effective threshold setting node. Internal node pixel 80/1
T84	GNDA2M	18972	140	Connected to measure GNDA2 inside the chip. Should not be connected to GNDA2 off chip.
T85	InjectInR40	19197	140	InjectIn (analog inject input) of columns 79 and 80 (leftmost). For monitoring or override.
T86	Ileakout	19423	140	Leakage monitoring output probed at the location of pad (connected to the global IleakOut)

Table 40: Top Row Pads. The ESD rail for these pads is VDDA_T with GNDA_T.

E. FE-I4A Wafer Information

2280 The FE-I4A chip is fabricated on 200 mm diameter wafers with 60 chips per wafer. Figure 48 shows the wafer layout along with the numbering of the chips. The stepping dimensions are given in Table 41. Although the crack stop is not active circuitry, it must not be removed during dicing as it is needed to protect the circuit from damage due to crack propagation.

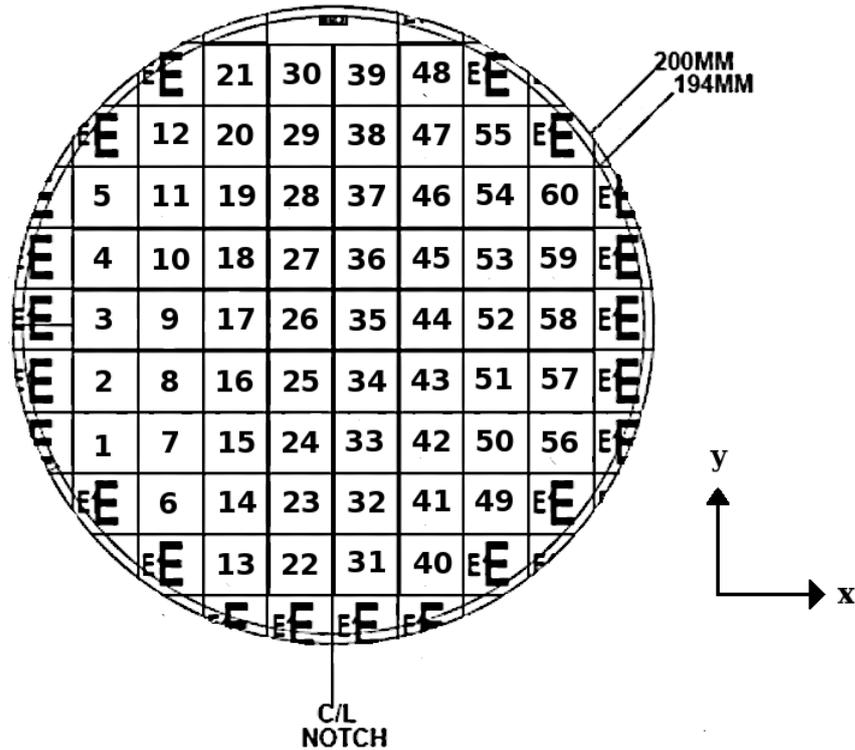


Figure 48: Layout of the FE-I4A wafer, showing the numbering of the individual chips. Partial chips marked with the letter “E” are empty reticles not actually printed on the physical wafer. The coordinate origin is at the center of the wafer.

	x (μm)	y (μm)
chip size	20030.16	18962.56
crack-stop	15.00	15.00
dicing road	270.00	270.00
chip to chip pitch	20330.16	19262.56
Chip 1 center	-71156.24	-36943.64

Table 41: Dimensions of circuit and wafer stepping. The coordinate origin is at the center of the wafer.

The 16-bit serial number to be programmed into the Efuse read only memory will contain the wafer number and chip number as shown in Table 42.

Bits [MSB-LSB]	[15]	[14-6]	[5-0]
Content	reserved	wafer number	chip number

Table 42: Content of programmable read-only 16-bit serial number