Event selector - the 1st level Trigger for the Mini-FOBOS Facility

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Purpose of instrument

This real-time processor decides upon readout or fast reset of the measurement units of the Mini-FOBOS data acquisition system (DAQ) (figure 1) depending on timing relation between fission fragments and their multiplicity as detected by the position-sensitive avalanche counters (PSAC).

1 Module mechanics

This device is a single CAMAC unit with 1 LED and 16 LEMO ERA-00 series connectors on the front panel and one 10-pole 2.54 mm flat cable plug on the rear side.

2 Signal specification

Signals are listed with top to bottom ordering of their corresponding LEMO connectors:

"Target"
Type: input
Standard: NIM, positive logic
Duration: (10 - 50)ns
Short description: fast cathode pulse from the fission target detector
Application: generates a "Stop" timing marker for the time-to-digital convertors (TDC) in the time-of-flight spectrometry (TOF)

"PSAC 1"
Type: input
Standard: NIM, positive logic
Duration: (10 - 50)ns
Short description: fast cathode pulse from the PSAC in the 1st spectrometer arm
Application: launches the readout system, generates a "Start" timing marker for the TDC in the 1st spectrometer arm

"PSAC 2"
Type: input
Standard: NIM, positive logic
Duration: (10 - 50)ns
Short description: fast cathode pulse from the PSAC in the 2nd spectrometer arm
Application: launches the readout system, generates a "Start" timing marker for the TDC in the 2nd spectrometer arm

"External gate return"

Type: input
Standard: NIM, positive logic
Duration: 10ns minimum
Short description: a standard width pulse launched by the first triggered PSAC signal and retarded by an external delay line
Application: closes the timing gate in the detector coincidence scheme

"Start BDP 1"

Type: output
Standard: TTL/CMOS, complementary logic
Duration: 1μs
Short description: a standard width pulse launched by the "PSAC 1" signal and retarded by an internal programmable delay line
Application: starts the Bragg digital processor in the 1st spectrometer arm

"Start BDP 2"

Type: output
Standard: TTL/CMOS, complementary logic
Duration: 1μs
Short description: a standard width pulse launched by the "PSAC 2" signal and retarded by an internal programmable delay line
Application: starts the Bragg digital processor in the 2nd spectrometer arm

"Start TDC 1"

Type: output
Standard: NIM, positive logic
Duration: same as "PSAC 1" pulse
Short description: a standard width pulse launched by the "PSAC 1" signal
Application: starts the TDC in the 1st spectrometer arm

"Start TDC 2"

Type: output
Standard: NIM, positive logic
Duration: same as "PSAC 2" pulse
Short description: a standard width pulse launched by the "PSAC 2" signal
Application: starts the TDC in the 2nd spectrometer arm

"Stop T1"

Type: output
Standard: NIM, positive logic
Duration: same as "Target" pulse
Short description: a standard width pulse launched by the "Target" signal
Application: stops the TDC TOF-channel in the 1st spectrometer arm

"Stop T2"

Type: output
Standard: NIM, positive logic
Duration: same as "Target" pulse
Short description: a standard width pulse launched by the "Target" signal
Application: stops the TDC TOF-channel in the 2nd spectrometer arm

"Gate QDC"

Type: output
Standard: NIM, positive logic
Duration: (0 - 102.35)μs
Short description: a programmable width pulse launched by the first triggered PSAC signal
Application: starts and stops the charge-to-digital convertor (QDC)

"External gate"

Type: output
Standard: NIM, positive logic
Duration: $\tilde{1}$00ns
Short description: a standard width pulse launched by the first triggered PSAC signal and retarded by an external delay line
Application: starts the timing gate in the detector coincidence scheme

"Common clear"

Type: output
Standard: NIM, positive logic
Duration: 1μs
Short description: a standard width pulse generated by the selector module itself after an event rejection or by the CAMAC command NA(X)F(10) ('X' - any) after an event readout
Application: global DAQ reset signal

"Common clear"

Type: output
Standard: TTL/CMOS, complementary logic
Duration: 1μs
Short description: a standard width pulse generated by the selector module itself after an event rejection or by the CAMAC command NA(X)F(10) ('X' - any) after an event readout
Application: global DAQ reset signal

"Ion / Neutron gate"

Type: output
Standard: TTL/CMOS, positive logic
Duration: (0 - 6.35)μs / (0 - 102.35)μs
Short description: a programmable width pulse launched by the first triggered PSAC signal
Application: monitor for DAQ timing adjustments using an oscilliscope

"Neutron counter"

Type: input
Standard: TTL/CMOS, positive logic
Duration: 10ns minimum
Short description: discriminated pulses from the neutron detectors
Application: neutron flux or fluence measurements

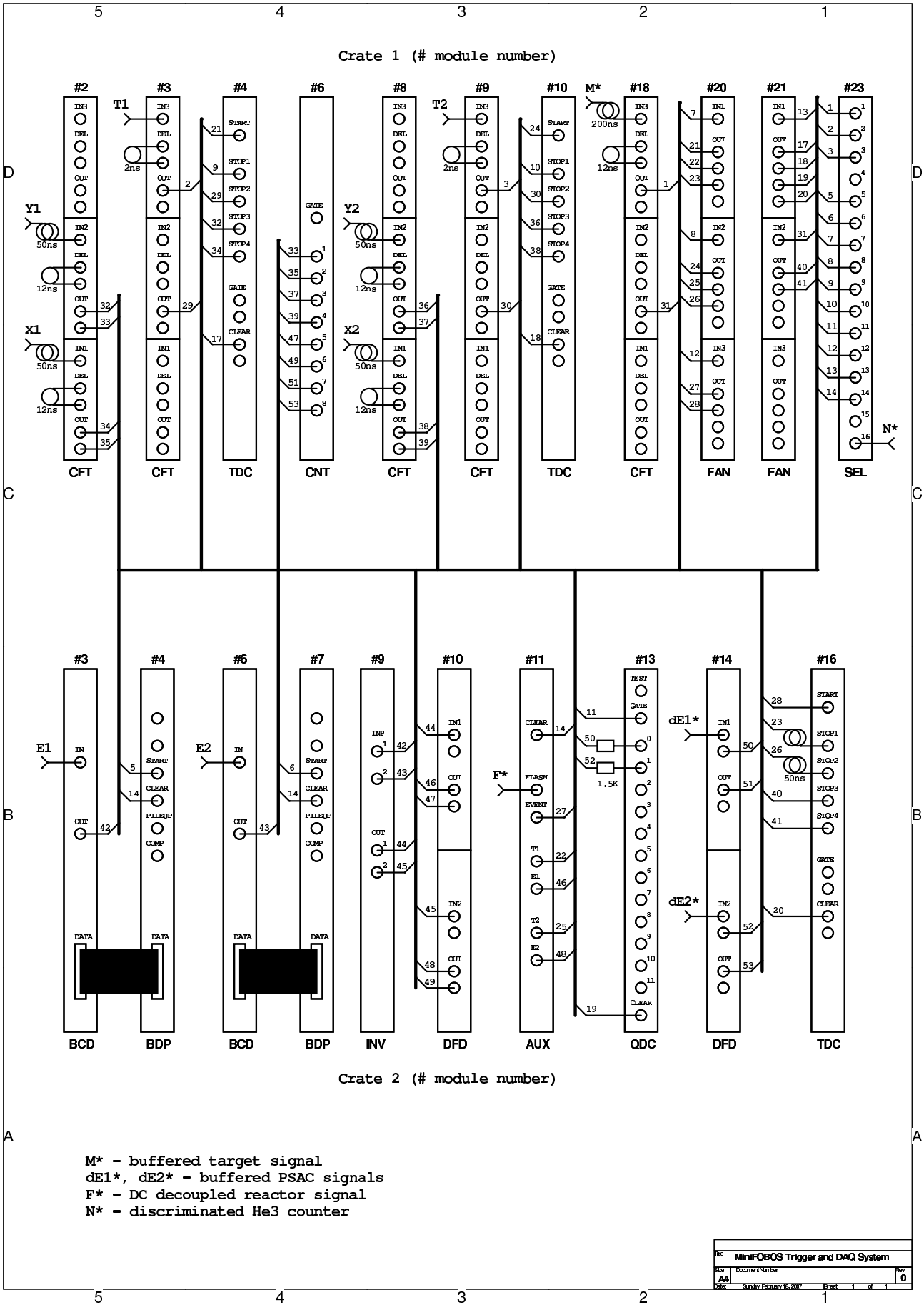

Figure 1: Mini-FOBOS data acquisition system (DAQ).

3 CAMAC dataway commands

Setting up the selector module for its operation as a DAQ trigger is performed by the **control commands** of the CAMAC interface. Some steering parameters are kept in the group # 2 registers, table 3, whose values are getting modified using the **register access commands**. Those commands are also used to read out the group # 1 registers, table 2, containing physical data aqcuired by the selector itself.

3.1 Common control commands

Common control signals operate on all modules connected to them without the need to be addressed separately by a command.

Initialize (Z) and **Clear** (C) - are the "system reset" commands to clear the group #1 registers, set up the group #2 registers to their default values (table 4), enable target, both detector arms, neutron gate and LAM signals, remove LAM from the CAMAC bus and close all timing gates

Inhibit (I) command disables any selector activity (executing of CAMAC commands, responding to input signals etc.). It has to be removed from the dataway before selector operation as most of CAMAC controllers keep it active after the power-on.

3.2 Addressed control commands

Addressed control signals require a CAMAC station number (N) to be selected and one of the valid addresses and control functions that are summarized in table 1.

Table 1: Control registers

Command	Module response	Description
NA(0)F(24)	Q=0, X=1	disable the LAM interrupt
NA(1)F(24)	Q=0, X=1	disable the 1st detector arm
NA(2)F(24)	Q=0, X=1	disable the 2nd detector arm
NA(3)F(24)	Q=0, X=1	disable the target detector
NA(4)F(24)	Q=0, X=1	disable the neutron gate
NA(0)F(26)	Q=0, X=1	enable the LAM interrupt
NA(1)F(26)	Q=0, X=1	enable the 1st detector arm
NA(2)F(26)	Q=0, X=1	enable the 2nd detector arm
NA(3)F(26)	Q=0, X=1	enable the target detector
NA(4)F(26)	Q=0, X=1	enable the neutron gate
NA(1)F(27)	Q=LAM, X=1	test the 1st detector arm
NA(2)F(27)	Q=LAM, X=1	test the 2nd detector arm
NA(3)F(27)	Q=LAM, X=1	test the target detector
NA(4)F(27)	Q=LAM, X=1	test the neutron gate

3.3 Register access commands

The tables 2 and 3 describe handling of the selector data registers:

Table 2: Read, write and clear commands for the group #1 registers

Command	**Module response**	**Description**
NA(0)F(0)	Q=0, X=1	read the KOI register
NA(0)F(2)	Q=0, X=1	read and clear the KOI register
NA(0)F(9)	Q=0, X=1	clear the KOI register
NA(0)F(16)	Q=0, X=1	write the KOI register
NA(1)F(0)	Q=0, X=1	read the PILEUP register
NA(1)F(2)	Q=0, X=1	read and clear the PILEUP register
NA(1)F(9)	Q=0, X=1	clear the PILEUP register
NA(1)F(16)	Q=0, X=1	write the PILEUP register
NA(2)F(0)	Q=0, X=1	read the event counter
NA(2)F(2)	Q=0, X=1	read and clear the event counter
NA(3)F(0)	Q=0, X=1	read the rate counter in the 1st arm
NA(3)F(2)	Q=0, X=1	read and clear the rate counter in the 1st arm
NA(4)F(0)	Q=0, X=1	read the rate counter in the 2nd arm
NA(4)F(2)	Q=0, X=1	read and clear the rate counter in the 2nd arm
NA(5)F(0)	Q=0, X=1	read the target rate counter
NA(5)F(2)	Q=0, X=1	read and clear the target rate counter
NA(6)F(0)	Q=0, X=1	read the neutron counter
NA(6)F(2)	Q=0, X=1	read and clear the neutron counter

Table 3: Read, write and preset commands for the group #2 registers

Command	**Module response**	**Description**
NA(0)F(1)	Q=0, X=1	read coincidence interval for ions
NA(0)F(11)	Q=0, X=1	set default coincidence interval for ions
NA(0)F(17)	Q=0, X=1	write coincidence interval for ions
NA(1)F(1)	Q=0, X=1	read collecting time for neutrons
NA(1)F(11)	Q=0, X=1	set default collecting time for neutrons
NA(1)F(17)	Q=0, X=1	write collecting time for neutrons
NA(2)F(1)	Q=0, X=1	read dE measurement time
NA(2)F(11)	Q=0, X=1	set default dE measurement time
NA(2)F(17)	Q=0, X=1	write dE measurement time
NA(3)F(1)	Q=0, X=1	read blocking interval
NA(3)F(11)	Q=0, X=1	set default blocking interval
NA(3)F(17)	Q=0, X=1	write blocking interval
NA(4)F(1)	Q=0, X=1	read Bragg processor delay time
NA(4)F(11)	Q=0, X=1	set default delay time for the Bragg processor
NA(4)F(17)	Q=0, X=1	write Bragg processor delay time
NA(5)F(1)	Q=0, X=1	read LAM delay time
NA(5)F(11)	Q=0, X=1	set default delay time for the LAM
NA(5)F(17)	Q=0, X=1	write LAM delay time
NA(6)F(1)	Q=0, X=1	read ion multiplicity scheme
NA(6)F(11)	Q=0, X=1	set default ion multiplicity scheme
NA(6)F(17)	Q=0, X=1	write ion multiplicity scheme
NA(7)F(1)	Q=0, X=1	read scaling factor for single ions
NA(7)F(11)	Q=0, X=1	set default scaling factor for single ions
NA(7)F(17)	Q=0, X=1	write scaling factor for single ions

Table 4: Data length and default settings of the group #2 registers

Addr.	Data mask	Signal range	Default value	Description
A(0)	0x7F	(0 - 6.35)μs	0x0B	Ion collecting time
A(1)	7xFF	(0 - 102.35)μs	7xD0	Neutron collecting time
A(2)	7xFF	(0 - 102.35)μs	0xC8	dE integrating time
A(3)	0x7F	(0 - 6.35)μs	0x64	TOF blocking time
A(4)	0x7F	(0 - 6.35)μs	0x28	BDP start delay
A(5)	7xFF	(0 - 102.35)μs	1x90	LAM delay time
A(6)	0x03	0, 1, 2, (1+2)	0x03	Multiplicity of ions
A(7)	0x7F	0 - 127	0x64	Scaling for single ions

4 Principle of operation

The automatic "power-on" device initialization acts similarly to the CAMAC "system reset" commands, after which the selector is ready for operation. The trigger logics is driven by the "PSAC 1" and "PSAC 2" signals. The successful event requires both signals to be present within a certain interval of time - the so-called "KOI gate". This gate is set by the fastest particle stemming from the nuclear reaction and detected in either detector arm. The leading edge of the particle signal starts the gate which is closed by the leading edge of the same pulse delayed.

The delay and hence the gate width is controlled through register NA(0)F(17) (table 3). When this register contains a zero value, the delay is defined by any external delay line inserted between LEMO connectors 4 and 12. The minimum delay amounts to 20ns in this case due to transient processes. The maximum delay is not specified, but it must no exceed the blocking interval described below. For the register settings between 0x1 and 0xA the delay is provided by the built-in tapped delay line which has 10 taps of 20ns each. The gate width could therefore be chosen between 20ns to 200ns in 10 steps of 20ns. A programmable timer is being used for a signal delay when the data ranges from 0xB to 0x7F representing a number clock periods of the synchronization frequency to be counted down. For the 20 MHz quartz oscillator the gate width jitter (the quantization error) remains below 10%.

To produce a coincidence the signal from the opposite detector arm must enter selector before the latter will close the KOI gate. The trailing edges of gated "PSAC 1" and "PSAC 2" signals will set respectively bits 1 and 2 of the KOI register NA(0)F(0) to '1' (tables 2 and 6). The number of ones in the KOI register accounts therefore for the ion multiplicity in the given event. It could be equal to one or two denoting the ion coincidence in time in the second case. Events with a multiplicity of one could be accepted if this is allowed by settings of register NA(6)F(17) (table 3):

- 0x0 - do not accept events at all
- 0x1 - accept events with only one "PSAC 1" or "PSAC 2" signal
- 0x2 - accept events with only two "PSAC 1" and "PSAC 2" signals
- 0x3 - accept all events

The trailing edge of the "Target" signal will set up the bit 3 of the KOI register (tables 2 and 6), but the coincidence logics does not rely on it. The LAM interrupt to be generated after closing the KOI gate if the ion multiplicity matches the programmed scheme. The data acquisition program must validate the LAM by the CAMAC command NA(X)F(8) before reading out the digitizers (table 5). To let all of them finish

their work the LAM could be delayed through the register NA(5)F(17) (table 3). This register stores the number of 50ns (20 MHz) counted down clock periods. The KOI bits 1 and 2 could mask the readout branches to minimize the system deadtime (skipping the readout of empty channels). Afterwards the reset CAMAC command NA(X)F(10) must be realized (table 5). ***A special system bit 4 has been introduced (table 6) which is not cleared by the CAMAC command NA(X)F(10).*** This bit could mask the readout of parameters which are common to both detector arms, for example time between "PSAC 1" and "PSAC 2" pulses, or independent of those arms like the system watch.

Table 5: LAM register

Command	**Module response**	**Description**
NA(X)F(8)	Q=LAM, X=1	test LAM ('X' - any)
NA(X)F(10)	Q=LAM, X=1	test and clear LAM ('X' - any) and clear the KOI and PILEUP registers except for the KOI bit 4, reset all active timers

In experiments with abundant single-ion events: triggering on alpha particles, assymetric arrangment of the spectrometer arms, their trigger rate could be downscaled to enhance statistics for multiple hits. Downscaling means reading out a fraction of events which satisfy the trigger conditions. This fraction (the scaling ratio) is kept in register NA(7)F(17) (table 3). Its zero value means no scaling at all, the value of one means selecting every second event, the value of two - every third and so on. Events containing signals in both detector arms are never downscaled (!)

Figure 2 shows a sequence of signals and their relations for the successful event. For rejected events the processor will generate promptly the "Common Clear" signal onto LEMO connectors 13 and 14. It will also clear the KOI and PILEUP registers except for the KOI bit 4. All running timers will be reset.

5 DAQ supervision

The selector module provides control signals for all measurement units of the Mini-FOBOS DAQ:

The **"Start TDC 1"** and **"Start TDC 2"** strokes synchronous to the leading edges of the "PSAC 1" and "PSAC 2" pulses initiate the TOF measurements in the corresponding detector arms.

The **"Stop T1"** and **"Stop T2"** strokes synchronous to the leading edge of the "Target" signal finish the TOF measurements in both detector arms.

The **"Start BDP 1"** and **"Start BDP 2"** strokes synchronous to the leading edges of the "PSAC 1" and "PSAC 2" pulses initiate the Bragg signal processing (BDP) in the corresponding detector arms. The signals from the Bragg ionization chambers (BIC) have a delay with respect to the PSAC pulses depending on the BIC gas pressure and on the high voltage applied. The BDP modules themselves monitor this delay (the so-called "drift time") and use it to validate their energy and charge measurements. The "Start BDP 1" and "Start BDP 2" controls must therefore be delayed by a number of 50ns clock periods given in register NA(4)F(17) (table 3).

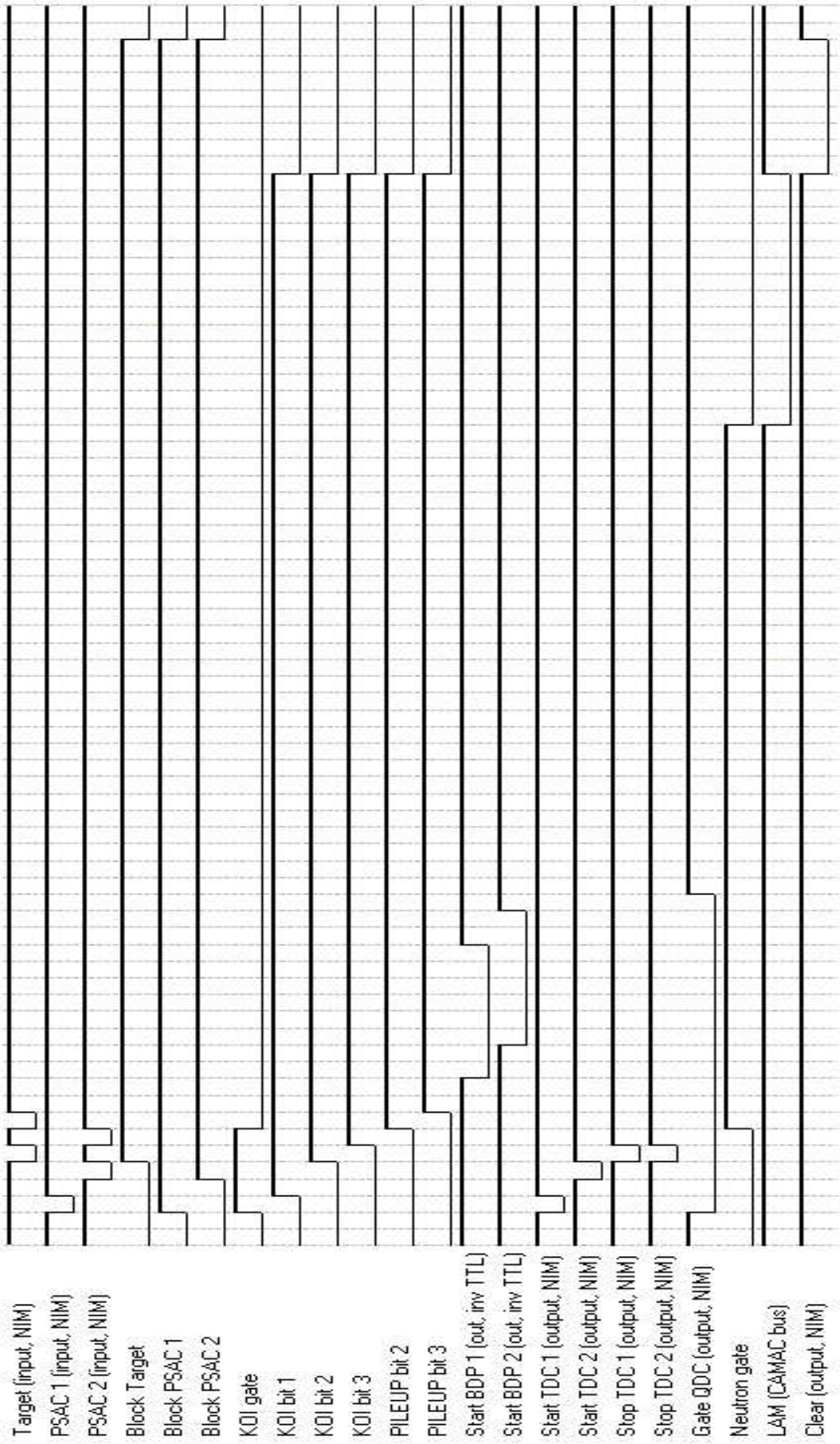

Figure 2: Selector timing diagram, the time axis is not to scale.

The **"Gate QDC"** signal starts by the leading edge of the earliest pulse "PSAC 1" or "PSAC 2" to measure the particle energy losses in a thin gaseous gap. As the analog signal is very long with respect to the time difference between the "PSAC 1" and "PSAC 2" pulses, this gate could therefore be common for both detector arms. The gate width is adjusted to the analog signal length through register NA(2)F(17) (table 3) whose value is equal to the number of 50ns clock periods.

To avoid retriggering of the KOI gate and to protect the TDC, BDP and QDC modules against multiple actuatings the inputs "PSAC 1", "PSAC 2" and "Target" are getting blocked out for the Bragg signal width + drift time. Each signal launches a count-down timer and the input stays disabled until the relevant timer will finish work. The time interval is stored in register NA(3)F(17) (tables 3) as a number of 50ns clock periods. The bits 1, 2 and 3 of the PILEUP register NA(1)F(0) to be set to '1' when two and more "PSAC 1", "PSAC 2" and "Target" pulses will be detected in the corresponding channel during this blocking time (see tables 2 and 7). The PILEUP register stamps events with overlapping signals from particles originating from different nuclear decays. It is therefore importent to have always the blocking interval longer than the KOI gate width (!) When the KOI gate closes with a positive event decision, the selector inputs "PSAC 1", "PSAC 2" and "Target" remain arrested until the "Common clear" signal will release. The prolonged inhibit does not affect logics of the PILEUP register, i.e. setting it up is not possible beyond the primary blocking interval. For test purposes the KOI and PILEUP registers could be overwritten by the CAMAC commands NA(0)F(16) and NA(1)F(16).

Table 6: Bit assignment of the KOI register

Bit 0	signal in the 1st detector arm
Bit 1	signal in the 2nd detector arm
Bit 2	signal in the fission target
Bit 3	system bit (not cleared by the fast reset)

Table 7: Bit assignment of the PILEUP register

Bit 0	1st detector arm
Bit 1	2nd detector arm
Bit 2	fission target

Table 8: Bit assignment of the rate counters

Bit 14 ... Bit 0	counter's value (0 to 32767)
Bit 15	overflow condition

The "Target" signal shows usually a much higher rate as compared to the frequency of launches of the KOI gate. This is because the fission target detector has a larger aperture than the angular acceptance of the PSACs. To avoid the bit 3 of the PILEUP register to be set from the earlier nuclear fission which was not registered in any detector arm, this bit is reset at the end of each "Target" blocking interval. The KOI gate cancelles the next reset command thus relating the bit content to the triggered event.

The front-panel LED indicates the LAM interrupt. The event rate (the LAM frequency) and the partial rates of the "PSAC 1", "PSAC 2" and "Target" signals could be measured by counters NA(2)F(2), NA(3)F(2), NA(4)F(2), NA(5)F(2) (table 2).

It helps in controlling the chamber gas content and pressure, in setting up the detector high voltages, in adjusting the discrimanator thresholds, in monitoring the beam conditions and for judging about the reasonableness of the ongoing experiment. The rate measurements require the "read and clear" CAMAC commands. The commands NA(2)F(0), NA(3)F(0), NA(4)F(0), NA(5)F(0) allow for integrating the count rates. The counter values are kept in bits 14...0 of the corresponding registers. The bit 15 of each register indicates the counter's overflow (table 8).

Neutrons emerging from the nuclear reactions are counted in register NA(6)F(2) (table 2) within a programmable interval of time. This interval (the "neutron gate") is defined through register NA(1)F(17) (table 3) whose value is equal to the number of 50ns clock periods. The neutron gate must be comparable with the moderation time constant which is in order of 30μs. The typical gate width for the neutron collection amounts to 100μs. The selector algorithm uses therefore the maximum value of two registers NA(1)F(17) and NA(5)F(17) to delay the LAM (!) The neutron counter is not reset by the "common clear" signal that allows for integrating the count rate. To prevent counter from the background accumulation the neutron gate starts only if the trigger condition is fulfilled (including a chosen fraction of single-ion events) upon closing of the KOI gate. When the neutron acquisition interval is set to zero, the detector pulses are counted continuously. The counter could be read out by the CAMAC command NA(6)F(0) for dosymetric measurements or by command NA(6)F(2) to monitor intensity of the neutron beam. The neutron gate could be monitored through LEMO connector 15 for any non-zero value of the NA(1)F(17) register, otherwise the KOI gate will be present at this pin.

6 Non-standard operation modes

For system adjustments any of the following signals could be disabled (see table 1):

Disable LAM by NA(0)F(24): the "common clear" (like after the NA(X)F(10) command) instead of the LAM interrupt will be generated by the LAM countdown delay. It is a practical option for cycling the system in a stand-alone mode (without controllers responding to interrupts).

Disable the 1st detector arm by NA(1)F(24): this is a gate for the "PSAC 1" input. It leaves the "PSAC 2" signal alone to be the system trigger.

Disable the 2nd detector arm by NA(2)F(24): this is a gate for the "PSAC 2" input. It leaves the "PSAC 1" signal alone to be the system trigger.

Disable the target detector by NA(3)F(24): this is a gate for the "Target" input.

Disable the neutron gate by NA(4)F(24): the neutron gate will not be generated and the LAM delay is exclusively defined by NA(5)F(17). In experiments with no neutron measurements it minimizes the system deadtime.

7 Device programming

Attach the "MV ByteBlaster programmer" to the rear 10-pin 2.54 mm connector, prepare in Quartus or MaxPlus II the device chain: EPC2LC20, EPC2LC20 and EP1C12Q240C6, select for those devices the following programming files: "selector.pof", "selector_1.pof", "selector.sof" and press a dedicated menu button to proceed.