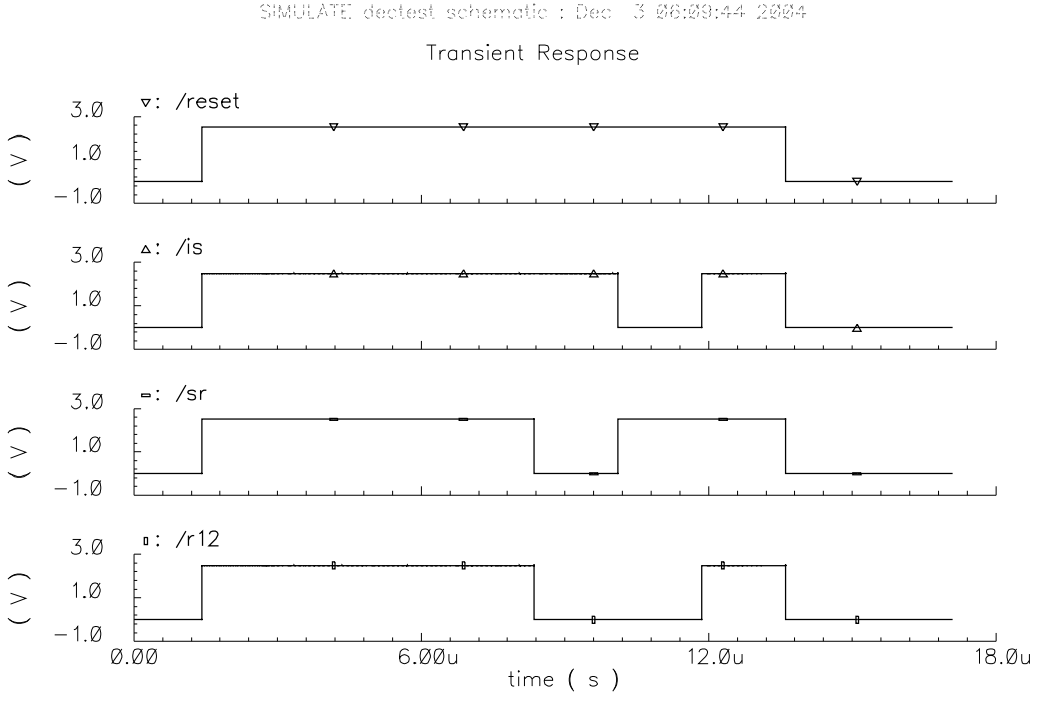
SIMULATE dectest schematic : Dec 3 08:09:44 2004
Transient Response
▽: /reset
△: /is
▫: /sr
▯: /r12
3.0
1.0
−1.0
(V)
0.00
6.00u
12.0u
18.0u
time (s)