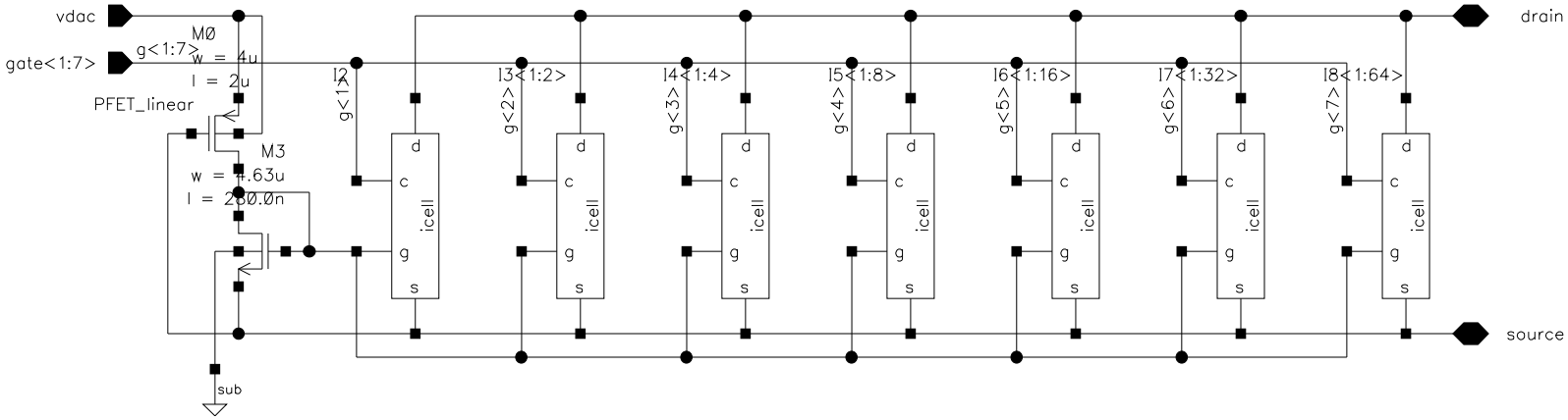
# matrix


vdac
gate<1:7>
M0
w = 4u
l = 2u
PFET_linear
M3
w = 4.63u
l = 200.0n
sub
I2
g<1>
I3<1:2>
g<2>
I4<1:4>
g<3>
I5<1:8>
g<4>
I6<1:16>
g<5>
I7<1:32>
g<6>
I8<1:64>
g<7>
d
c
g
s
icell
drain
source