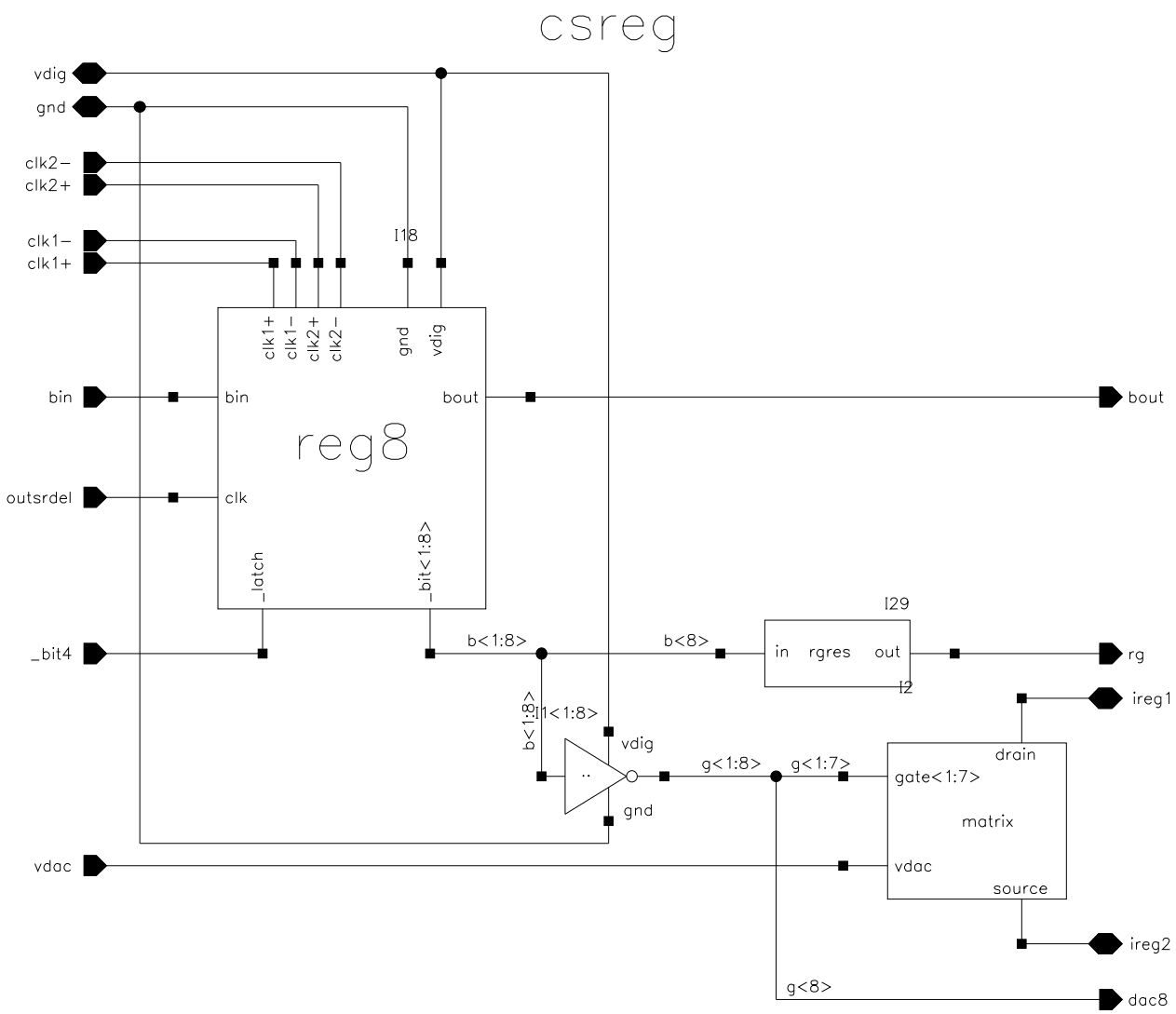
csreg
vdig
gnd
clk2−
clk2+
clk1−
clk1+
I18
clk1+
clk1−
clk2+
clk2−
gnd
vdig
bin
bin
bout
bout
reg8
outsrdel
clk
_latch
_bit<1:8>
_bit4
b<1:8>
b<8>
I29
in
rgres
out
I2
rg
ireg1
b<1:8>
I1<1:8>
vdig
gnd
g<1:8>
g<1:7>
drain
gate<1:7>
matrix
vdac
source
vdac
ireg2
g<8>
dac8