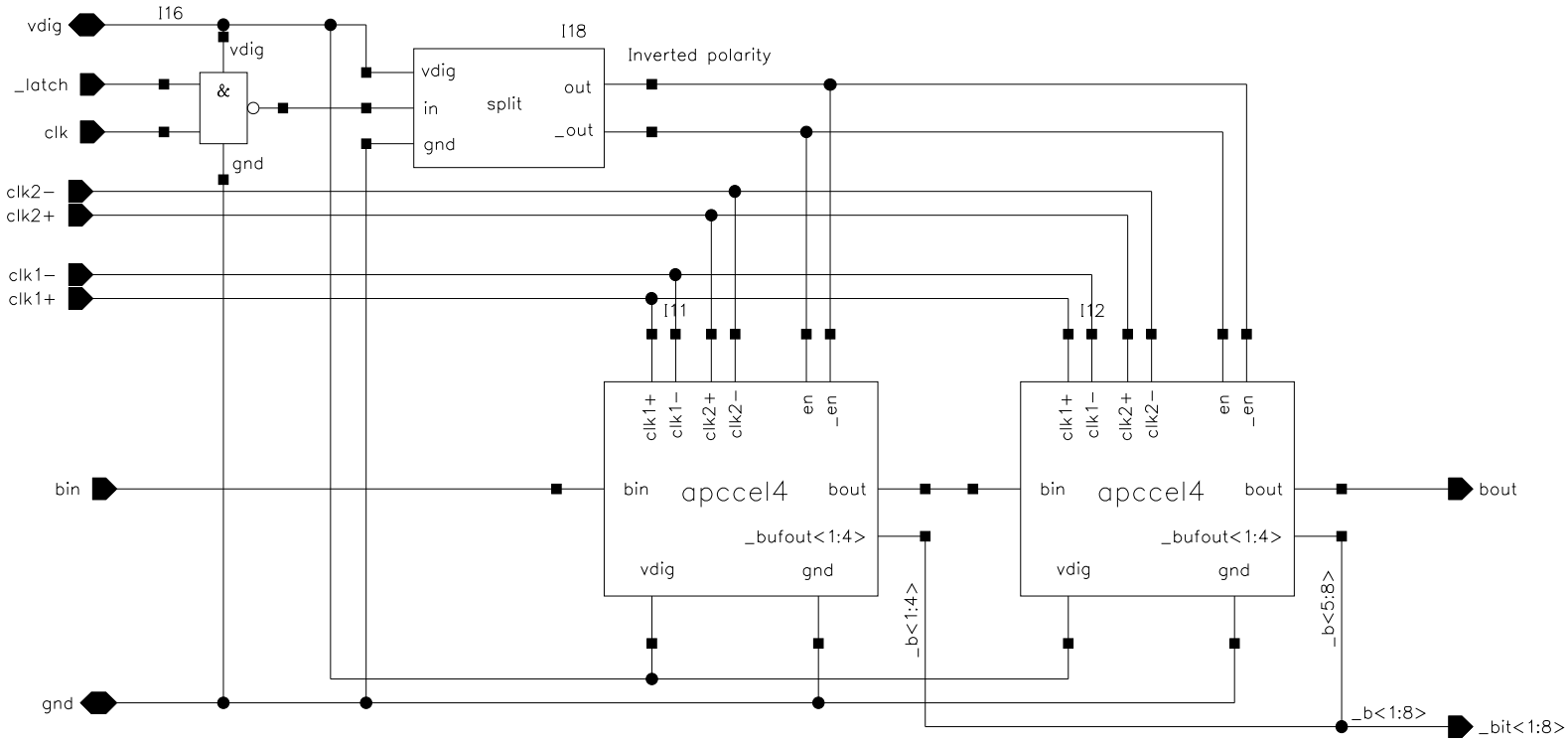
reg8


vdig
I16
vdig
_latch
&
clk
gnd
I18
vdig
in
gnd
split
out
_out
Inverted polarity
clk2−
clk2+
clk1−
clk1+
I11
I12
clk1+
clk1−
clk2+
clk2−
en
_en
bin
apccel4
bout
_bufout<1:4>
vdig
gnd
bin
apccel4
bout
_bufout<1:4>
vdig
gnd
bout
_b<1:4>
_b<5:8>
gnd
_b<1:8>
_bit<1:8>