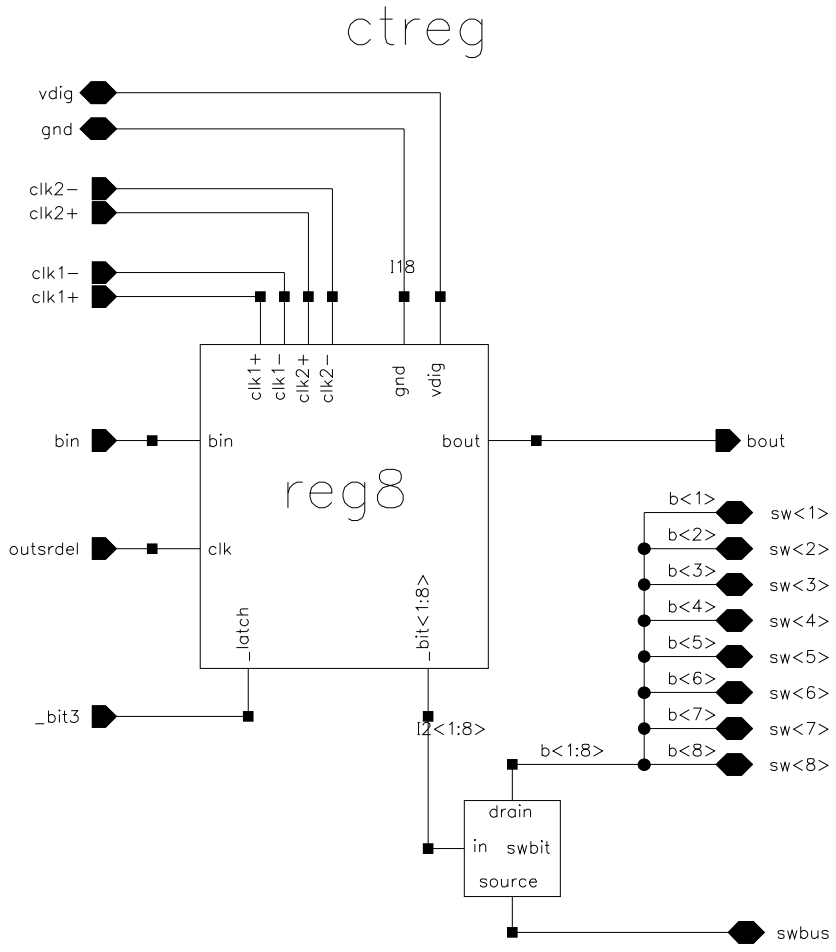
ctreg
vdig
gnd
clk2−
clk2+
clk1−
clk1+
I18
clk1+
clk1−
clk2+
clk2−
gnd
vdig
bin
bin
bout
bout
reg8
outsrdel
clk
_latch
_bit<1:8>
_bit3
I2<1:8>
b<1:8>
b<1>
b<2>
b<3>
b<4>
b<5>
b<6>
b<7>
b<8>
sw<1>
sw<2>
sw<3>
sw<4>
sw<5>
sw<6>
sw<7>
sw<8>
drain
in
swbit
source
swbus