Main

vana
vdig
le
reset
is
is2
sr
rg
r12
cs
vthres
_rbi
rbi
rphi1
rphi2
rbo
vana+_well!
vdd_well!
vss_sub!
aref
adum
aout
cal
_se
_sbi
sbi
_sphi1
sphi1
_sphi2
sphi2
null
gnd