Belgian Federal Science Policy Office

The research grant "Development of the topological trigger of the H1 experiment using the silicon pad detectors"

Final report

The aim of this project has been to take high quality data for physics by using new detector components and with an advanced configuration of the H1 trigger. The final report is given here on work performed between April 2005 and August 2006.

Research program

Detector preparation:

1. Manufacturing and tests of the silicon strip detectors BST and FST
2. Repair, test and assembly of the silicon pad detectors

Monte Carlo studies:

1. Generating masks for the silicon pads for the vertex-pointing track trigger
2. Simulation of the online background rejection with topological data constraints
3. Generating masks for the SPACAL to match its energy clusters with BST tracks (the "topological trigger")

Data taking and analysis:

1. Configuring the level-two topological trigger
2. Configuring the new SPACAL topological trigger
3. Trigger efficiency studies

1 Upgrade of the silicon strip detectors

The postdoctoral work started with functionality tests of the newly developed APC128-UMC25 readout chip for the silicon strip detectors. This chip replaces an earlier version (in SACMOS) the properties of which (the amplitude hold time) had degraded due to the high radiation background of HERA.[1] The new chip is built of special ring-shaped field-effect transistors in the deep-submicron process (the minimum pitch is 250 nm). Their gate contacts enclose the drains thus leaving no path for the leakage current through the crystal bulk. A large width-over-length ratio for those transistors requires a current limitation circuitry for each elementary cascade making the entire chip design somewhat complicated. The area of the silicon wafers (8-inches in diameter) was shared between the APC128UMC25 and the SLS11 readout chips - the latter was developed at the Paul-Scherrer Institute for the Swiss Synchrotron Light Source. The design and manufacturing of both ASICs was coordinated by the Belgian company IMEC. In total 10 wafers cointaining about 20.000 integrated circuits APC128UMC25 and the same number of decoders were produced by the UMC company (Taiwan) without any iteration and were shipped to PSI and to DESY for acceptance and quality checks.

[1] This is estimate between 100 krad and 1 Mrad per year depending on the running conditions.

1.1 Chip evaluation setup in Zeuthen

A serial test of the new ASICs and their evaluation has been done with a semi-automatic setup assembled at DESY Zeuthen. This was based on the "Wentworth Laboratories" vacuum holder for up to 12 chips in a row. A custom-made probe card provided an electrical contact to one of the chips through an array of needles carrying in the supply voltages, routing the control signals and conducting the amplified detector pulses to an external Analog-to-Digital converter. The amplitude analysis of those pulses helped to select chips with the uniform structure and the best signal-to-noise ratio. The positive outcome was 50%. Devices from the crystal boundary region were mostly rejected. These results were reported to IMEC for technology improvements.

1.2 Hybrid test setup in Hamburg

A test setup for the fabricated detector modules was built at DESY Hamburg. The assembled modules were checked twice: after the ASIC mounting (it was yet harmless for the silicon sensor at this step to replace the detector components) and after the detector completion. All readout channels were calibrated to high precision with internally-generated calibration pulses equivalent to the particle signals. The new detectors showed a 3 times better signal-to-noise ratio as compared to the old chip under the same measurement conditions. A few failures per module, caused by mechanical impacts on dice or due to ageing effects in recycled silicon sensors were found for some detectors. A map of those channels was prepared.

1.3 Detector calibration with the $^{90}_{38}$Sr source

The local data acquisition system for the silicon detectors of H1 (Si-DAQ) was upgraded during the HERA shutdown in December 2005. The detector data were poor during the first luminosity runs. This could be due to the yet unknown feature of the readout chip or due to coherent data losses of the Si-DAQ itself. Although the detector modules and their readout chips were tested several times with a laser flash, this method with a large energy deposit was not good enough to understand the chip functionality at smaller but real amplitudes. The detector response to the minimum ionizing particles was checked therefore with a radioactive source $^{90}_{38}$Sr ($\sim$500 keV electrons). One spare detector module was implemented into Si-DAQ running in the "raw data mode" to read out the amplitudes from all silicon strips (usually this mode is not used because of the limited bandwidth of the Si-DAQ). The particle amplitudes $\sim$50 mV in this measurement were consistent with the chip simulation results. Thus the efforts were focused on the Si-DAQ improvement and the experts modified the online data processing code. It was also found that the analog-to-digital converters (ADC) had a wrong synchronization with detector signals as the current ADC settings were different from the vendor specification. The latter has been verified in a series of measurements with a variable delay of the conversion strobe to scan the signal shape and to choose an optimal ADC aperture.

2 Upgrade of the silicon pad detectors

2.1 Exchange of the PRO/A pad readout chip

The pad detectors were irradiated to a high dose (up to 3.5 Mrad) in a short period between 2002 and 2003. A 10-fold increase of the leakage current was measured for the silicon sensors, from tens to hundreds of nanoamperes. This doesn't affect the functionality of the readout chips because they have an AC-coupling to the silicon pads (the latter have embedded coupling capacitors). The chip can also tolerate these currents at the inputs when the pad capacitors break through.

Damages to the chips themselves, shifted trigger thresholds and wrong response to the loaded sequencer code, have been observed from a series of tests with the $^{90}_{38}$Sr source and with calibration pulses. The irradiated ASICs (even those which passed the functionality check) were thus exchanged in 2005 to improve the detectors reliability.

2.2 Hybrid calibration

A calibration setup was assembled at DESY Hamburg to measure the signal gain of the newly assembled pad readout chips. Produced in 1999 by Austria Micro-Systeme, these ASICs were kept within 6 years in the clean room in special boxes with a nitrogen flow. Nevertheless oxydation of their wafer's backplane occured thus making impossible a uniform biasing of the chip substrate. Although each transistor in this chip has a local biasing of its substrate region, the signal gain of the entire analog circuitry degrades in this regime.

The gain was estimated from the chip response to electrical calibration pulses whose amplitudes were equivalent to the particle's energy losses in the silicon detectors. The readout chip amplifies and discriminates these signals which are counted for different threshold settings. The curve obtained from the threshold scan has a plateau whose width is a measure of an average signal amplitude. For the 200 mV threshold range, the scan interval of 5 mV and with about 20 seconds relaxation time for the chip between measurements (the ASIC settings had to be changed), a few weeks were needed to calibrate 48 detectors with 32 trigger channels each.

2.3 Front-end redesign

The front-end electronics of the pad detectors has been modified to withstand the high radiation load inside H1. The destroyed by radiation digital-to-analog converters for generating trigger thresholds have been removed from the boards and their function was transferred to a digital algorithm for a complex programmable logic device (CPLD) ALTERA ACEX EP1K30 found to be tolerant to the radiation background at HERA. The ALTERA program generates pulses with an adjustable duty cycle which are converted to certain DC-level by an external low-pass RC-circuitry.

The ALTERA routine was developed for the power-on sequence for the analog and digital circuitries of the pad readout chip to prevent them from the latch-up effects that could be enhanced by radiation. The latch-up happens mostly during the device powering and results in a breakthrough current in the substrates of the field-effect transistors. The pad readout chip has a possibility to bias inversely its substrate before switching on the main power. The ALTERA program drives first the analog supply voltages for the chip biasing. Turning on the digital supply voltages is delayed by one

second. The ALTERA code uses signals from external voltage comparators to alarm at 10% undervoltages and overvoltages which may potentially trigger latch-ups. The power-on sequence includes also ramping down the trigger thresholds and initalization of the PRO/A chip: loading the bitstream for the gain selection, turning on and off cascades for the common mode noise suppression and compensation for the detector leakage current, enabling or disabling the trigger channels. The buffers which convert signals from the pad readout chip into CMOS pulses for the ALTERA are disabled during the power-on procedure to prevent the entire circuitry from a self-oscillation at the maximum frequency that may result in a system deadlock.

The former ALTERA-based slow control and the online data processors were included into controller-area network (CAN) by help of a serial linked input/output chips (SLIO) PHILIPS PCA82C250 which turned to be weak against radiation. The serial CAN chain was disturbed by any malfunctional SLIO chip. All front-end boards in the upgraded system were made independent of each other, the ALTERA codes were extended to support a specially developed protocol for the data transfer. The data packages for the new protocol became much shorter thus speeding up the system performance. When radiation damages to the ALTERA chip itself occured, its floorplan and the pin layout were rearranged to activate the new chip resources. Some new design rules have been established for electronics working in the radiation environment:

- Switching circuitry is preferable over the static one.
- Interfacing of several devices must be in parallel, any serial connections or the line sharing are impractical.
- The program size for the front-end must not exceed 50% of the the FPGA capacity to have enough spare gates.
- Important input and output FPGA signals must be routed to several I/O pins. These could be connected in parallel and configured to drive a high-ohmic state when unused.

The new radiation-hard readout for the Forward and Backward Silicon Trackers of H1 was presented at the 10th European Symposium on Semiconductor Detectors in Wildbad Kreuth (near München) in Germany in June 2005. The travel expenses and the conference fee were covered by DESY.

2.4 Extension of the VME interface

The ALTERA-based trigger algorithm distributed between the front-end and the VME interface has been extended to acquire and keep information about all triggered pads to make these data available for the readout upon demand of the H1 event builder. The "raw" data are essential to develop and to verify the trigger strategies which exploit timing (for the level-1 trigger) and spatial (for the level-2 trigger) correlations between different subdetectors of H1. Before being matched the signals from calorimeters, trackers and muon detectors pass the amplitude, timing and geometrical (pattern recognition) filtering, afterwards they contribute with some weights to the event trigger. The cut parameters, the weights and the trigger thresholds for the best efficiency must be found from the randomly collected raw data (unbiased by the trigger itself).

For the hardware monitoring and for data consistency checks the polar angles Θ and ϕ of any triggered track are being readout by the standard H1 data storage

system "PQZP" whose faulty synchronization circuitry leads to coherent data losses. The "PQZP" readout has been exchanged by the ALTERA subroutine which appends the topological data to the raw data stream.

The new VME module has been developed (schematic design, printed circuit board layout and programming of ALTERA) to interface six front-end boards with computer for the detectors control.

3 Detector assembly and installation

The Backward Silicon Tracker (BST) was rebuilt in Zeuthen in 2005 in collaboration with DESY colleagues. 144 silicon strip and 48 pad detectors have been selected after tests and calibration and mounted onto tracker's mechanical support structure, attached to the water cooling system and connected to the front-end readout electronics. The detectors were tested continuously during tracker assembling. Comprehensive tests were held before and after the BST installation in H1 in December 2005. These activities required often traveling from Hamburg to Zeuthen, the travel expances were covered by DESY.

3.1 Tests of the new BST readout

Based on the TCP/IP client-server system, the new "Si-DAQ" provides a parallel readout of all storage devices containing data from silicon strip and pad detectors. The system commissioning showed 3.5 ms response time for the pad readout alone although the estimate for it was 200 μs. In addition one data bank had an irregular structure. The joint tests of the upgraded VME interface and of the "Si-DAQ" code helped to reveal wrong assignment of the VME address variable in the acquisition software which was fixed by the "Si-DAQ" experts.

3.2 The new slow control program

The new program has been developed in the "LabView" package to operate the silicon pad detectors by the H1 shift crew during HERA luminosity runs. The main role of this program is to turn on and off depletion voltages for the silicon sensors and supply voltages for the front-end electronics. Further tasks are to steer the front-end electronics and the VME readout: to overwrite the power-on settings of ASICs and ALTERAs to enable or disable the trigger channels, to set up trigger thresholds, to delay trigger signals by a number of clock periods of the HERA synchronization frequency, to select in the pipeline the raw and the topological data to be readout for a certain HERA bunch crossing, to check the power watchdogs and the PRO/A initialization status, to downscale the count rate of the radiation monitor, to generate visual and sound alarms for different operating conditions: detected hardware failures, high radiation dose rate etc. The program was optimized for the old type Macintosh "Quadra 700" with a limited available processor memory. The program's manual has been prepared for the H1 shift crew.

3.3 Power supply redesign

The supply unit to generate depletion voltages for the silicon sensors was redesigned to reduce the noise-induced pad triggering. The pickup noise originated in the ground

loops between supply and signal cables to the front-end. The new board has six galvanically isolated HV channels and makes the front-end supply truly floating. The entire trigger system has now a single junction for grounds of the signal cables.

4 Simulation of the pad trigger system

4.1 Generating the trigger masks

The first set of trigger masks (track patterns) has been computed with a random generator imitating charged particles in the solenoidal magnetic field of H1 ($|\vec{B}| = 1.15$ T) scattered into the silicon pad detectors. The polar scattering angle Θ was weighted by the differential cross-section as a function of Θ known from the earlier measurements. The particle energy in this naive approach was constant or had a uniform distribution in the range from 0.5 to 27 GeV. Every track pattern required triggered pads in all 4 detector layers. To compensate for inefficiency of every silicon sensor, the mask permutations containing signals in any 3 out of 4 layers were allowed increasing also the angular acceptance for the trigger. This resulted in 92% overall trigger efficiency as measured during the HERA luminosity. For the efficiency fine tuning the masks were recalculated using the "DJANGO" simulation package which generated the electron energies and scattering angles accordingly to their probabilities in deep-inelastic scattering. An efficiency of 95% was then achieved. Simulation of the pad detector for Monte Carlo studies has been implemented into the standard H1 software.

4.2 Beam halo trigger for the FST alignment

An additional trigger signal from the pad detectors has been provided on request of the "ELAN" (electron analysis) physics group to align the Forward and Backward Silicon Trackers (FST and BST) with respect to each other (to find exact positions and orientation of all their silicon sensors). The BST could be aligned in H1 by the help of the Central Jet Chamber (CJC) and of the backward calorimeter SPACAL thus making possible the FST alignment too. A set of trigger masks to select tracks parallel to the beampipe and crossing the FST and BST was prepared. Introduction of the new trigger bit required changes in the conventional data format and reprogramming of the front-end and of the VME interface.

5 The new FTI0 detector for H1

A new detector based on organic scintillation counters and on silicon photomultipliers was installed near the beampipe during the shutdown in December 2005. The tasks of this device are to monitor the radiation background of HERA in H1 and to trigger on the particle tracks in the FST acceptance.

5.1 The FST trigger based on FTI0

A Forward Silicon Tracker is situated in H1 between the scintillation plate called FTI2 and the newly installed FTI0. The timing and spatial correlation of the FTI0 and FTI2 signals provide therefore the level-one track trigger for the FST. The new trigger system

has been developed using spare electronic modules for the silicon pad detectors. The FTI0 and FTI2 raw data readout through the VME interface has been established and the new trigger databank has been introduced for the offline analysis. Steering of the FTI0 system (gating of the FTI0 trigger channels, signal delays to match the unique decision time of H1, phase adjustment for the synchronization frequency, pedestal rate subtraction for the radiation monitor etc.) was added to the pad slow control program.

5.2 The new radiation monitor

The silicon photomultipliers collect light emitted by scintillators and convert it into electrical pulses. Usage of these devices in H1 became their first test under real luminosity conditions. Their volt-amper characteristics has been measured regularly to monitor their breakdown voltage drift for increasing total ionization dose.

The algorithm to measure precisely the dose rate and the integrated dose by the silicon pad detectors has been extended silicon photomultipliers: the subroutine running on the ALTERA chip modulates the carrier frequency by the number of triggered diodes for each HERA bunch crossing. The resulting frequency is sent to the central trigger of H1 where it is being measured and could be recalculated into dosimetric units.

5.3 Beam dump watchdog

The radiation monitor based on the BST silicon pad detector measures the background of HERA at about -40 cm from the nominal interaction point along the beam axis and the FTI0 radiation monitor measures it at +40 cm respectively. Either detector forces an automatic dump of the leptonic beam which the main background component is attributed to. Their reliability has therefore been a major issue to avoid false dumps.

6 Development of trigger strategies for the L2TT

6.1 System maintenance

Besides development of the new programs for the H1 topological level-2 trigger (L2TT), its ageing hardware components were inspected and fixed: the data from subdetectors stored in the corresponding databanks have been compared to data received and kept by the L2TT itself. Inconsistencies in these datasets have been found and eliminated by exchanging the 12-years old data cables between subdetectors and the L2TT. The trigger hardware initialization script written in TCL has been adapted to the new Linux version after the computer platform upgrade.

6.2 Topological cuts with L2TT

Every physics group of H1 uses a set of triggers for selecting events with favoured kinematical properties. These triggers are input to the central data acquisition system (CDAQ) whose bandwidth is limited by 50 Hz. The maximum number of H1 triggers is 128, their rates range between centihertz to a few dekahertz and most of triggers have no rate overlap. The research policy of H1 prescribes a limited frequency for each trigger because altogether they must fit into CDAQ performance, otherwise a rate downscaling is to be used for too frequent triggers.

The scaling factors are considered monthly during the H1 collaboration meeting. The "ELAN" trigger "S9" selects events with minimum possible energy of the scattered lepton. It thus obtained a high scaling factor to keep the "S9" rate within budget. Physics background (light particles and γ-quanta stemming from ep-interactions) had a large contribution to the "S9" rate, scaling down of which leads however to significant loss in the useful data. The statistics should be enhanced by rejecting the neutral background component by the pad detector which triggers on the charged particle tracks.

During the BST repair the background suppression was achieved by exploiting an angular distribution of interaction products: events whose electromagnetic energy clusters were found in the inner part of the SPACAL were attributed to background and were refused. Scattered leptons which may occur in this region, were not interesting for the analysis because the particle tracks could not be measured without BST.

Taking into account the calorimeter's radial symmetry with respect to the beam-line, the L2TT was configured to select events with no SPACAL clusters inside a circle of 40 cm radius. The trigger response to Monte Carlo data from subdetectors was simulated and verified. The new event topology did not change distributions of kinematical variables as seen from the pilot ep-runs. In August 2005 this temporary trigger strategy was activated for the data taking. Another "ELAN" triggers relied on leptonic energy clusters in SPACAL apart from its central region with 20 and 30 cm radii.

6.3 The topological track trigger

Studies of the neutral current deeply inelastic scattering (DIS) require data samples with measured probing particles - electrons or positrons, the online identification of which relies on the backward calorimeter SPACAL and on the silicon pads: the pad detectors register charded particles originating from the interaction region and the SPACAL discriminates muons, mesons and hadrons against electrons and positrons according to their energy deposits, because the latter show much higher radiative energy losses. The level-1 trigger "S7" chooses events for which the SPACAL and the tracker signals belong to the same interaction bunch crossing. A big fraction of those events contains random coincidences of hadronic tracks with conversion gamma rays in SPACAL. These are two background components independent of each other, whose powerful rejection and extraction of a true electron signal becomes possible with a level-2 trigger by utilizing an event topology.

Realization of such topological filter was a major task of this research grant. Originally the L2TT system was considered for the project. The level-2 trigger acquires fine-granularity data from all subdetetectors of H1 and searches for their predefined combinations to keep an event. The strategy how to separate physics from background has been developed from the offline analysis of the ep-data and the trigger patterns were obtained from the Monte Carlo simulation of the DIS events.

Linking of the BST track with the most energetic cluster in SPACAL has been investigated for the trigger algorithm. Most of DIS events have a small difference in the cluster position as measured by the silicon strip detectors and by the SPACAL: $|R_{BST} - R_{SPACAL}| \leq 3.5cm, \quad |\Phi_{BST} - \Phi_{SPACAL}| \leq 15^\circ$ (conventially the polar coordinates are being used). On the other hand the background shows simultaneously large ΔR and $\Delta\Phi$. Thus the requirement for the SPACAL cluster to stay within $\pi/8$ angular acceptance of one Φ-sector of the BST removes a substantial background component

The front-end of the silicon pad detectors was reconfigured to send to the L2TT

the scattering angles Θ and Φ of the triggered track. The SPACAL data available for the L2TT contains triggered cells. All possible combinations of these cells for each triggered BST sector have been found with Monte Carlo calculations taking into account the path deflection of the charged particles in the solenoidal magnetic field in H1. The logical scheme to match the BST sector number with triggered SPACAL cells has been prepared for the L2TT and checked with ep-data, but the algorithm could not be implemented because of firmly programmed L2TT data receivers which combine together several bits thus making the SPACAL granularity very coarse.

The trigger strategy for "S7" was therefore translated into codes for the newly developed SPACAL topological trigger (STT). Based on CPLDs and containing freely reprogrammable VME interface, the STT system allows for matching the SPACAL and the BST topological data already for the level-1 trigger! It reduces the background triggering of "S7" by factor 3.5. An additional improvement to the trigger response for the SPACAL energies between 6 to 20 GeV could be achieved by selecting events with not more than 6 clusters in total. A monitor trigger has been introduced for the "S7" by help of the STT selecting all SPACAL clusters in the BST angular acceptance without tracking information from pads.

7 Work at the Joint Institute for Nuclear Research

Retaining the post at the home institute for the whole period of work at the University of Antwerpen was required by this research grant. That was ensured by the JINR director Prof. A. N. Sissakian. Extension of the JINR contract assumed taking part in preparing and conducting experiments at the Flerov Laboratory of Nuclear Reactions (FLNR) to study the modes of spontaneuos nuclear decay and of induced nuclear fission. On the visit to Dubna during vacations, the new electronic boards in the CAMAC modular standard have been designed and a new data acquisition system for the "Mini-FOBOS" spectrometer has been assembled.

7.1 System trigger

This is a CAMAC station based on a complex programmable logical device. The CPLD algorithm written in VHDL programming language makes a decision to accept a physical event depending on multiplicity and timing relations between nuclear reaction products which are detected by gaseous avalanche chambers.

The module provides the "start" and the "stop" strobes for time-to-digital converters to measure velocity of emerging ions, generates gating signals for analog-to digital converters to measure the particle charges and kinematic energies. It launches the computer-based readout system and issues a common to all measurement devices clear pulse after the event readout or event rejection.

Its internal logics measures the count rate of detector pulses that helps to adjust the detector's supply voltages and the discriminator thresholds. The pile up events are being registered when more than one particle occurs in any detector in a given interval of time. Some auxiliary functions such as general purpose input-output register, watch and event counter have been implemented.

7.2 Multichannel time-to-digital converter

Based on the ALTERA chip, this CAMAC module uses the new principle of measuring time. Commercial devices perform an expansion of the measured time interval T $\rightarrow$ T' by analog circuitry and the clock pulses are counted during the new interval T'. In this scheme the measurement range is limited by analog components, the resolution is usually of the order of 0.5%.

The purely digital algorithm of the new module relies on a number of synchronous counters whose clock frequencies have the same period but a different phase shift. Quantization of the phase shift stands for a measurement resolution. All counters are incremented between the timing markers "start" and "stop". Before readout the counter values are summed up giving the final result. The prototype board showed a 1 ns timing resolution. With a better ALTERA chip the resolution down to 300 ps could be achieved.

An advantage of this module, besides its dramatically lower price, is the nearly unlimited measurement range depending on the ALTERA capacity only. The principle of free reprogramming allows for implementing a single start and multiple stop signals or vice versa for the same channel, whose results could be kept in different registers (not yet done). The time-to-digital converter (TDC) is being used to determine the particle's range in the gaseous volume of the Bragg ionization chamber (BIC), to control the drift velocity of electrons in BIC (to optimize the gas pressure and the detector's high voltage) and to measure the time-of-flight for neutrons to determine their energies.

7.3 Ultrafast analog-to-digital converter

Based on the ALTERA chip, an ultrafast analog-to-digital converter (ADC) with a few millivolt RMS noise and 1 GHz sampling frequency has been designed. Similarly to the TDC principle, the ADC algorithm uses a number of integrated circuits for the amplitude conversion which are synchronized by frequencies with a constant phase shift equal to the sampling period. The data from all converters are kept in the pipeline to be readout via the CAMAC interface. This module may exchange analog constant-fraction discriminators (CFT) in the detecting techniques. The timing relations between signals could be also measured with up to 300 ps resolution. Together with an event selector this module makes possible to build up any nuclear-physical experiment.

The complete and up-to-date technical documentation on the BST trigger system and on electronics for the "Mini-FOBOS" experiment could be found under:

http://www.desy.de/~tsurin/Data

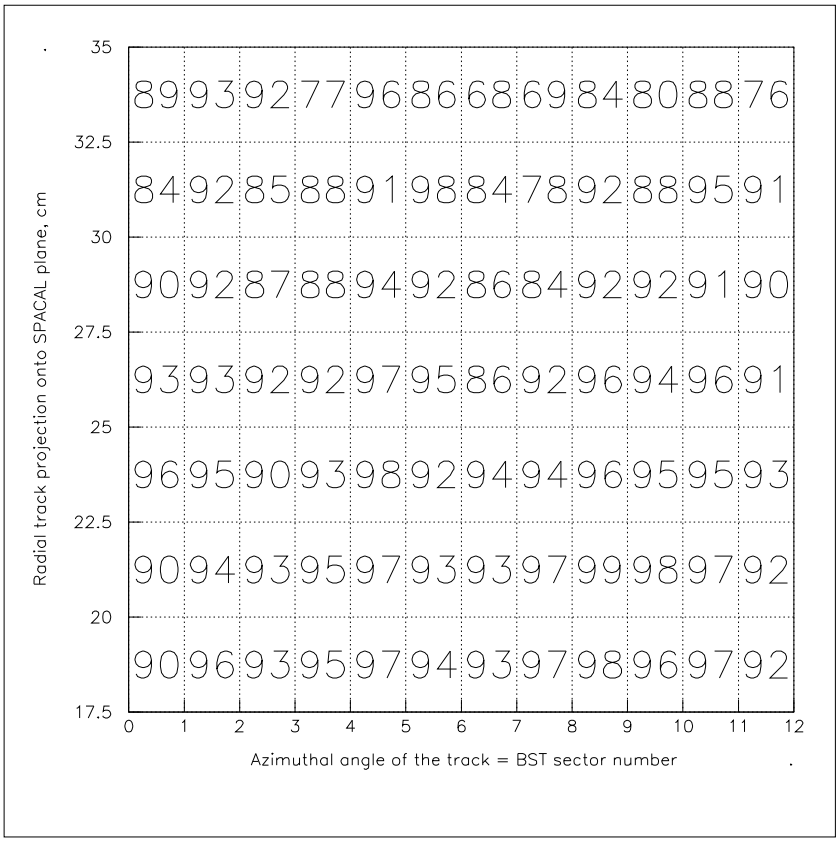

Figure 1: Trigger efficiency (%) of "S7" in the $R - \Phi$ plane, from ep-data

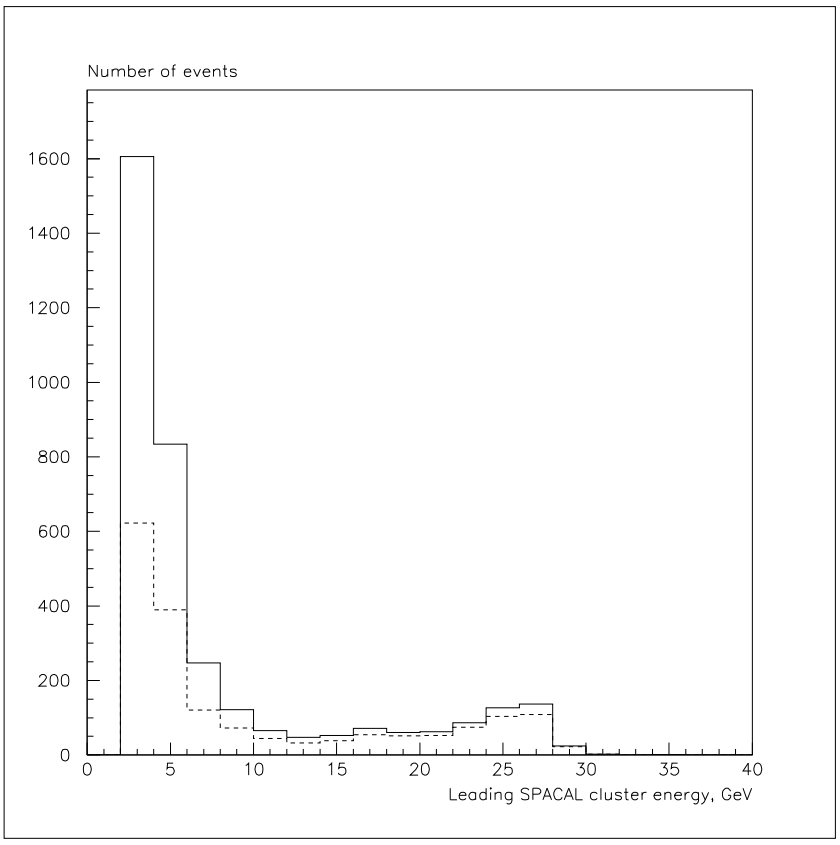

Figure 2: Trigger rate of "S7" raw (solid) and validated by STT (dashed).

Short summary / Schedule

April 2005 Assembling of a measurement facility in Zeuthen for evaluation of the newly produced radiation hard APC128UMC25 readout chips. Doing tests, inspection of the silicon wafers, discussing the obtained results with the IMEC Company.

May 2005 Assembling of a measurement facility in Hamburg for calibration of the manufactured strip detectors, doing tests and working out improvements to the technological process.

June 2005 Repair and modification of the front-end electronics for the silicon pad detectors. Updating the technical documentation on the BST trigger system.

July 2005 Extending the online data processing code for the front-end electronics and for the VME interface of the BST trigger system to transmit the raw data from the silicon pad detectors to the H1 CDAQ.

August 2005 Preparing and tests of the new configuration for the L2TT to implement geometrical constraints on acquired data to reduce the background triggerring of "S9" for more DIS statistics for "ELAN".

September 2005 Design of a new VME card to interface the the front-end of the silicon pad detectors with computer for their automated control. Re-writing the LabView detector's control application for the new command set of this card.

October 2005 Assembling of a measurement facility in Hamburg for calibration of the silicon pad detectors. Doing tests and bookkeeping of the obtained results.

November 2005 Mounting the silicon pad detectors and their front-end electronics onto Backward Silicon Tracker, doing the BST tests.

December 2005 BST installation and tests in the H1 experiment.

January 2006 Working at JINR in Dubna: commissioning of electronical modules for the "Mini-FOBOS" facility, assembling of its new data acquisition system, preparing of data taking.

February 2006 Setting up the FST trigger and the new H1 radiation monitor based on organic scintillators and on silicon photomultipliers.

March 2006 Tests of the silicon strip detectors with the $^{90}_{38}$Sr source. Search for the proper phase shift between the analog detector pulses and the synchronization strobes of their ADC.

April 2006 Redesign of the HV power supply for the silicon pad detectors.

May 2006 Development of the simulation tools for the silicon pad detectors.

June 2006 Trigger efficiency studies for the silicon pad detectors.

July 2006 Development of an algorithm for the SPACAL topological trigger including the tracking signals from the silicon pads. Studies of the STT efficiency and of its background rejection power.

August 2006 Writing the completion report.

Participation in conferences

1. 10th European Symposium on Semiconductor Detectors, Wildbad Kreuth, Germany, June 12-16 2005 "The New Radiation-hard Readout for the Forward and Backward Silicon Detectors of H1" - poster presentation of the new readout chip APC128UMC25 for the silicon strip detectors of H1. Travelling expenses and the conference fee were covered by DESY.

2. 12th High Energy Physics International Conference on Quantum Chromodynamics, Montpellier, France, July 4-9 2005 "Studies of Proton Structure at HERA" - presentation of the new measurements of the neutral and charged current DIS cross sections by the H1 and ZEUS experiments at HERA with polarized lepton beams. Travelling expenses and the conference fee were covered by DESY.

Mission grade (from 0-bad to 5-good): **4.5**

Explanation: In the first half of the scholarship period the main activities were concentrated on comissioning of the silicon pad and strip detectors which were upgraded in collaboration with DESY Zeuthen during the HERA shutdown in 2005. Studies of the detector performance were necessary for the HERA luminosity in the beginning of 2006. Afterwards simulation and analysis chains have been established to investigate geometrical distributions for ep collision products. Based on these studies, event signatures were extracted and have begun to be used for more efficient data taking for the "ELAN" group of H1.

Ilya Tsurin, Hamburg 16.09.2006