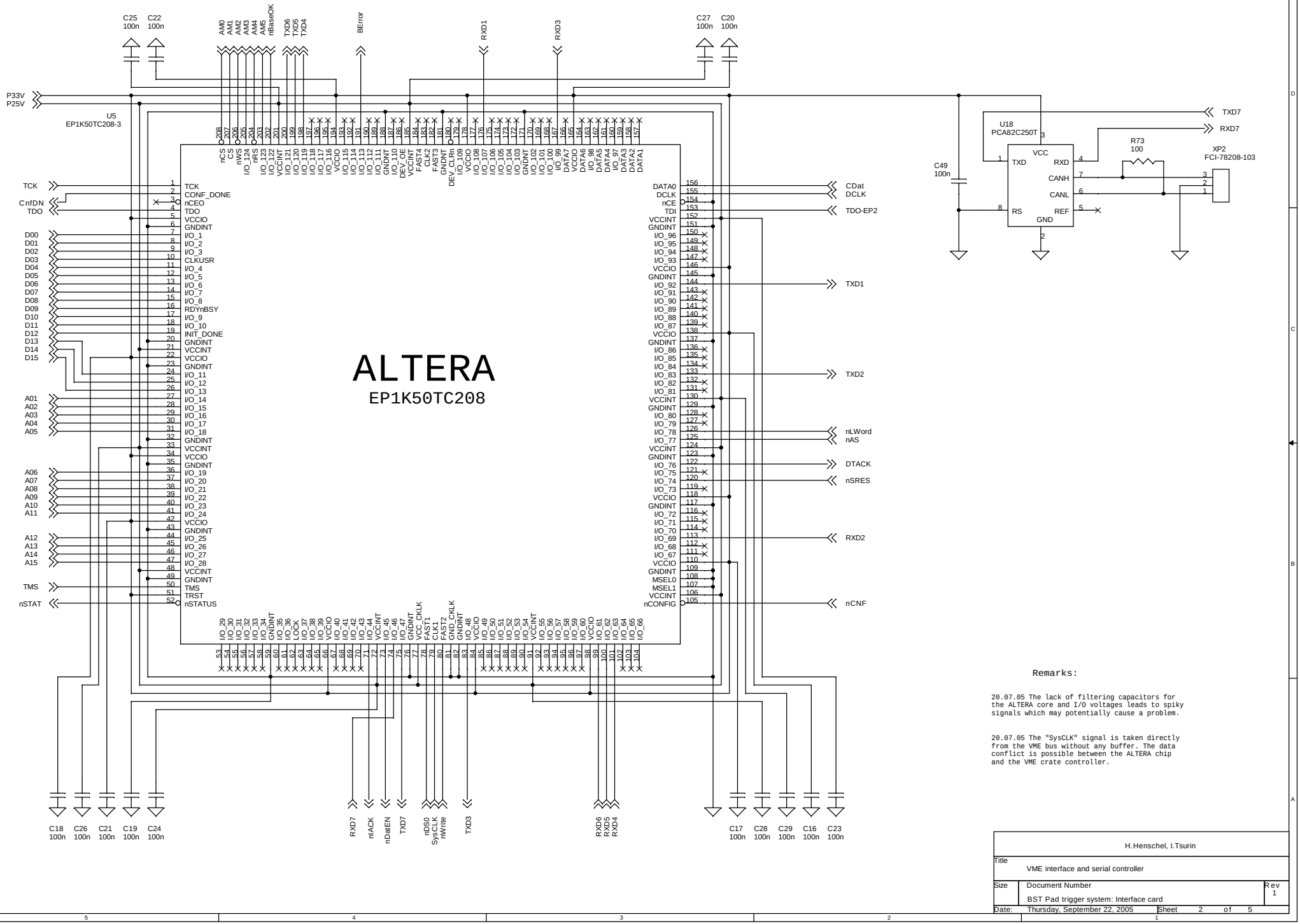

Remarks:

20.07.05 The lack of filtering capacitors for the ALTERA core and I/O voltages leads to spiky signals which may potentially cause a problem.

20.07.05 The "SysCLK" signal is taken directly from the VME bus without any buffer. The data conflict is possible between the ALTERA chip and the VME crate controller.

	H.Henschel, I.Tsurin	
Title	VME interface and serial controller	
Size	Document Number BST Pad trigger system: Interface card	Rev 1
Date: Thursday, September 22, 2005	Sheet 2 of 5	