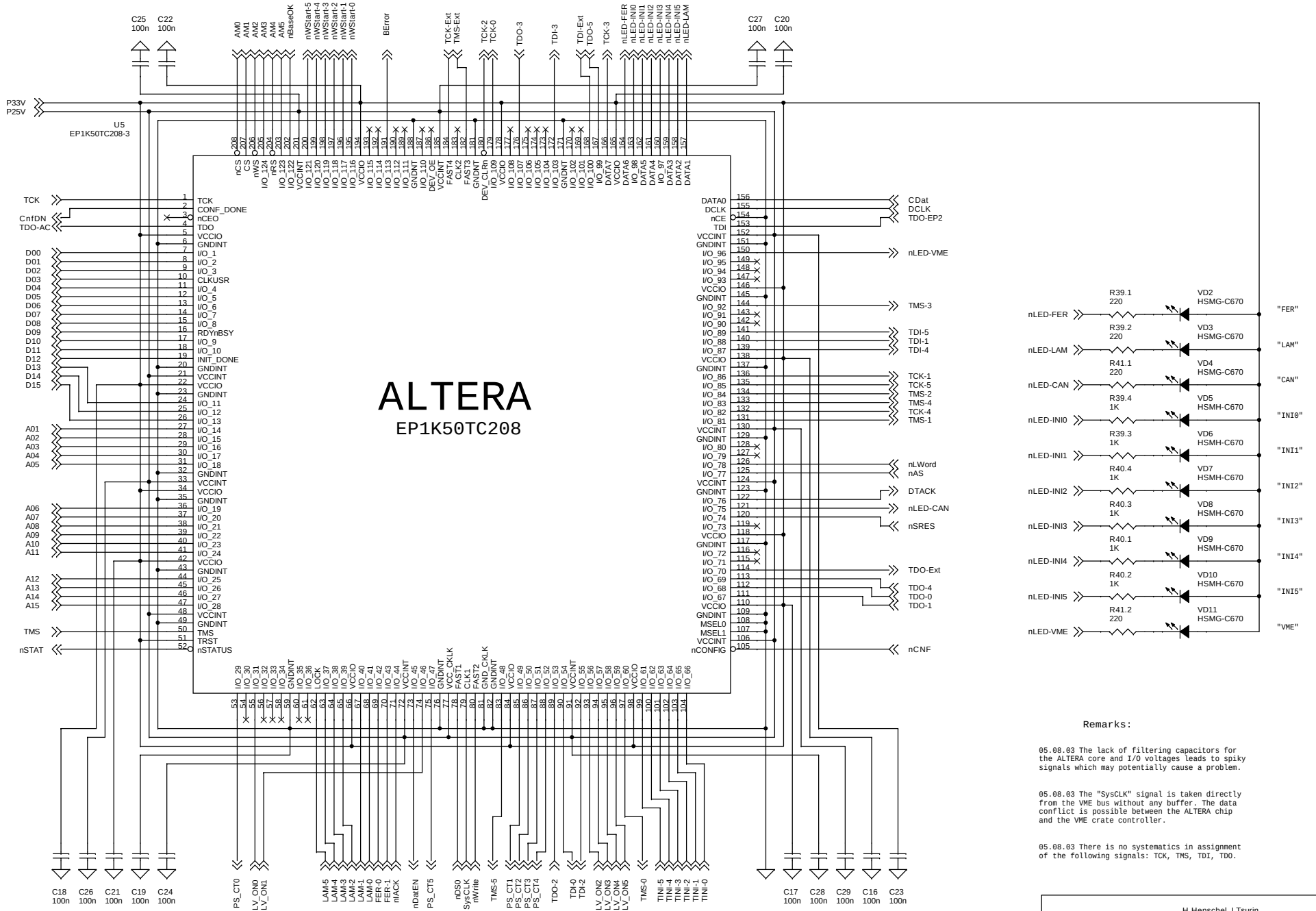

Remarks:

05.08.03 The lack of filtering capacitors for the ALTERA core and I/O voltages leads to spiky signals which may potentially cause a problem.

05.08.03 The "SysCLK" signal is taken directly from the VME bus without any buffer. The data conflict is possible between the ALTERA chip and the VME crate controller.

05.08.03 There is no systematics in assignment of the following signals: TCK, TMS, TDI, TDO.

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Title	Data processor and VME interface	
Size	Document Number BST Pad trigger system: Download card	Rev 1
Date: Friday, September 23, 2005	Sheet 2 of 6	