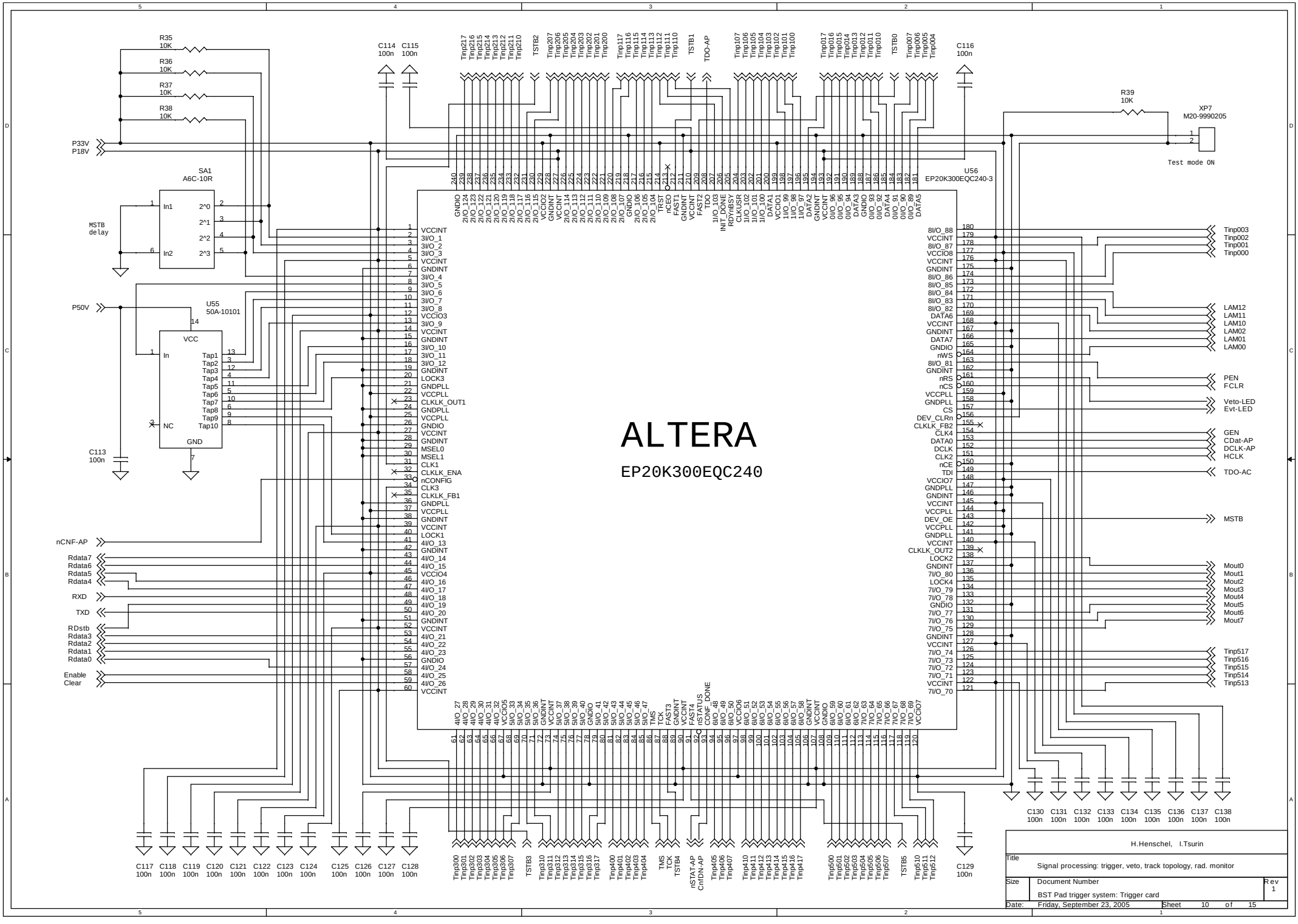
ALTERA
EP20K300EQC240
U56
EP20K300EQC240-3
SA1
A6C-10R
U55
50A-10101
XP7
M20-9990205
Test mode ON
MSTB delay
P33V
P18V
P50V
R35 10K
R36 10K
R37 10K
R38 10K
R39 10K
C113 100n
C114 100n
C115 100n
C116 100n
C117 100n
C118 100n
C119 100n
C120 100n
C121 100n
C122 100n
C123 100n
C124 100n
C125 100n
C126 100n
C127 100n
C128 100n
C129 100n
C130 100n
C131 100n
C132 100n
C133 100n
C134 100n
C135 100n
C136 100n
C137 100n
C138 100n
nCNF-AP
Rdata7
Rdata6
Rdata5
Rdata4
RXD
TXD
RDstb
Rdata3
Rdata2
Rdata1
Rdata0
Enable
Clear
Tinp003
Tinp002
Tinp001
Tinp000
LAM12
LAM11
LAM10
LAM02
LAM01
LAM00
PEN
FCLR
Veto-LED
Evt-LED
GEN
CDat-AP
DCLK-AP
HCLK
TDO-AC
MSTB
Mout0
Mout1
Mout2
Mout3
Mout4
Mout5
Mout6
Mout7
Tinp517
Tinp516
Tinp515
Tinp514
Tinp513
TSTB2
TDO-AP
TSTB0
TSTB3
TSTB1
TSTB4
TSTB5
nSTAT-AP
CnfDN-AP
H.Henschel, I.Tsurin
Title
Signal processing: trigger, veto, track topology, rad. monitor
Size
Document Number
BST Pad trigger system: Trigger card
Rev 1
Date: Friday, September 23, 2005
Sheet 10 of 15