Minimising injected ground noise in multiple module arrays of silicon detectors Tony Smith Dec '99

Take a simple case of **two modules overlapping** along the full **length of 12cm** with a 3mm gap between the strips on one module and the strips on another module. (as in the Atlas SCT forward region)

The amplifier inputs are virtual earths so the strips on each detector will be forced to the potential of the amplifier ground reference point on each of the modules. Therefore any potential difference between the ground reference points on the two modules will appear as a potential difference between the two silicon detector faces. From the point of view of a single strip on one of the detectors in the overlap region, the opposing face of the superposed detector will appear as an equipotential second plate of a **parallel plate capacitor** with a capacitance determined by the area of the strip and the separation of the strip and plate.
For a 12cm strip of width 100um (assume all field lines in the width of one strip pitch terminate on the strip)
and separated by 3mm from the overlying detector then:

$$C = \frac{12e\text{-}2 * 1.0e\text{-}4 * 8.85e\text{-}12}{3e\text{-}3} = \mathbf{35.4\ fF}$$

This parasitic capacitance is connected directly to the input of the strip amplifier and consequently any voltage change across it will inject a signal in the same way as the on chip calibrate capacitor is used to inject a known calibration charge.

In order to get a feel for the problem which may be caused by this parasitic capacitance let us calculate the magnitude of a **voltage step** which would be required across this parasitic capacitance to inject a charge equal to **1mip.**

$$= \frac{22500 * 1.6\ e\text{-}19}{3.54e\text{-}14} \quad \mathbf{=100mV\ for\ 1mip}$$

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Now this is for a 1mip signal injection and clearly such a large parasitic input would completely swamp real signals- what we really need to know is the **maximum noise voltage which we can allow between the detector grounds before the performance of the detector is compromised.**

For this purpose let us now assume that we are dealing with non correlated random noise where the noise contributions are RMS values and add in quadrature. (N.B. questionable mathematical and noise spectrum assumptions here but it gives a ballpark idea of the problem - needs more work)

The noise in RMS electrons of the unirradiated module is expected to be around 1500e. If we now say we can allow **an additional 100 electrons** total noise so that the total noise will become 1600 e then we can allow a contribution from the injected signal of 556 electrons. - dividing this by 22500e and multiplying by 100mV gives us an **allowed noise voltage between the two detector grounds of 2.5 mV RMS.**

It is clear that one way to minimise voltage differences between module grounds, and hence minimise injected noise, is to short the sensor reference grounds together by a low impedance path..

It may be possible to use the cooling tube as a common reference conductor and also as a common (safety) ground point in the detector.

NOTE 1)-- this grounding scheme will only be effective if the star ground points of the module (low end of detector backplane decoupling capacitor) are tied to the tube. If this tie is made from any other point in the module ground plane where power supply current is flowing then common impedance coupling can couple power supply noise into this loop.

NOTE 2) Each of the multiple power supplies to each of the modules are (should be!) ohmically isolated at the remote (power supply) end. and the low ends of the supplies are then tied together at the module to form a star point ground. This ensures, at least for the DC case, that there will be no common impedance coupling between noisy digital and sensitive analog supplies. Additionally there is not (should not be!) any ohmic connection between the remote (power supply) ends of the supplies to different modules. This ensures that for the DC case there will not be any circulating currents between individual modules via a common ground link between the module star points. However for the AC case this ideal cannot be realised as there will always be parasitic capacitive coupling between power cables in the cable harnesses. (around 1nF between two superposed tapes 3mm wide, 1m long and separated by 100um of kapton or about 4 ohms at 40 Mhz).

To avoid problems from high frequency transients generated by the module logic which can circulate through the common gound tie, this tie must not only be a low resistance connection, but must be a low reactance connection also. (6cm of 2.5mm diam wire has an inductance of around .0.03uH giving a reactance of 0.18 ohms @ 1Mhz or around 7 ohms @ 40 Mhz, this will not be greatly different from a 3mmo/d tube).