Low-Power Analog IC Design Activities at CNM

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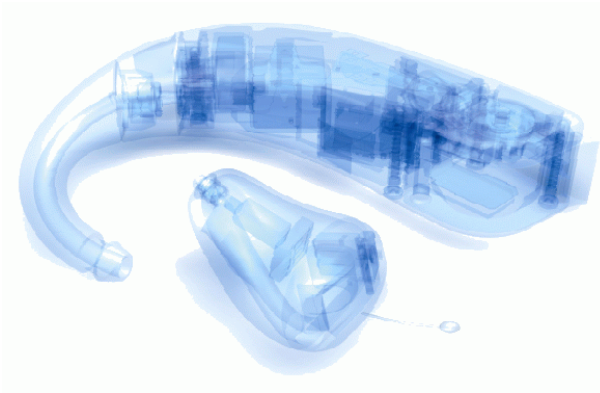
Skills

- Wide experience on **R+D/industrial** IC applications
- Deep **CMOS** technology knowledge
- Advanced MOS device **modeling**
- State-of-the-art **analog/mixed/RF circuit** techniques
- **System-on-Chip** development
- **Full-custom** sub-micron IC design
- **Custom test** capabilities

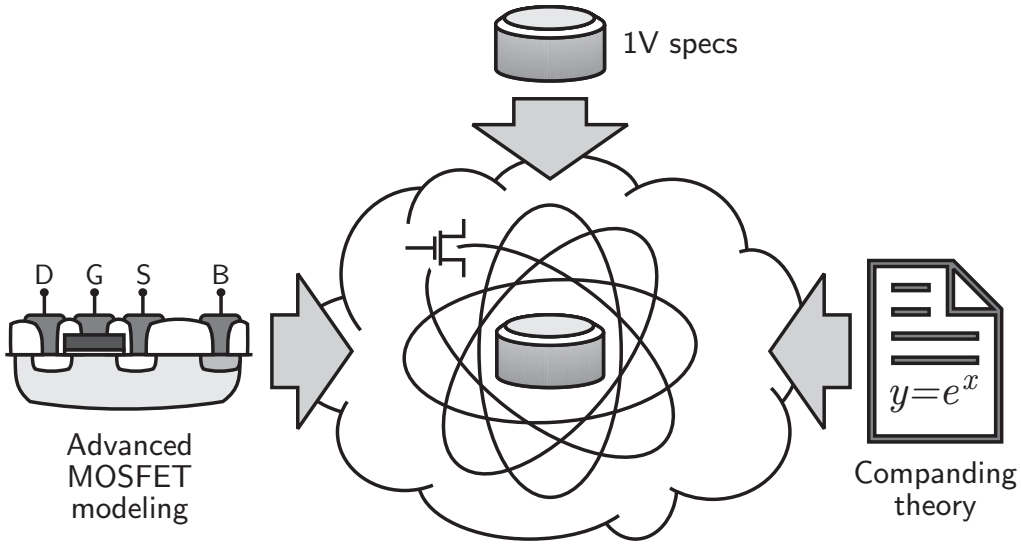
Environment

- In-house: state-of-the-art **nanotechnology**
  basic **CMOS** technology
  advanced hybrid **MCM** packaging
- Full access to **Europractice**/**Mosis** programs
- Wide variety of supported **CAD** workflows
- High-value **equipment** facilities
- Good interaction between design/technology **staff**
- Experience on **funding** strategies
- Many other research lab **partners**

Hearing Aids



- Small battery: 1.0V + <0.5mA
- Small package: <10mm^2 + few components
- Complex audio processing
- Large dynamic range: >70dB
- Low-cost: CMOS + program. BTE...CIC



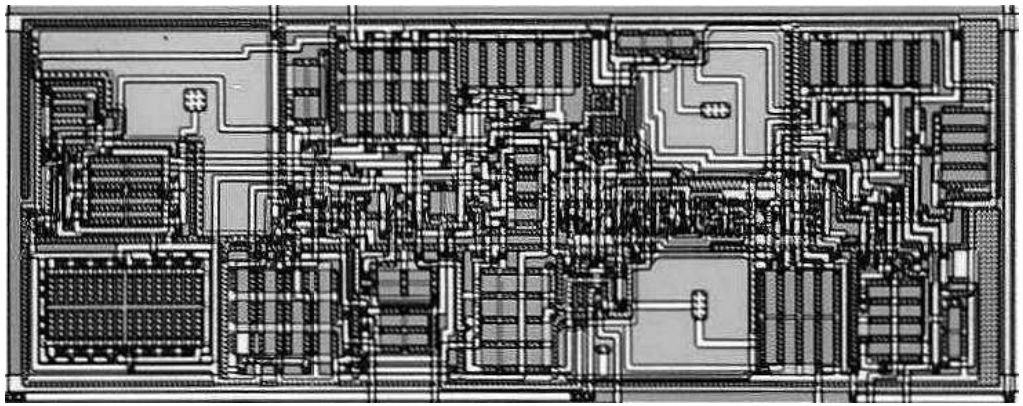
True-1V analog operation using novel subthreshold log-domain circuit techniques

Hearing Aids

- Library driven research:
  - Pre-amplification
  - Dual-AGC
  - Arbitrary filtering
  - PDM conversion
  - Class-D output
  - Built-in references
  - Digitally programmable

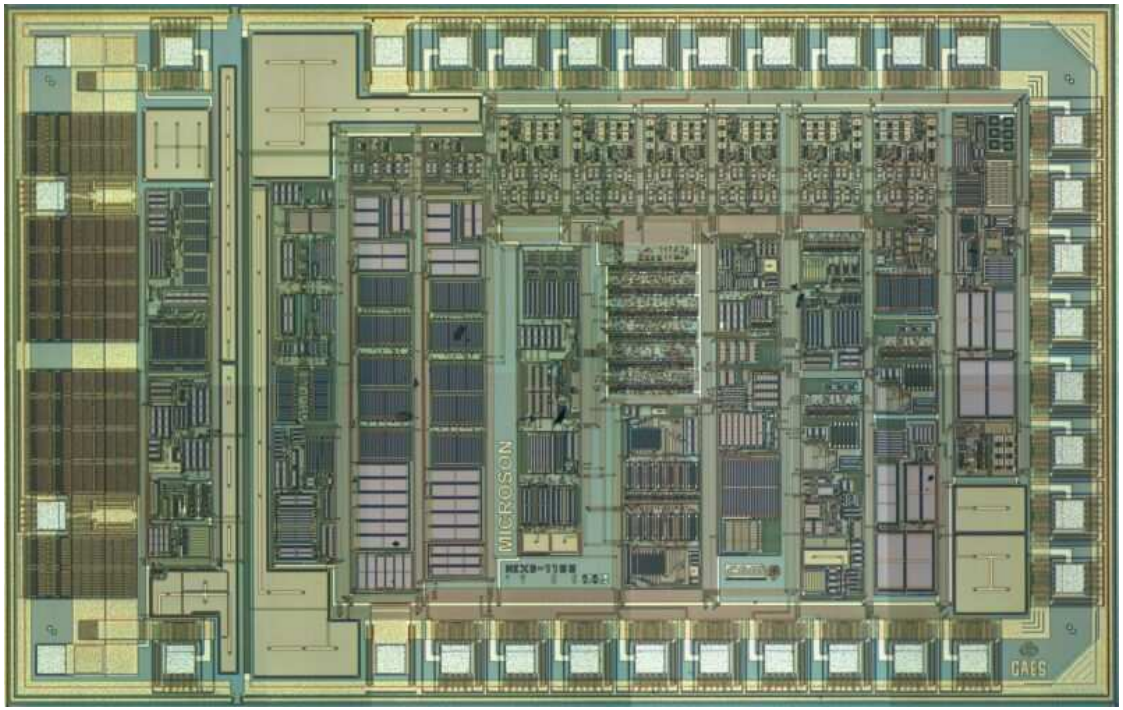
1997-99 **CICYT-TIC97-1159**
Low-Power and Low-Voltage Microelectronics for Hearing-Aids

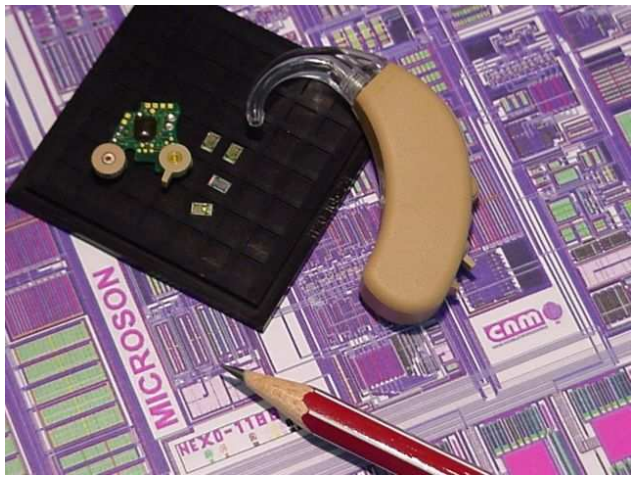
1998-00 **ESPRIT-FUSE-23068**
Microelectronic Device for Hearing Aid Application



Hearing Aids

- Industrial product:

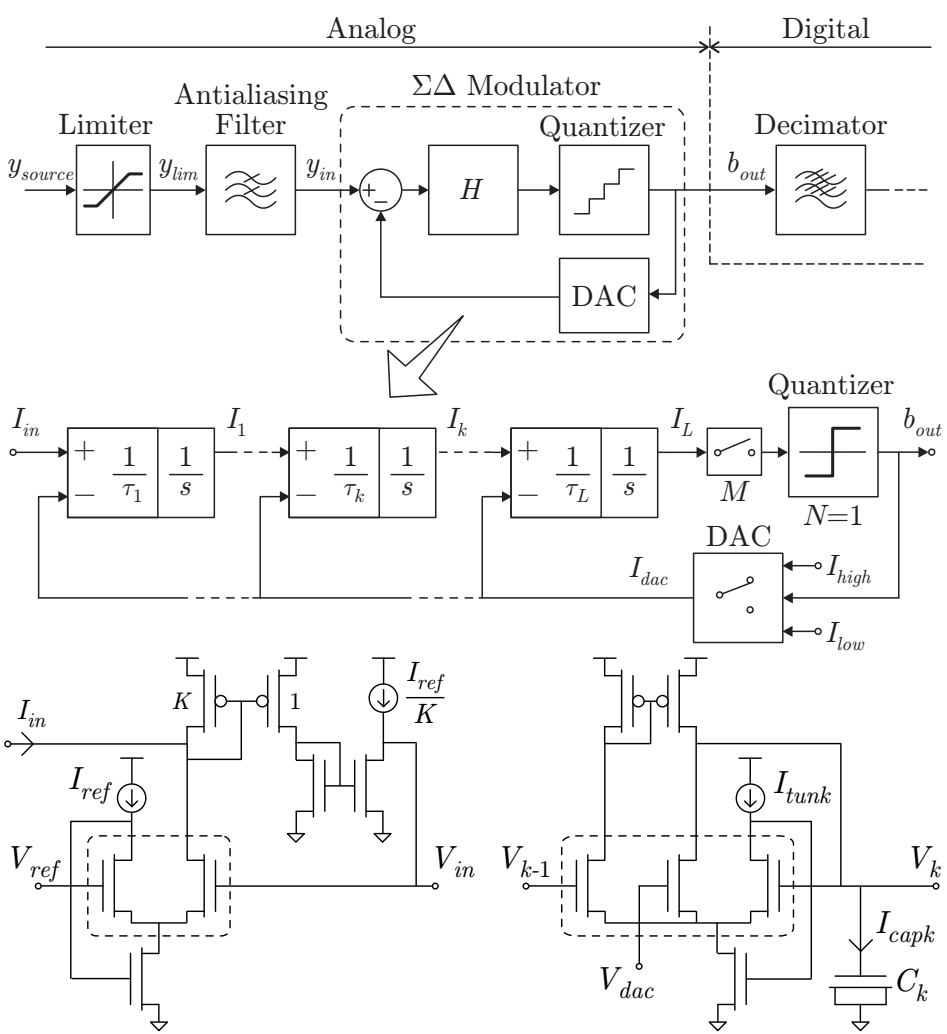


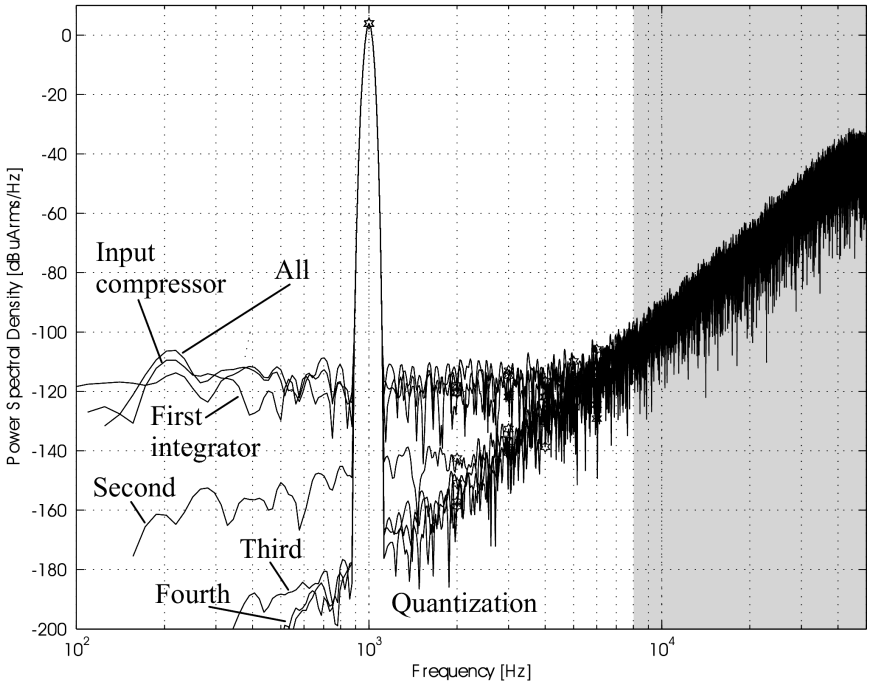


NEXO
GAES-MICROSON

A 1V 300μA 1.2μm CMOS analog hearing-aid-on-chip

Oversampling ΣΔ A/D Converters





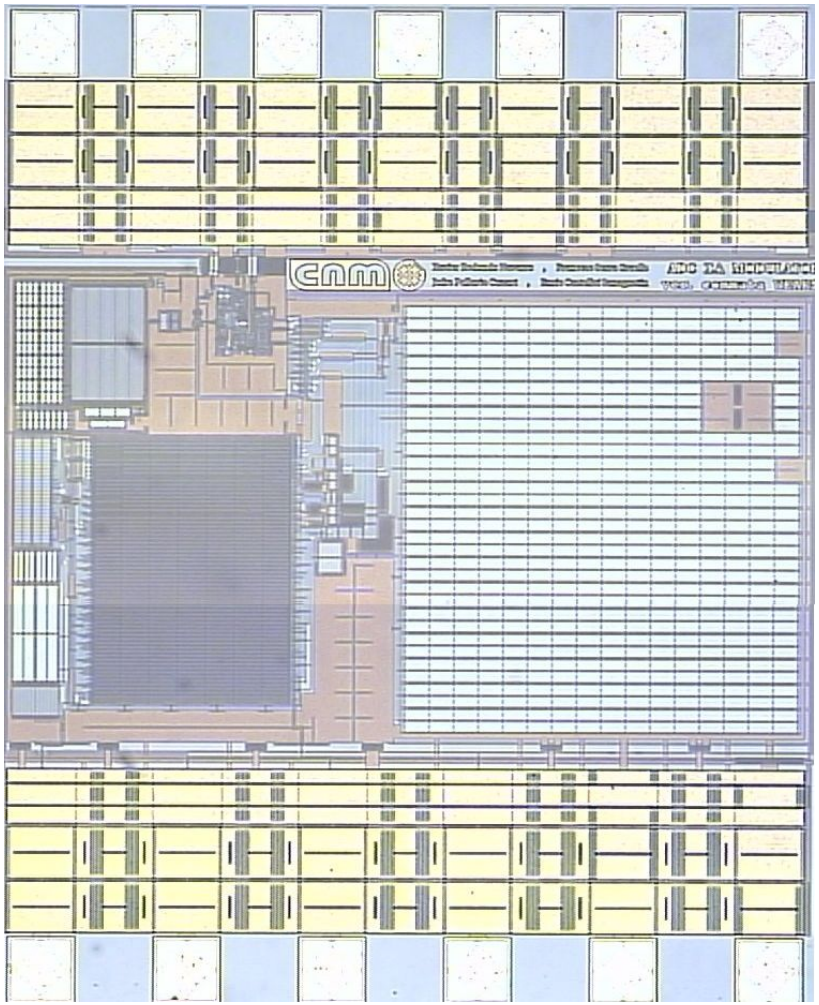
- CMOS log-domain techniques
- Subthreshold operation
- All-MOS implementation

Oversampling ΣΔ A/D Converters

2000-01 **FEDER-1FD97-2351**
Design of a CMOS Low-Power Digital Biophone

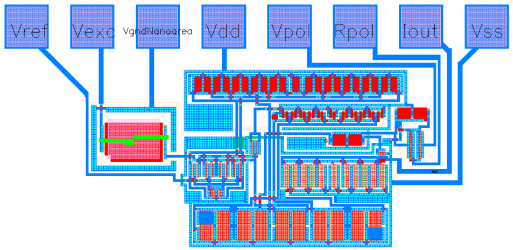
2000-02 **CICYT-TIC99-1084**
CMOS Circuit Techniques for Analog Subsystems in Digital Hearing Aids

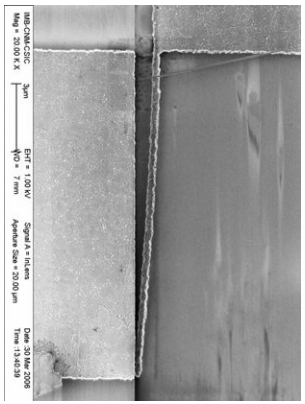
A 1.2V 100μW
0.35μm MOS-only
10/12-bit 8KHz ΣΔ ADC



Sensor Interface for N/MEMS

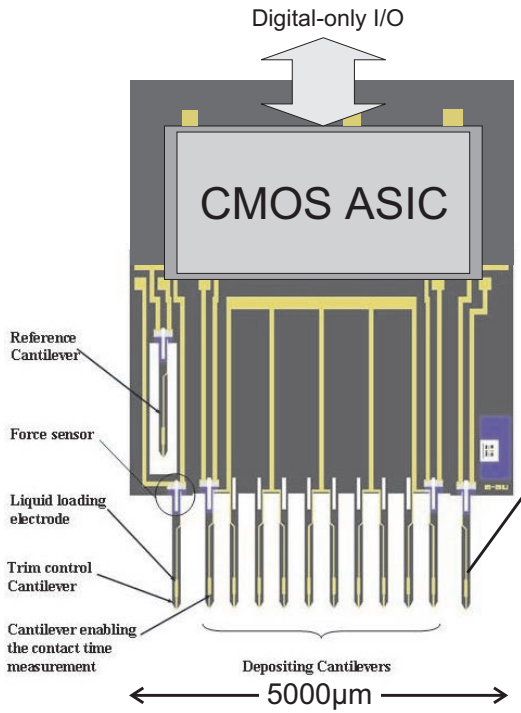
2003-06 **NMP4-CT-2003-500120** *Emerging Nanopatterning Methods*



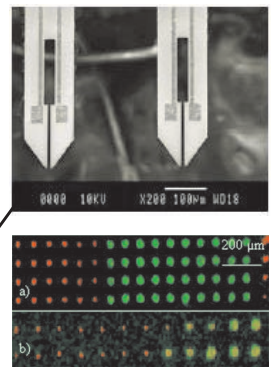


In-house 2.5μm CMOS
read-out circuit
for MEMS resonator

An integrated
fluidic system
for nano-dispensing

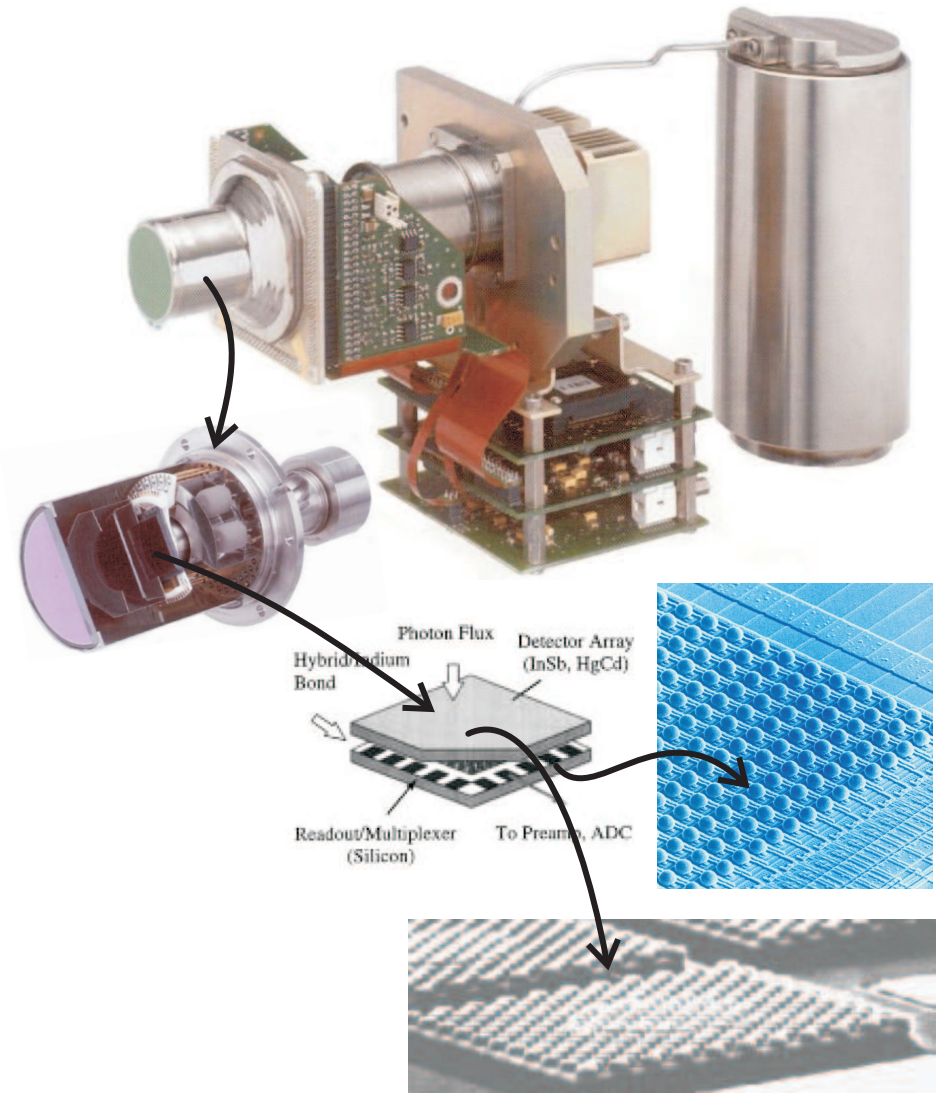


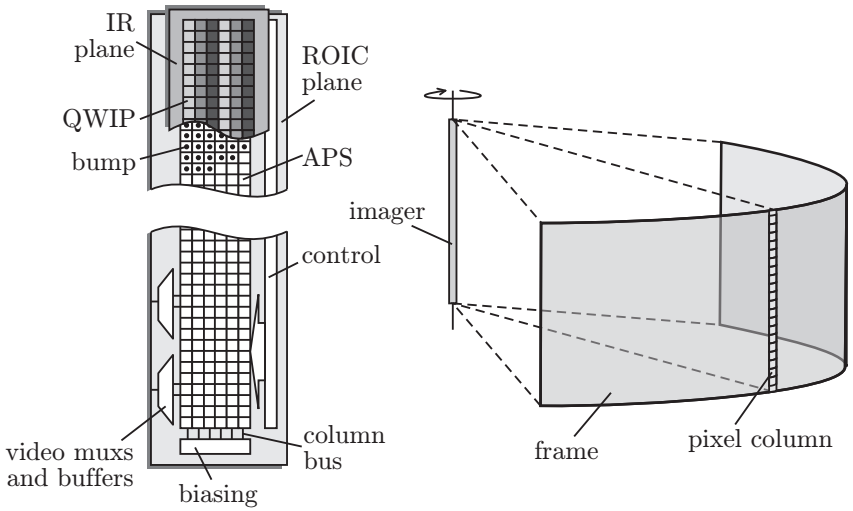
NaPa
Emerging Nanopatterning Methods
Bioplume



Fluorescent droplets

Cryogenic IR Scanning Imager

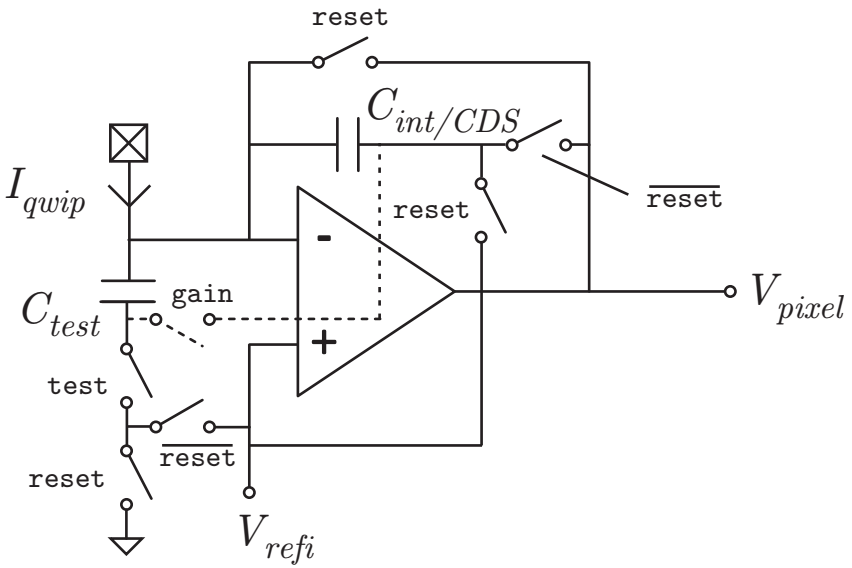


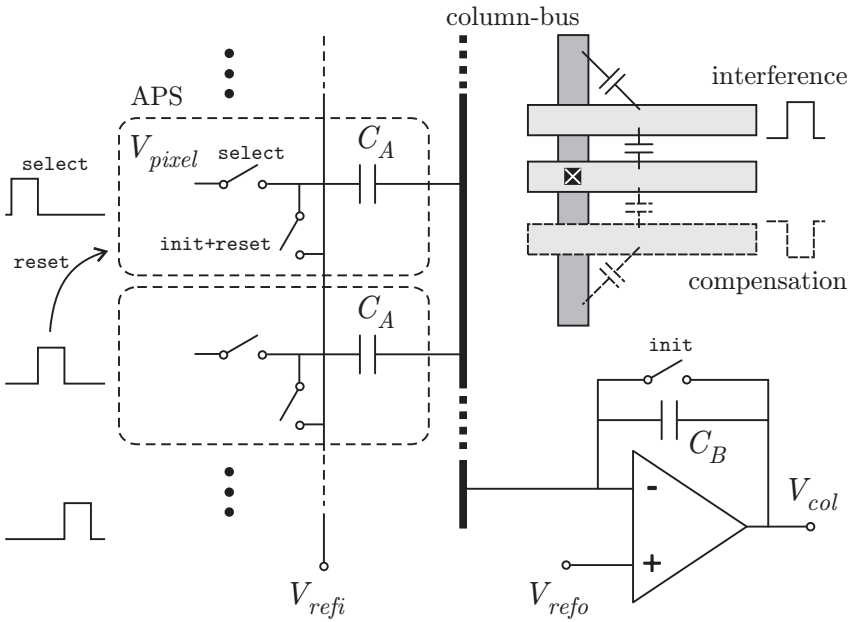


- QWIP sensors
- Low-current signal (∼5nA)
- Cryogenic temperature (77K)
- Small pixel size (100μm×50μm)
- 500×12 FPA
- Complex APS (CDS+test+prog)
- High-speed video streaming (60ns/s)
- Hybrid packaging (high capacitance)

Cryogenic IR Scanning Imager

- Novel SC techniques for compact APS + low-power video:



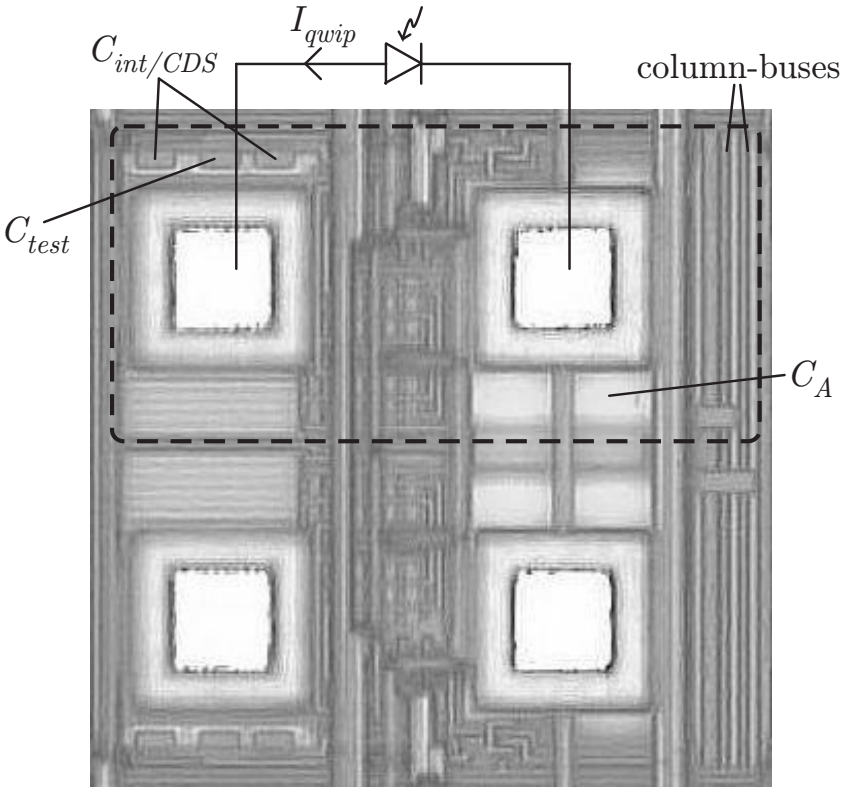


- Single-cap integration+CDS
- Built-in test
- Gain programability

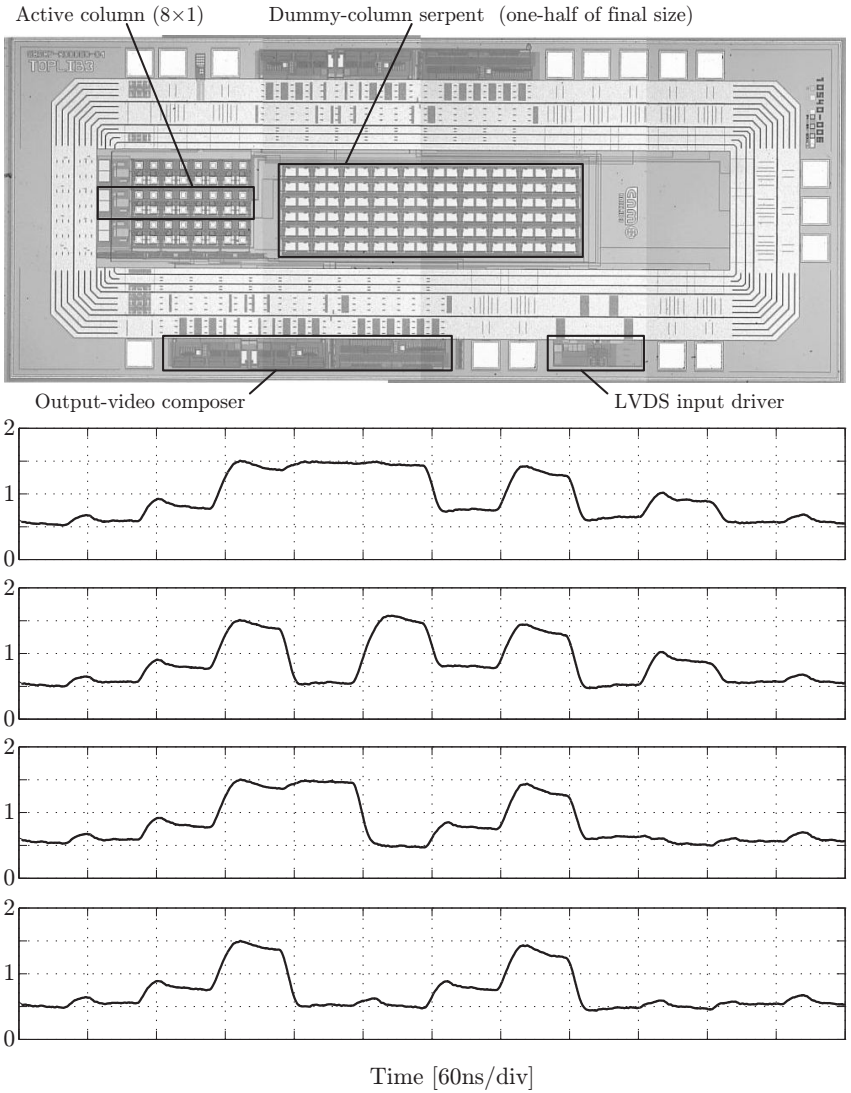
- Analog charge-multiplexing
- Pseudo Class-AB buffering

Cryogenic IR Scanning Imager

- Library driven research:

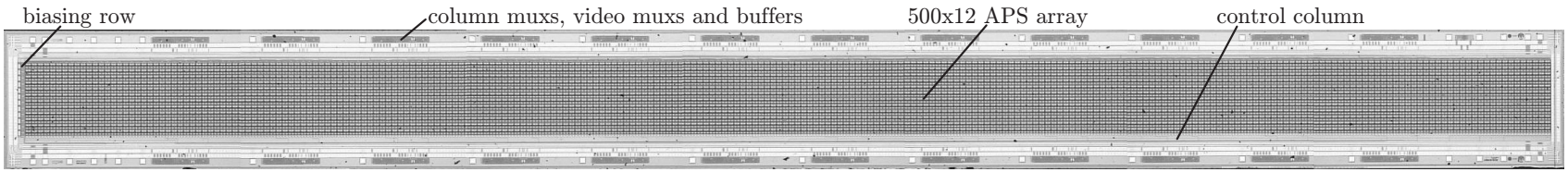


50μm×100μm APS cell



Cryogenic IR Scanning Imager

- Cryogenic specific MOSFET modeling (CNM⇔AMS)
- Industrial product in standard CMOS 2P 3M technology:



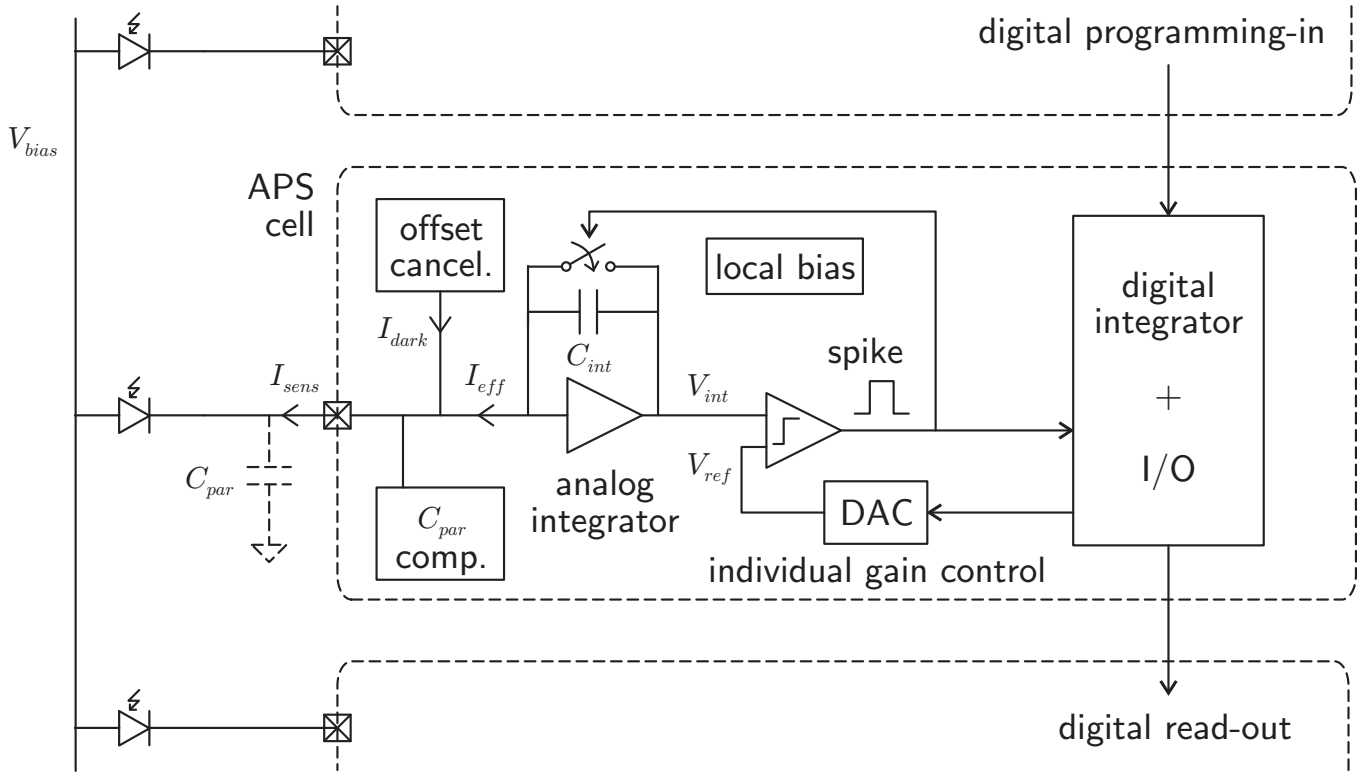
2002-04 **DN-8644 SIRIO**
A low-power CMOS ROIC for cryogenic tri-color quantum-well IR photo-sensors

Indra

Pixel array size	500×12	pixel^2
Pixel pitch	50	μm
Pixel size	50×100	μm^2
Temperature operation	77	K
Integration time	15.6	μs
Video sampling	60	ns/pixel
Video resolution	10	bit
Pixel oversampling	4	times
Typical frame	640×500@100	pixel^2@fps
Supply voltage	3.3	V
Power consumption	210	mW
CMOS technology	0.35	μm
Silicon Area	25×2	mm^2
Complexity	∼250K	devices

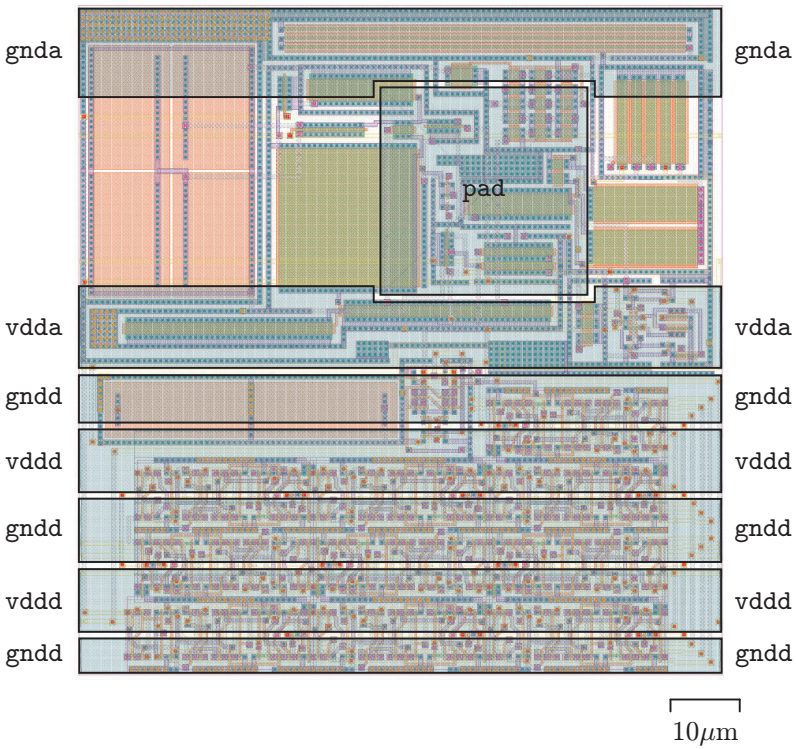
Room-Temperature IR Digital FPA Imager

- A self-biased and FPN-compensated digital APS:



. . . with pixel built-in asynchronous integrating A/D converter.

Room-Temperature IR Digital FPA Imager

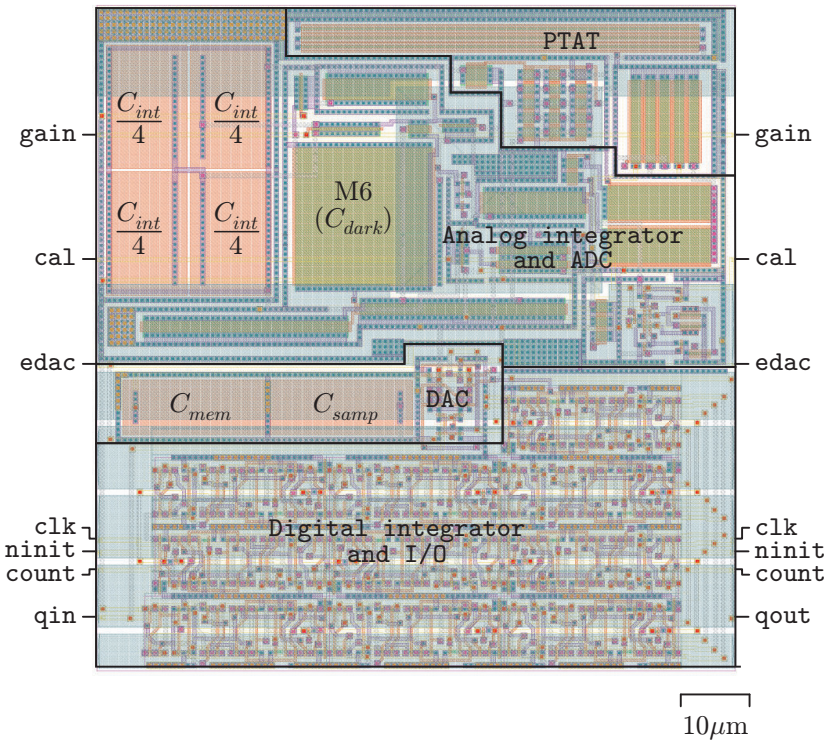


2005-06 **DN-8835 SEADIR**

A modular and digital CMOS imager for hybrid focal plane arrays of IR sensors

Dark current range	0.2-5	μA
Dark current retention	1-10	s
Max. input capacitance	15	pF
Signal range	1-1000	nA
Integration time	1	ms
Programming/read-out speed	10	Mbps
Supply voltage	3.3	V
Power consumption	<1	μW
Biasing deviations ($\pm\sigma$)	± 15	%
Total Silicon area	100×100	μm^2

Room-Temperature IR Digital FPA Imager



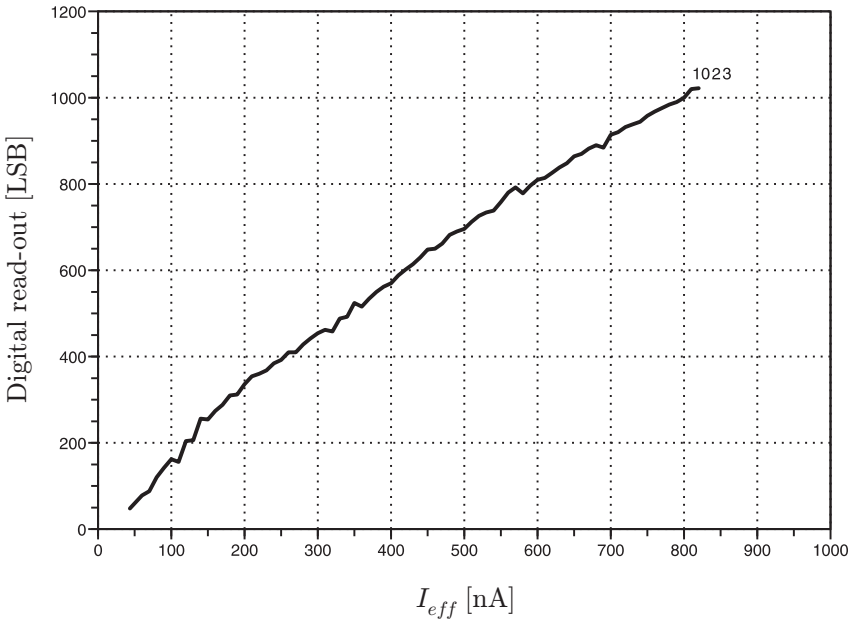
2005-06 **DN-8835 SEADIR**

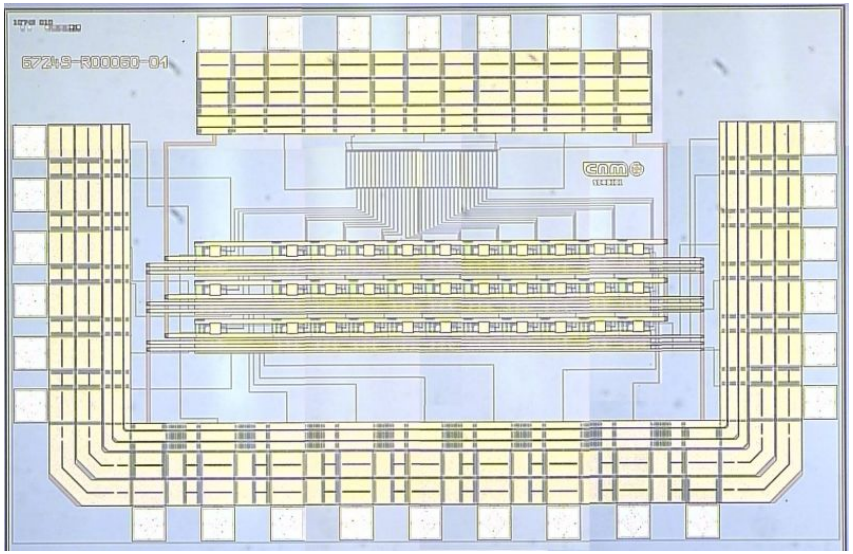
A modular and digital CMOS imager for hybrid focal plane arrays of IR sensors

Dark current range	0.2-5	μA
Dark current retention	1-10	s
Max. input capacitance	15	pF
Signal range	1-1000	nA
Integration time	1	ms
Programming/read-out speed	10	Mbps
Supply voltage	3.3	V
Power consumption	<1	μW
Biasing deviations ($\pm\sigma$)	$\pm$15	%
Total Silicon area	100×100	μm^2

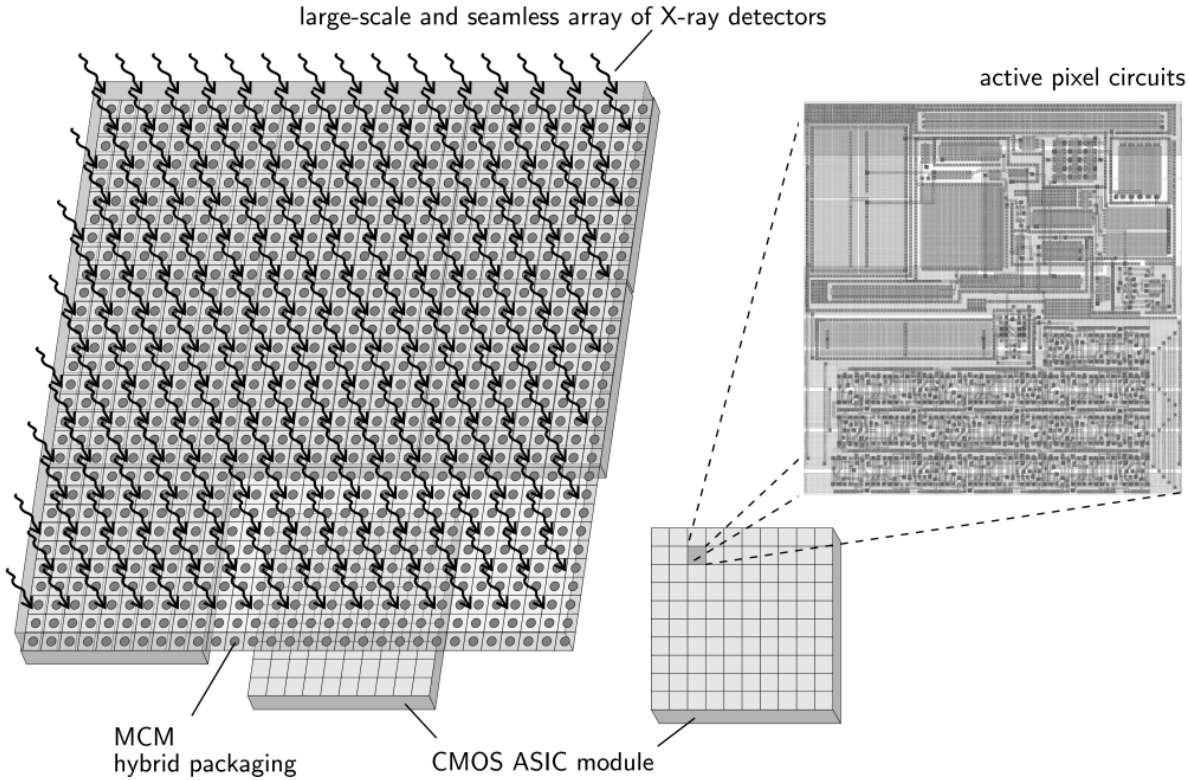
Room-Temperature IR Digital FPA Imager

- Test vehicle implemented
- 0.35μm 2P 4M CMOS technology





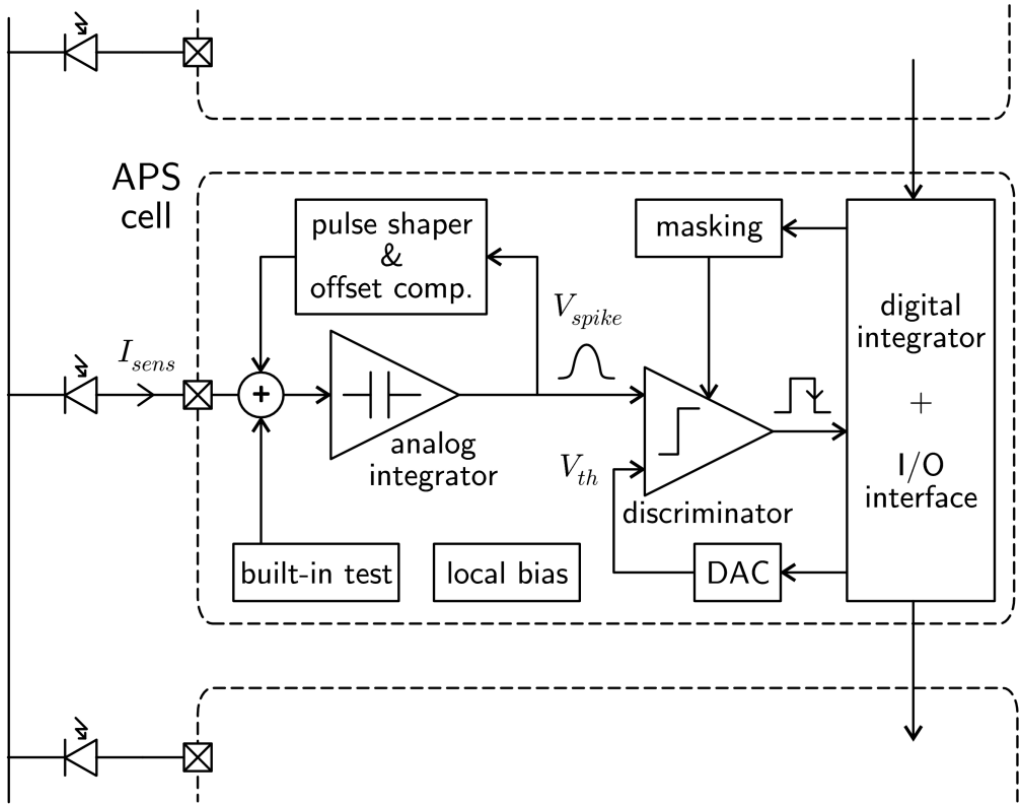
Large-Scale and Modular X-Ray Digital FPA Imager



- $6\times6cm^2$ 800×800pix (>0.5Mpix) seamless X-ray images
- True modularity
- High flexibility
- Improved IC yield & costs
- Advanced in-house MCM packaging

Large-Scale and Modular X-Ray Digital FPA Imager

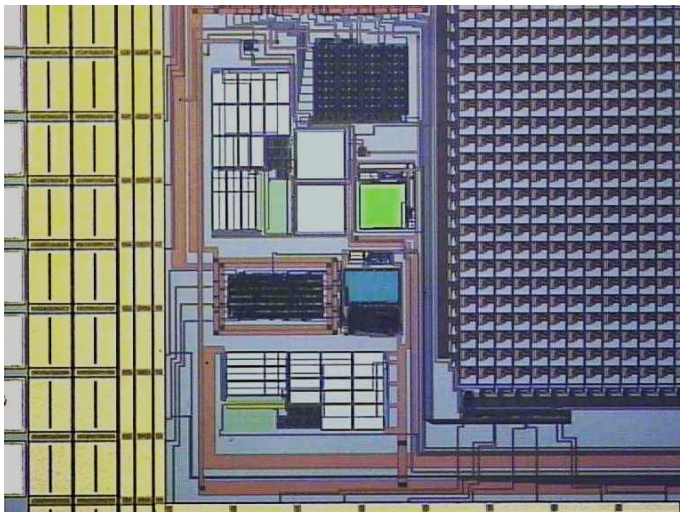
- Based on photon counting digital APS cells:



2006-07 **FIT-330101-2005-4 PHOCPix** *A new integrated circuit and electronic system for capturing radiology images*

Low-Power and RF Imagers for Optical Character Recognition

- **Built-in** sensor FPA
- Digital **OCR**
- **RF** communications
- **Battery** powered
- 0.35μm 2P 4M CMOS technology
- Industrial product



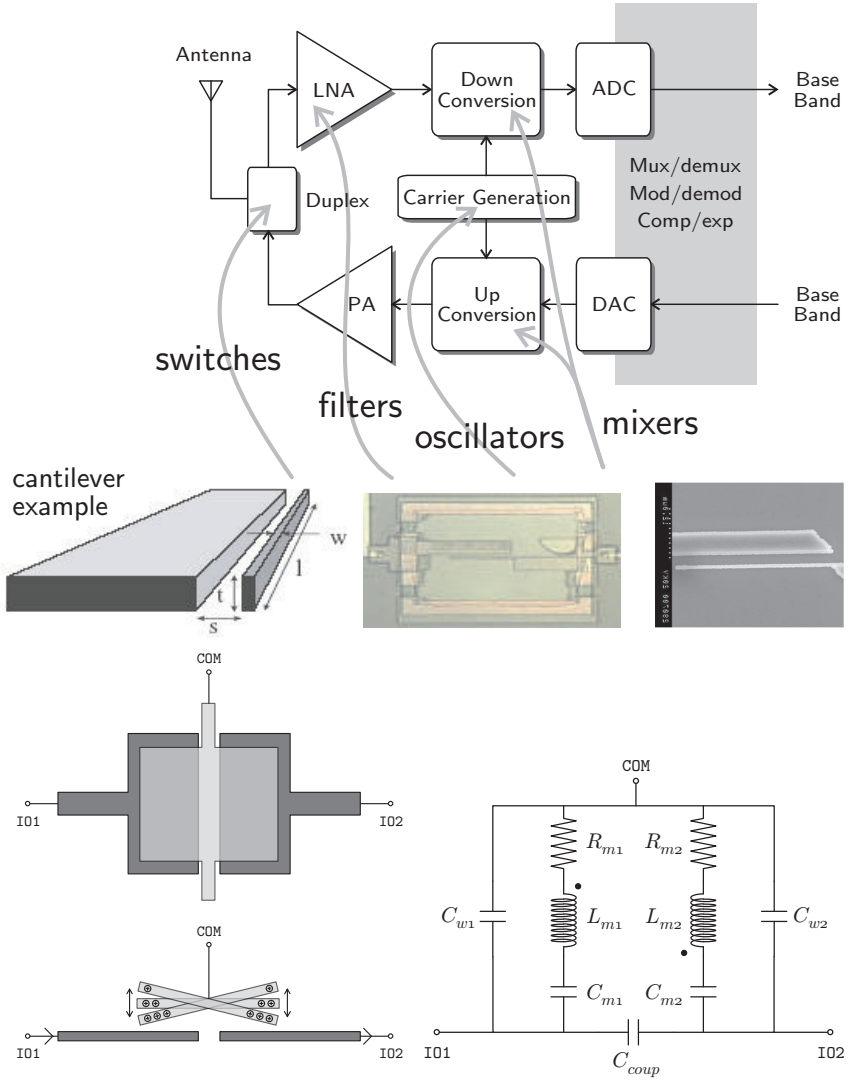
2003-05 **FIT-070000-2003-968**
Telecontadores
A low-power and compact OCR system for remote water metering

Very Low-Power Mixed CMOS/NEMS RF Transceivers

- High-Q and low-power NEMS resonators
- **NEMS device** modeling and CMOS interface
- 0.35μm 4M RF CMOS technology

2003 **CICYT-TIC02-1981**
Radio frequency CMOS integrated receivers for hearing-aids-on-chip

2004-06 **CICYT-TIC03-07237**
Low-power NEMS and CMOS systems for signal sensing and processing in portable applications



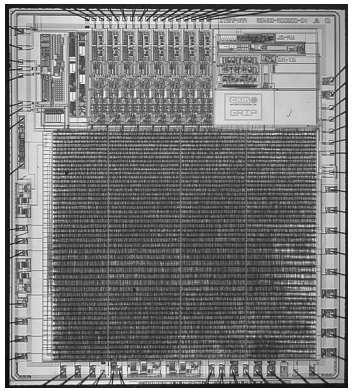
Very Low-Voltage and Low-Power Bluetooth Frontend

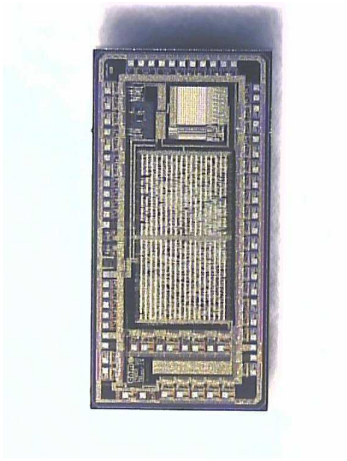
- Low End Extension (**LEE**) open standard
- **1V** battery powered
- Supply life **>1 year**
- 0.18μm 6M RF CMOS technology
- Application to networks of **sensors**

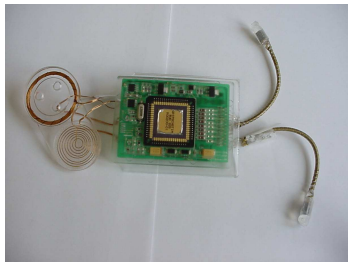
2006-07 **BluLite** SEIKO-EPSON industrial project

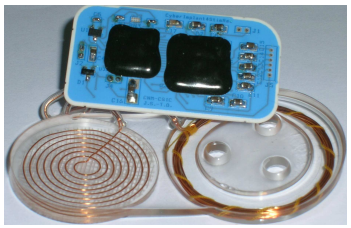
Implantable SoC for multi-channel neural processing

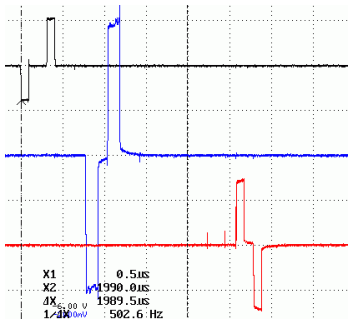
- Transcutaneous **RF-coupling** link for **supply** and digital **communications**
- Low-power SoC
- Nueral **recording** and **stimulation**
- 0.8μm and 0.35μm high-voltage CMOS technologies
- Applications:
  - Restoring mobility in SCI people
  - Control of artificial prosthesis

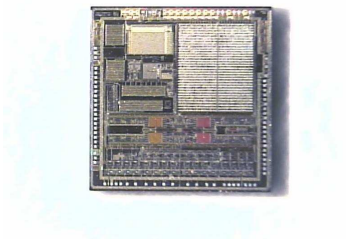












What is next?

Emerging research on...

- **Heterogeneous** systems (sensors, NEMS, CMOS)
- Distributed and **parallel** processing (inter/intra-IC)
- **Energy scavenging** (battery-less, very low-power)
- **Packaging** optimization (RF, sensors, stacked MCM)