Microelectronic Technologies for HEP

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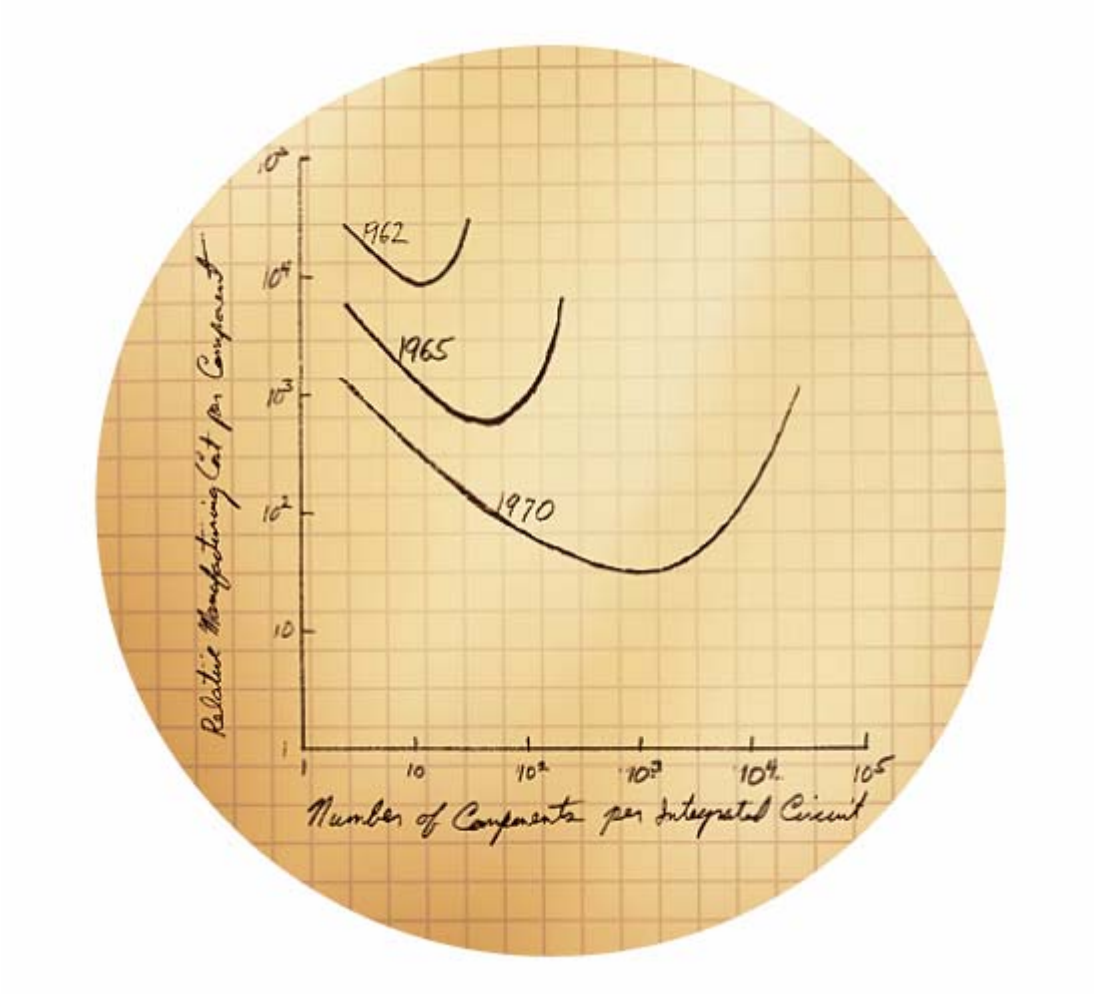
Topics

- Perspectives for using new CMOS technologies in HEP applications
  - Advantages and benefits
  - Difficulties with newer technologies
- Projections for simple case studies
- Availability and access:
  - Tools for designing
  - MPW runs
- Conclusion

Moore's Law and its impact on Instrumentation for HEP



ITRS roadmap until 2020

Today

Year of Production		2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)		70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	90	78	68	59	52	45	40	36	32
MPU Printed Gate Length (nm) ††	54	48	42	38	34	30	27	24	21
MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
ASIC/Low Operating Power Printed Gate Length (nm) ††	76	64	54	48	42	38	34	30	27
ASIC/Low Operating Power Physical Gate Length (nm)	45	38	32	28	25	23	20	18	16
Flash ½ Pitch (nm) (un-contacted Poly)(f)	76	64	57	51	45	40	36	32	28

Table 1b Product Generations and Chip Size Model Technology Trend Targets—Long-term Years

Year of Production	2014	2015	2016	2017	2018	2019	2020
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	28	25	22	20	18	16	14
MPU Printed Gate Length (nm) ††		17	15	13	12	11	9
MPU Physical Gate Length (nm)		10	9	8	7	6	6
ASIC/Low Operating Power Printed Gate Length (nm)	24	21	19	17	15	13	12
ASIC/Low Operating Power Physical Gate Length	14	13	11	10	9	8	7
Flash ½ Pitch (nm) (un-contacted Poly)(f)	25	23	20	18	16	14	13

SLHC/ILC

Microelectronics challenges for ILC

	Industry @ 2010	*HEP @ 2010*
Speed of technology	☺	☺
Integration capabilities	☺	☺
Analog Performance	☺	😐/☹
Accessibility	☺/😐	😐/☹
Radiation tolerance	n.a.	☺
Power consumption	☺/😐	😐/☹
Packaging	☺	☹
Development costs	😐	☹☹
Engineering resources/structure	☺	☹

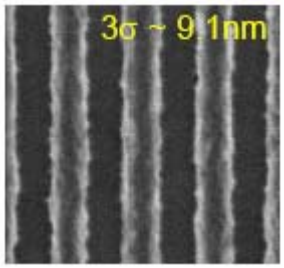
Records of 2006

- First > 1B Transistors Microprocessor
  - Intel: 1.328B transistors
- 1.25 GS/s, 4 bit flash A/D @ 2.5 mW in 90 nm CMOS
- 9 GHz Pentium Integer core @ 10.4 W
- 56 nm NAND flash technology (Toshiba)
- 25 Gbit/s CMOS Clock-Data-Recovery (IBM)

… with some difficulties ahead

- Significant challenges:
  - Power Dissipation
  - Troubles for Analog Designs
  - Device variability

LER



from IMEC

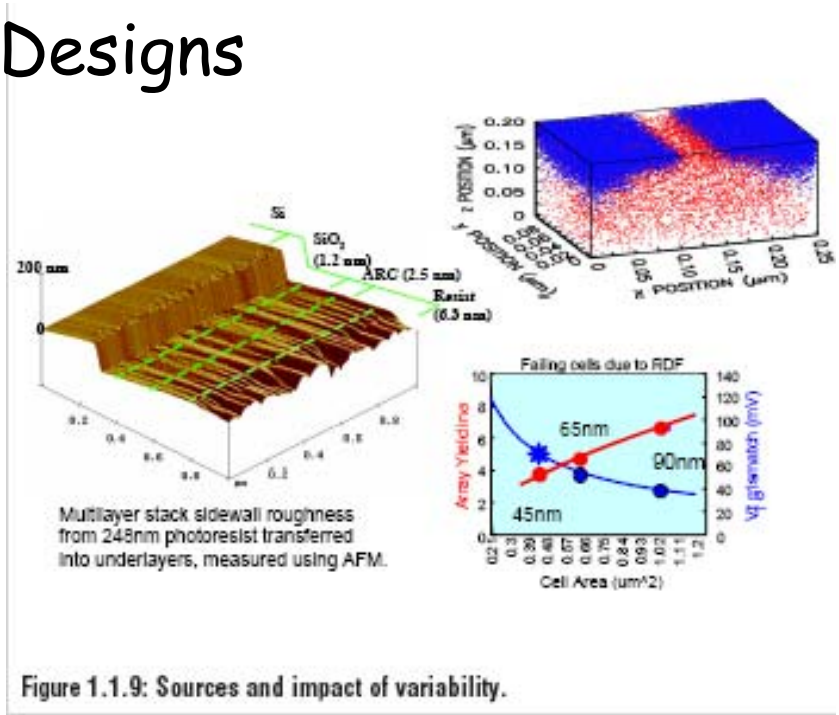
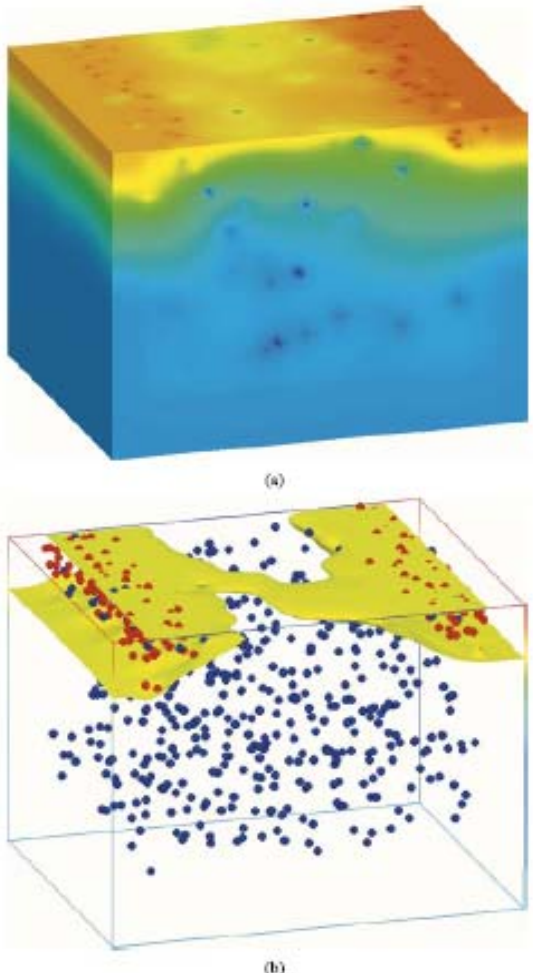


Figure 1.1.9: Sources and impact of variability.

Transistors becoming atomistic…



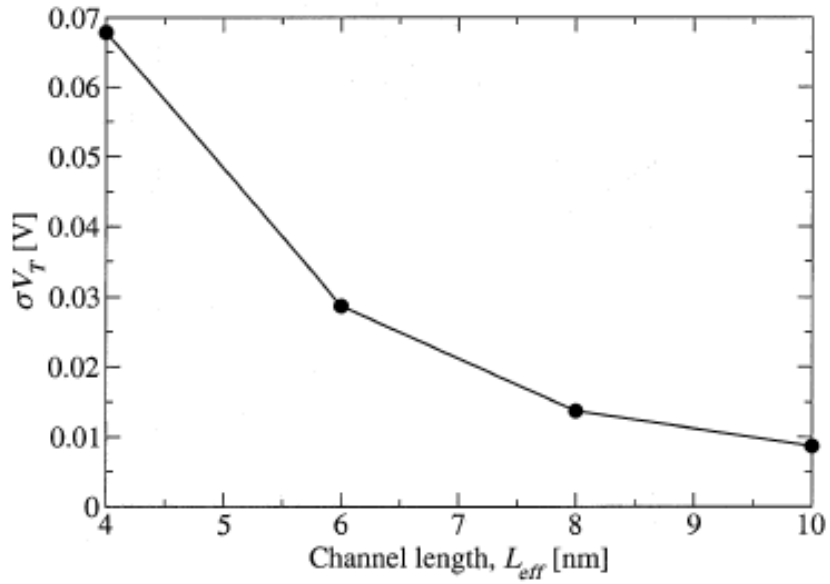


Fig. 9. Standard deviation in threshold voltage, σV_T, due to random discrete dopants in the source and drain of double gate MOSFETs with different channel lengths.

from: Asenov et al., Simulation of 50x50 nm MOS, from IEEE Trans on El. Dev.

… mean trouble for circuit designers

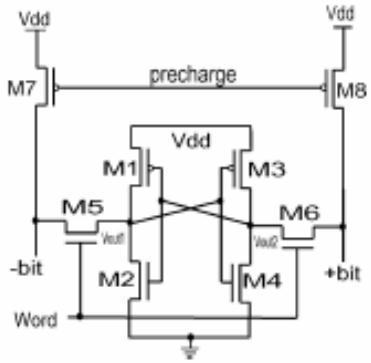


Fig. 8. Circuit schematics of CMOS SRAM.

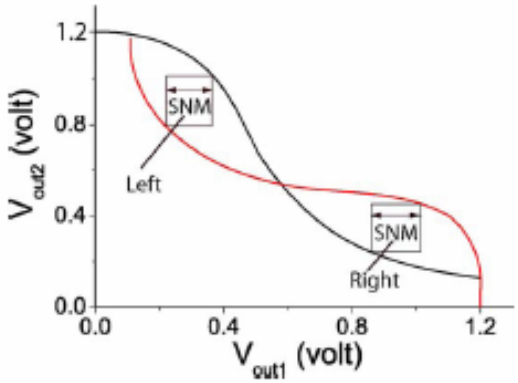
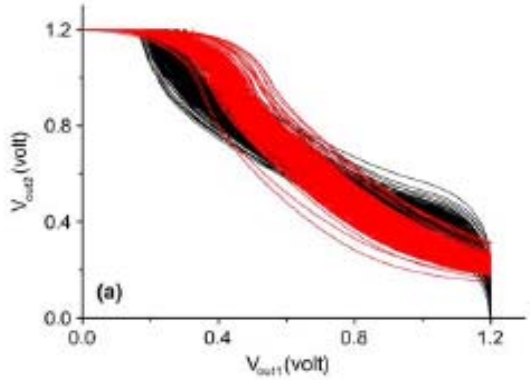


Fig. 9. The static transfer characteristics and SNM of a normal SRAM case.



from: B. Cheng et al. / Solid-State Electronics 49 (2005) 740–746

Comparing generations

Specifications	
Voltage	2.5 V
Lithography	0.25 µm
Nch L_{eff}	[illegible]
I_{Dsat}–Nch	595 µA/µm
Pch L_{eff}	[illegible]
I_{Dsat}–Pch	295 µA/µm
Levels of metal	2 - 5
M1, M2/M3 thickness	0.40, 0.54 µm
M1 pitch (uncontacted)	0.64 µm
Mx pitch (contacted)	0.80 µm
MT pitch (last, contacted)	0.80 µm

CMOS specifications (common to 130-nm technology platform)	
Lithography	130 nm
Voltage (V_{DD})	1.2 V or 1.5 V
Additional power supply options	2.5 V / 3.3 V I/O
Standard NFET / PFET	
L_{min}	0.12 µm
L_p	0.09 µm
V_{tsat}	[illegible] 0.300 V
I_{Dsat}	530 µA/µm / [illegible]10 µA/µm
I_{off}	[illegible] / 350 pA/µm
T_{ox}	2.2 nm
Thick-oxide NFET / PFET	
L_{min}	0.24 µm
L_p	0.21 µm
V_{tsat}	0.41 V / -0.44 V
I_{Dsat}	660 µA/µm / 260 µA/µm
I_{off}	10 pA/µm / 10 pA/µm
T_{ox}	5.2 nm

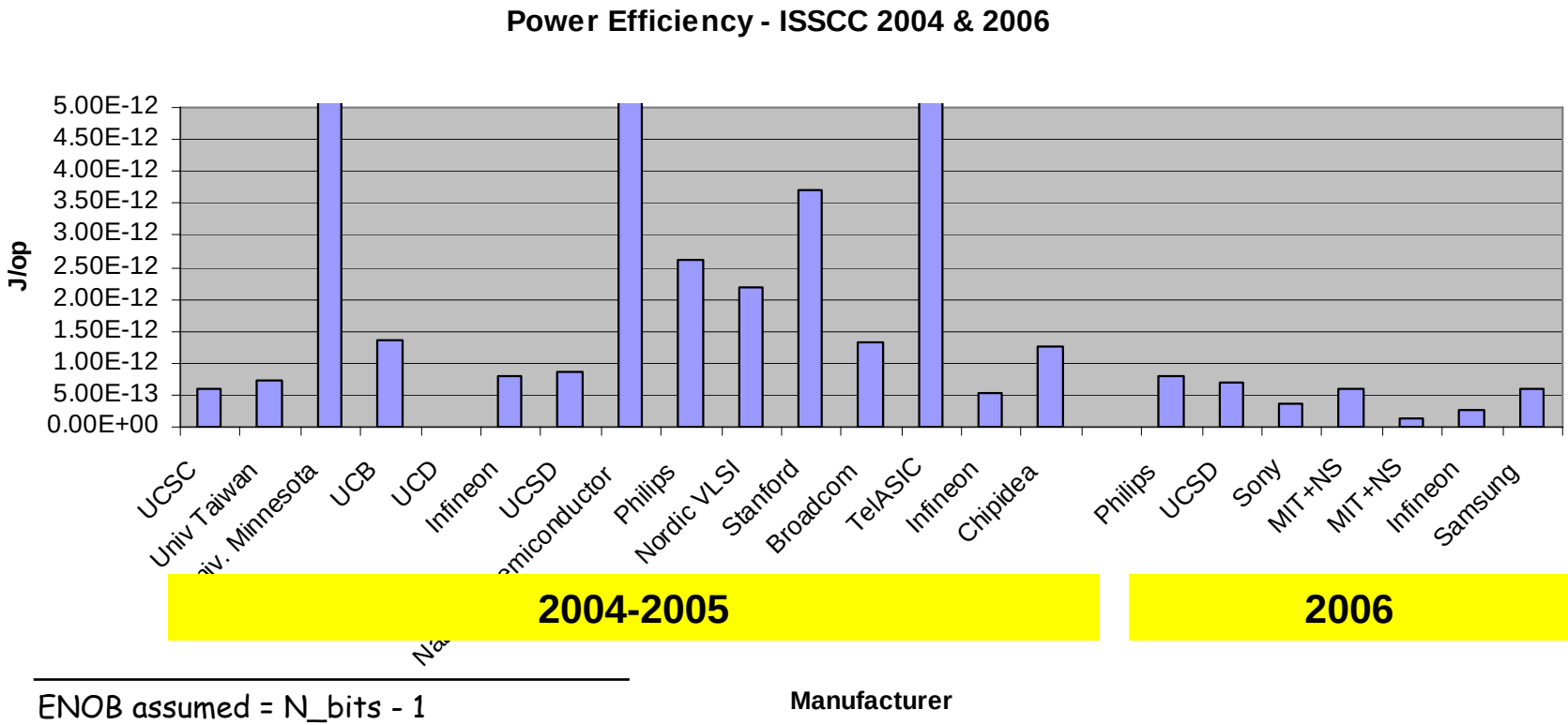
Show-stoppers for analog?

- # of papers @ISSCC2006 in different technologies:

	≤0.25μm	0.18 μm	0.13 μm	90 nm
UWB Transceivers	-	5	2	1
ADCs	-	4	2	2
RF & Channel Processing	2	2	3	1
Image Sensors	3	5	1	-

Technology Directions
Building blocks: ADCs

$$FM = \frac{Power}{Freq * 2^{\wedge} ENOB}$$



ENOB assumed = N_bits - 1

Architectural consequences:

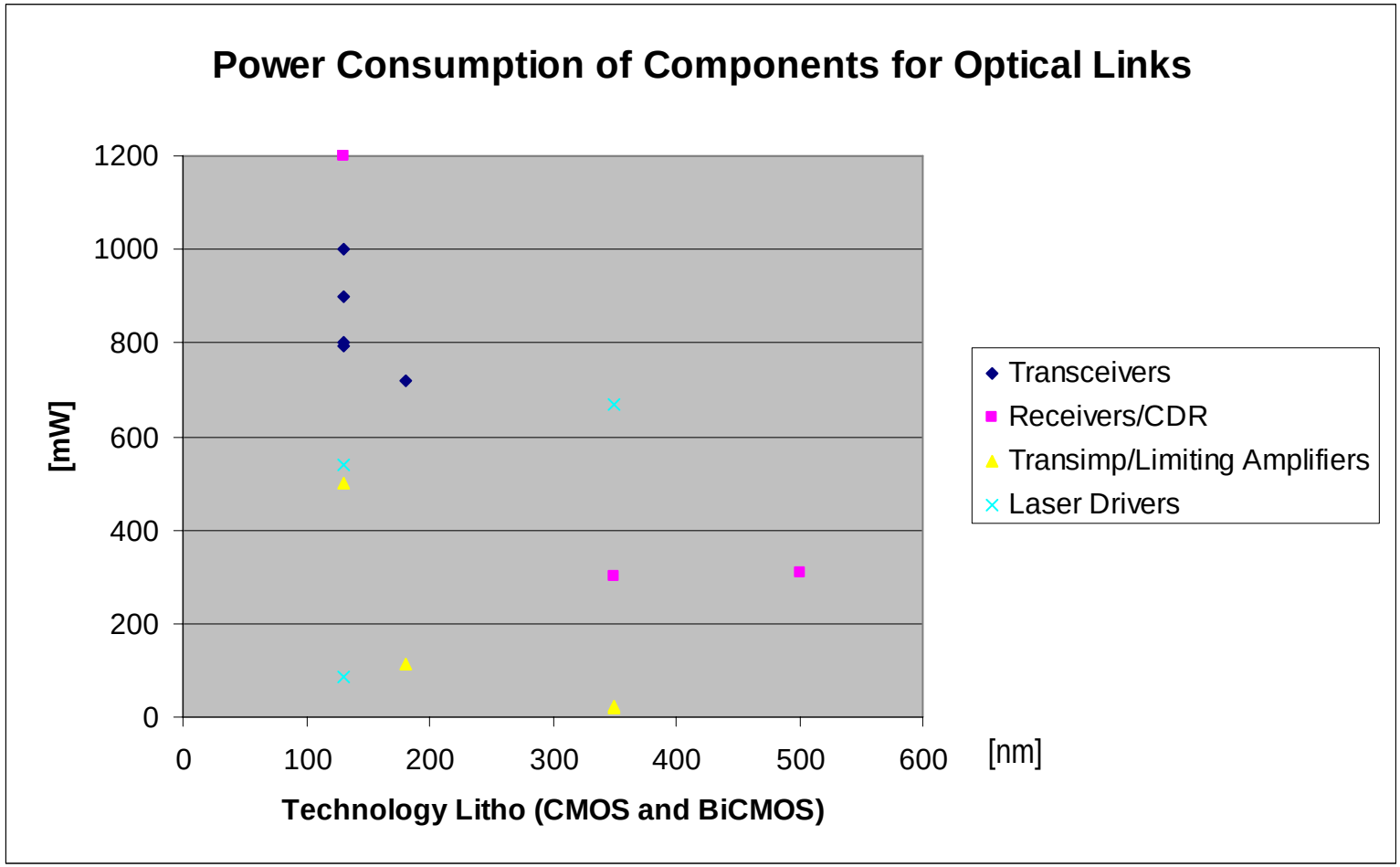
- TPC:
  - 10 M channels
  - 10 bit range (ENOB = 9 bits)
  - 20 MHz

P = 20.5 KW

- Tracker:
  - 100 M channels
  - 6 bit range (ENOB = 5 bits)
  - 50 MHz

P = 32 KW

Power required for Data Transmission



From ISSCC 2004-2006 Conference data

Example:
Current CMS Tracker

- Current Approx Data
  - 16,000 modules with 512 strips/module = 8.1 M strips,
    - 64,000 FE chips
    - 40,000 analog optical links
    - Total electrical power for links
      = 12mA/diode*2.5V*2*40,000 = 2.4 KW
    - Raw Data Rate = 40,000 ADC@40 MHz *1B/ADC=1.6 10^6 MB/sec
    - Actual Data Rate per FEchip
      = 1 B/ch * 128 ch * 100 KHz * 4% occ = 0.5 MB/(FEchip*sec)

Example:
Power for Optical Links for a SLHC tracker

- Assumptions
  - ◊ 10x Luminosity
    - ➢ 100 M strips (i.e. 10x)
    - ➢ 1 M FE chips
  - ◊ 1 W @ 10 Gbit/sec for full TX chip (i.e. 1 W @ 1 GB/sec)
  - ◊ 1 KW available
    - ➢ 1,000 Links @ 1W
    - ➢ raw transmission capacity 10^{12} B/sec
    - ➢ with ~ 1,000 FEchip/link
    - ➢ … or 1 MB/(FEchip*sec)
  - ◊ Multiplexing 1000:1 may not be all that easy

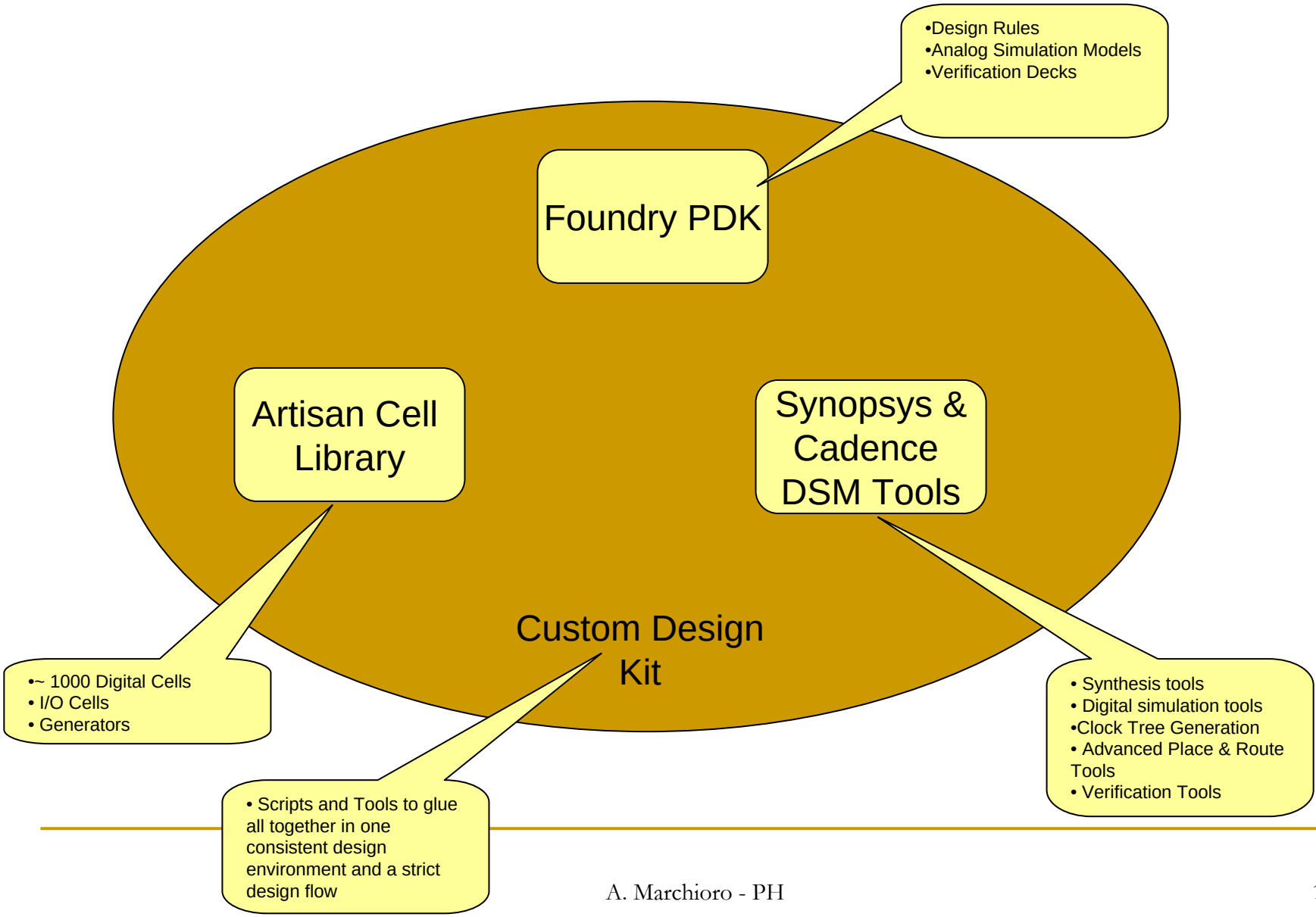
Availability and access of new 130nm

- Technologies
- Design tools
- MPW runs

Technologies

- 130 nm "base" technology with RF extensions from 2006
  - 6 metals standard, option to 8 available
  - 90 nm contract will be in place at the same time
  - Future technologies can be negotiated with the same manufacturer once the necessity will arise
- BiCMOS option is included today
  - Validation studies to be started

Technology Design Assistance Package



Tools

- 130 nm available through CERN contract to every HEP Institutes for 2,000 €/year
  - We expect that "normal" Cadence licenses are available in each Institute
  - Commercial Digital Library from Artisan-ARM available for free for download (library is paid by submitted wafers at production time)
  - A service for advanced P&R and design verification can be organized at CERN if enough demand present

MPW Runs

- CERN MIC group has organized 16 MPW runs since 2000 in $\frac{1}{4}$ micron
  - Each run had up to 20 participants
  - Easily delivered several hundred chips/run
  - Smooth transition to production runs
  - Encourage and support the organization of shared production runs for modest volumes

MPW runs in 130 nm

- Community needs to collect about 3/4 designs of 5x5 mm2 or larger to be competitive with commercial MPW services
  - Advantages:
    - Short turn-around time
    - Many more parts
    - Flexibility in submission date
    - Technology's "quality" monitoring is guaranteed

Perspective

- 20 years ago chips such as:
  - Pixels for Atlas, CMS, LHCb and Alice
  - Altro for Alice
  - GOL, TTCrx
  - ADCs for CMS ecal
  - or 32 channels TDC with 10 ps resolution

  were unthinkable
- Technology is there, still (from a system perspective) plenty of exciting work to do in area of:
  - Power optimization and cooling
  - Packaging
  - System integration
  - Transfer of prototypes to production

Conclusions

- "Time constants" of microelectronics industry and HEP are vastly different
  - Instrumentation and detectors can be greatly enhanced by using modern microelectronic technologies
  - … at the cost of keeping an appropriate level of investment even during the long inter-generational periods alive
- Technologies and tools for ILC and SLHC are indisputably there
  - HEP internal organization should be adjusted to the challenges ahead as to avoid some of the mistakes done in the past