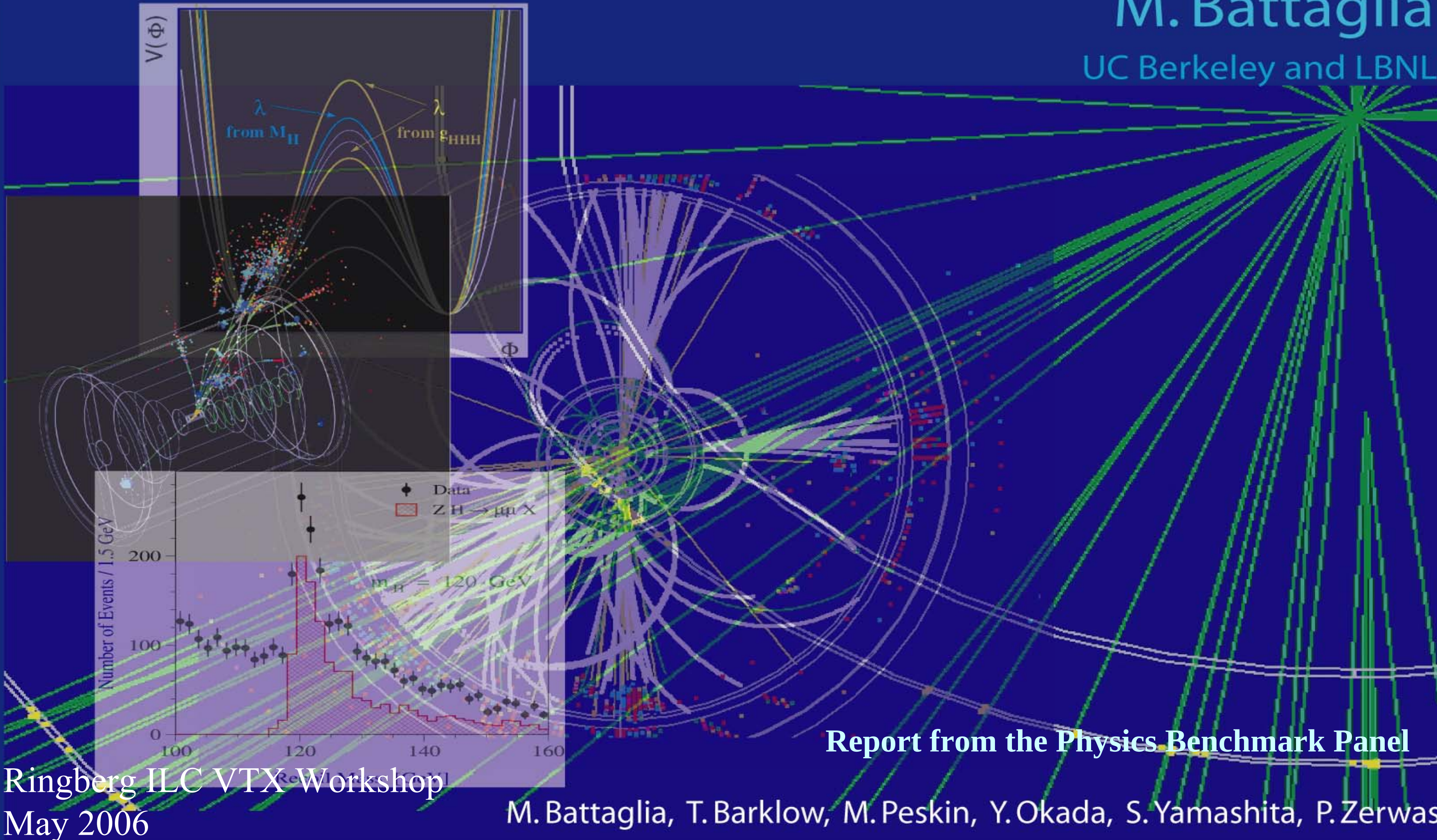
Summary of Ringberg Vertex Detector Workshop

- Physics Requirements/ Benchmarks
- Detector Concepts
- Mechanical Structure and Integration
- ILC Environment
- Pixel Technologies

Benchmarking the ILC Detectors

M. Battaglia
UC Berkeley and LBNL



Report from the Physics Benchmark Panel

M. Battaglia, T. Barklow, M. Peskin, Y. Okada, S. Yamashita, P. Zerwas

Ringberg ILC VTX Workshop
May 2006

Charge to the Benchmark Panel from the World Wide Study

Detector concept studies for ILC are now moving from basic concepts to optimization of detector parameters. The **aim of the benchmark panel is to aid this process by proposing a minimum set of physics modes that cover capabilities of detector performance** such as vertexing, tracking, calorimetries, muon system, machine-detector interface, and overall issues of particle flow and hermeticity, such **that concept studies can use these modes to evaluate and optimize given detector designs**. For such evaluations to be effective, benchmark panel may suggest important backgrounds to be taken into account and other assumptions used in evaluating the benchmark modes. The **panel is to submit to WWS a document that contains the information as stated above by the beginning of July**. The document will be made available to concept studies and wider linear collider communities by appropriate means.

arXiv:hep-ex/0603010 v1 6 Mar 2006

Report to the ILC World-wide Study

Physics Benchmarks for the ILC Detectors

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This note presents a list of physics processes for benchmarking the performance of proposed ILC detectors. This list gives broad coverage of the required physics capabilities of the ILC experiments and suggests target accuracies to be achieved. A reduced list of reactions, which capture within a very economical set the main challenges put by the ILC physics program, is suggested for the early stage of benchmarking of the detector concepts.

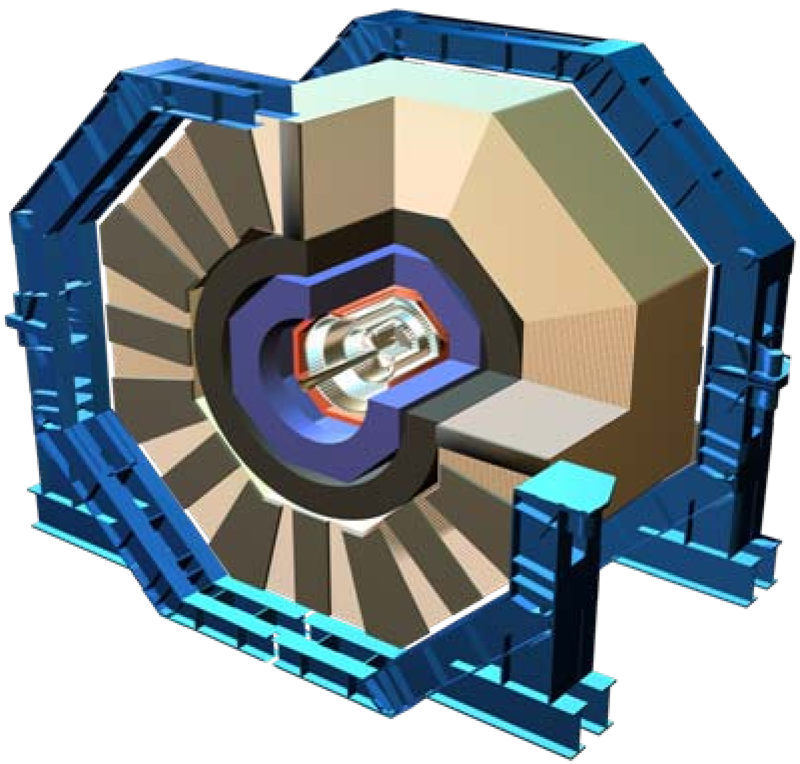
Benchmark panel report sent to WWS and Detector Concepts contacts
to appear on the LCWS05 proceedings and available as arXiv:**hep-ex/0603010**

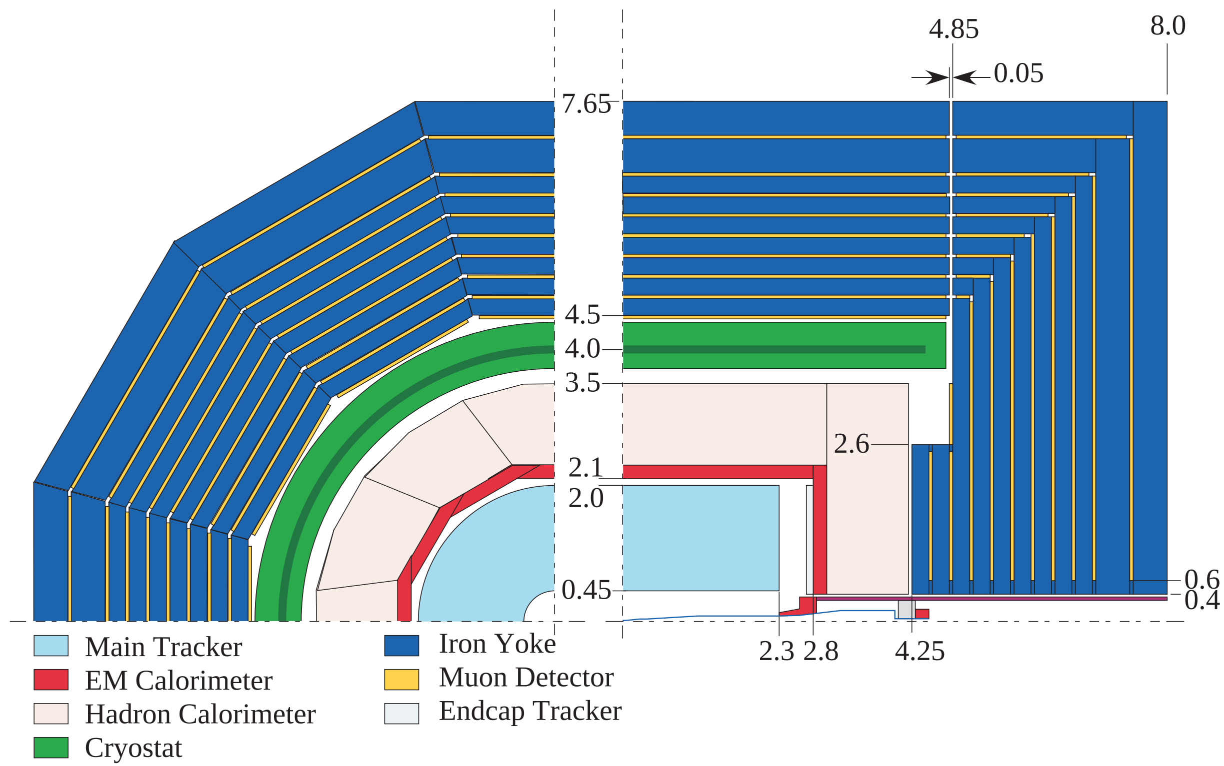
Physics Benchmarks - Detector Performance Matrix

Process	Vertex	Tracking		Calorimetry		Fwd		Very Fwd	Integration					Pol.
	σ_{IP}	$\delta p/p^2$	ϵ	δE	$\delta\theta,\ \delta\phi$	Trk	Cal	θ^e_{min}	δE_{jet}	M_{jj}	ℓ-Id	V^0-Id	$Q_{jet/vtx}$	
$ee \to Zh \to \ell\ell X$		x									x			
$ee \to Zh \to jjbb$	x	x	x			x				x	x			
$ee \to Zh, h \to bb/cc/\tau\tau$	x		x							x	x			
$ee \to Zh, h \to WW$	x		x		x				x	x	x			
$ee \to Zh,\ h \to \mu\mu$	x	x									x			
$ee \to Zh,\ h \to \gamma\gamma$				x	x		x							
$ee \to Zh, h \to invisible$			x			x	x							
$ee \to \nu\nu h$	x	x	x	x			x			x	x			
$ee \to tth$	x	x	x	x	x		x	x	x		x			
$ee \to Zhh,\ \nu\nu hh$	x	x	x	x	x	x	x		x	x	x	x	x	x
$ee \to WW$										x			x	
$ee \to \nu\nu WW/ZZ$						x	x		x	x	x			
$ee \to \tilde{e}_R\tilde{e}_R$ (Point 1)		x						x			x			x
$ee \to \tilde{\tau}_1\tilde{\tau}_1$	x	x						x						
$ee \to \tilde{t}_1\tilde{t}_1$	x	x							x	x		x		
$ee \to \tilde{\tau}_1\tilde{\tau}_1$ (Point 3)	x	x			x	x	x	x	x					
$ee \to \tilde{\chi}^0_2\tilde{\chi}^0_3$ (Point 5)									x	x				
$ee \to HA \to bbbb$	x	x								x	x			
$ee \to \tilde{\tau}_1\tilde{\tau}_1$			x											
$\chi^0_1 \to \gamma + \not{E}$					x									
$\tilde{\chi}^\pm_1 \to \tilde{\chi}^0_1 + \pi^\pm_{soft}$			x					x						
$ee \to tt \to 6\ jets$	x		x						x	x	x			
$ee \to ff\ [e, \mu, \tau; b, c]$	x		x				x		x		x		x	x
$ee \to \gamma G$ (ADD)				x	x			x						x
$ee \to KK \to f\bar{f}$		x									x			
$ee \to ee_{fwd}$						x	x	x						
$ee \to Z\gamma$		x		x	x	x	x							

Vertex detector in the SiD, LDC and GLD concepts

- SiD – Bill Cooper
- LDC – Sonja Hillert
- GLD – Yasuhiro Sugimoto



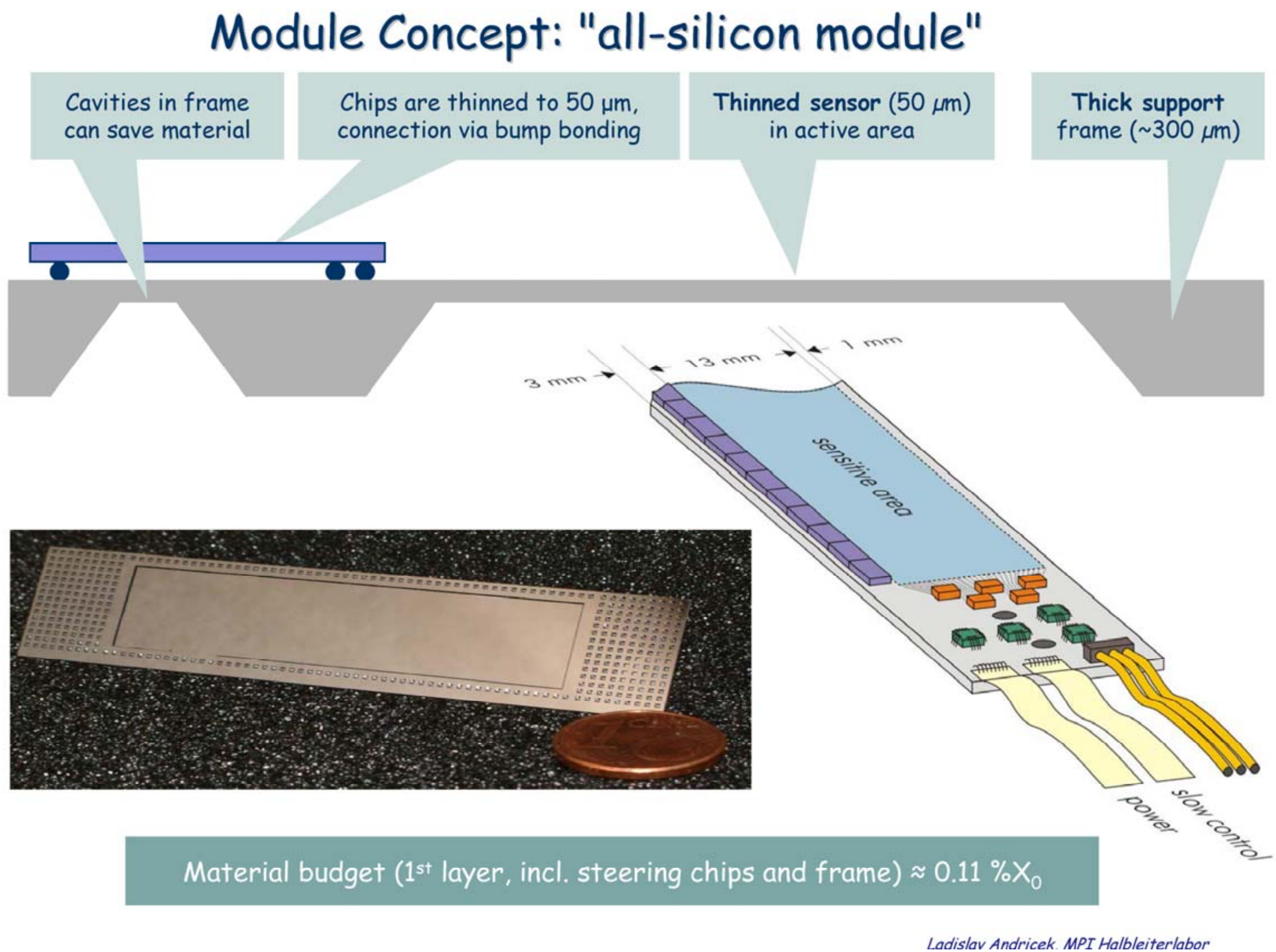


Vertex Detector Mechanics

- Bill Cooper.
- Overall approach to mechanical support and cooling developed in conjunction with SiD.
- Cooling with forced flow of dry gas has been assumed.
- Support structures studied rely heavily on the use of carbon fiber laminate.
- Offers a high stiffness x radiation length product.

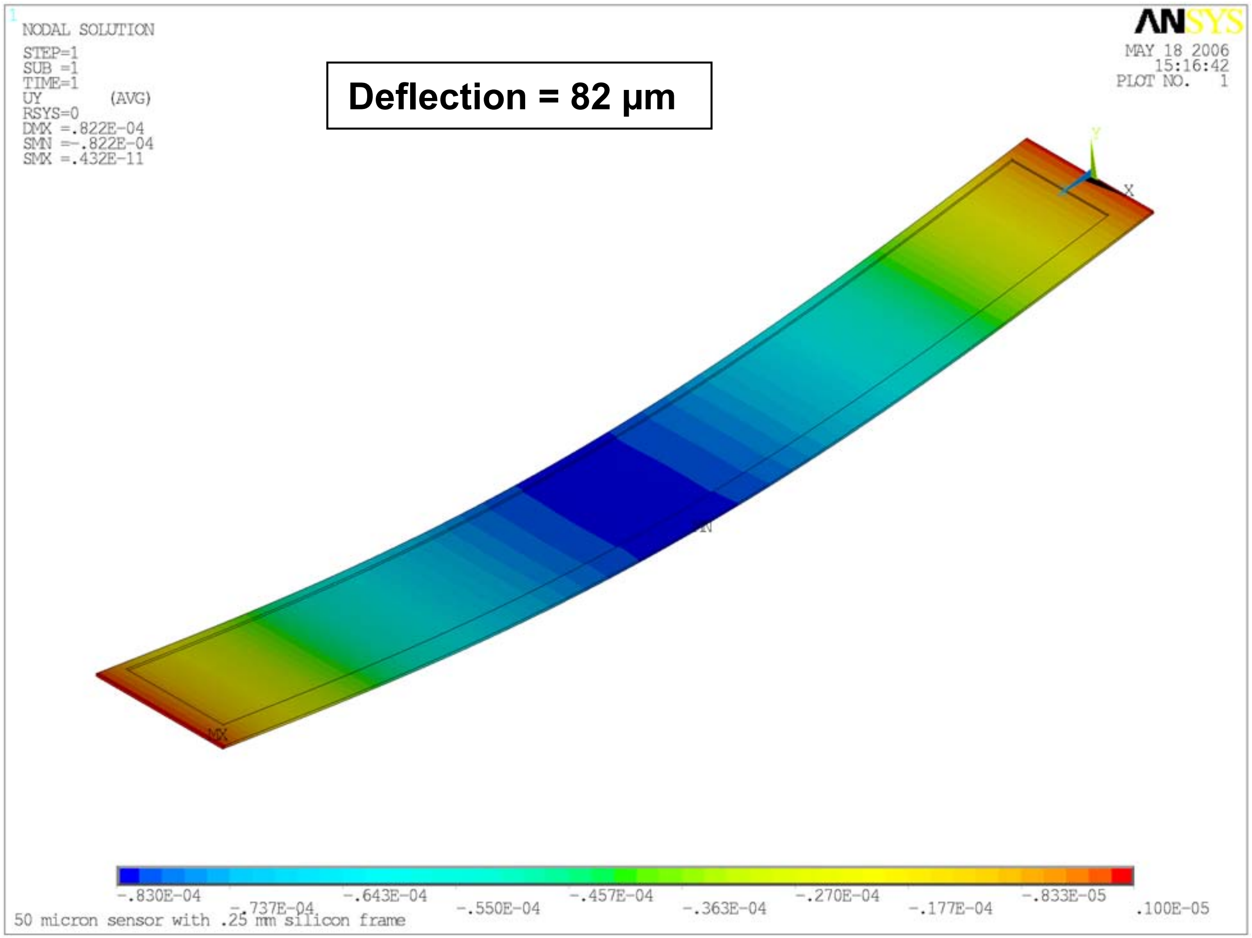
Material	Silicon	Beryllium	CF	¼ CF
Density (g/cm^3)	2.33	1.848	1.56	0.39
Elastic modulus (GPa)	131	290	228	57
Radiation length average (cm)	9.37	35.43	24	96
Relative deflection	1	0.36	0.38	0.38
Relative number of radiation lengths (average)	1	0.26	0.39	0.10
CTE (ppm/^{o}C)	2.6	11.6	-0.6	-0.6

Studies of DEPFET ladder concept



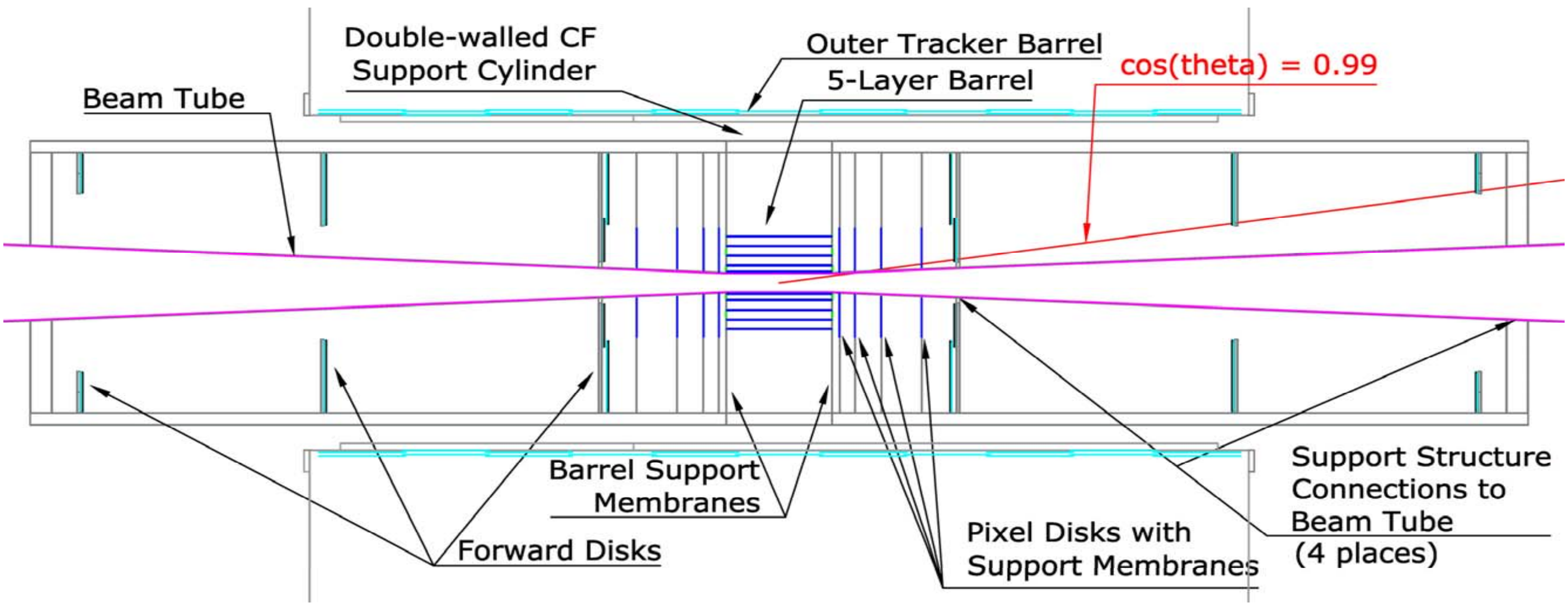
Studies of DEPFET ladder concept

- FEA: need for additional support demonstrated.



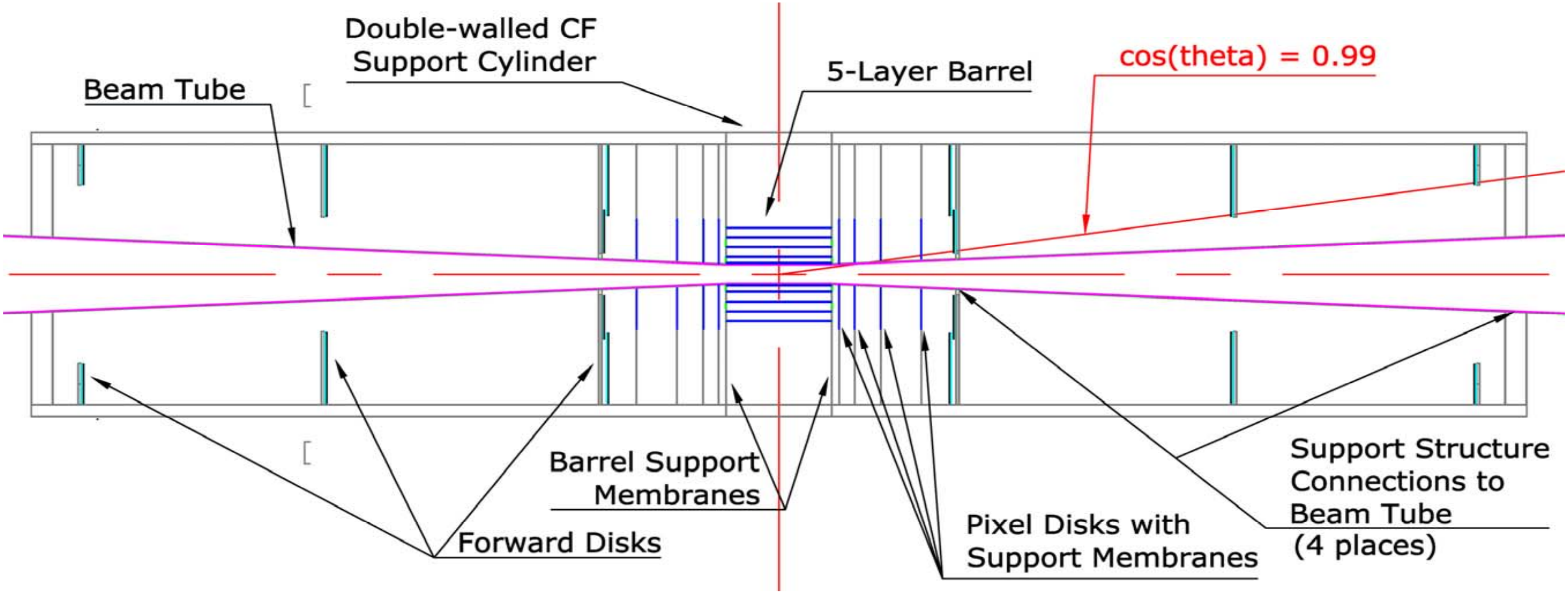
SiD VXD Elevation View

- 5-layer pixel barrel: Z = ±62.5 mm; 14 mm < R < 61 mm
- 4 pixel disks per end: Z = ± 72, ± 92, ± 123, ± 172 mm; R < 71 mm
- 3 forward disks per end: Z = ± 208, ± 542, ± 833 mm; R < 166 mm
  - Could be pixels or pairs of micro-strips
- Coverage extends to cos(theta) = ± 0.99.



SiD VXD Elevation View

- Outer split cylinders couple to the beam tube at Z = ± 214 and ± 882 mm, are supported by the beam tube, and stiffen it.
- High modulus CF has been assumed for most support structures.
  - Typical thickness, 0.26 mm, assumes 4 layers of pre-preg.
  - In many places, average thickness can be substantially reduced by cutting holes.
- CF membranes support the barrel and disks.



SiD Mechanical Summary

- Initial FEA model developed for barrel sensor structures.
  - Gravitational deflections for 125 mm barrel sensors are small.
  - Deflection of a single-material ladder with simple support at its ends is noticeably larger.
- We have begun to re-examine beam pipe deflections and the outer vertex detector support cylinder.
  - Changes could result.
- An initial study suggests that approximately 20 watts can be removed from the barrel, and 50 watts from the entire vertex detector, by air cooling with laminar flow.
- The number of radiation lengths represented by VXD structures has been reduced considerably.

Studies of silicon ladders

- Joel Goldstein

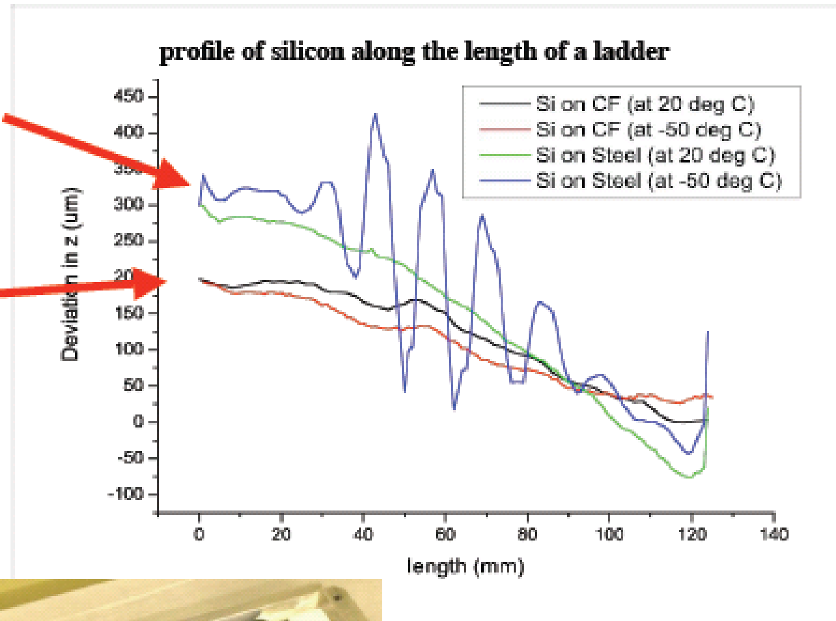
Target of ~0.1% X_0 per layer

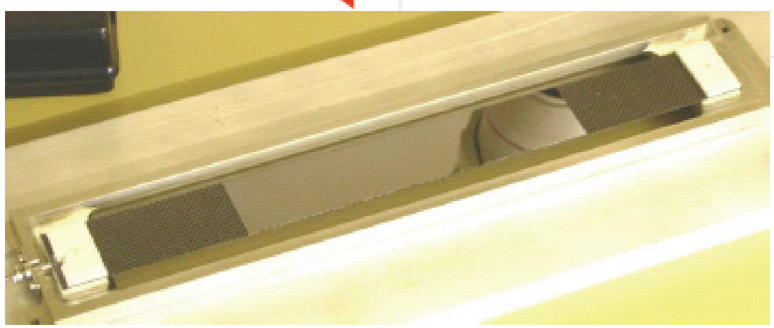
(100μm silicon equivalent)

1. **Unsupported Silicon**
   - Longitudinal tensioning provides stiffness
   - No lateral stability
   - Not believed to be promising
2. **Thin Substrates**
   - Detector thinned to epitaxial layer (20μm)
   - Silicon glued to low mass substrate for lateral stability
   - Longitudinal stiffness still from tension
3. **Rigid Structures**
   - No tensioning required

Thin substrates

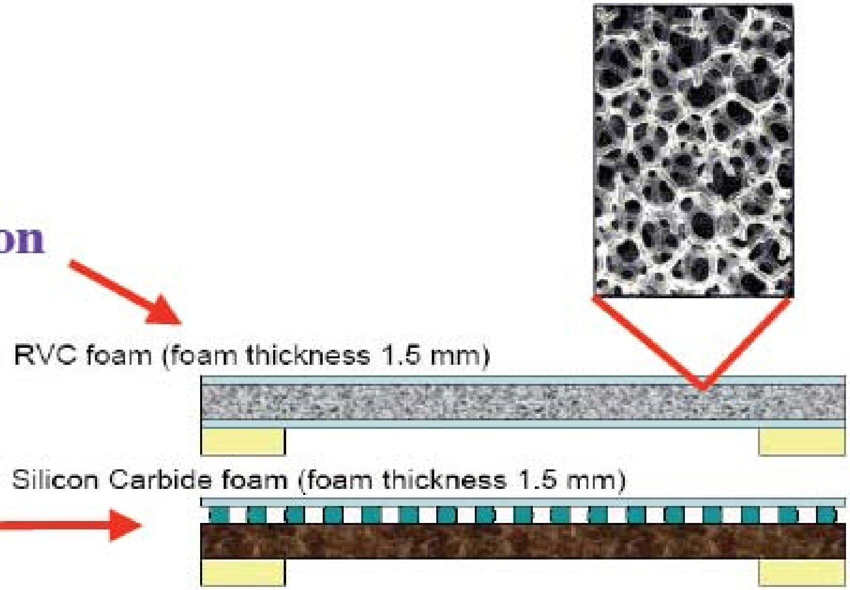
- **Beryllium**
  - **CTE mismatch too large**
- **Carbon fibre**
  - **0.09% X_0 prototype**
- **Ceramics**
  - **Fragile**





Rigid structure - foams

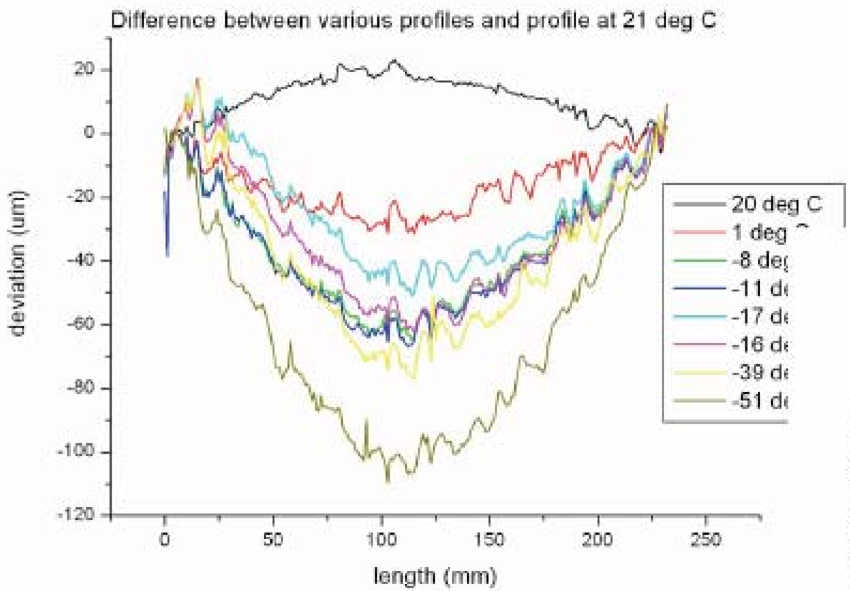
- **3% RVC Sandwich**
  - **0.09% X_0**
  - **Working on glue application**
- **8% Silicon Carbide**
  - **0.14% X0**
  - **3-4% believed possible**



20 μm silicon

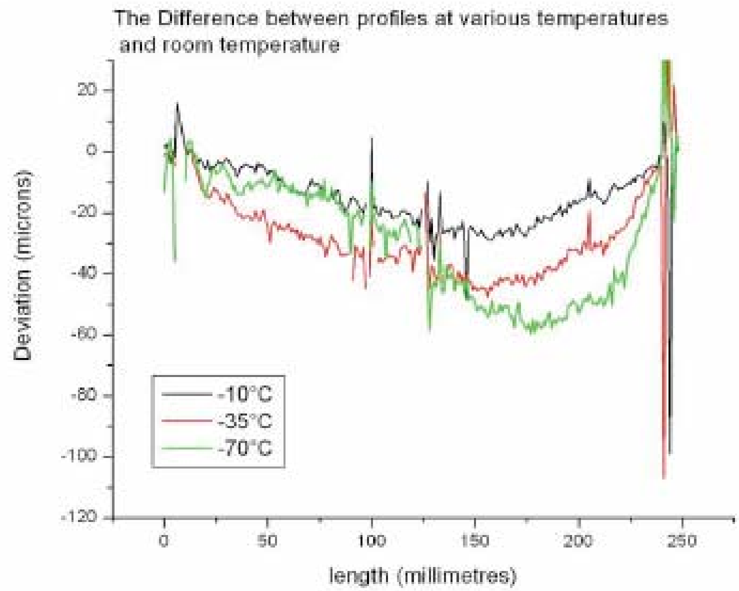
1.5 mm silicon carbide

SiC foam results



Thin glue layer

Glue "pillars"



Pair background

Adrian Vogel

Background at the ILC

e^+e^- pairs are a main source of background

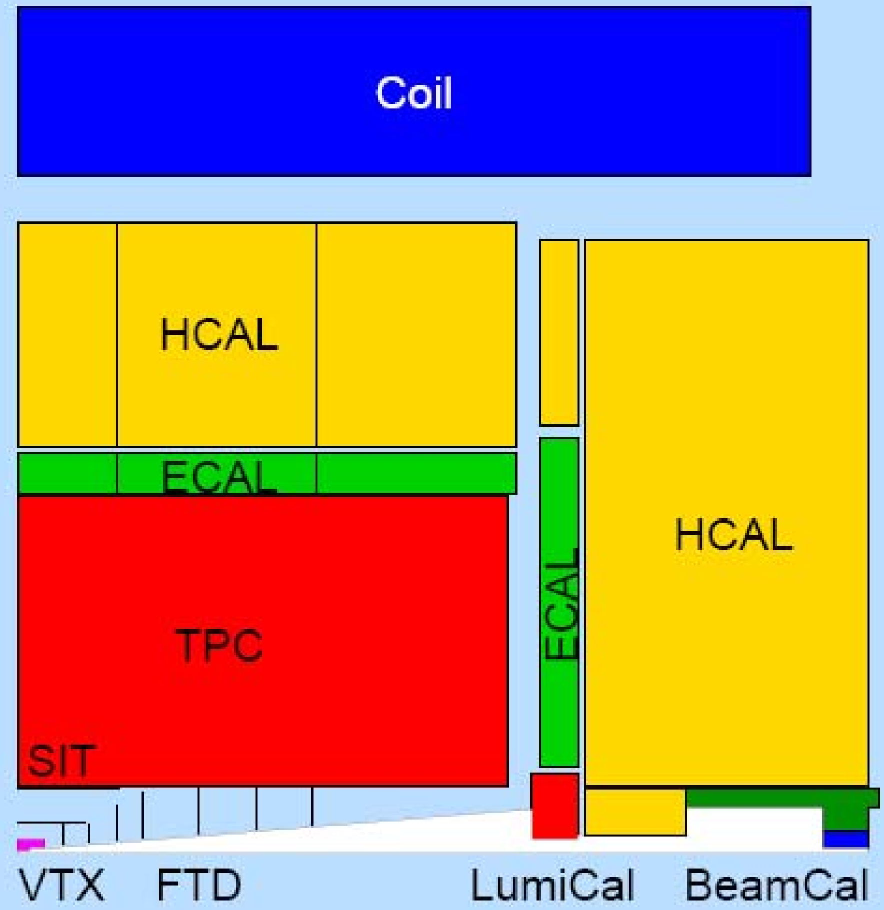
- created through beam-beam interaction
- crash into forward calorimeters (BeamCal) and magnets of the beam delivery / extraction line
- create neutrons, photons, and charged particles

Different kinds of impact on the detector

- direct hits from primary e^+e^-
- indirect hits from backscattered secondaries
- radiation damage from particle fluence (esp. neutrons)

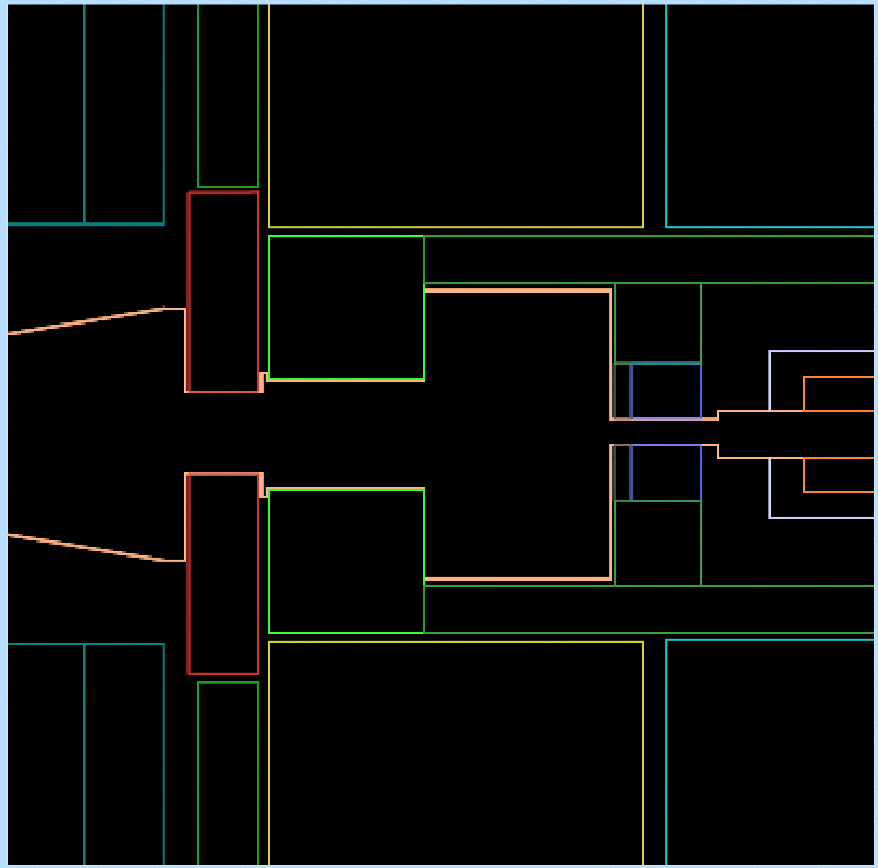
"Small" LDC detector considered

- Coil and TPC have been shortened
- ECAL and LumiCal have been pulled towards the IP
- FF at $L^* = 4.05$ m remains unchanged
- BeamCal stays where it was
- New layout of the forward region



Forward region – 2 mrad

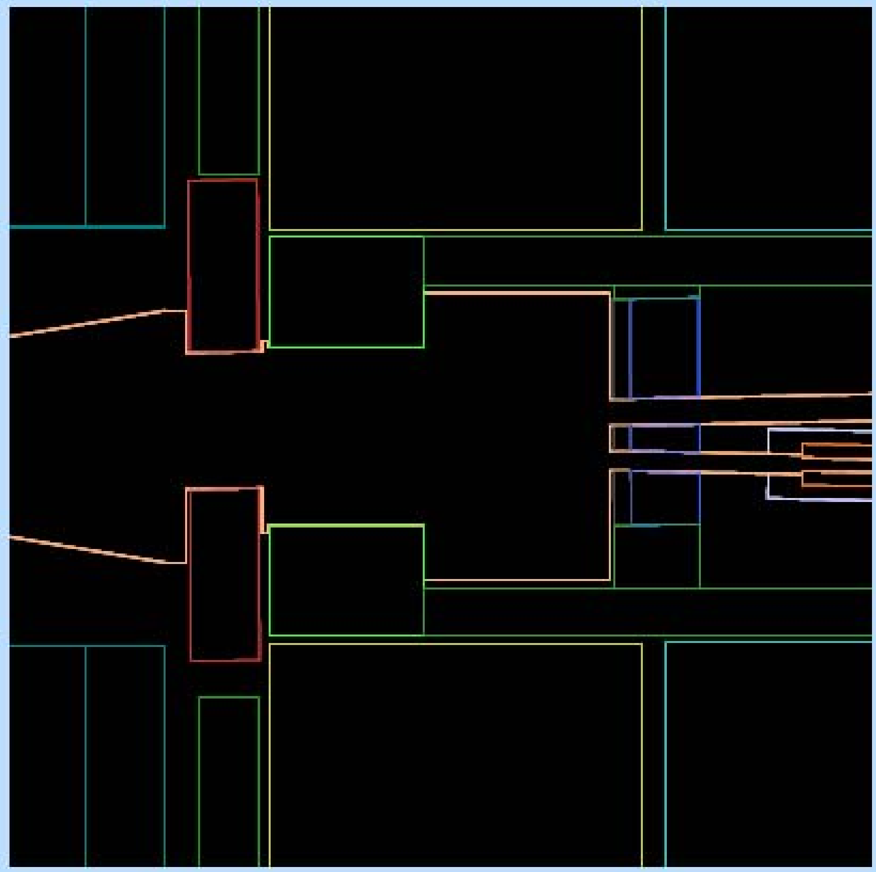
- LumiCal (red)
  R_i = 80 mm
- Low-*Z* absorber
- BeamCal (blue)
  R_i = 20 mm
- Centered on the downstream axis
- No DID field



Compressed view 1:2

Forward region – 20 mrad

- LumiCal (red)
  R_i = 120 mm
- Low-*Z* absorber
- BeamCal (blue)
  $R_{i\,1}$ = 15 mm
  $R_{i\,2}$ = 20 mm
- Centered on the downstream axis
- 20 mrad DID field

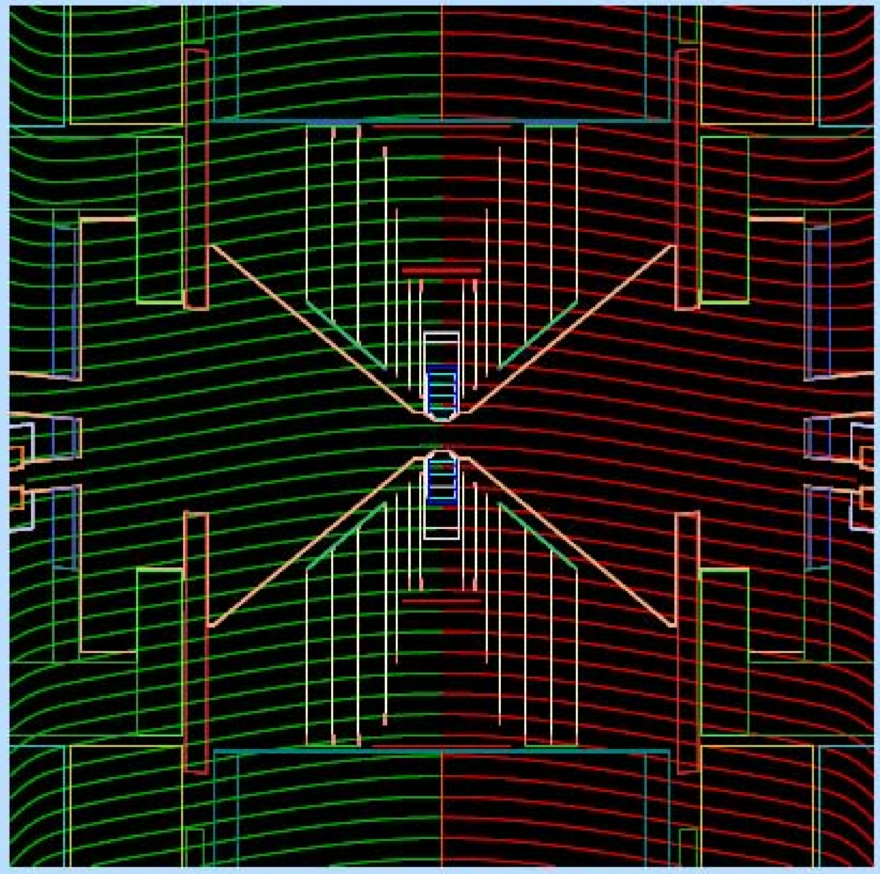


Compressed view 1:2

Detector Integrated Dipole

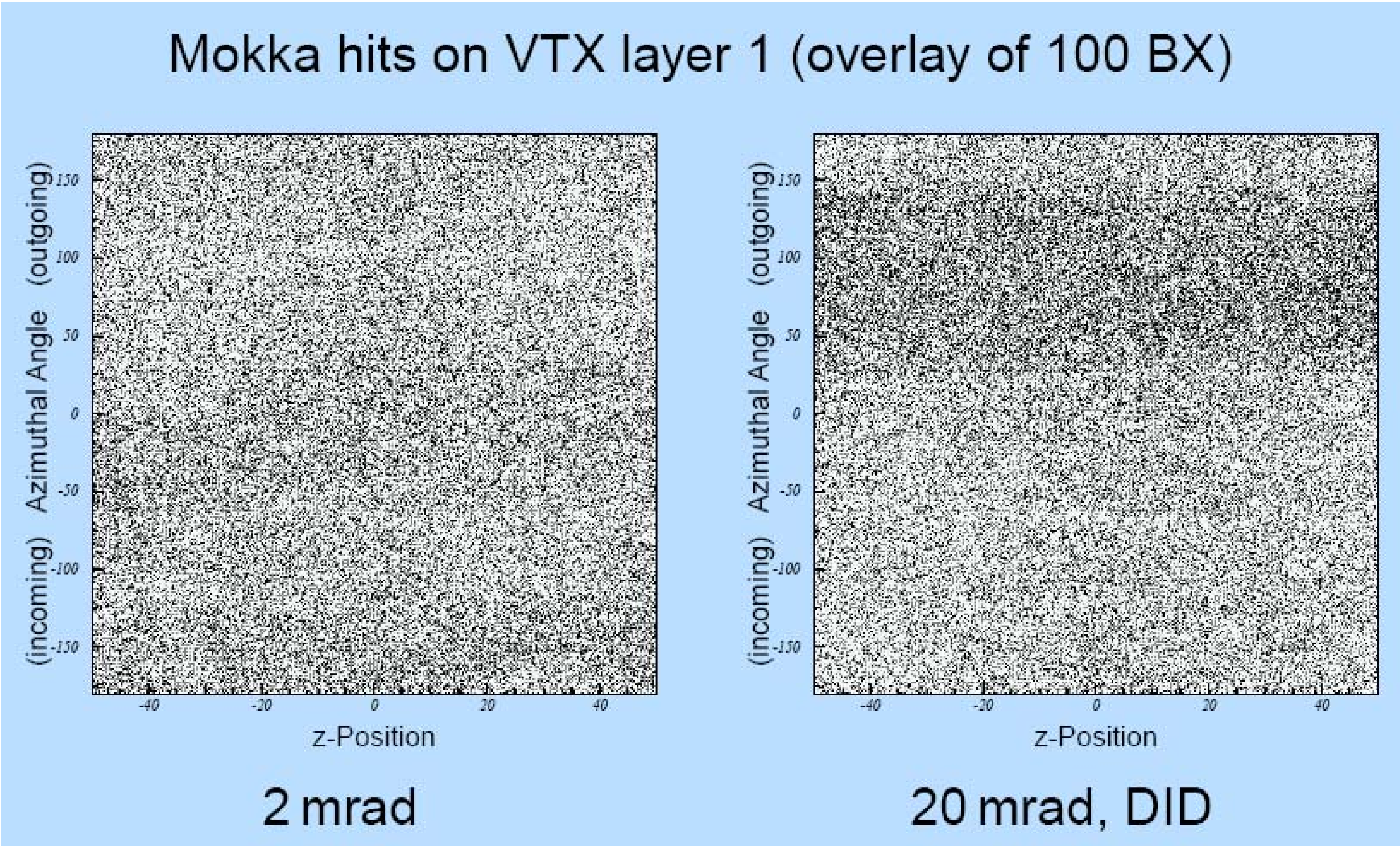
- Superimposed on the main solenoid field
- Introduced to prevent spin precession
- But has also a major impact on background

- Low-energy particles follow the field lines
- Tracks can be shifted in the *x*-direction



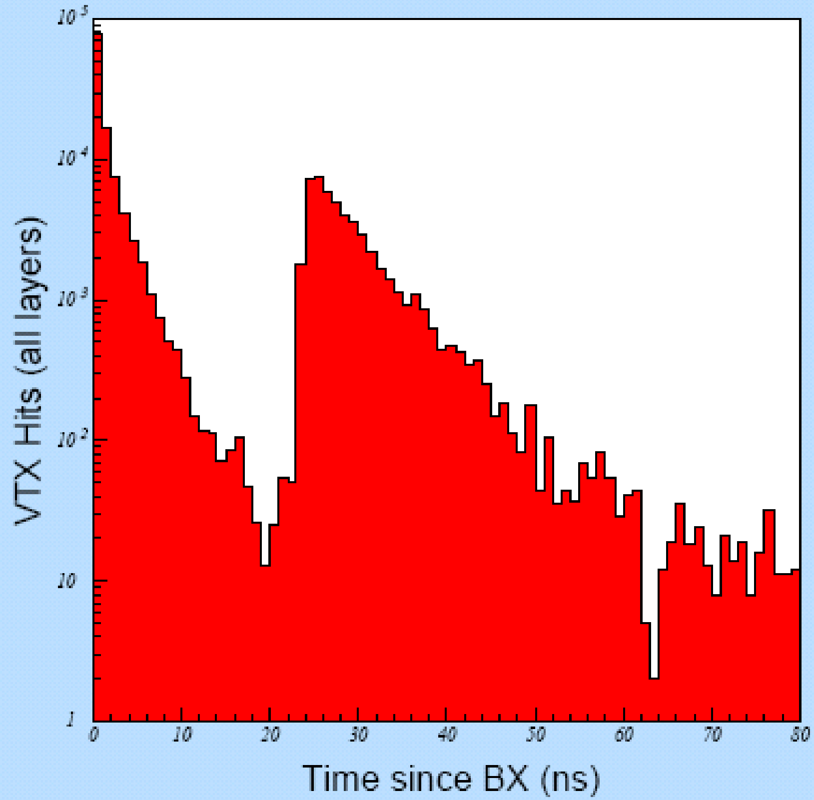
Compressed view 1:10

Hits on VXD


Mokka hits on VTX layer 1 (overlay of 100 BX)
(incoming) Azimuthal Angle (outgoing)
150
100
50
0
-50
-100
-150
-40
-20
0
20
40
z-Position
2 mrad
(incoming) Azimuthal Angle (outgoing)
150
100
50
0
-50
-100
-150
-40
-20
0
20
40
z-Position
20 mrad, DID

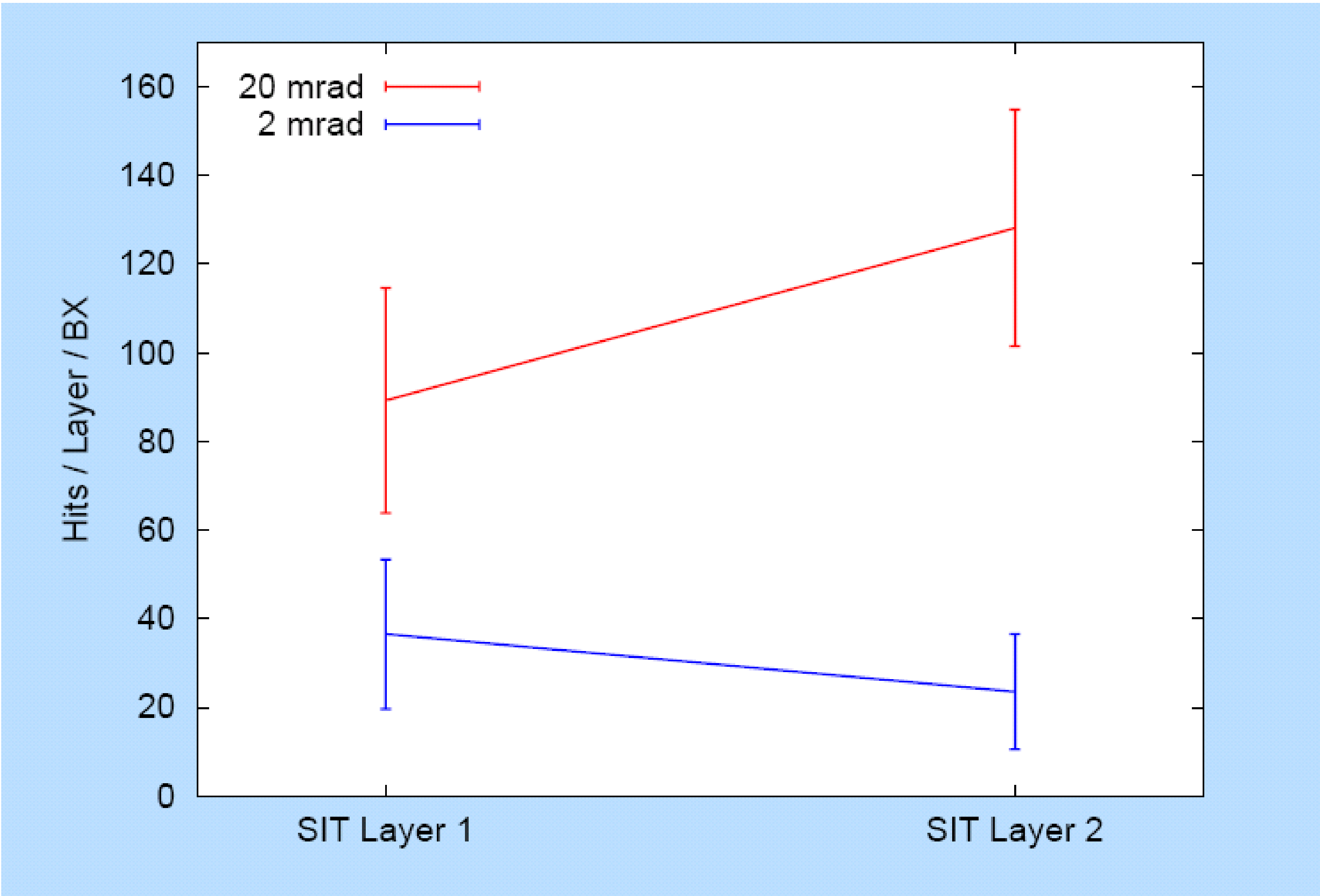
Time structure of VXD background hits

- Clear separation between direct hits and backscattered particles
- $t \approx 23\,\text{ns}$ corresponds to a distance of 7.0 m (3.5 m in each direction)
- Most backscatterers come from the BeamCal



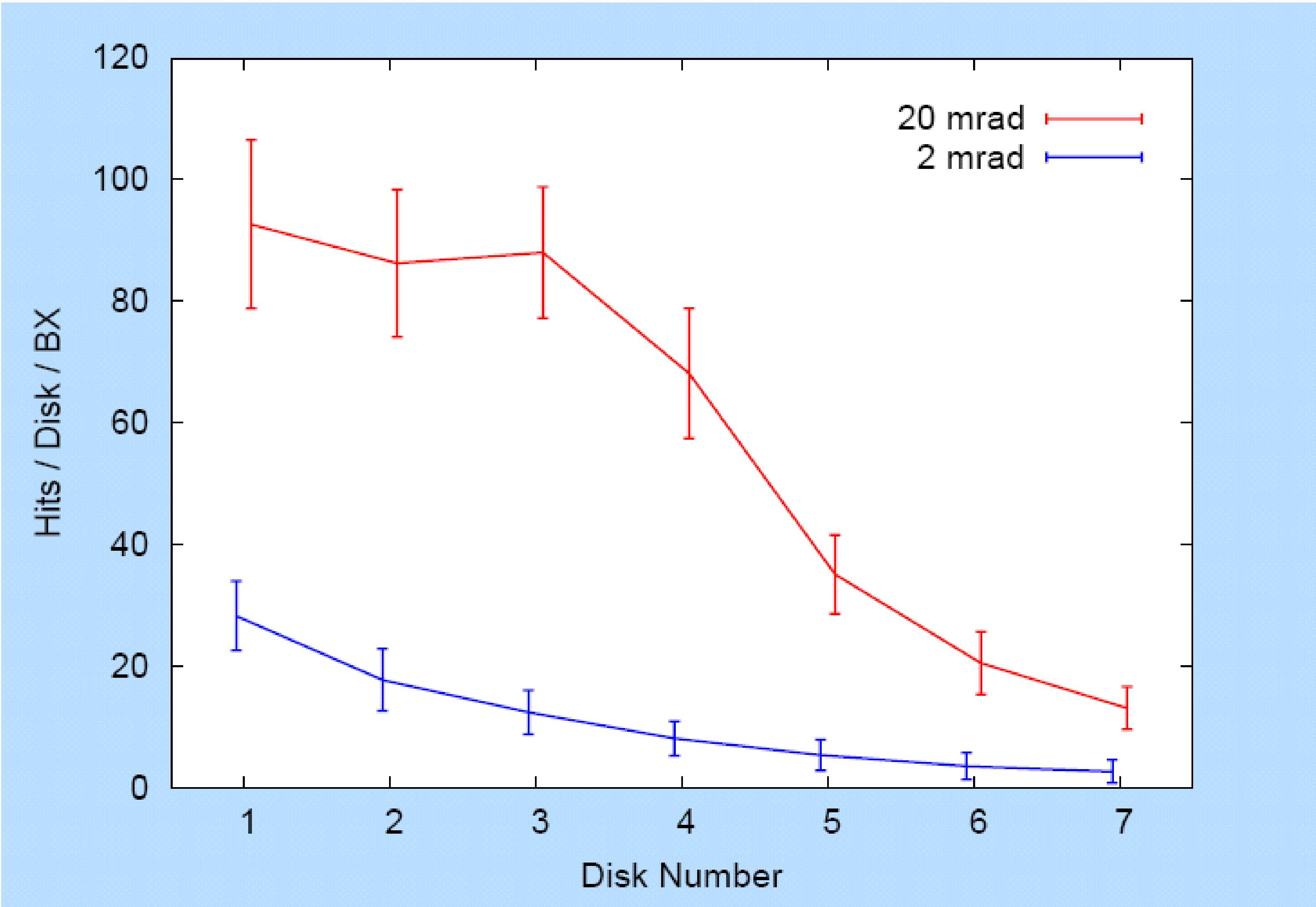
Structures for 2 mrad and 20 mrad look similar

SIT hits



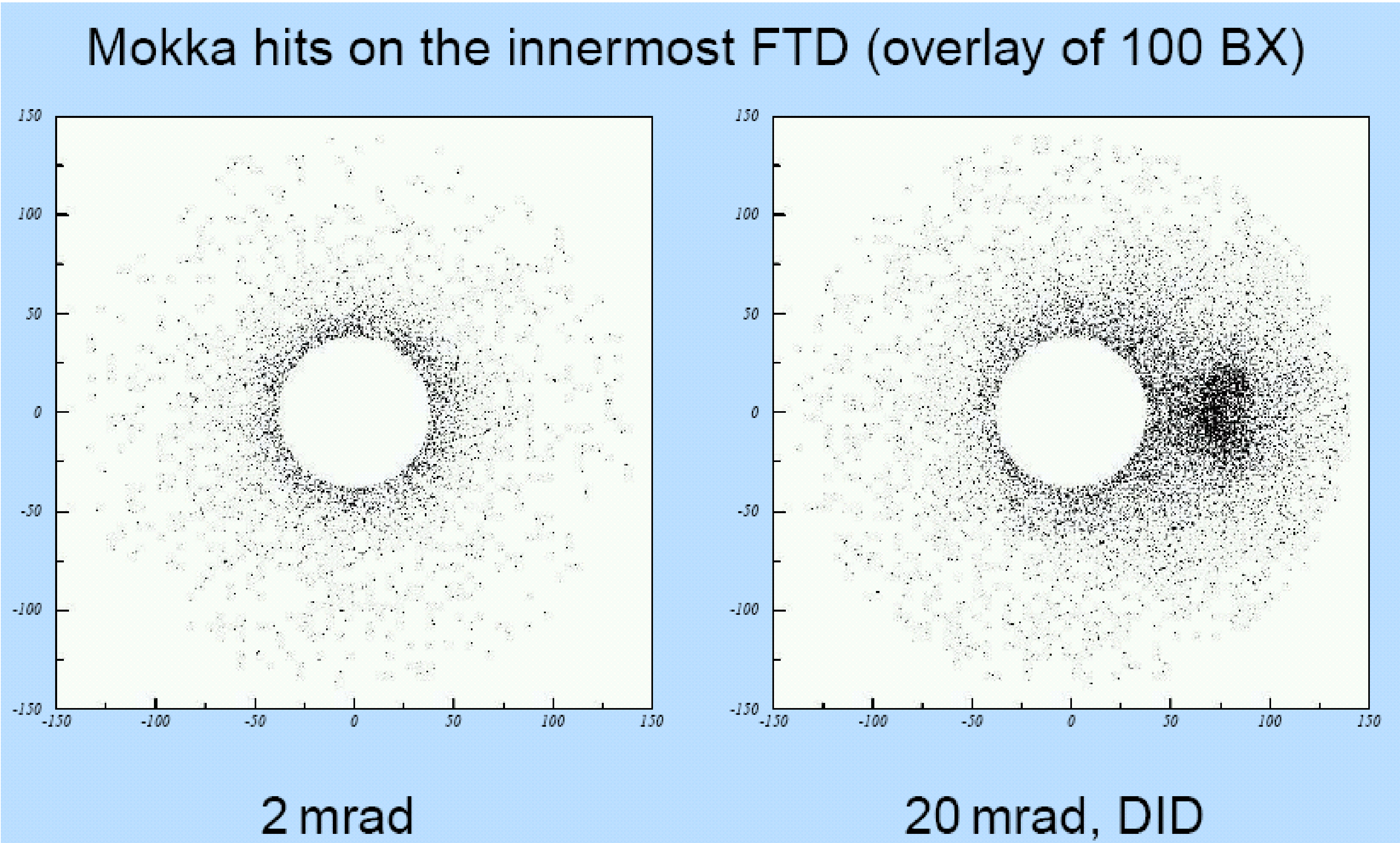
Hits / Layer / BX
160
140
120
100
80
60
40
20
0
20 mrad
2 mrad
SIT Layer 1
SIT Layer 2

FTD hits



120
100
80
60
40
20
0
Hits / Disk / BX
1
2
3
4
5
6
7
Disk Number
20 mrad
2 mrad

FTD hits, x-y plane



BG summary

Backscattering is a significant contribution

- may be reduced by optimisation of geometries
- work is in progress (in collaboration with FCAL)
- small modifications (e. g. radii) can have large effects

Simulation effort is going on

- this talk contains data from 1 CPU-year
- jobs were run on the Grid (3 days on $\approx$ 120 nodes)
- the parameter space is large and multi-dimensional

Further runs are planned

- different geometries, beam parameters, . . .

EMI Issues

Chris Damerell

- *The problem*
  - On scale of 0.3 mm, most detector F-cages riddled with slot aerials and other apertures through which RF sails unimpeded
  - Once inside the enclosure, high frequency radiation bounces off the metal walls repeatedly, creating an isotropic radiation bath including standing waves, able to couple power in to the waveguides provided by the sensors
- *The 'solution'*
  - UHF bulkhead connectors
  - Wide conducting gasket seals to avoid small discontinuities in the contact areas between parts of the F-cage – ideally a welded vessel
  - Double screened coax cables, maybe installed in rigid pipe welded to the (thick) ends of the F-cage
  - Absorptive coating (foam, plastic, often in form of paint) on interior of F-cage. There are a number of commercial products, developed for defence and other industries. 1 mm thickness provides ~10 dB attenuation for 1-10 GHz
- *But you really don't want to do that…*

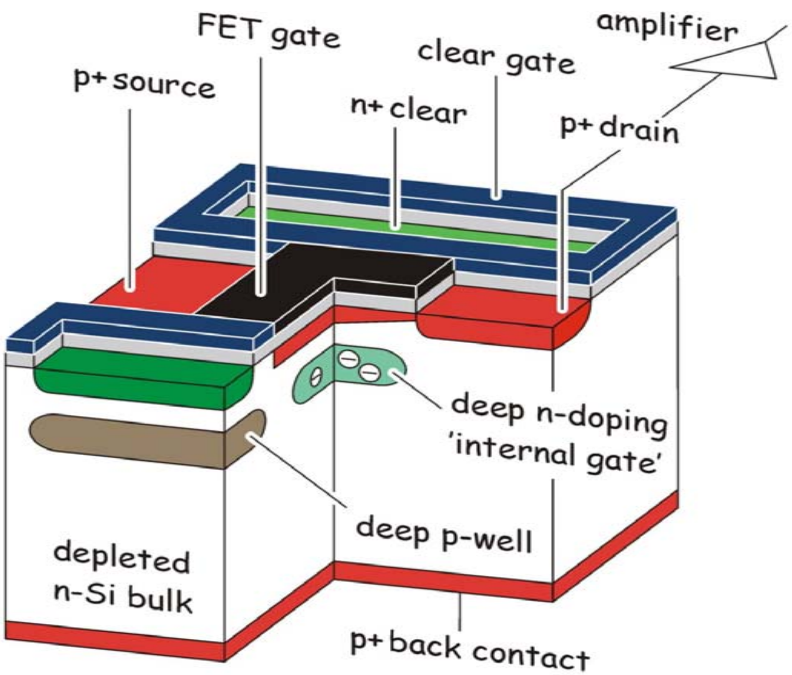
EMI – the way forward?

- *Sensor development*
  - Follow standard industrial procedures to characterise response of sensors to external RF, injected by cables and radiation in RF-anechoic chamber
  - Use these results in feedback to the sensor development
  - Use these results, along with the other performance parameters, to reach a balanced decision when choosing detector technologies
- *ILC Commissioning*
  - Near agreement that this should be carried out in a relatively open environment (within a blockhouse free of the detector, as was done at SLC)
  - If so, should be possible to include in the machine commissioning a vigilant evaluation of all RF leakage, and fix problems such as badly made connectors, loosely screwed cover plates, dirty gaskets on BPM monitor boxes, whatever
  - For investigation within the IR blockhouse, maybe some highly directional antennae or (new idea) an array of sensors with ~1 ns timing resolution, to permit location of the RF leakage source with ~30 cm precision

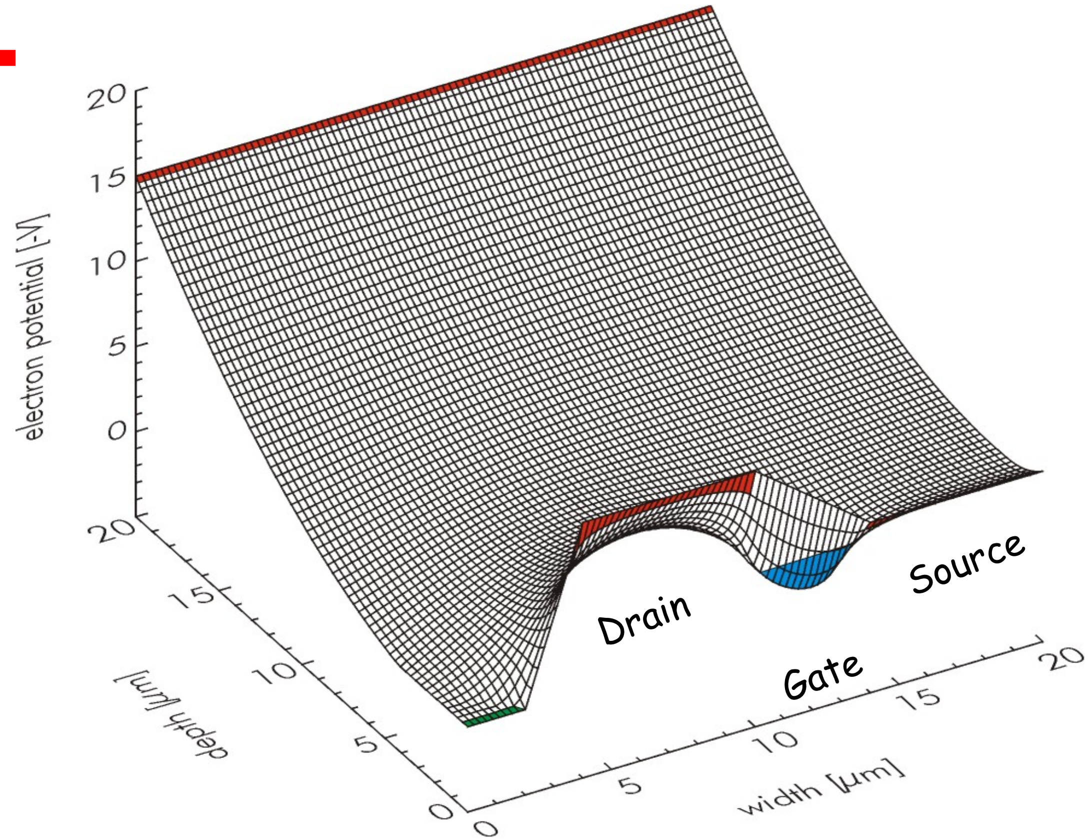
DEPFET Principle

Rainer Richter

J. Kemmer & G. Lutz, 1987



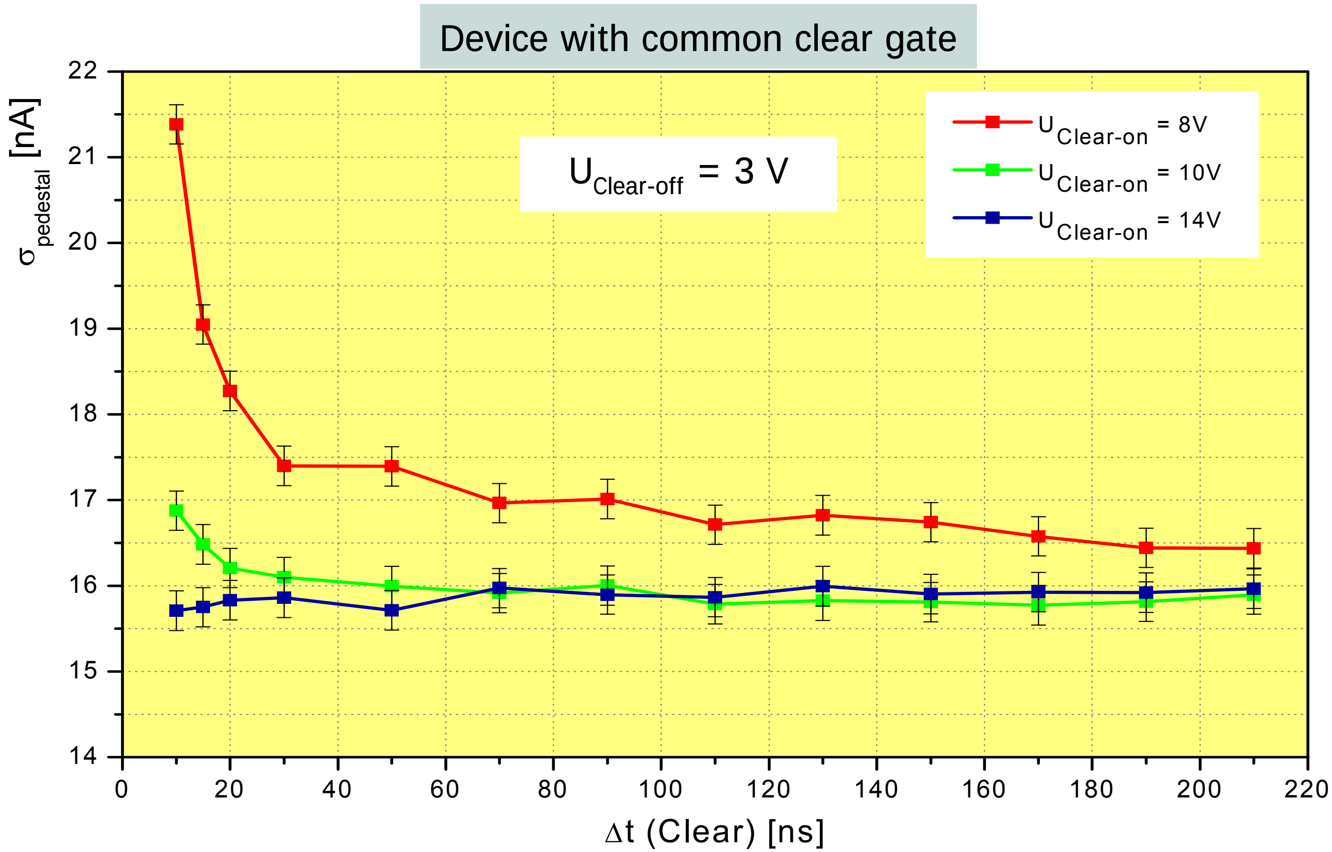
Depleted P-channel FET



- fully depleted sensitive volume
- internal amplification
- Charge collection in "off" state, read out on demand

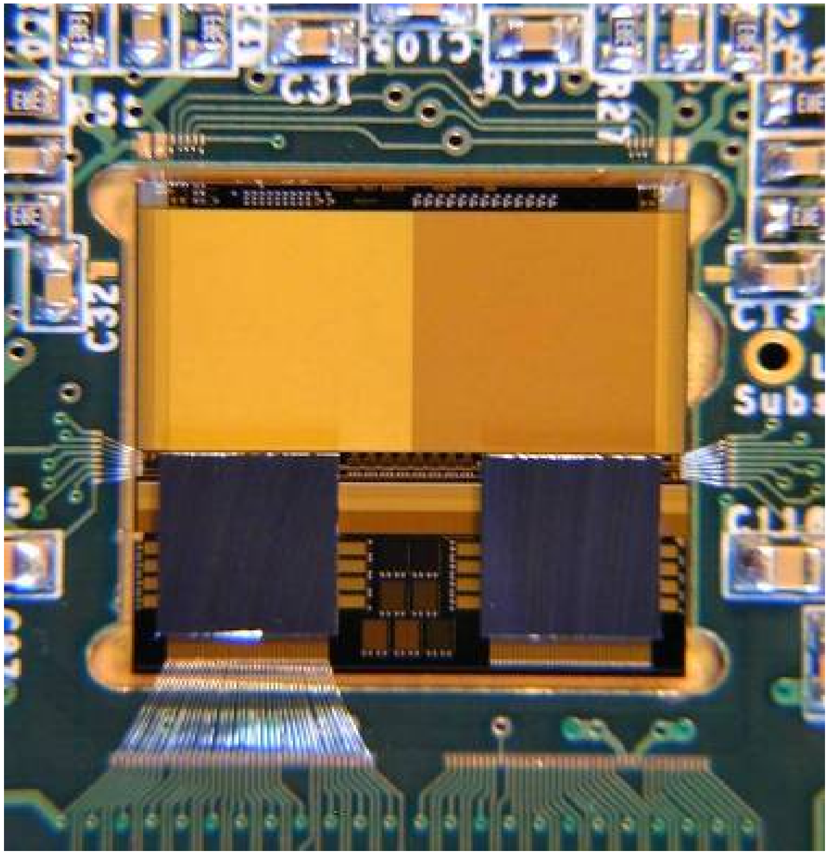
Fast Clearing

- Study clear efficiency for short clear pulses



Complete clear in only 10-20 ns @ ΔV_{clear} = 11-7 V

Hybrid assembly with Column-Parallel CCD (CPCCD) and CMOS ASIC



Bump-bonded CPC1/CPR1 in a test PCB

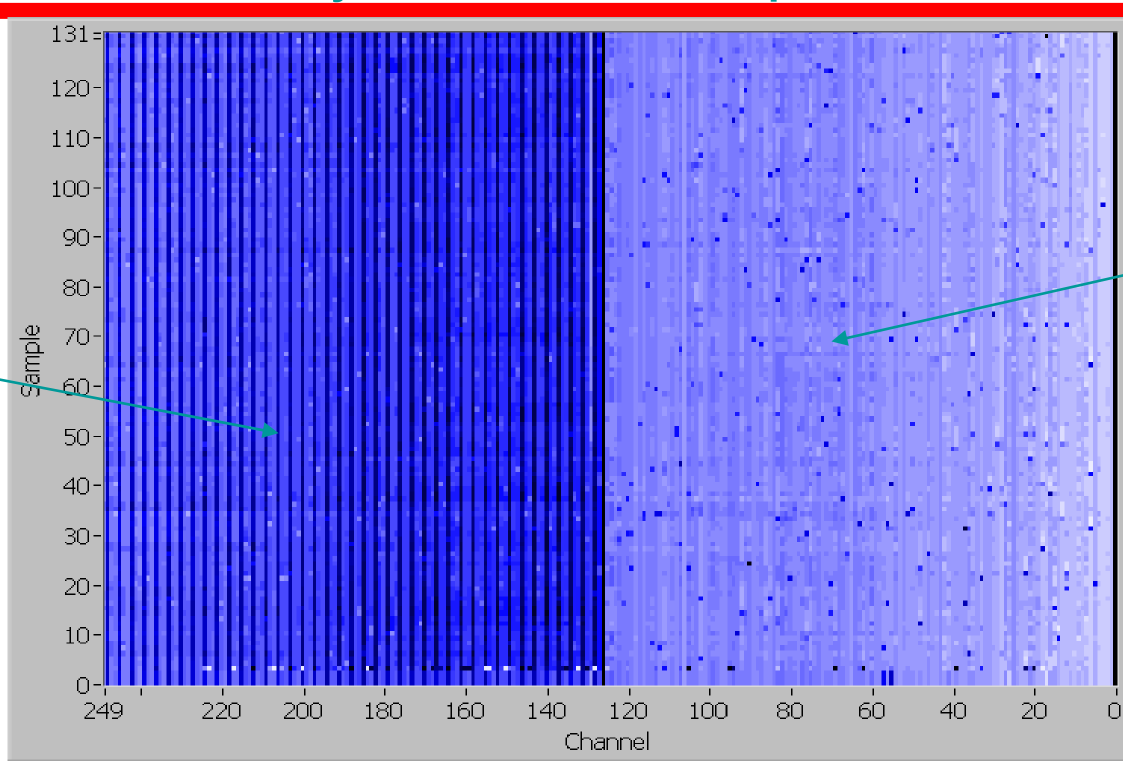
- CPC1 : Two phase CCD, 400 (V) × 750 (H) pixels, 20 μm square;
- CMOS readout chip (CPR1) designed by the Microelectronics Group at RAL:
  - ❖ 0.25 μm process
  - ❖ Charge and voltage amplifiers matching the outputs of CPC1
  - ❖ Correlated double sampling
  - ❖ 5-bit flash ADCs and 132-deep FIFO per column
  - ❖ Everything on 20 μm pitch
  - ❖ Size : 6 mm × 6.5 mm
  - ❖ Manufactured by IBM
- Bump-bonded by VTT (Finland) using solder bumps

CPC1/CPR1 Performance

5.9 keV X-ray hits, 1 MHz column-parallel readout

Charge outputs, inverting (positive signals)

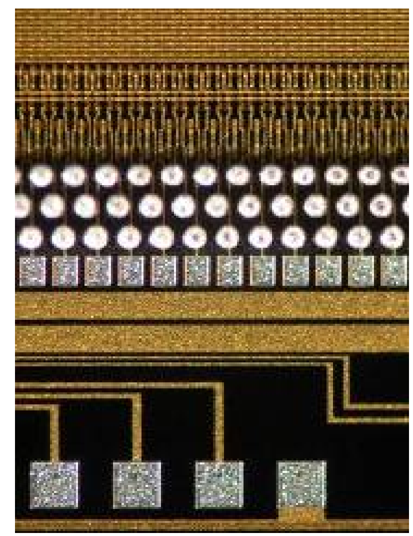
Noise ≈100 e-



Voltage outputs, non-inverting (negative signals)

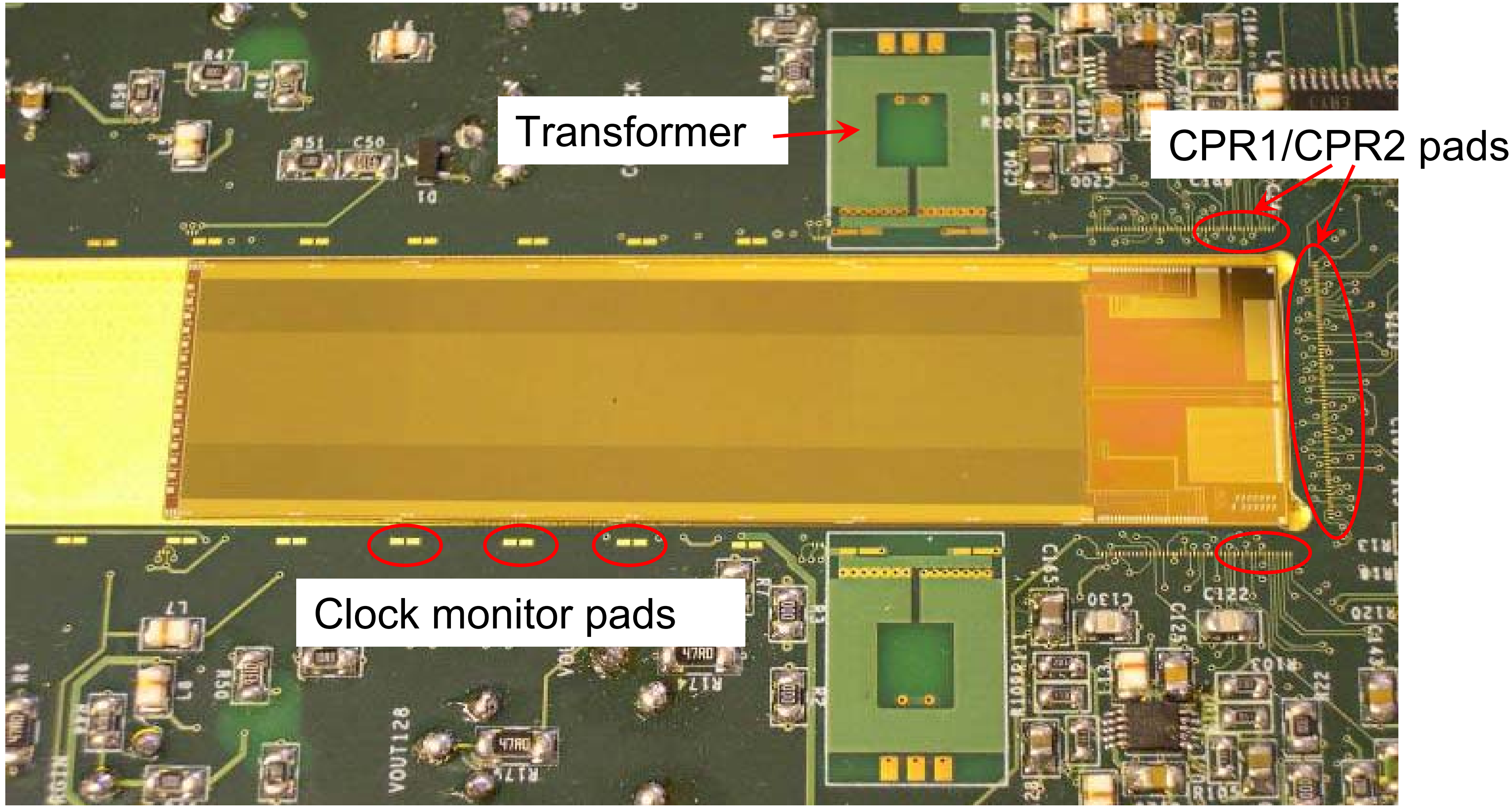
Noise ≈60 e-

- **First time e2V CCDs have been bump-bonded**
- **High quality bumps, but assembly yield only 30% : mechanical damage during compression suspected**
- **Differential non-linearity in ADCs (100 mV full scale) : addressed in CPR2**



Bump bonds on CPC1 under microscope

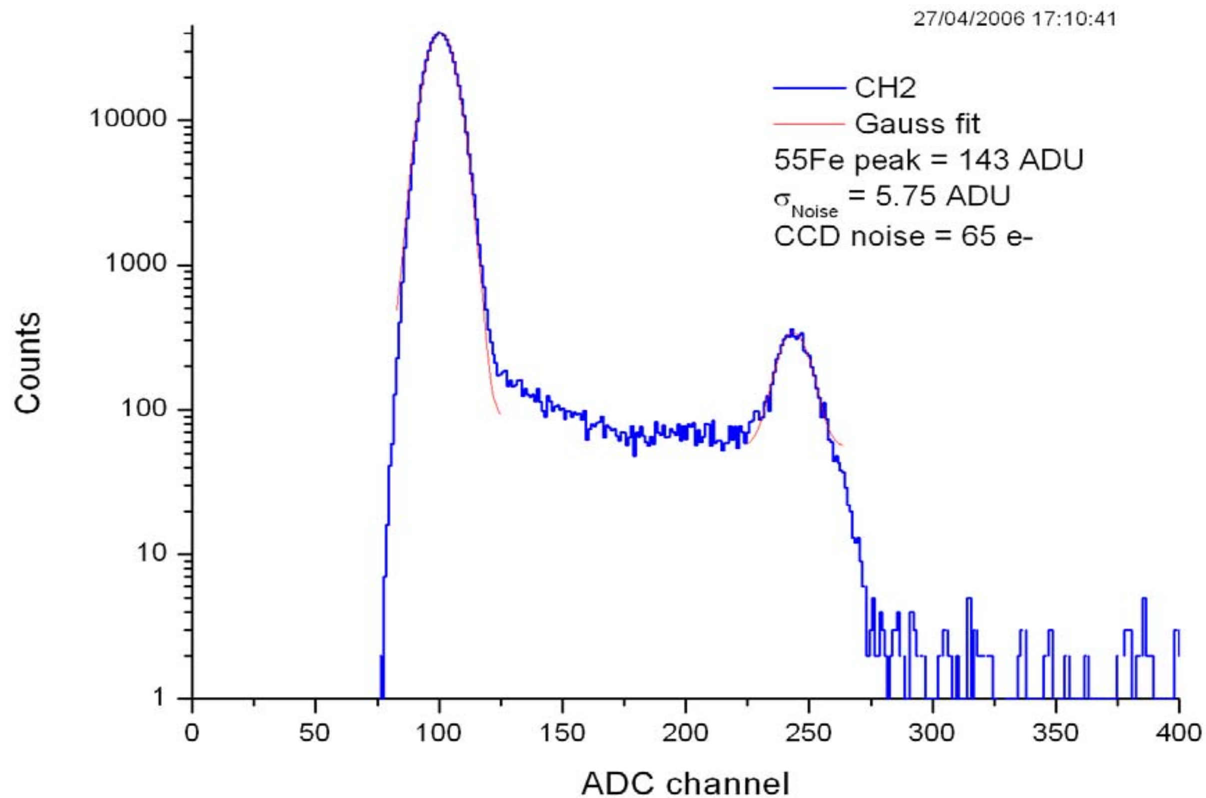
CPC2-40 in MB4.0



Johan Fopma, Oxford U

- ❖ **Transformer drive for CPC2**
- ❖ **"Busline-free" CCD: the whole image area serves as a distributed busline**
- ❖ **50 MHz achievable with suitable driver in CPC2-10 and CPC2-40 (L1 device)**
- ❖ **First clocking tests have been done**

First Data from CPC2

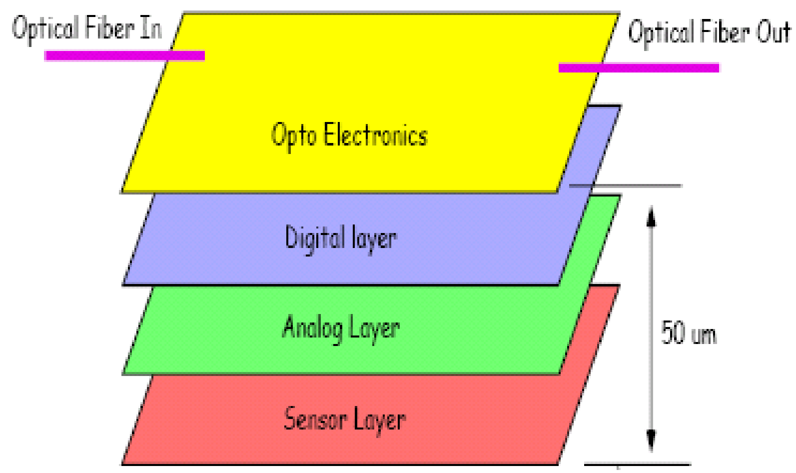


- CPC2-10 (low speed version) works fine, here at 1 MHz clock
- ^{55}Fe spectrum at -40 °C and 500 ms integration time
- Noise is a bit too high, external electronics is suspected
- Devices with double level metal (busline-free for high speed) are being manufactured now

What is a 3D chip?

Ray Yarema

- A 3D chip is comprised or 2 or more layers of semiconductor devices which have been thinned, bonded together, and interconnected to form a "monolithic" circuit.
- Frequently, the layers (also called tiers) are comprised of devices made in different technologies.

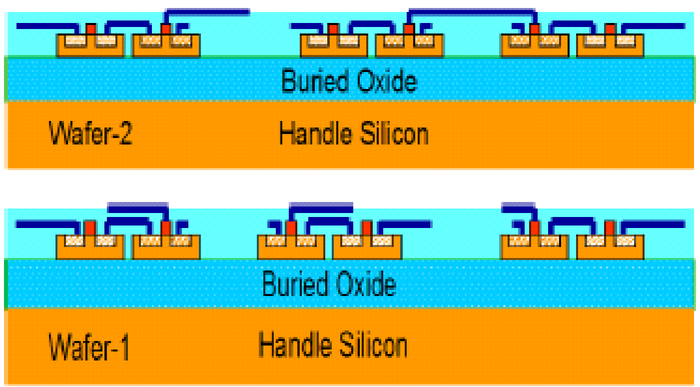


Designer's Dream

Process flow for a 3D chip

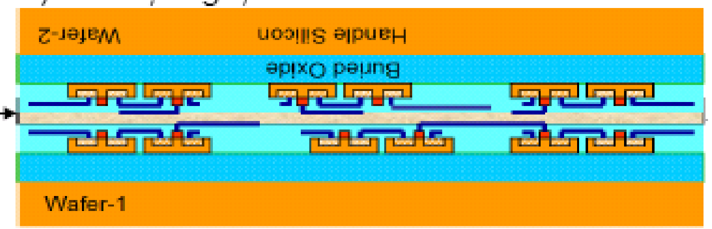
- 3 tier chip (tier 1 may be CMOS)
  - 0.18 um (all layers)
  - SOI simplifies via formation
- Single vendor processing

1) Fabricate individual tiers



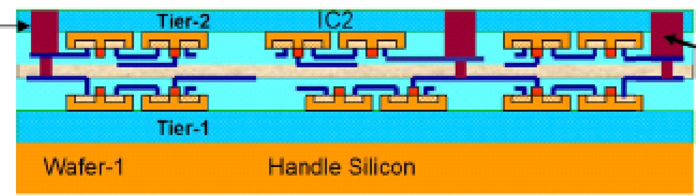
2) Invert, align, and bond wafer 2 to wafer 1

Oxide bond

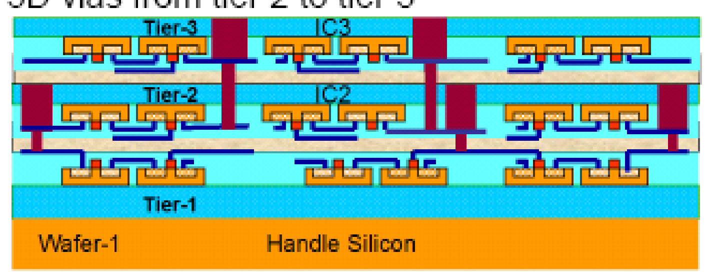


3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten

3D Via



4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



Summary

- Interesting workshop for vertex detector builders...
- ...but also information of interest to SiLC.
- Brief summary of some talks given here.
- Lots more information available at:
  http://www.hll.mpg.de/~lca/ringberg/