A Proposal for a Flexible CCD Readout System

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Introduction

The CCD test stations proposed for the LCFI vertex detector R&D at RAL and Liverpool University will require instrumentation for CCD clock control and for signal processing. The R&D proposal suggests the use of a modular VME-based system, under the control of a CES RIO-2 Processor, with the digital processing and data storage being performed on PMC mezzanine cards residing on the RIO-2 mother-board. All other functions (clock sequencing, digitisation, etc.) would be realised in custom-designed VME modules.

This document suggests a modification to this scheme, exploiting some recent developments in test system design for the ATLAS level-1 calorimeter trigger programme. The Data Source and Sink (DSS) module is a powerful general-purpose device designed to generate, transmit, receive and process programmable data patterns for testing various elements of the trigger. The core functions reside on the mother-board, with customised mezzanine cards enabling the module to be interfaced to a wide variety of different systems. Flexibility is achieved by the extensive use of large powerful FPGAs on the mother-board, which can be re-configured for each new application. The FPGA configuration may be performed either by using an ISP port to download configuration files into EEPROMs on the daughter-cards (as will be done for the trigger system), or by downloading the configuration files directly into the FPGAs via the VME interface.

Implementation

As each DSS module is designed to accommodate up to two mezzanine cards it is proposed to use a single module to provide the functions of CCD clock sequencing and signal processing. Two such cards would be designed to provide these functions. The architecture of the module (Figure 1) allocates eight FPGAs and eight blocks of 32K x 32 dual-port memory to the CMC cards, each of which may be configured as either an output (source) or input (sink) device. The use of an external system clock enables synchronous clocking of both cards, ensuring that the CCD data digitisation is always correctly timed.

Figure 1 shows how one of the two CMC cards can be designed to drive the appropriate trigger signals to the CCD Clock Drive system, when the associated FPGAs are programmed with the desired clock sequences by means of simple nested state machines. The Clock Sequencer CMC card, which simply provides suitable buffers and line-drivers, is fed with 80 data I/O lines and associated control lines which can be clocked at up to 50 MHz. The architecture also provides the capability of phase-shifting blocks of signals in programmable 1 nS steps. As the CCD Clock Drive system will actually require only a very small number of trigger signals, there is clearly more than adequate power available. One important requirement of the clocking system is to provide programmable fine control on the transition times of each clock phase, but this function would best be incorporated in the Clock Driver VME module which the Clock Sequencer card feeds.

The second CMC card is somewhat more complex, performing the functions of signal digitisation and frame-store memory for four channels of CCD data. Each channel of the Signal Processor CMC card consists of a buffered 10-bit FADC chip which feeds the digitised data via the CMC connector into a dedicated processing FPGA on the mother-board. Strobes for the FADC chips are supplied from the mother-board system clock with the appropriate programmed delays. The FPGAs may be configured with a variety of pipelined processing algorithms, downloaded via the VME interface, to explore different cluster-finding techniques, and the resultant sparsified data are stored in the on-board dual-port 32K x 32 memories. (These memories can be trivially replaced by 64K devices if desired, giving each channel a storage capacity of up to 256 Kbytes.) In addition to feeding the processing FPGAs the raw FADC data are captured "on the fly" on the CMC card in 4 Mbyte SRAMs, which together are large enough to contain a full CCD frame.

Readout of the processed data from the dual-port memories on the mother-board proceeds directly by the equivalent of block-transfer via the VME-bus, but the frame-store memories on the Signal Processor card are read out via their associated mother-board FPGAs.

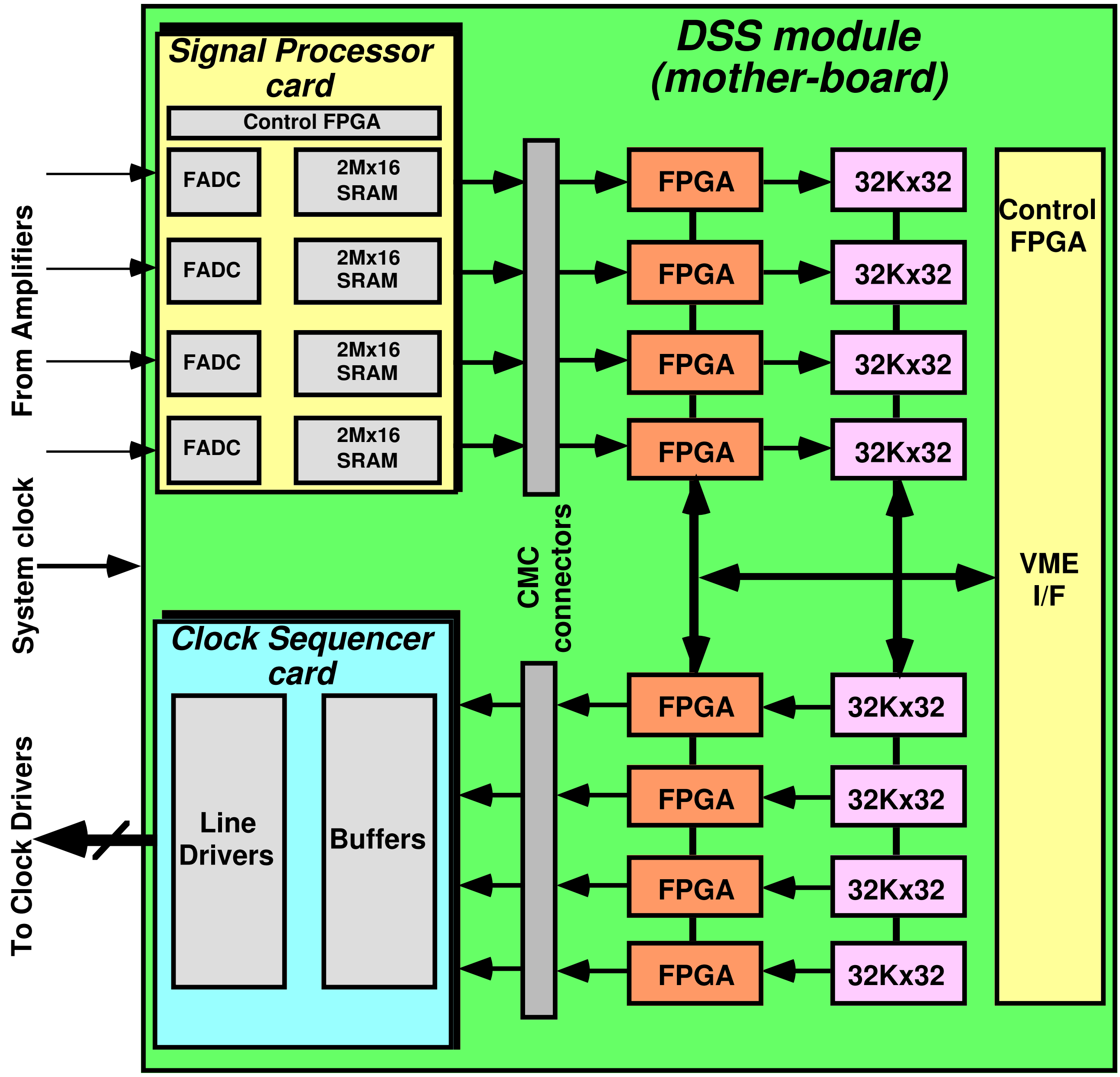

Figure 1 — Block diagram of CCD Readout Module

Clock Sequencer card specifications

		{Trigger 1 }	
Output trigger signals:	—	{Trigger 2 }	*(NIM signals on 50-ohm LEMO 00 connectors)*
		{Trigger 3 }	
		{Trigger 4 }	

		{R clock }	
Output clock signals:	—	{I clock }	*(LVDS signals on IDC connector)*
		{Node Reset }	
		{*Spare* }	

		{Control 1 }	
Output control signals:	—	{Control 2 }	*(LVDS signals on IDC connector)*
		{Control 3 }	
		{Control 4 }	

Signal Processor card specifications

No of analogue input channels	—	4
Analogue signal range	—	0 — -2 volts *(to match amplifier outputs)*
Analogue signal input impedance	—	50 ohms *(LEMO 00 connectors)*
Digitisation	—	10-bit flash
Sampling rate	—	≤ 50 MHz
Possible FADC chips:	—	SPT7871 *(Signal Processing Technologies)* AD9020 or AD9051 *(Analog Devices)* ADS823 *(Burr-Brown)*
Latency	—	*(Not important)*
Memory	—	2M x 16 SRAM per channel