A Flexible CCD Readout System

- **1998 R&D proposal suggested using VME-based Clock Sequencer with signal processing on RIO-2 PMC cards**

- **ATLAS level-1 trigger has developed a flexible test system — the Data Source-Sink (DSS) module**

- **Based on a FPGA-driven mother-board with 2 custom CMC daughter-cards to interface to external systems**

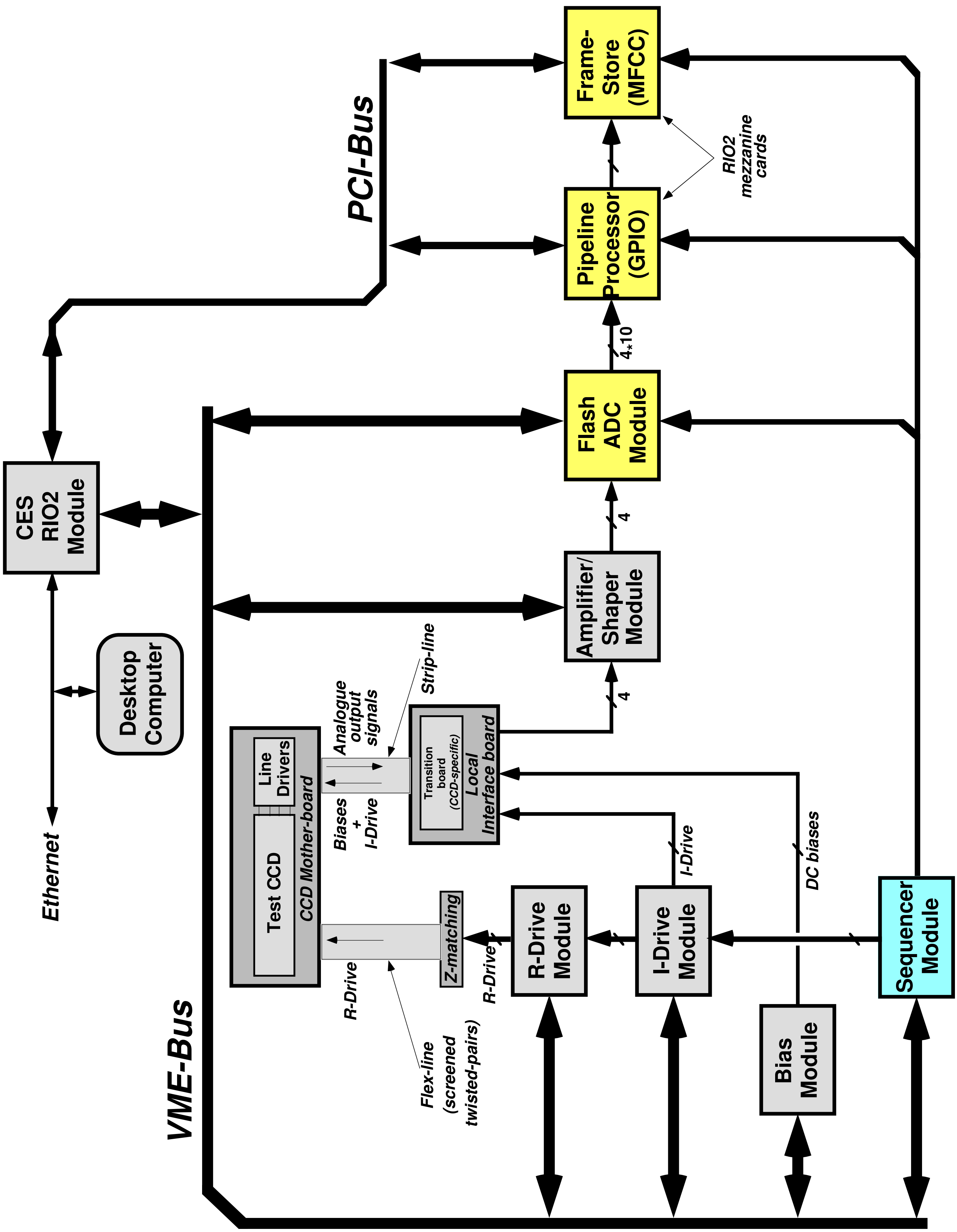
- **One CMC card will be designed as a Clock Sequencer to feed triggers to Clock Drive system and external stimuli**

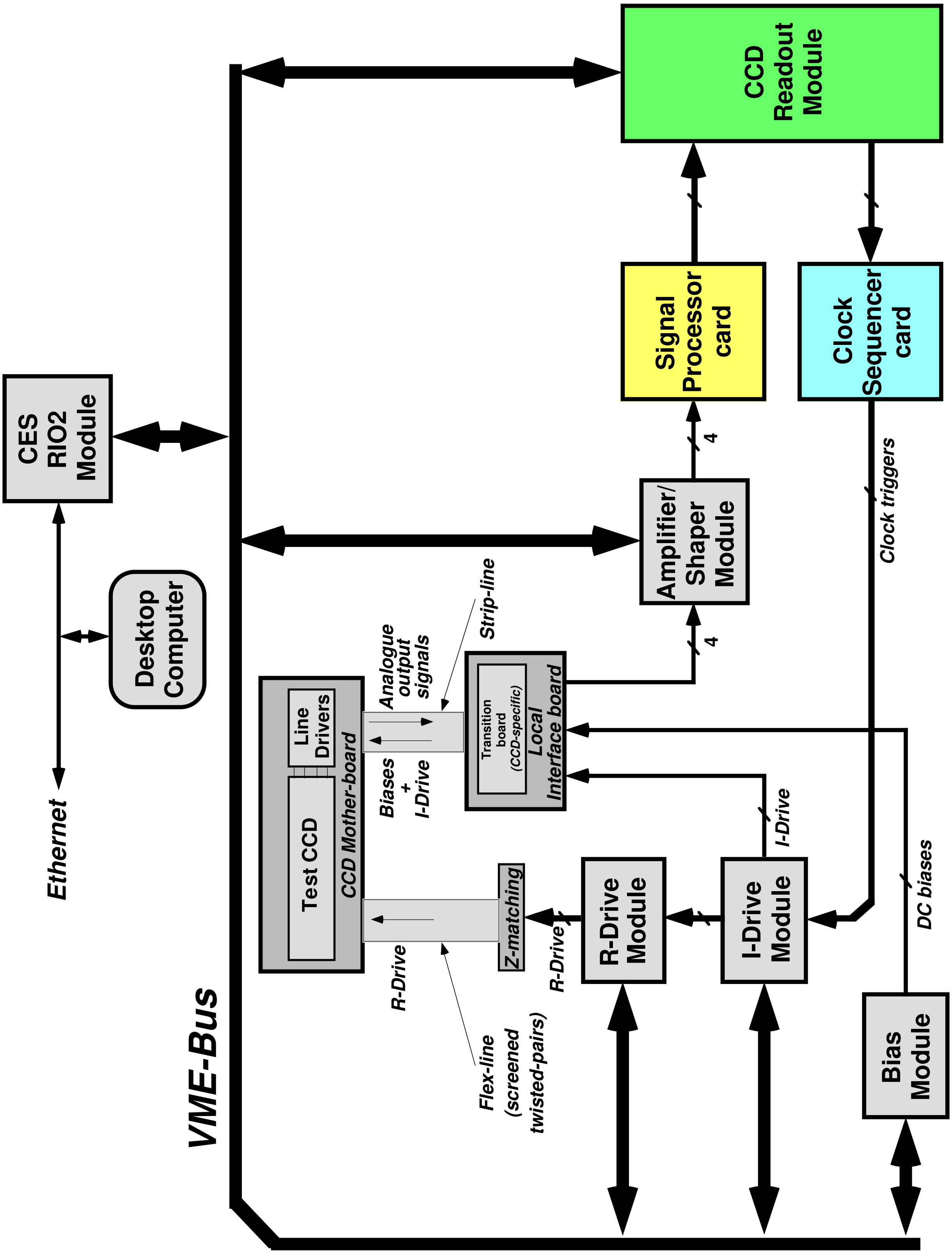
- **Clock Drive system provides programmable transition times on each I and R clock phase → 16 delay values**

- **Other CMC card will be designed as a Signal Processor to accept signals from CCD Amplifier system**

- **Raw FADC data stored in large SRAMs — mother-board FPGAs configured with processing algorithms (cluster-finding, etc), sparsified data stored in smaller DPRAMs**

- **Multiple DSS modules can driven synchronously at up to 50 MHz by external clock**


PCI-Bus
Frame-Store (MFCC)
Pipeline Processor (GPIO)
RIO2 mezzanine cards
4*10
Flash ADC Module
CES RIO2 Module
4
Amplifier/ Shaper Module
Desktop Computer
Ethernet
Strip-line
Analogue output signals
4
Line Drivers
Transition board (CCD-specific)
Local Interface board
Biases + I-Drive
Test CCD
CCD Mother-board
I-Drive
DC biases
Z-matching
R-Drive
R-Drive
R-Drive Module
I-Drive Module
Sequencer Module
Flex-line (screened twisted-pairs)
VME-Bus
Bias Module


CCD Readout Module
Signal Processor card
Clock Sequencer card
CES RIO2 Module
Desktop Computer
Ethernet
VME-Bus
Amplifier/ Shaper Module
4
4
Clock triggers
Strip-line
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Transition board (CCD-specific)
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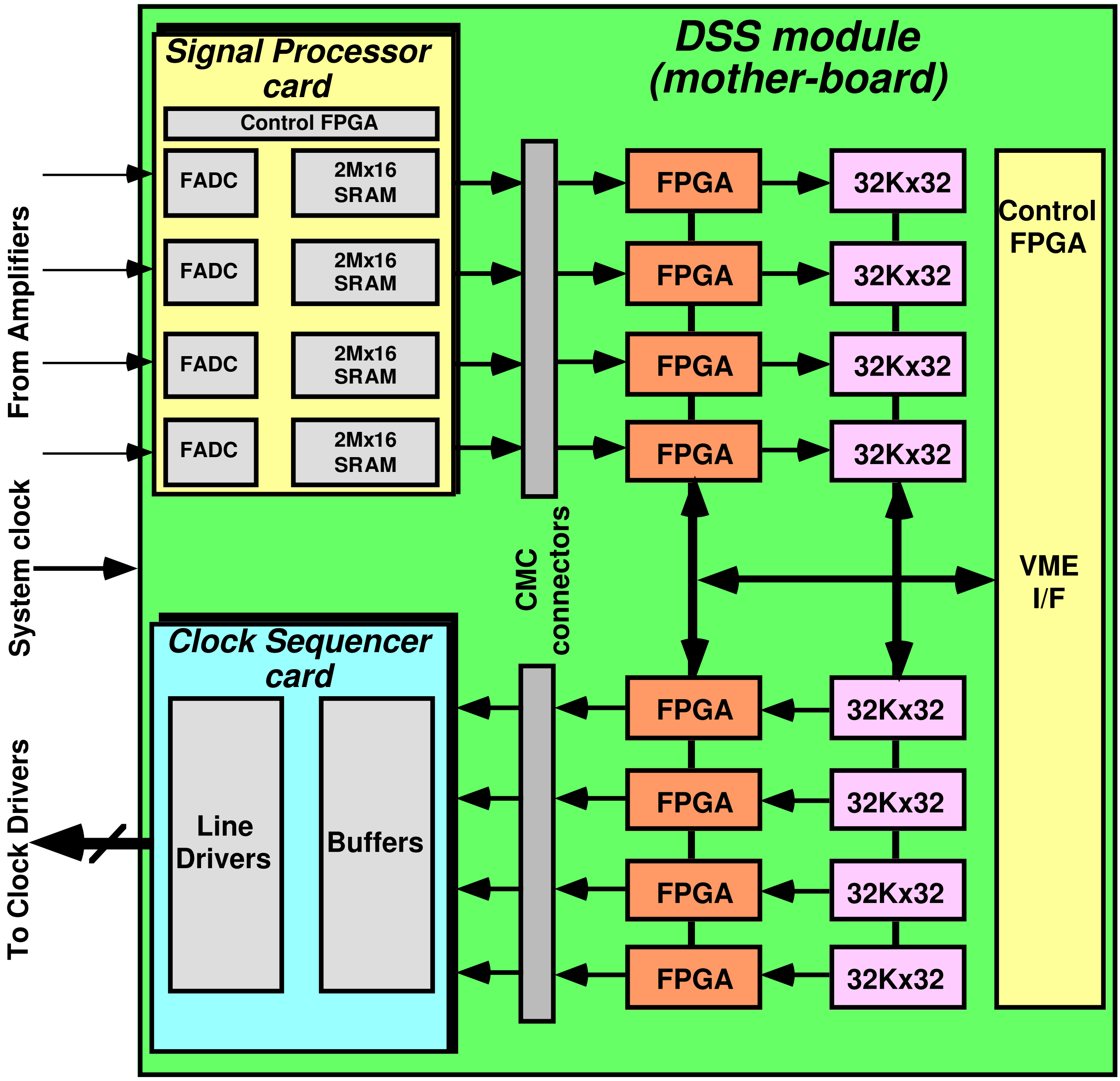

- **DSS mother-board:**

  — 4 FPGAs per CMC card — re-configurable via VME

  — 1 Mbyte DPRAM per CMC card

- **Signal Processor card:**

  — 10-bit Flash ADC chips *(SPT, AD, Burr-Brown, etc)*

  — 4 Mbyte SRAM per channel — >1 full CCD frame

- **Total estimated cost — ~ £3.5K per system *(plus NRE)***