as a world facility, that construction will begin in the middle of the next decade, and that first physics results will come towards the end of the decade, after a few years of LHC running. The project will most likely be phased, starting at $\sqrt{s}$ = 3-500 GeV, and evolving over several years up to 1 TeV and perhaps beyond, in an analogous manner to the LEP1/2 project. In the event of an exciting discovery in the next few years, for example a low-mass Higgs, one can imagine that the schedule might be somewhat accelerated.

1.3 The physics challenge

In parallel with the extensive accelerator R&D programme the physics potential of e^+e^-colliders has been explored at the international Linear Collider Physics Workshops (LCWS), held in Saariselka (1991), Hawaii (1993), and Morioka (1995) [1], with the next to be held in Sitges, Spain in May 1999. These workshops have demonstrated that the events of interest can be characterised as a complicated mixture of multi-jet final states, some produced with low cross-sections, i.e. yielding few events. These will often contain several heavy quark jets, and will require excellent jet energy resolution and heavy-flavour tagging capability to be identified above the potentially large combinatorial (QCD, W^+W^-) multi-jet backgrounds. A recent broad review of the physics can be found in [2]; here we give just three illustrative examples.

1) $e^+e^- \to Z^0H^0 \to q\bar{q}f\bar{f}$

For a light Higgs the most straightforward channel to identify is $H^0 \to b\bar{b}$, yielding a 4-jet final state with two *b*-jets. With highly efficient *b*-tagging the H^0 mass reach can be significantly increased [3].

Moreover, it is vital to measure in addition the H^0 branching ratios to $c\bar{c}, \tau^+\tau^-$... so as to eliminate/constrain particular non-SM Higgs models. It is the charm- (and tau-) tagging capability that presents a more severe challenge to the vertex detector (see below).

For a heavy Higgs, the modes $H^0 \to W^+W^- \to 4$ jets, $H^0 \to t\bar{t} \to bW\bar{b}W \to 6$ jets give rise to 6- and 8-jet final states respectively; the more jets that can be *b- or c*-tagged the smaller is the QCD multi-jet background.

2) $e^+e^- \to HA \to t\bar{t}t\bar{t} \to WbW\bar{b}WbW\bar{b}$

This yields a 12-jet final state containing four *b*-jets!

3) $e^+e^- \to \tilde{t}\bar{\tilde{t}}$

If stop is the lightest squark one has $\tilde{t}\bar{\tilde{t}} \to c\chi^0\bar{c}\chi^0$, requiring the identification of *two* charm jets. Further examples illustrating the requirements for high-performance vertex detectors can be found in [4].

1.4 Current world physics and detector programme

Major coordinated efforts are taking place now in Europe, the USA and Japan to refine the physics studies, understand their implications on the detector design, and start the R&D necessary to achieve the challenging performance requirements (see below). The intention of these efforts is to prepare baseline detector designs to be presented, together with accelerator designs, to the funding agencies in 2001. An important milestone is provided by the last in the current round of ECFA/DESY Workshops, to be held in Oxford in March 1999, as well as similar meetings in the USA and Japan. The international community will then gather to share results in May 1999 at the LCWS meeting in Sitges, Spain. A world coordinating body for the physics and detector studies has been formed, and has already succeeded in defining common group structures among the three regions, with overall international coordinators. It is hoped that these collaborative efforts, focused on physics and detectors, will flourish independently of the details of specific accelerator technologies or sites.

A number of us are already participating in these international working groups on specific physics and detector topics, as well as on relevant accelerator issues, and simulations. The LCFI Collaboration aims both to take a broad view of these developments, and to develop key expertise in crucial areas. We believe it is now prudent to commence an R&D programme on the vertex detector design. Through this proposal we hope to make substantial progress in learning how to build a 21st Century vertex detector that can meet the requirements for EWSB physics studies. We aim to collaborate fully with our European, American and Japanese colleagues, but it is clear that a modest, carefully staged R&D programme will allow the UK to play a major role in the eventual detector

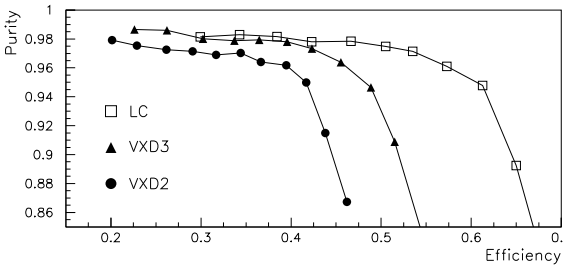

Fig. 1 Performance of *b*-jet flavour tag. VXD2 and VXD3 refer to the original and upgrade SLD detectors.

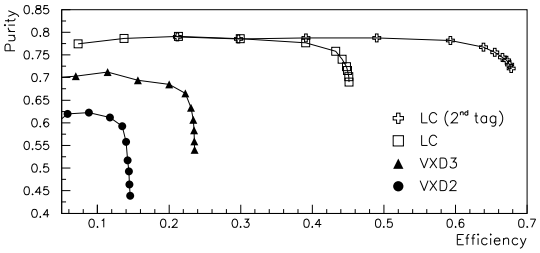

Fig. 2 Performance of *c*-jet flavour tag. The 2nd tag refers to use of 1-prong decays (see Section 2.2)

construction project, and in the physics studies that depend crucially on it.

1.5 Evolution of vertex detector design

Though the experimental environment at an e^+e^- collider is in some respects less challenging than that facing the LHC detectors, the requirements on the detector if it is to be capable of disentangling numerous multi-jet heavy-flavour final states with small event samples, are indeed very stringent and require an extended R&D phase, involving both simulations and hardware development.

From previous studies [5] it is clear that a first-generation LEP vertex detector, based on silicon microstrips, with impact parameter resolution in the plane normal to the beamline characterised by

$$\sigma_{r\phi} = 20 \oplus \frac{100}{p \sin^{3/2}\theta}\,\mu\mathrm{m},$$

is not adequate. The poor resolution reflects the intrinsically thick detectors, the coarse segmentation, and the large radius that would be required to maintain an acceptably low hit density from beam-related background. Highly segmented pixel-based CCD detectors provide 3-D position measurements, are much more tolerant of background, and hence can be placed much closer to the beamline. The state-of-the-art is represented by the SLD upgrade detector [6]. With only 0.4% X_0 per layer, and three azimuthally complete layers with the first at radius 28 mm, the impact parameter resolutions are far superior:

$$\sigma_{r\phi} = 9 \oplus \frac{33}{p \sin^{3/2}\theta}\,\mu\mathrm{m}$$

$$\sigma_{rz} = 17 \oplus \frac{33}{p \sin^{3/2}\theta}\,\mu\mathrm{m}.$$

Combined with the tiny, micron-sized SLC beam spot, this allows heavy-flavour physics measurements that are highly competitive with LEP, despite a data sample size smaller by an order of magnitude.

The LCWS studies have led to a conceptual CCD vertex detector design comprising a 5-layer layout, with the innermost layer at approximately 12 mm radius, where beam-related backgrounds (Section 2.1) are alleviated by a high (4 T) magnetic field in the detector solenoid. The impact parameter resolution is given by

$$\sigma_{r\phi} \approx \sigma_{rz} \approx 4.5 \oplus \frac{5.5}{p \sin^{3/2}\theta}\,\mu\mathrm{m}$$

where full 3-D self-tracking is made possible by the 5-layer construction.

Quantitative studies of the flavour-identification performance of the conceptual detector have been performed for simulated *b*- and *c*-jets in Z^0 decays and are summarised in Figs. 1 and 2 [7,8]. The *b*-tagging efficiency can be pushed out to about 60% for a *b*-jet purity of 98%, far exceeding the performance of even the SLD upgrade detector. Moreover, the *c*-tagging efficiency can reach 65% for a *c*-jet purity of 75%, a factor of 3 better than achieved by SLD. Since the combined efficiency for tagging *n* jets is proportional to ε^n, the factor of 3 in relative *c*-tagging efficiency per jet would correspond to, for example, a factor of 9 for physics example 3) above, which might well make the difference between observing and not observing, a handful of events in a rare channel.

In parallel with the detector R&D programme presented here, we plan to continue these quantitative simulation studies, extending them to specific benchmark reactions defined in the coordinated world studies. We anticipate strong interplay between the evolution of the detector design and the results of the physics

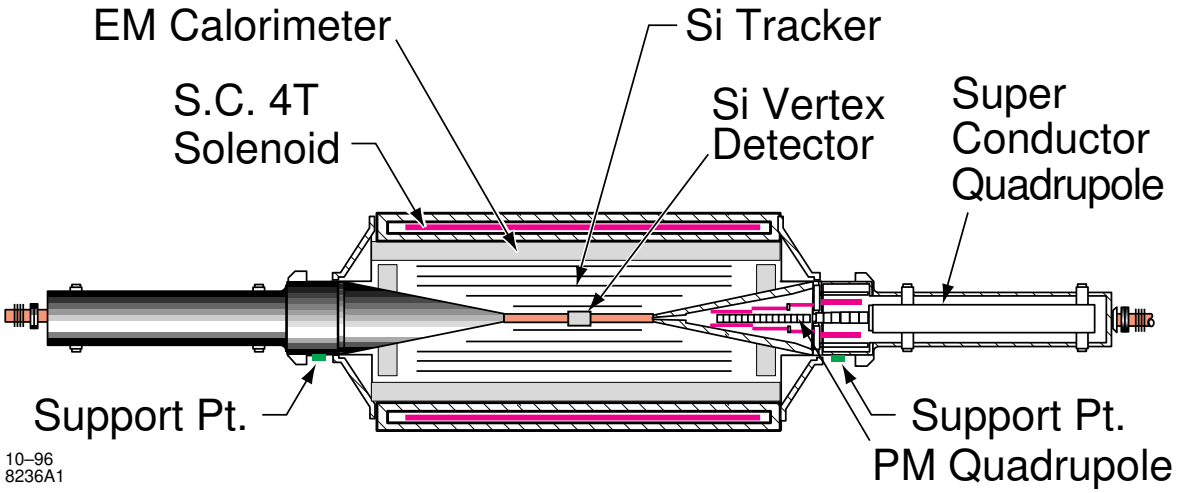

Fig. 3 Inner region of a conceptual central detector. Solenoid vacuum tank is clamped to quadrupole support barrels. For each beam, the outer quadrupole of the final doublet is a superconducting and the inner one a permanent magnet.

studies. In addition, realistic simulations of the detector will be used in formulating the benchmark designs that are to be submitted in 2001, allowing determination of the full physics potential of the complete detectors.

1.6 The detector challenge

The current conceptual vertex detector design is extremely challenging in many respects, which are discussed extensively in Sections 2 and 3. Briefly, the design requires:

- Large-area CCDs for sufficient angular and radial coverage: the largest have 2.3 times greater area than those currently used at SLD.
- Very thin ($0.12\% X_0$) layers (0.3 times current SLD) with excellent mechanical stability.
- 50 MHz pixel readout frequency, 10 times faster than SLD to reduce background, yet still with power dissipation compatible with almost massless gaseous cooling.
- Adequate radiation tolerance w.r.t. ionizing radiation and neutrons.
- Compatibility with the LC interaction region environment, in particular the 4 T solenoid field and RF pickup from the beams.

It is these issues which we wish to address with a carefully phased programme of R&D that will allow the vertex detector to be designed and constructed on a timescale well-matched to the collider project. This proposal represents the first phase of that programme. The second phase will involve CCDs and integrated circuits custom-designed for this detector.

2. Design Issues

2.1 Collider options and background conditions

The two most serious contenders for the high energy linear collider are the room temperature X-band machine being developed jointly by SLAC and KEK, and the superconducting RF machine TESLA, being developed at DESY. We consider in turn the characteristics of these two designs as they impinge on the vertex detector and hence on the potential for heavy flavour physics. It should be noted that the characteristics of both designs are subject to ongoing development. A major task of the LCFI Collaboration (and our colleagues in equivalent groups in the USA and Japan) is to follow these developments, in particular to ensure that changes in the final focus design or diagnostic equipment (laser-based beam-size monitors etc.) remain compatible with a small-radius vertex detector. Nowhere is the machine-detector interface more critical, and some early suggestions from accelerator physicists would have blown the detector out enormously in radius. This would be in nobody's interest, since an optimised

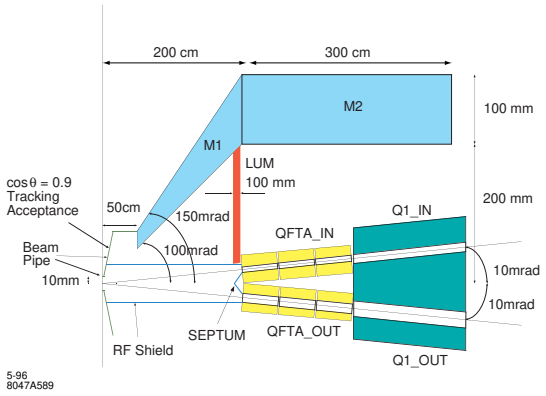

Fig. 4 The interaction region masking and magnet layout, in one conceptual design. (Note the factor 10 expansion of the transverse scale.)

detector is worth at least an order of magnitude in luminosity for some physics processes.

In the following discussion, we take for the purpose of illustration the machine parameters at 0.5 TeV c.m. energy. From the viewpoint of the vertex detector and overall event reconstruction, conditions up to 1 TeV are not substantially different.

For both accelerator options, the main sources of background are:

- Muons produced in the upstream beam collimation system.
- e^+e^- pairs produced by beam-beam interaction processes.
- Neutrons photoproduced from the various electron dump locations.
- Beam-gas collisions in the interaction region.

Those which are relevant to the vertex detector are discussed below, for each machine design option.

2.1.1 X-band machine

The beams cross at an angle of 8-20 mrad. The rigid mechanical link between the entry quadrupoles for each beam (essential for preservation of luminosity) is provided by clamps to the vacuum tank of the superconducting solenoid (see Fig. 3). Thus the entire inner volume is available for tracking (the vertex detector followed by, for example, the silicon microstrip detector). The finite crossing angle is an important feature of this design, since it permits use of separate, larger aperture, exit quadrupoles for each beam, as shown in Fig. 4. These exit quads accept the full flux of synchrotron radiation and beamstrahlung, which can then continue far downstream and be deposited safely on the main beam dumps. This approach to background control profits from the painful lessons learned at the SLC, where SR photons from the final focus could interact with material a few metres downstream of the IP. The resultant fluorescence photons produced acceptable backgrounds in the vertex detector, but conditions could become intolerable in the central tracking detector, due to its relatively coarse segmentation. For the future machine, these particular backgrounds should be negligible.

Despite these improvements, the TeV scale machine will be subject to one new and dangerous source of background. Beamstrahlung photons interacting with the intense electromagnetic field of the opposite bunch can initiate pair production (the Bethe-Heitler process). These pair electrons receive a p_T kick and so can emerge at wide angles. In the absence of the detector solenoid, they would create intolerable background in the vertex detector. By operating with a solenoid field of 4 Tesla, this can be reduced to 5 hits/mm^2 at R = 12 mm (radius of VXD layer 1) and to 0.5 hits/mm^2 at R = 24 mm (radius of VXD layer 2), per bunch train.

The time structure of the X-band machine is ~ 80 bunches at 2.8 ns intervals per train, with a bunch train frequency of ~ 180 Hz. As far as the vertex detector and most other detectors are concerned, signals are simply integrated through each train. The long time interval between trains allows highly multiplexed readout. Reading out via optical fibres as at SLD permits an extremely hermetic overall detector with very little extra material or dead space occupied by cables, cooling pipes, etc.

There are additional background sources to be considered for the X-band machine. While the primary high energy beamstrahlung and synchrotron radiation photons are dumped remotely, the pair electrons spiral around the solenoid field lines and are dumped on the faces of quadrupoles and other instrumentation within the M1 mask aperture (Fig. 4). Though relatively soft, these electrons constitute a weak source of photoproduced neutrons, some of which find their way back to the detector. Beam-gas collisions constitute another

background source. Current estimates suggest that both these are negligible, but, as discussed in Section 3.7, CCDs are unusually sensitive to damage induced by hadronic interactions, and there are uncertainties about their radiation resistance under the linear collider readout conditions. The Interaction Region group at SLAC is currently refining the above background estimates.

In summary, the principal background of concern to the vertex detector at the X-band machine appears to be the irreducible e^+e^- pair background associated with the beam-beam interaction. If this proves to be the case, the situation is far more favourable than was encountered at SLC. Under conditions of poor machine performance (low beam current and/or badly focused spots) the pair background will be reduced. One will see the highest background, equal to the calculated background, only at full luminosity. In SLC it was just the reverse; poor beams often gave large tails in phase space, which generated excessive SR background in the detector.

2.1.2 TESLA

Much of the above discussion (e.g. the requirement for a conical mask M1 to contain background) applies equally to TESLA, but there are important differences.

Firstly, there is the question of luminosity. At 0.5 TeV, the TESLA group are now offering 5×10^{34} cm^{-2} s^{-1} (up by a factor 10 compared with the X-band machine, and with last year's TESLA design). This will open up some wonderful physics opportunities if it can indeed be realised. We assume this figure in assessing the highest possible background levels.

Secondly, the TESLA collimation system is at present less developed than that at the X-band machine, where a 5 km region downstream of each linac is devoted to collimation and beam cleanup. The very cautious X-band design is based on many years experience at SLC, where it was found that immeasurably small tails on the beam phase space distribution could generate ferocious SR background if not effectively collimated. Due to the more modest collimation system currently planned for TESLA, the swath of primary synchrotron radiation traversing the IR is broader, and may itself limit the beam-pipe radius in the region of the IP. This question is under study by the TESLA beam group, who are confident that if the 10 mm beam-pipe radius is justified by ongoing physics studies, they can deliver it.

Thirdly, one should consider the effect of the different time structures of the X-band and superconducting RF designs. At TESLA, the bunch train frequency is 5 Hz. Therefore, if other things are equal, the integrated luminosity and background per bunch train will be higher at TESLA by a factor $\frac{180}{5}=36$. If the TESLA luminosity is really higher, this factor will be further increased.

Fourthly, TESLA is currently designed with 0^0 crossing angle for the two beams. This means that the entrance and exit quadrupoles must be the same, and enforces a much earlier dump of the beamstrahlung photons. Neutron background from this dump is a cause for concern regarding a CCD-based vertex detector; fluxes could be much higher than from the e^+e^- pair dumps, which are similar in the X-band and TESLA designs. The detailed design of this dump and associated collimation has yet to be undertaken by the TESLA beam group.

Fifthly, there is the question of the detector solenoid field. For the X-band design, the value of 4 Tesla proposed at the Snowmass workshop was favoured by the tracking group, and was acceptable for calorimetry (since the electromagnetic calorimeter is inside the coil). However, many issues related to the calorimetry remain to be studied, particularly the required radius and the issue of possibly needing at least part of the hadron calorimeter inside the coil. For TESLA, a different emphasis in the design of the tracker has led to a somewhat lower solenoid field. This however is not fundamental to the superconducting collider. For the present, we assume the greater physics reach associated with the higher solenoid field to be equally available at TESLA.

In summary, the ongoing design of the collimation system and study of tracking detector options makes the issue of backgrounds at TESLA somewhat uncertain at this stage. The final vertex detector design might look very similar to that at the X-band machine, or it might require a factor two larger radius for the inner layer. In the worst scenario, the environment might be so hostile (due to neutrons generated at the beamstrahlung dump) as to rule out a CCD detector at any radius, which would seriously compromise the physics. These issues will be resolved by ongoing studies by the different groups interested in the TESLA option.

What is inescapable (due to the different time structures of the two designs) is the much higher background per bunch train at TESLA.

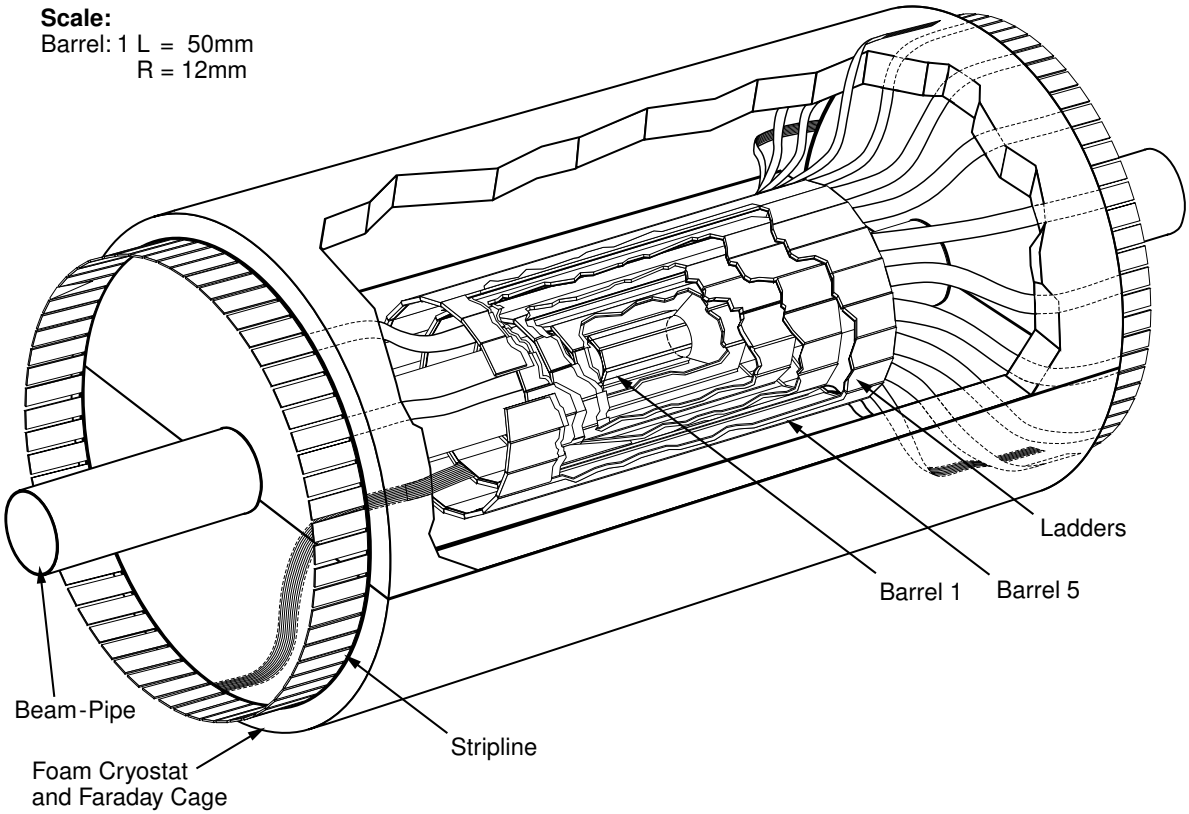

Fig. 5 Cut-away isometric drawing of the suggested 5-barrel vertex detector. All non-CCD electronics is external to the cryostat, in the small-angle region below the limit of tracking.

As a later phase of our R&D programme, we would propose to address this specific issue, via a 'fast-clear' feature of the vertex detector. The TESLA bunch train (last updated in May 1997) consists of 1130 bunches at 708 ns intervals. For conventional detectors, this means that (in contrast to the X-band case) one can latch and read out the data from a single bunch. Even with CCDs, integration through such an extended train is unnecessary. One can subdivide the train into say 50 sub-trains, fast-clearing the CCDs at intervals of 22 bunches, in the absence of a trigger during the preceding 22-bunch period of 15.6 μs. On receipt of a trigger, the CCDs would be put into normal readout mode and the generation of further pair background would be eliminated by using a modest kicker magnet to push the beams out of collision. This scheme depends on the trigger rate for events with vertex detector readout being moderate, otherwise the deadtime penalty would be unacceptable. There may well be exotic triggers, for example searching for charginos close in mass to neutralinos, for which the trigger rate will be high, the energy threshold being limited only by calorimeter noise. However, there would be no advantage in reading out the vertex detector in association with all such exotic triggers.

A preliminary design exists for the fast-clear feature on the large CCDs for this detector, but the detailed design and R&D represents a significant project, and is not included in the present start-up proposal. It will be reassessed as the R&D programme progresses, and the relative prospects for the TESLA and X-band colliders become clearer.

2.2 Overview of the vertex detector conceptual design

The conceptual design has been reasonably stable since the Snowmass workshop two years ago. There remains the possibility that the ongoing physics studies will reveal the need for further changes (e.g. in angular coverage, number of layers etc.) but at present the design seems to be reasonably optimised. Recent performance data from the SLD upgrade detector lend support to the most optimistic

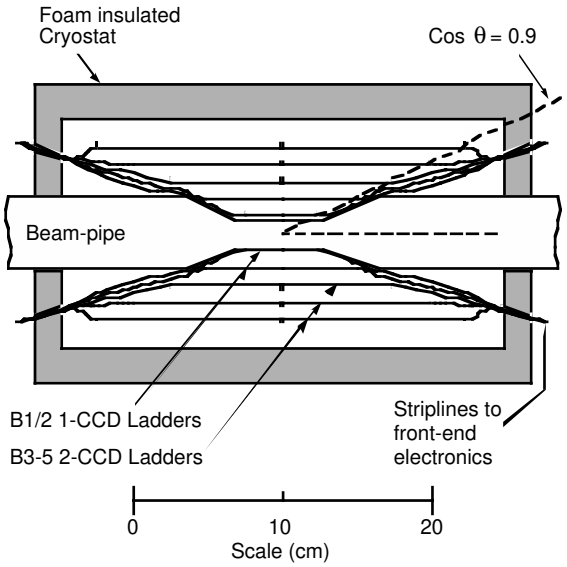

Fig. 6 Cross-section of the suggested vertex detector.

features of this design. The largest ongoing uncertainty is probably that of the solenoid field. If this were required to be less than 4T due to overall detector design considerations, the vertex detector inner radius would need to expand, with a consequent (modest) degradation in performance.

The basis for the detector design parameters, and the resultant performance in terms of jet flavour identification, is discussed in [8]. The general detector layout is shown in an isometric view in Fig. 5 and in cross-section in Fig. 6. Key parameters are listed in Table 1. Background densities refer to the X-band design with 4 T solenoid field. The tapered beam-pipe is designed to accommodate the envelope of nearly all the background e^+e^- pair electrons that were discussed in Section 2.1.1.

The general idea behind the 5-barrel (660 Mpixel) layout is as follows. While the background in the inner barrel detectors (B1) is perfectly compatible with their use for track fitting, by using the on-track cluster to refine the impact parameter measurement, the hit density would make it difficult to use in the pattern recognition. The intention is to achieve stand-alone track finding in the vertex detector using layers B2-B5. This provides a comfortable degree of redundancy. Found tracks are then extrapolated outwards for linking to the Central Tracking Detector, and also inwards for linking to B1 hits, prior to a global fit and optimal determination of track parameters. Including B1 in this fit gives almost a factor of two improvement in the precision of the impact parameter at the IP (multiple scattering term).

There is generous radial spacing between the barrels:

$R(\mathrm{B2}) = 2 \times R(\mathrm{B1});\ R(\mathrm{B3}) = 3 \times R(\mathrm{B1});$ etc

This provides excellent impact parameter resolution, while retaining achievable CCD lengths even for B5. Note the use of single CCDs per ladder on B1 and B2, and two CCDs beyond.

The mechanical support structure (not shown in the drawing) will be similar to that used in the SLD vertex detector [6]. It will introduce very little additional material into the vertex detector tracking region $(|\cos\theta| < 0.9)$ but will hold the ladders rigidly at each end, providing excellent resistance to bowing; the

Table 1 Parameters of CCDs and ladders. For each barrel, R = barrel radius, L = ladder length, W = ladder width. For comparison, some parameters of an SLD ladder are included.

Barrel	R mm	L/2 mm	W mm	CCDs/ Ladder	CCD size (MPix)	Outputs/ CCD	Ladders	Read Time ms	Hit Density mm^{-2}
SLD	≥ 28	80	16	2	3.2	4	48 total	180	~ 0.1
1	12	25	12	1	1.5	12	8	4.5	5
2	24	50	24	1	6.0	12	8	18	0.5
3	36	75	24	2	4.5	2	12	40	0.2
4	48	100	24	2	6.0	2	16	54	0.15
5	60	125	24	2	7.5	2	20	67	0.1

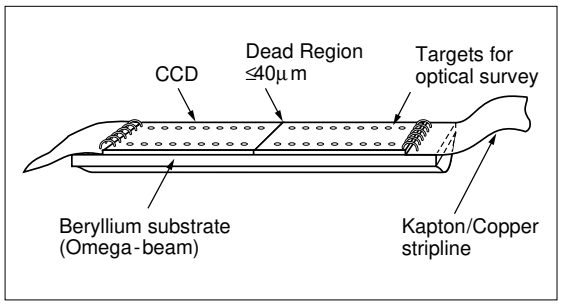

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Fig. 7 Conceptual 2-CCD ladder design. The beryllium omega-beam substrate assembly is no thicker than that used for the SLD detector, but over 50 times more rigid.

intrinsic ladder flexibility would otherwise make them particularly susceptible to such distortions. The cryostat consists essentially of a foam shell with adequate thermal insulation characteristics, and thickness ~ 0.5% X_0. This material, being outside the vertex detector, has a negligible effect on the impact parameter precision. The detector is cooled to the operating temperature of around 180 K (chosen to reduce the effects of bulk radiation damage in the CCDs to an acceptable level) by nitrogen gas.

The key to the detector performance is the design of the ladders; see Fig. 7. Each ladder consists essentially of a substrate (probably beryllium) which (in conjunction with the endplates of the support structure) provides the mechanical support for the CCDs. The CCDs are attached face-up to the ladder substrate. By novel processing procedures discussed in Section 3.2 the CCDs can be thinned to the edge of the epitaxial layer (~20 μm overall thickness).

The devices on the 1-CCD ladders (B1 and B2) can be read out through each end, while those on the 2-CCD ladders are read out only through the outer end. Thus (unlike the SLD detector) there is no need to route any electrical connections to the inner region of the ladder, hence permitting the minimal ladder thickness. The overall ladder (or barrel) thickness in the active vertex detector volume thus becomes 0.07% (substrate) + 0.02% (adhesive) + 0.03% (CCD), a total of 0.12% X_0, compared with 0.4% X_0 for the SLD detector. These thin barrels will permit unprecedented performance capability; even for low momentum tracks, one is able to make effective use of the point measurement precision of the CCD, which has been measured in SLD to be approximately 3.5 μm. Simulating the performance of the vertex detector, we obtain the following for the impact parameter measurement precision (in microns) for a track of momentum p GeV/c and polar angle θ :

$$\sigma_{XY} = \sigma_{RZ} = (4.5 - R/8) \oplus 5.5(1 - R/12)/\left(p \sin^{3/2}\theta\right)$$

where R is the radial distance from the IP at which the impact parameter is evaluated, in mm. Note that for decays that occur at a radial position which is a significant fraction of R(B1), the impact parameter precision at the vertex is considerably improved. For high energy jets, this leads to an enhancement in the fraction of secondary/tertiary vertices found.

A number of other technical points should be noted. The inner section of beam-pipe (of radius 10 mm) is made of beryllium, followed by a transition to stainless steel for the conical section and beyond. By using thin walled stainless steel in the region where the beam-pipe penetrates the cryostat, the heat flow into the cryostat can be held down to a comfortable level.

The most difficult problem with the SLD front-end electronics (which eventually forced a reduction in the readout frequency from 10 to 5 MHz) was crosstalk between the clock pulses of the CCD readout register and the analogue signal output. A key requirement of the new R&D programme is to increase this frequency to the HDTV-like clocking rate of 50 MHz with low clocking-related noise. We can then expect to read out the background-critical Barrel 1 within one bunch train interval (BTI) of 5.5 ms, the much quieter outer barrels within a sufficiently small number of BTIs (see Table 1), and all this with a modest number of output channels (384, comparable to that of the SLD detector). With this arrangement, the front-end electronics can be accommodated within a very small polar angle range, attached to the outer surface of the conical SR mask M1 shown in Figs. 3 and 4. As with the SLD detector, all electronics other than the CCDs themselves and miniature line drivers for the analogue signals are located outside the cryostat, so that the almost massless gaseous cooling can be retained (total in-cryostat dissipation ~ 20W).

The point measurement precision and tracking efficiency (99.5% on the middle layer) measured with the SLD detector permit us to be

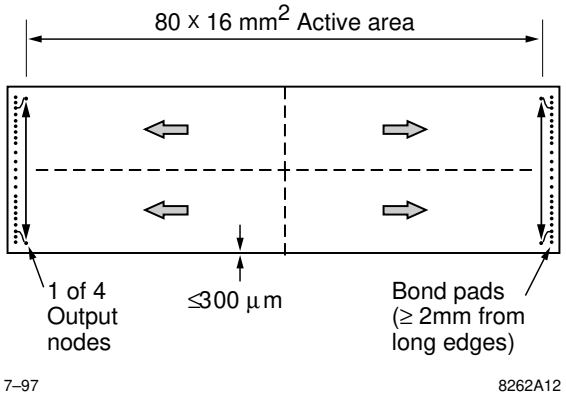

Fig. 8 CCD32 basic architecture. The parallel register (I register) shifts signal charge packets to each end of the device. The serial register (R register) at each end shifts charge packets to a pair of output circuits. Chip area = 13 cm^2.

extremely confident in the recognition of 1-prong charm decays with this 5-layer detector design, in order to enhance the efficiency for charm identification as indicated in Fig. 2. Under the estimated background conditions, the incidence of fake tracks in such a sample will be negligible.

2.3 State-of-the-art in CCD design, and short-term prospects

The evolving physics capability of CCD-based vertex detectors (from the 0.2 Mpixel NA32 detector in 1985 [9] to the 120 Mpixel SLD detector in 1992 [10] and the 307 Mpixel SLD upgrade in 1996 [6]) depended partly on developments in the system engineering as experience was gained and new ideas emerged, but more importantly on developments in CCD design and manufacturing technology. Here the particle physics users have been fortunate. Despite our small market for CCDs, the requirements overlap sufficiently with other scientific and defence customers that we have been able to profit from their ongoing R&D programmes. Progress continues to be rapid (pushed also by the huge investment in CCDs for HDTV applications) and there are currently available devices which come close to the requirements for the future collider detector in several respects. Discussions with CCD manufacturers suggest that the greatest challenge in reaching our performance specifications may be less in the CCD design than in the overall *system* design. Nevertheless, the readout conditions and signal range required are unique, and past experience has shown that we may well uncover CCD performance problems that are serious for our application but invisible to others. As with any novel detector system, only by studying these devices in a well controlled test programme will it be possible to assess their suitability for our application, and to initiate appropriate developments where there are shortcomings.

It should be noted that the NA32 experiment used devices with type number CCD01. The SLD upgrade commissioned a full custom design which was labelled CCD32. The manufacturer EEV [11] is now up to CCD76, so the past two years have brought a large number of new designs and innovative ideas into being, from one manufacturer alone. Some of these developments appear to be very interesting for our application. Indeed, the fruitful collaboration between UK particle physicists and the British company EEV over the past 20 years has been essential to the successful development of CCDs as particle detectors.

The critical CCD performance requirements, current state-of-the-art, and perceived room for development, can be summarised as follows:

Imaging register Required transfer rate 1 MHz. Register width ≤ 24 mm.

For CCD32, sketched in Fig. 8, the width was 16 mm and the rate limit was 200 kHz. A recent option is to go from a 3-phase to a 2-phase register, but this may not significantly increase the rate capability (needs detailed study). Another option is to greatly reduce drive voltage (from ~ 12V to ~ 3V) by more refined control of the implant levels. This will be extremely useful in drastically reducing the detector power dissipation.

Gate capacitances may be further reduced by use of higher resistivity epitaxial material, possibly also thicker than the current 20 µm. This needs detailed study. A thicker epitaxial layer could also be valuable for distinguishing between signal and background clusters (the latter due to spiralling electrons).

The best prospect for achieving the desired transfer rate is with metal tracks over the electrodes, but the technology required to achieve this is quite complex.

Readout register Required transfer rate 50 MHz. Register length ≤ 24 mm.

Here a 2-phase register (as in CCD32) is planned, but again with the possibility of reduced drive voltages.

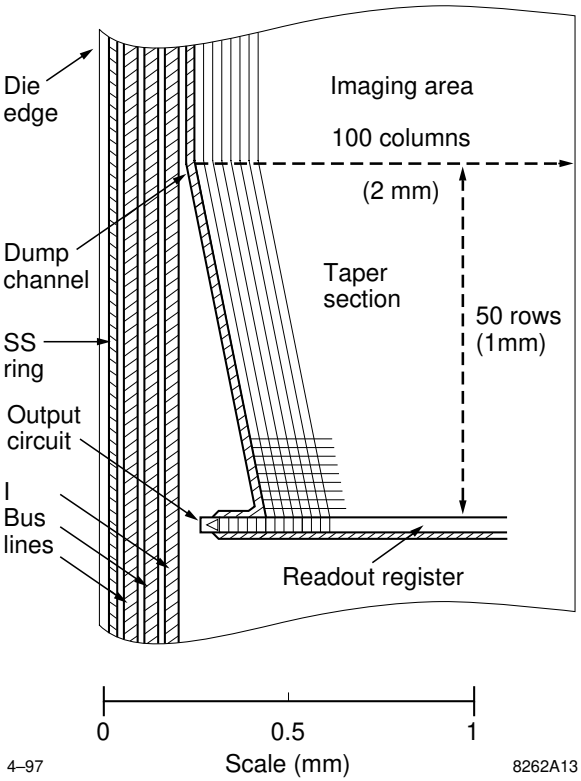

Fig. 9 Sketch of taper section in each corner of CCD32, providing room for the output circuit within the device width required for the image area bus-lines. The SS (substrate) ring provides edge passivation, and the dump channel defines the sensitive area of the detector.

Given the beneficial effect of drift fields in the structure, the maximum charge transfer frequency is given by

$$f_{\max} \sim \frac{5\times10^5}{L^3}\,\mathrm{MHz}$$

where L is the CCD element length in microns. Thus we have $f_{\max}$ ~62 MHz for devices with pixels of length 20 µm. However, this is purely a theoretical limit for a simplified field profile. Irregularities in the I-to-R transfer structure can degrade performance. Detailed simulation and experimental study are required.

Output circuit Up to 6 outputs per register. ≤ 100 e^- rms noise at 50 MHz.

This is extremely challenging. As shown in Fig. 8, CCD32 had two outputs per register. In order to fit the circuitry in the available chip width (without increasing the dead region along the edge of the device) the active area was slightly tapered in each corner region. The

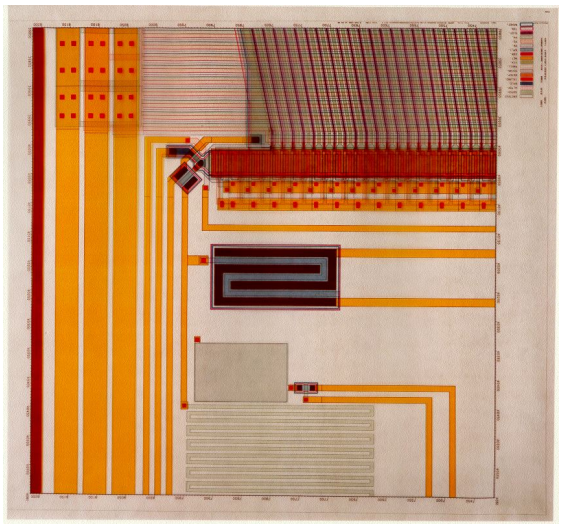

Fig. 10 Design layout of corner region of CCD32. Elements can be identified by relating to Fig. 9.

general idea is shown in Fig. 9, and the actual design layout in Fig. 10. On the bench, this device delivered the required noise performance at 10 MHz, but was limited to 5 MHz under experimental conditions.

EEV have already produced devices with multiple outputs (see Fig. 11). The main problem is increased R clock feedthrough, which was circumvented in the architecture shown by means of a series of dummy outputs. We would prefer to avoid these since they double the analogue power dissipation and degrade the noise by a factor $\sqrt{2}$. There are ideas for reducing the R clock feedthrough, but they need detailed study and experimental tests. There may be a fundamental problem with the bandwidth (limited by the inter-stage time constant in a 2-stage source follower) but this needs study. An alternative approach (e.g. the double gate floating surface detector of Toshiba [12]) may be possible. This has spectacular (sub-single-electron) noise performance, but may not be compatible with a deep n-channel design. Here there is a need for new ideas.

One positive feature of our application is the low duty cycle readout, so pulsed power (as implemented in SLD) can help. This also reduces the possible impact of light generation by the output circuit, which is a common feature of multi-stage source followers.

Fast-clear capability Triggered clear with duration ≤ 700 ns for TESLA.

CCDs have been provided with drain diffusions to achieve anti-blooming features. By including additional vertical gate structures,

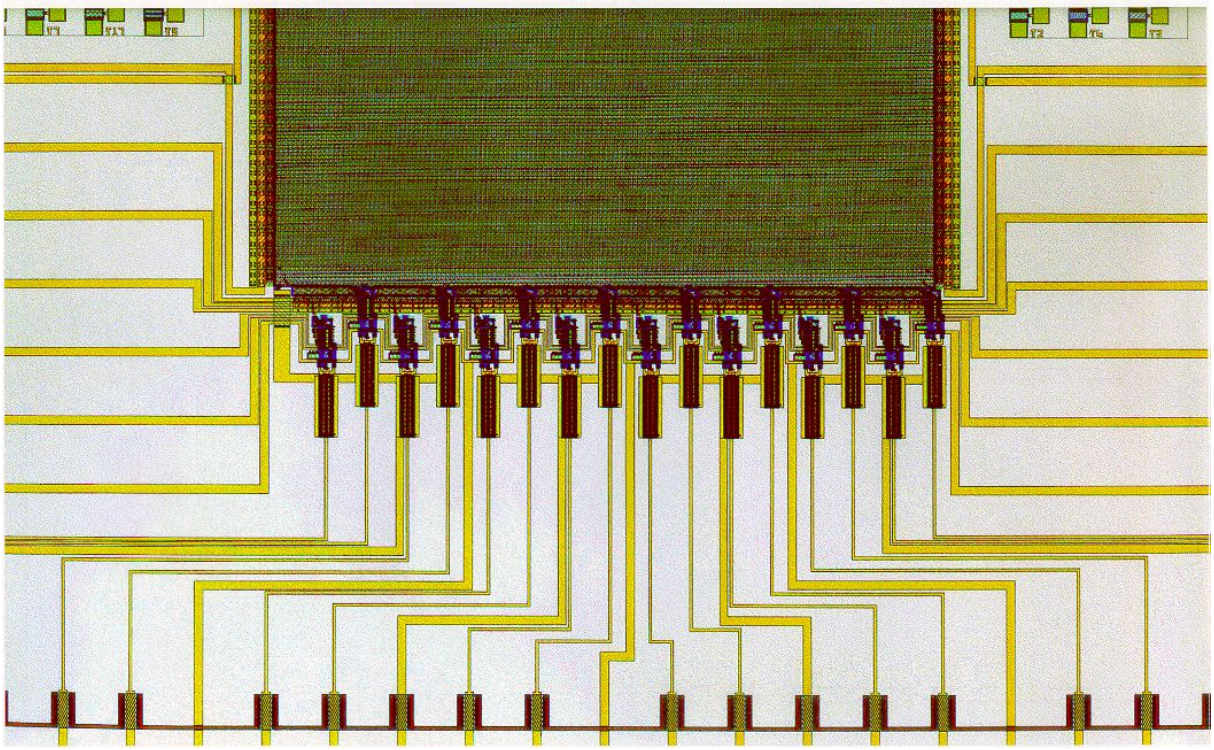

Fig. 11 Layout of an advanced CCD design with 8 outputs along the length of the R register (at the bottom of the imaging array). Each signal is taken differentially with respect to an adjacent dummy output, which sees the same R feedthrough signal as the real output.

it is possible to provide a gated clear functionality. Such a structure would result in some loss of signal from min-I particles (that within and adjacent to the depletion region of the drain diffusion), but this should not lead to any serious loss of efficiency if the goals set for the system noise can be achieved. More problematical is the distribution of the clear signals over the area of the device, including the effects of parasitic capacitance to the imaging gates. This will require a detailed design study, tests with lumped equivalent circuits, and finally the fabrication of custom CCDs. While such triggered clear features have been implemented previously, the large CCD area combined with the speed requirements for TESLA constitute a unique challenge

Radiation Hardness

Unless some of the novel features of the output circuit produce unexpected radiation sensitivity, the weakest element in the CCDs in this application will continue to be degradation in charge-transfer efficiency (CTE, often described by the charge-transfer inefficiency: CTI=1-CTE). This is induced by bulk traps generated both by ionizing radiation and by hadronic interactions. The effects are different within the imaging and readout registers, and depend on the nature of the radiation and the dose, operating temperature, clocking rate, background signal level, as well as on a number of design details. This is discussed in Section 3.7. For the present, it should be noted that the CTI is proportional to the storage volume of the charge packet in the imaging or readout register. Given the small charge packets for which the charge transfer performance is of concern in our application (min-I signals of ~ 2000 e^-) there are a number of possibilities for drastically reducing the storage volume. One such idea has been demonstrated even for much larger charge packets in the EPIC XMM devices. This could be a fruitful area for the R&D programme, in conjunction with the CCD manufacturers.

Recently, an old idea has been revived, with some refinements, namely the use of *p*-channel devices for increased resistance to bulk damage, due to the absence of the Si-E centre. Such devices have been manufactured and will be tested for our application area. Despite the lower hole mobility, there is reason to believe that the speed capability may be sufficient for our requirements.

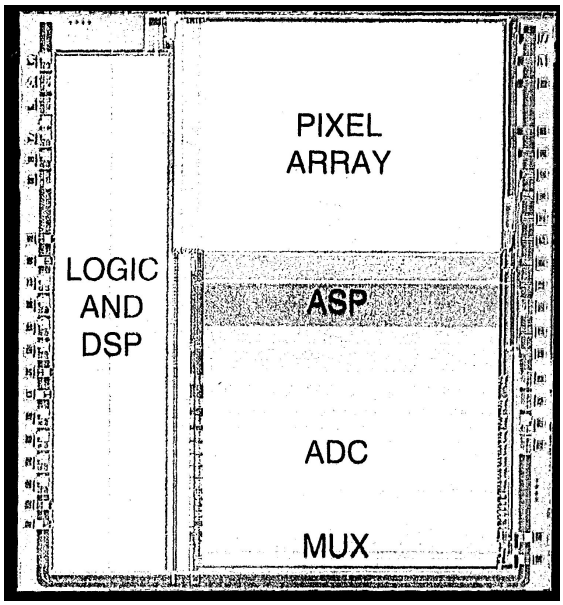

Fig. 12 Recent CMOS APS device from the Photobit Corporation. As well as the limited area of the pixel array, it should be noted that only 20% of the area of each pixel is photosensitive, due to the amplifier and address logic within the pixel.

Wafer size and device yield

The largest devices for the future linear collider design will require 6" wafers, whereas 5" is the largest size currently in use for the manufacture of CCDs for the scientific market. Fortunately, EEV are progressively upgrading their processing equipment for the larger size, and this will be standard by the time production of devices for this experiment needs to begin. The defect density is constantly being improved and, even with the present processing quality, the anticipated yield for the largest devices ($\sim 30\ cm^2$) would be acceptable.

As well as fatal defects, CCDs may fail the stringent requirements for min-I detection due to low level processing anomalies creating local potential wells that are too shallow to detect by the standard test procedures. For the SLD CCDs, tests were developed involving data samples with millions of X-ray hits (possible due to the high speed readout) which pin-pointed such defects over the CCD area. Most devices were essentially perfect, but CCDs from one batch exhibited a significant level of problems. Fortunately, high powered microscopic examination at RAL revealed the cause of these defects, and the manufacturer was able to understand and avoid them in future batches. However, this illustrates the essential requirement for representative high speed test facilities if processing problems are to be understood and controlled. Other scientific users may be oblivious to some of these problems, since the effects depend critically on the readout conditions.

2.4 Possible alternative technologies

An enormous effort has been put into designing active pixel sensors (APS) for the LHC general-purpose detectors. Here the principal challenge is the unprecedented requirement for radiation hardness. This inflicts a heavy price in detector thickness, which would make them unsuitable for the LC application, particularly since the radiation environment is so much more benign (by at least a factor 10^6). Comparing critical parameters, the CCD-based detector has $\sim\frac{1}{10}$ the layer thickness and $\sim\frac{1}{20}$ the pixel area of the APS design. Consequently it has a much higher tolerance to background, much higher tracking precision, and (important for low momentum tracks) causes much less multiple scattering. Note that for both types of detector, for the X-band machine the background would be integrated through the bunch train.

The only factor in favour of the lower performance APS technology would be a neutron radiation background beyond the tolerance limits for CCDs. In this event, it is clear that the hybrid APS detector of LHC would represent gross overkill in radiation resistance. It might then be appropriate to consider monolithic devices such as silicon thin film transistor (TFT) arrays or CMOS APS devices. For the latter, the technology is moving forward rapidly, driven by potential commercial markets for still and video cameras. These can be made much thinner than the hybrid devices and also with small pixels comparable to CCDs. However, the current commercial devices are manufactured using the mainstream CMOS processes and have an intrinsically thin active region ($\sim 1\ \mu m$), insufficient for min-I detection. This can of course be avoided by branching out into 'non-standard' processes, as happened in the '70s with CCDs, but so far there has not been much impetus for this. Furthermore, while they can be made physically thin, monolithic APS devices by definition carry an overhead of peripheral processing: some or all of the timing generator, row select, control registers, interfaces, biases, ASP (analogue signal processing), ADC, MUX and column select logic

are on the chip and may occupy 60% or more of its area (see Fig. 12). As well as adding effective layer thickness in a 4π detector system using a tiled APS geometry, this logic adds power dissipation, hence additional mass associated with a higher capacity cooling system (e.g. evaporative cooling).

In summary, CCDs combine the attributes of high segmentation, high spatial precision, low power dissipation (since only the bare minimum of processing, two transistors, is on-chip) and extremely low overall thickness per layer. However, the extremely high degree of multiplexing makes them slow to read, and the requirement of transporting the raw charge packet through centimetres of silicon makes them prone to bulk damage from hadronic interactions. The readout characteristics of CCDs fit in harmoniously with the time structure of linear colliders, and the hadronic backgrounds at the SLC and the X-band machine are modest. With the 0^0 crossing angle, there may however be a problem at TESLA. We shall constantly review the situation and watch the rapidly evolving CMOS APS detector programme with interest. Should a case emerge for such detectors at TESLA, our currently proposed test facilities would provide much of the infrastructure required to evaluate these devices for min-I particle detection.

It should finally be noted that recent progress with large area, flat panel amorphous silicon imagers, primarily under development for medical X-ray applications [13], may in future lead to very exciting particle tracking possibilities. For the present, their spatial resolution makes them more credible as candidates for external tracking than for vertex detectors, but this area certainly needs to be watched.

3. Proposed R&D Programme and Test System

3.1 Ongoing physics studies and detector design

We intend to refine the flavour-tagging studies described in Section 1.5. Since we want to design a detector with the broadest possible discovery potential, in the first phase a matrix of jet-by-jet tagged-flavour probabilities will be built up for jets of true generated light (*u,d,s*), charm, bottom, top and gluon flavour, as a function of jet energy and polar angle. This will establish benchmark flavour-tagging performance in a 'model-independent' manner, i.e. not restricted to specific SUSY, Higgs, Technicolour… scenaria, none of which may correspond to nature.

We expect these studies to be sufficient to assess the main implications of the required physics capability on the principal design features, namely pixel size, inner layer radius, and ladder thickness.

The second stage will comprise generation of realistic samples of events representing reasonable benchmark physics processes identified by each working group, and application of the existing parameterised version of the vertex detector response to obtain a first-order understanding of the efficiencies and purities for jet/event *b*- and *c*-tagging in specific realistic event environments. By definition these processes will be chosen to be most challenging to various aspects of the overall detector performance. Background processes will, of course, be included in all cases.

In a third stage, calorimeter information will be incorporated to make the jet topology reconstruction more realistic, as well as to study isolated π^0 reconstruction; previous studies have shown that the latter can significantly enhance the power of flavour identification.

In parallel with these steps the vertex detector simulation will be refined to match the other detector elements, especially the main tracking chamber(s), as the GEANT models are developed. In addition, the topological secondary-vertex-finding algorithms are continually being refined at SLD and LEP, and we shall take advantage of improvements gained from analysis of Z^0 data to maximise the flavour-tagging potential at the LC. Finally, additional relevant information from other detector subsystems, for example particle identification, will be included as the technology choices are made and simulations are developed.

Turning finally to the low-level detector design, the above discussion suggests that this can realistically be almost decoupled from the higher level studies, as these advance beyond the level of detail already covered. We have already produced estimates of the vertex detector material for the GEANT simulations, and the primary tasks of the ongoing detector design are now those which can influence the R&D programme. There is firstly the question of the silicon active thickness. To date we have assumed ~ 20 μm (making each detector element approximately a cube of side 20 μm) but there could be an argument for a thicker epitaxial layer, possibly around 50 μm, perhaps

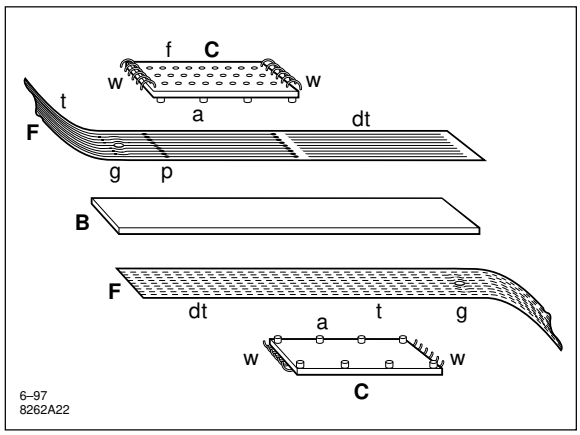

Fig. 13 Exploded view of ladder used in the SLD upgrade detector, showing the main components. *B* = beryllium substrate. *F* = Flex-line with traces *t*, dummy traces *dt*, bond pads *p* and ground aperture *g*. *C* = CCD with adhesive pads *a* and wire bonds *w*.

also of higher resistivity (deeper depletion). Since (unlike at SLD) there is expected to be a small X-ray background at the linear collider, there will be no signal/noise rate penalty in increasing the active detector thickness. The spiralling pair electrons would be better discriminated from signal particles by having a thicker detector, though with the calculated rates, this additional feature may not be important. What could be interesting would be the improved spatial resolution (by refined cluster centroid finding) achievable with a thicker detector. Sub-micron resolution may be possible. However, this needs to be weighed against the effects of increased multiple scattering and secondary interactions. Such studies require a more detailed simulation of the detector signals, track finding and fitting than has been undertaken to date. From the SLD work, we do have very realistic code for generating and transporting the signal charge in such detectors, based on the calculations of [14] and implemented explicitly for CCDs by Su Dong. Fine tuning the CCD design (pixel size and active layer thickness) will be important, in parallel with the R&D programme, in defining the prototype custom devices that will eventually be manufactured for this project.

As well as the actual detector, other aspects of on-CCD and local electronics need to be carefully simulated, if the performance specifications are to be met without a huge amount of trial and error, which would be simply unaffordable. The first requirement is for clean delivery of the R-drive pulses, and for adequate on-CCD isolation between these and the analogue readout circuits. The second is for adequate bandwidth and noise performance in the analogue outputs. For the latter, EEV have well developed simulation code, which has been proven on CCD32 and numerous other devices. For the former, we attempted simulations for the SLD upgrade detector using commercial software able to evaluate inter-element capacitances in systems of arbitrary complexity. However, the first experience with the SLD system testing revealed much higher crosstalk than had been calculated, mostly coming from the striplines connecting the local electronics to the CCD ladders. Tests revealed that the problem arose from electromagnetic radiation coupling from the drive to the analogue circuitry. Even the CCD wire bonds are believed to contribute significantly to this crosstalk.

Commercial software has recently become available [15] that will enable a full simulation of these effects. The program EMLAB_ISE is based on the finite difference time domain method. It is a general purpose Maxwell solver that can be used in a wide range of applications. It is combined with TCAD_ISE, which provides full 3-D simulation of semiconductor device structures. This program will provide accurate modelling of the charge transport within the CCD, including visual display of the time development that may be of considerable help in designing devices with enhanced radiation resistance, as mentioned in Section 2.3. While the full commercial cost of such software is high, the academic price is reasonable, and it can certainly be expected to save a large amount of time and money in the longer term, by guiding the design and layout of system elements both on and off the CCD. While the use of such software for the off-CCD electromagnetic simulation is reasonably straightforward, the device simulation requires considerable understanding of the CCD structural details. Here we would work closely with EEV, where many of the critical parameters (e.g. doping profiles) have been studied in detail both theoretically and experimentally. They have available a wealth of data which will permit reliable simulations to be made, in considerable detail.

3.2 Mechanical structure

According to current plans, much of the mechanical structure of the detector will closely follow that of the SLD upgrade detector [6]. The gas cooling system (with a mix of vacuum

jacketed external pipes and low-mass foam-insulated internal pipes), cryostat, beryllium detector support shell, etc. are all expected to follow the design developed for SLD. The one area that can manifestly be greatly improved, with a corresponding enhancement in the physics capability of the detector, is the CCD ladder design. It is proposed to concentrate some of our R&D effort on this topic.

For the SLD upgrade detector, the ladders were reduced by a factor 3 in thickness compared to the original detector, to $0.40\ \%\ X_0$. The structure of these ladders is illustrated in Fig. 13. The basic support structure was a thin beryllium beam $21\ \text{cm} \times 1.6\ \text{cm} \times 0.381\ \text{mm}$ (0.015 in) thick, having an initial flatness after machining of better than 100 μm sagitta over its full length. Onto this was bonded, in one operation for both sides, a pair of kapton/copper microstrip lines: 13 μm kapton, carrying $\frac{1}{2}$ oz (17.8 μm) rolled, annealed copper traces, passivated by a kapton cover layer. These circuits ran the full width and length of the ladder, with 'pigtail' extensions to carry the electrical traces to micro-connectors, approximately 5 cm beyond each end of the ladder. An acrylic thermoplastic adhesive was used to attach the microstrip lines to the motherboards under pressure, at a temperature of approximately 180°C. The CCDs (thinned by mechanical lapping to ~ 180 μm) were attached to the ladders by adhesive pads, and wire bonded from each end of the CCD to gold-plated pads (electroless gold with an electroless nickel barrier) on the traces of the microstrip lines.

This arrangement of the beryllium substrate sandwiched between two essentially identical microstrips provided a balanced structure with respect to thermally induced stresses. Note the presence of the dummy traces (Fig. 13) which optimally balanced the real traces carrying connections to the inner end of the CCD on the opposite face of the ladder. On cooldown, the thin kapton/copper skins were obliged to follow the contraction of the beryllium substrate. Internal forces within this assembly were considerable, but the tendency to bow was minimized by the balanced structure.

However, this balance was in principle disturbed by the attachment of the CCDs on either side of the ladder, one at each end. Furthermore, the elastic modulus of silicon is too great to allow a rigid connection to the beryllium, given the considerable difference in thermal expansion coefficient between these materials. This situation was dealt with by attaching the CCDs with eight relatively thick (200 μm) pads of NuSil, a phenyl silicone adhesive. This adhesive, having a low elastic modulus and a very low glass transition temperature (well below 170 K), provided a compliant bond which ensured excellent mechanical stability with low shear stress for repeated thermal cycling of the detector. Thus on cooldown, the ladder motherboard felt very little stress arising from the CCDs attached to it.

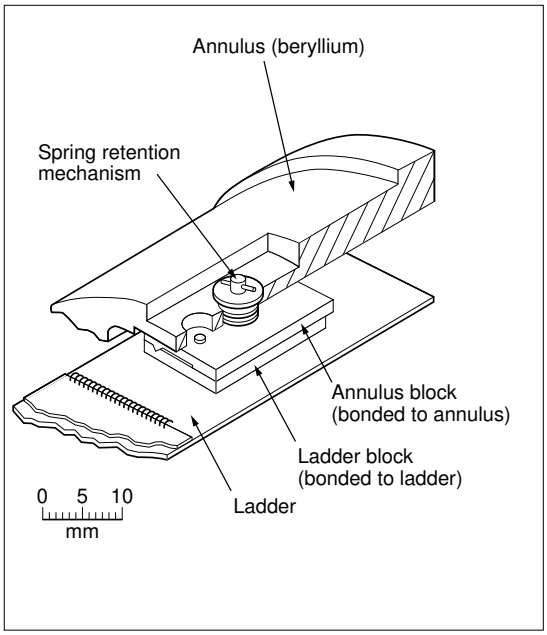

Fig. 14 Sprung blocks with sliding joint (vee and flat contact areas) for relief of stress due to differential contraction between ladder and support structure.

There were two sources of potentially damaging thermal stress which needed to be considered. Firstly, the sandwich described above would never be perfectly balanced. Measurement of unsupported samples cooled to 200 K revealed shape changes which could be described by a quite uniform change of curvature (bow) along the length of the ladder of magnitude in the range 50 to 100 μm. This of course would be quite unacceptable for any assembly required to achieve tracking precision of a few microns. However, the ladders in the assembled detector were not free, but attached at each end to the essentially rigid support structure, via the ladder block/annulus block assemblies sketched in Fig. 14. These blocks were themselves attached to their substrates with thin layers of adhesive, and their rigidity in this assembly was such that a ladder which would bow by 100 μm when unsupported, would have its sagitta reduced to 0.8 μm when attached to

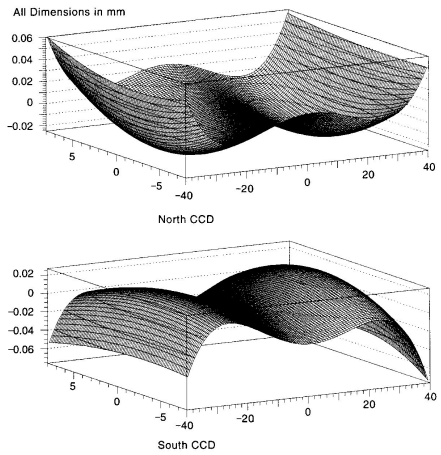

Fig. 15 Typical surveyed shapes of CCD active surfaces in the SLD upgrade detector. The North and South CCDs are on the upper and lower surfaces of the ladder respectively.

these block assemblies. Thus the tendencies of the unsupported ladder substrates to flex on cooldown were suppressed extremely effectively in the overall support structure. However, these attachment blocks, while solving one potential thermal problem, tended to create another one. The support structure can be considered to be a homogeneous beryllium assembly. However, the operating temperature of the overall detector is by no means uniform. Due to the thermal dissipation on the CCDs, the ladders are slightly warmer than the parent structure, and the outermost ladders are warmer than the inner ones due to the flow direction of the coolant gas. A minute excess expansion of a rigidly clamped ladder relative to its supports would induce massive bowing of that ladder. This problem was avoided by allowing one degree of freedom (longitudinal sliding) between one pair of ladder/annulus blocks for each ladder (see Fig. 14). Including this low-friction sliding joint in the overall assembly guaranteed extremely good shape stability of the ladder substrates under thermal cycling. Stress relief between the dissimilar materials used in this assembly (ceramic blocks on beryllium substrates) was again achieved by controlled-thickness layers of the phenyl silicone adhesive mentioned above. In this situation an adhesive layer of 100 μm thickness was sufficient to provide the necessary stress relief.

For the CCDs themselves, they could be expected to track precisely the movement of their ladder substrate, as long as their eight adhesive pads were of uniform diameter (~ 1 mm) and thickness. Appropriate procedures were developed to guarantee that this was the case and these were backed up by careful quality control.

From the excellent stability of the vertex fits through the 3-year period in which this detector has been operated, it is apparent that this design achieved its goals. No measurable shape variations of the detector have been suggested by the data, other than one transition in which the operating temperature was reduced by 40°C. This is discussed in Section 3.7.

While the stability of the SLD detector was all one could ask, and encourages us to retain the same design principles in the future, the CCD shapes were rather complex (see Fig. 15). While the degree of irregularity is highly exaggerated in the plots, it is at a level where these shapes (and variations between them for different CCDs) are significant in the fitting of oblique tracks. These shapes reflect the inherent concave form of the thinned devices (due to the higher thermal expansion coefficient of the oxide grown at high temperature on the processed side) compounded by the stresses from the 8-point support, which take effect once the assembly jigging (which holds the devices flat during curing of the adhesive pads) has been removed.

These observations, together with the goal of reducing the ladder thickness by a further factor of 3, suggest a revision of the ladder design principles, taking advantage of the newly available CCD design options.

The CCD design goals for the new project are defined partly by operational requirements (as will be discussed in Sections 3.3 and 3.4) and partly by mechanical design considerations, as follows:

- Layer 1 and Layer 2. CCDs cover full barrel length, so they can all be fitted on the inner ladder surface. Multiplexed readout at both ends, with no requirement of electrical tracks within the sensitive aperture.
- Layers 3-5. CCDs (two per ladder) buttable, with a central inactive region of ~ 40 μm staggered in polar angle between each layer. Again, all CCDs on inner ladder surface (unlike in SLD) and no electrical tracks within the sensitive aperture.

This design frees up the outer surface of each ladder to provide enormously increased mechanical stiffness (Omega-beam structure) as shown in Fig. 7. This in turn permits a more aggressive approach to the CCD thinning and attachment. The suggestion we wish to pursue is to thin the devices all the way down to the edge of the epitaxial material, by a combination of mechanical lapping and chemical etching. After thinning, the back surface will be

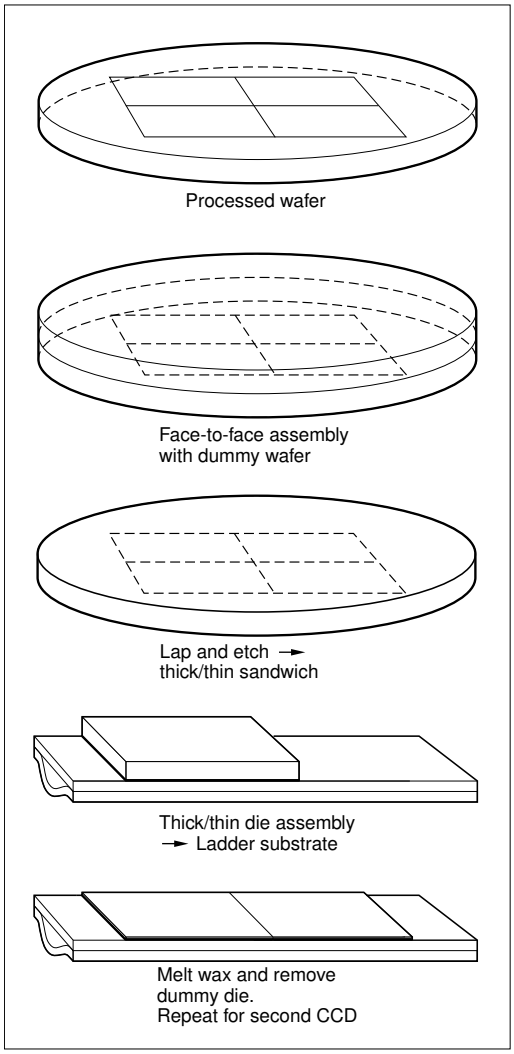

Fig. 16 Hypothetical sequence of operations in thinning the CCDs and attaching them to low-mass substrates.

implanted with a *p*-layer to provide efficient reflection of signal electrons which diffuse towards this surface. Such procedures have already been developed for the production of optically back-illuminated devices. What has still to be developed are the procedures for transferring these delicate devices to the beryllium substrates. These ultra-thin CCDs are of course not self-supporting (indeed they would curl up tightly if released). Various ideas exist for such procedures, which will need to be explored. From past experience, the optimal solution is likely to be rather different from these initial ideas.

Figure 16 gives an idea of a possible procedure for construction of the new ladders. A processed wafer is attached face-down with wax adhesive on a matching dummy wafer. The processed wafer is then thinned by a combination of mechanical lapping and chemical etching, to the edge of the epi layer. The back surface is now implanted with boron and activated. Using an infra-red microscope to guide the diamond saw, the assembly is then diced. The thick/thin die assemblies are then attached to the ladder substrate with an appropriate adhesive. Finally the dummy dice are removed by heating the ladder and melting the wax. The plan is to bond the CCDs to the substrate with a thin adhesive layer ($\sim 50\,\mu$m) and full-area coverage. The choice of adhesive is one of the open questions. Given the cross-section and elastic modulus of the silicon relative to substrate, the expectation is that the assembly will cool down with very little overall bowing. If the adhesive coverage is complete, stress should be uniformly distributed through the CCD and cracking of the crystal may be avoided.

The main purpose of the mechanical R&D programme is to develop reliable procedures for making these very thin ladders, initially using non-working devices, moving on later to working CCDs. The distortions in unsupported ladders on cooldown will be monitored, using an automated coordinate measuring machine with excellent ($\sim 2\,\mu$m) depth precision. We hope to obtain occasional access to one of these modern systems, perhaps the one to be used for measurement of the ATLAS SCT modules.

Should problems arise with the beryllium substrates, other materials such as boron carbide with expansion coefficients better matched to silicon will be considered. Apart from its excellent mechanical properties, one strong advantage of beryllium for SLD was the fact that it provided a very effective ground plane. At the readout frequencies being considered now, this could be critically important. Thus the choice of substrate material and the overall ladder design are linked by a number of possibly conflicting aspects. On past experience, it can be hoped that dedicated R&D efforts plus the time to study ideas in detail will pay the dividends of uniquely thin detectors combined with excellent mechanical stability at the operating temperature. Lack of time would enforce lesser goals with consequent loss of capability for physics.

It is true that the multiple scattering term in the impact parameter formula scales only with the square root of the layer thickness, but for bremsstrahlung and secondary interactions the dependence is linear.

Beyond the ladders, the principle of attachment to extremely rigid annuli with a

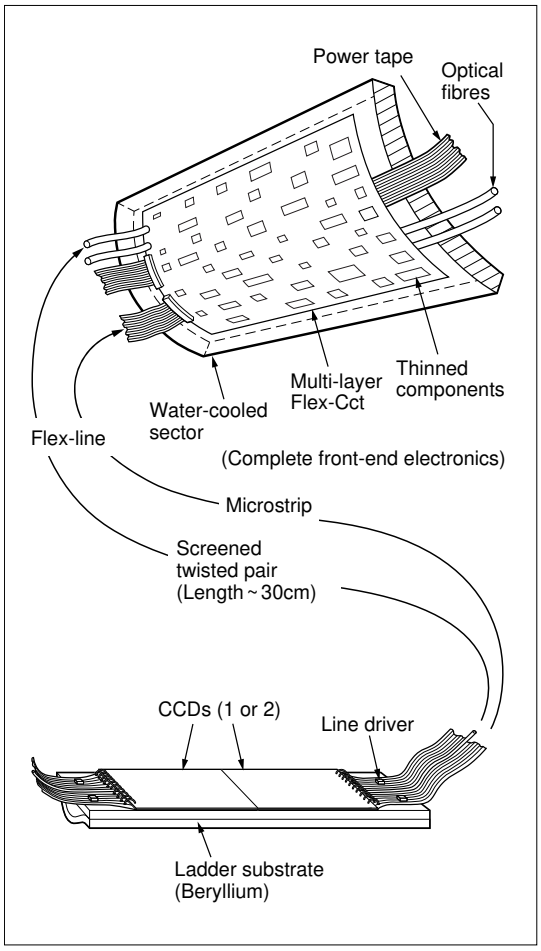

Fig. 17 Conjectural layout of a segment of local electronics in the real detector, mounted on part of the M1 mask.

fixed joint at one end, and 1-dimensional sliding at the other, will be maintained. Ideas for the flex-lines attached to each end of the ladder are discussed in Section 3.3; they should make no impact on the mechanical design or stability of the detector. This is an important advance on the SLD system, where the tracks running below the CCDs had significant mechanical impact (additional material, thermal stresses, etc.).

Finally, a topic which always threatens to adversely affect the mechanical design is that of the detector cooling. As long as the overall in-cryostat power dissipation is below about 30 W, gas cooling is effective, and this carries essentially no material overheads. Some ideas for the future detector (e.g. drive ICs wire-bonded locally to the CCDs) would have violated this desirable feature. While such an approach cannot be ruled out till the more elegant solution has been shown to work, it remains very much a fallback option at this stage. For the CCDs themselves, the dissipation associated with fast-clocking the I- and R-registers could be a problem. Here the design developments noted in Section 2.3 (reduced gate capacitance and possibly drastically reduced operating voltages) give promise of a way out. The low readout rate ensures that pulsed power to the analogue circuit will maintain its average dissipation at a low level. Consequently it seems reasonable at this stage to plan on preserving the gas-cooling concept which has been so effective in minimizing the material budget in SLD.

3.3 Drive and readout electronics

For the real detector, as with SLD, the plan is to generate the CCD drive pulses locally, but external to the cryostat. Similarly for the analogue signal processing and A/D conversion. Thus, the long external connections will again consist only of a few power tapes, and optic fibres for timing control and for the multiplexed digital readout of the CCD data. The physical layout of the local electronics for this system is sketched in Fig. 17.

For the phase 1 R&D system, we can usefully disregard these longer term requirements, designing for the present a much more flexible modular system for all the electronics outside the cryostat. This has the obvious advantage that design developments from our own collaboration or from our international colleagues will most easily be incorporated into our system, with no disruption to other areas. The overall plan is for a VME-based system as indicated by the block diagram in Fig. 18.

The general aim is to be able to handle a wide variety of CCDs with different pinout and different functional requirements (e.g. 2- or 3-phase registers, different numbers of analogue outputs). This can be achieved firstly by designing a flexible computer-controlled system for bias control, drive pulse generation and overall readout sequencing. Secondly, one needs a simple arrangement for matching the module inputs and outputs to the corresponding pins on the CCD under test, bearing in mind the speed requirements and concerns regarding crosstalk between R-drive and analogue signals. This leads to the connection scheme shown in Fig. 19.

The first component needed for each CCD type is a custom 2-layer motherboard, in which the signals are distributed for compatibility with the local flex-line. The CCD is adhesive bonded

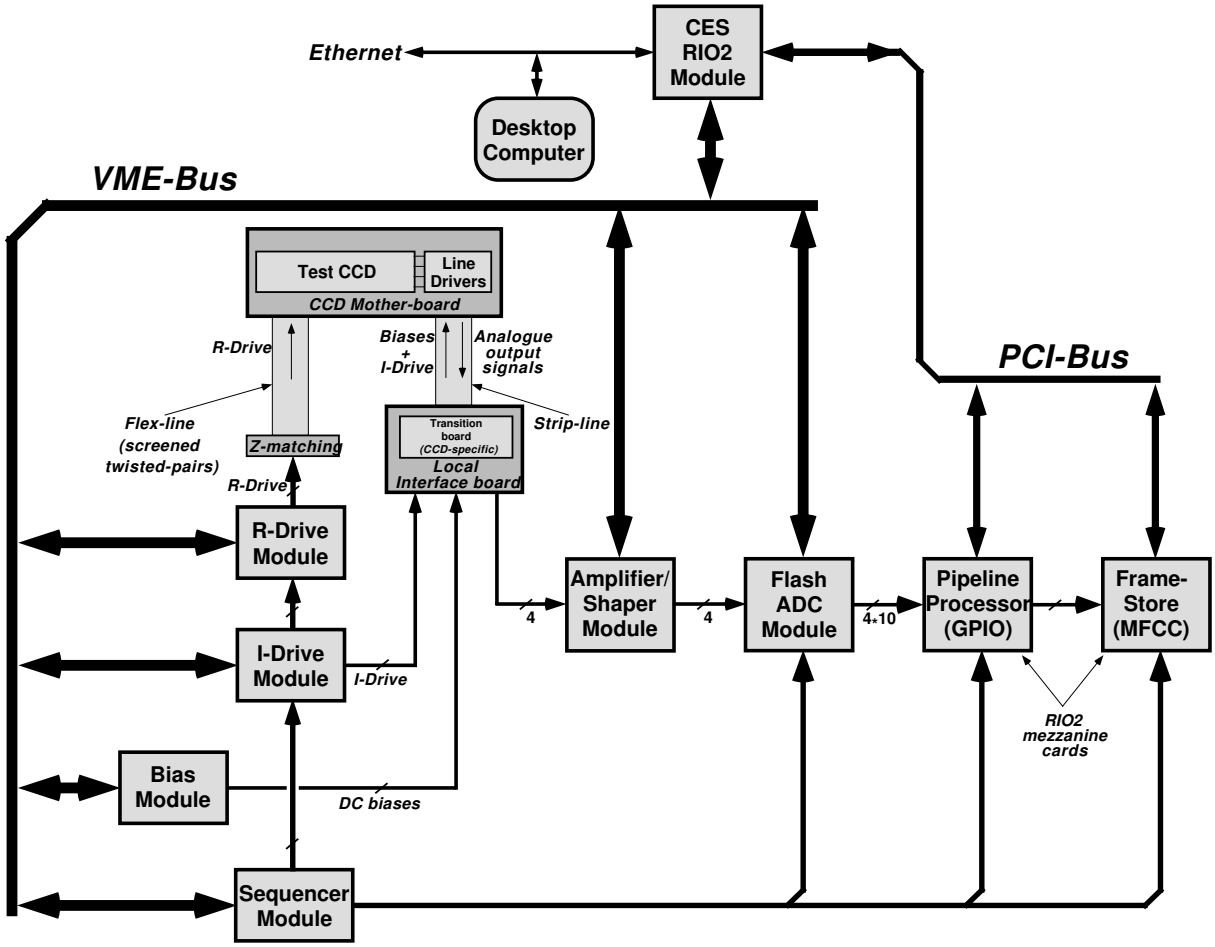

Fig. 18 Block diagram of proposed CCD test system readout electronics, phase 1.

to this motherboard, with electrical connections made by wire bonding. The R-drive connections are linked within ~ 1 mm of the CCD edge to a group of screened twisted pair cables forming one element of the local flex-line. The other connections are linked to a microstrip or stripline. In the case of the analogue signals, these each pass through a miniature surface-mount line driver on the motherboard. The local flex-line of length ~ 30 cm passes through the cryostat to local interface connections.

The R-drive cable will be kept separate, entering a screened box in which it will connect to an impedance-matched low-loss coaxial cable of length ~ 5 m which connects to the R-drive module in the VME crate. Due to the risetime requirement on the CCD, this and the local drive line will in the test system be cable bundles, to achieve characteristic impedance $\leq 10\ \Omega$. For the actual detector, short low impedance screened twisted pair cables will be custom made.

The local interface board will include a CCD-specific transition card to match the functions of the external electronics to the CCD pinout (other than the special case of the R-drive). A new CCD type is thus accommodated by making a new motherboard and transition card, plus changes to the software-controlled sequencing and voltage levels. All other hardware is constant. Such flexibility will enable us to respond to world-wide developments as we and our colleagues obtain new test devices from various manufacturers.

One of the most critical issues, as already mentioned, will be crosstalk between the fast R-drive pulses of amplitude up to 10 V and the high bandwidth analogue outputs, where min-I signals are of amplitude ~ 1 mV. So far, when pushing for maximum rate, we have been limited by the external electronics rather than

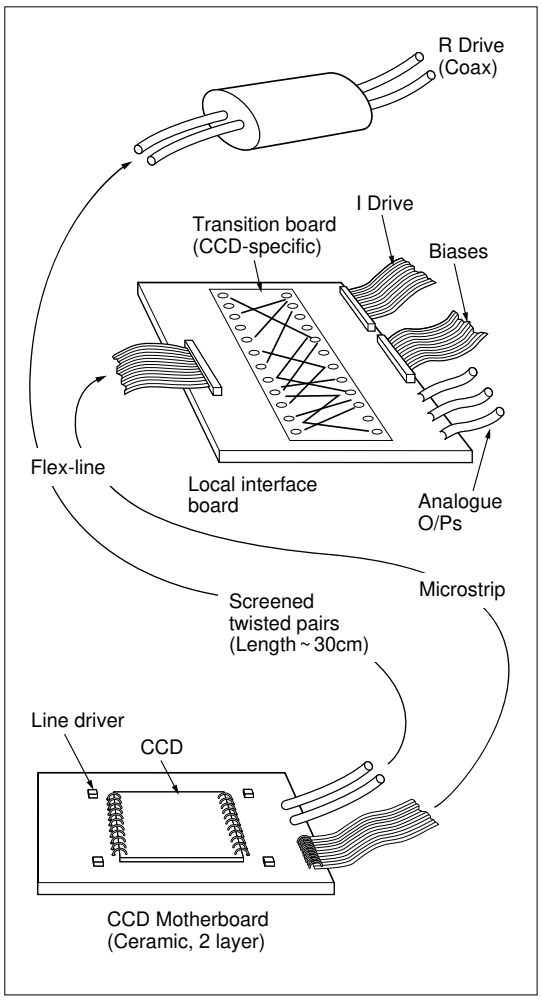

Fig. 19 Connection arrangements for CCD, CCD motherboard and local interface board, in the phase 1 readout system.

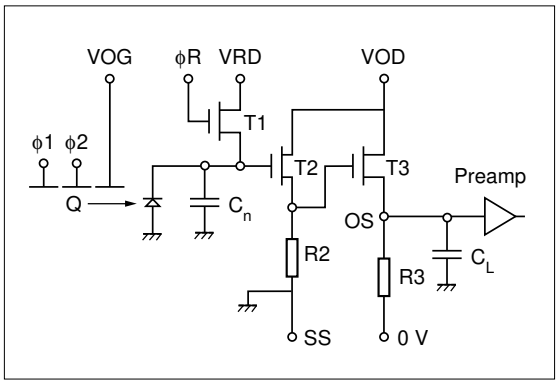

Fig. 20 Proposed output circuit. T1 resets the node to a standard voltage VRD at the end of each row readout. T2/3 provide the 2-stage voltage sensing circuit. Load R2 is on the CCD, while R3 and the line driver/preamp are on the CCD-end of the stripline.

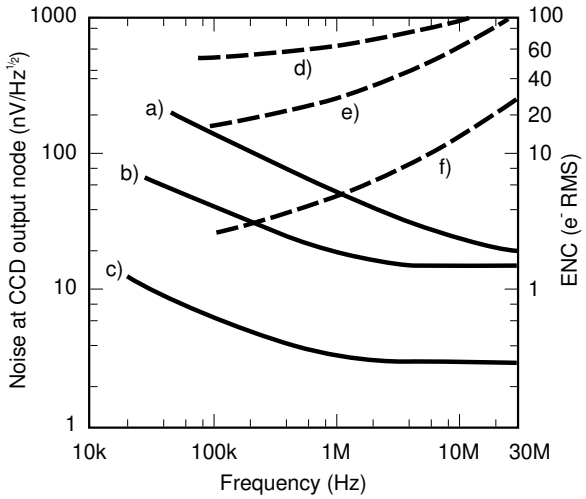

Fig. 21 Noise spectra (LH axis) of (a) surface-channel and (b) buried-channel devices as used in the SLD experiment. (c) shows the performance of a currently available design. (d)-(f) show the corresponding noise performance (RH axis).

on-CCD effects. It is hoped that the layout described above will solve these external problems, so that we can focus on the CCD-specific issues. These system-wide effects can be challenging to understand, but we are confident that this flexible test system (with the option to plug in a CCD motherboard fitted only with dummy loads, etc.) will allow us to disentangle these effects. Once one reaches the level of the CCD-plus-motherboard assembly, the EMLAB_ISE program already referred to will provide an invaluable tool for identifying the most critical sources of crosstalk. As one example, it is suspected that the wire bonds may be very significant. This hypothesis can be tested by simulation. If it is seen to be a problem, one can very easily simulate the benefits of other options, e.g. tape-automated bonding (TAB). Sorting such problems out in the hardware would be much more onerous.

For the R-drive pulse generation, it is likely that currently available IC drivers will be suitable [16] for the phase 1 system. Elantec do provide a custom design service and they may well be able to produce very compact devices tailored to the requirements of this detector, in the second phase of the programme.

For the I-drive, the requirement to perform a parallel shift in ~ 1 μs provides a serious challenge to the on-CCD pulse distribution system, as already mentioned. For the larger area devices (e.g. on Barrel 5) polysilicon gates with the current technology will fail to deliver

full-amplitude pulses at the remote end of the device. The most promising approach to this problem appears to be additional metal bus lines running the length of the CCD within the active area. This problem will be studied in the R&D programme.

Turning now to the CCD analogue output and signal processing, the optimal on-CCD processing is still believed to be the floating diffusion type, consisting of a reverse-biased diode followed by a 2-stage source follower (Fig. 20) as used for the SLD upgrade detector. Lower output impedance is available with a 3-stage system, but this is very much a case of diminishing returns, due to increasing gate capacitances. In any event, the on-CCD circuit would fall far short of the required bandwidth if the parasitic capacitance C_L were the entire stripline capacitance, as in SLD. Instead, R_3 is moved onto the stripline adjacent to the CCD, along with the line driver which now precedes the preamp. These changes increase the in-cryostat dissipation, but with pulsed power this can remain acceptable. The line driver provides a source which drives the remote preamp input of impedance 50 Ω. The possibility of more revolutionary output circuits as discussed in Section 2.3 will certainly be pursued, but there has been so much progress recently with the standard circuit (particularly in reducing the node capacitance) that this may remain entirely adequate for our purposes. Figure 21 demonstrates that, as long as the clock feedthrough problem can be controlled throughout the system, noise of ~ 40 e^- rms may be achievable at 50 MHz readout rate. These noise figures are based on the principles of 'correlated double sampling' [17, 18]. Up to 5 MHz, clocked noise performance close to the unclocked levels has been achieved in our earlier work. We believe it to be a realistic goal to push up by another factor 10 in frequency, but this implies much tighter control and better simulation of all aspects of the system. If such measures are insufficient, there are other longer term options to consider. As well as novel CCD output circuit architectures, ideas such as local R-drive generators can be pursued if necessary. It is still too early to predict which are the most likely bottlenecks. The analogue pre-processing ('shaper' in Fig. 18) ideally represents a transversal filter circuit to provide effective integration of the signal through the sample interval. In practise at these frequencies it probably will be limited to a simple signal integration prior to digitization. However, this may change as higher speed parts become available. The flash ADC module will be based on readily available 8- or 10-bit devices able to run up to 50 MSPS. A software-controlled pedestal level will be set at the ADC input.

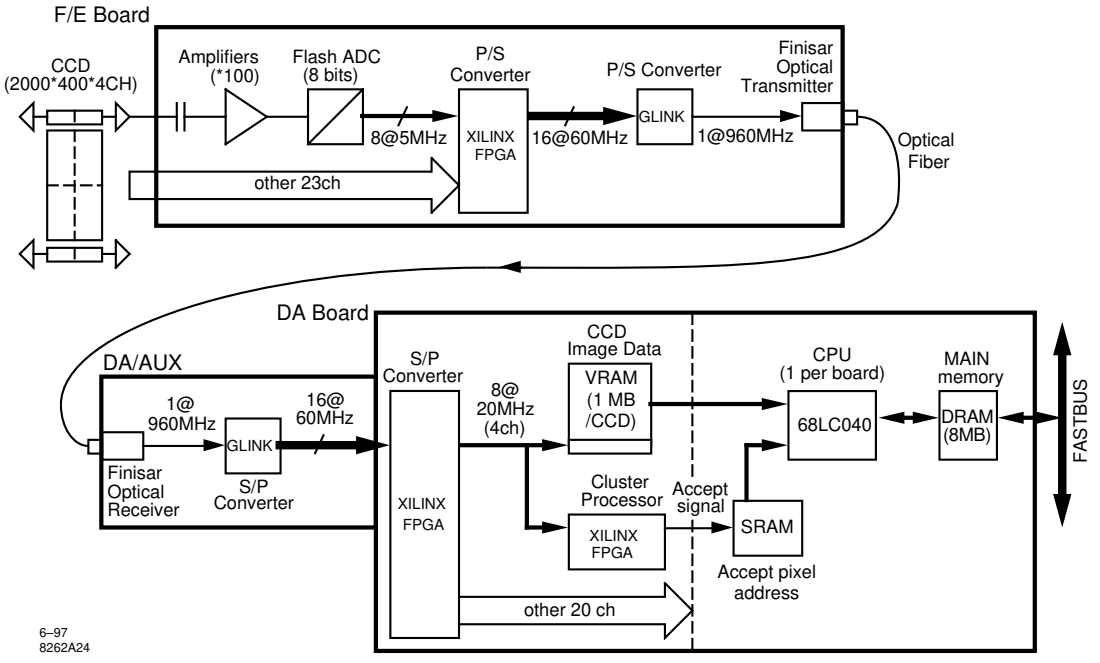

Fig. 22 Schematic diagram of the full electronics processing chain for one channel of the SLD upgrade detector.

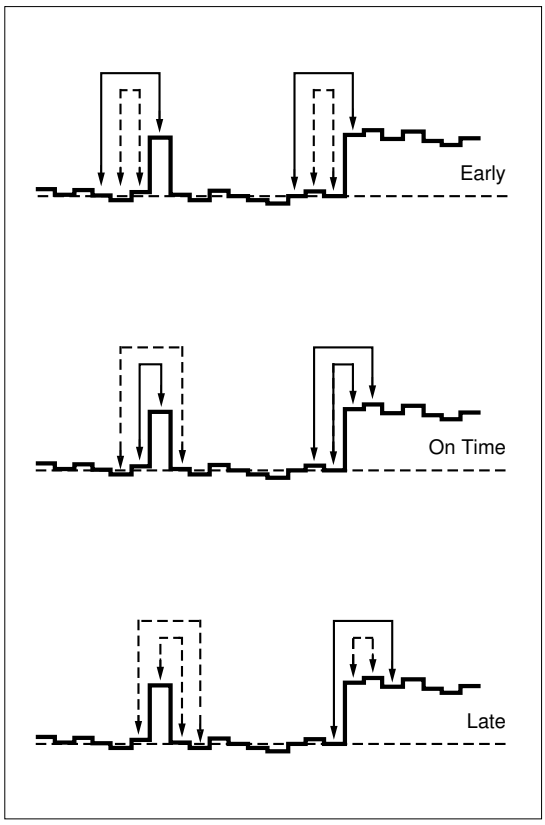

Fig. 23 Extended row filter operating on a row of CCD digitized data. Whereas both overlapping samples register a hit when 'on time' for valid data, this never happens for the pickup/noise spike.

The digital processing can proceed along the lines developed for the SLD readout system (Fig. 22), omitting in the phase 1 system the optical fibre and parallel/serial/parallel data conversions. The processing can be set to two principal operation modes: raw data and processed data, with some intermediate modes for diagnostic purposes. If set to raw data, a full frame of digitized pixel information is stored for inspection on a colour monitor. Such displays are extremely useful for diagnosing faults and setting parameters such as pedestal and gain settings. For processed data, the main concern, with raw data samples of hundreds of megabytes, is obviously noise suppression. A secondary problem in a laboratory environment is possible sources of RF pickup. The basic procedure for noise suppression that we developed and have refined over the years consists essentially of the extended-row filter [19] illustrated in Fig. 23. Since the CCD output node is reset only at the end of each row, digitized data show a step (modulo small AC coupling effects) for each hit pixel. On the

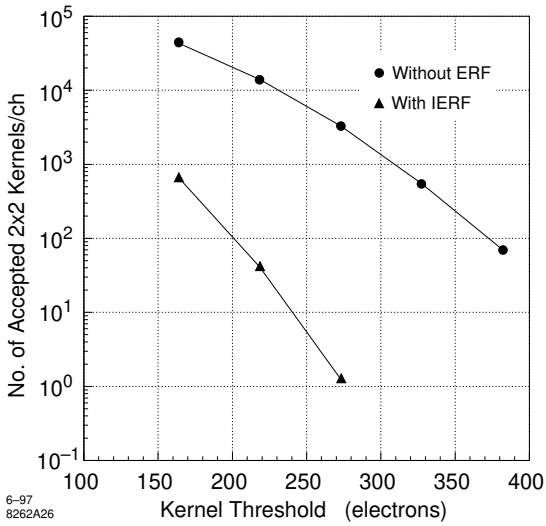

Fig. 24 Threshold dependence of the noise hit rate in the cluster processor with and without the IERF.

contrary, noise fluctuations and fast pickup generally disturb an isolated digitization. Looking at two overlapping differences separated by 1 and 3 pixels respectively, and taking the minimum step as representing the data for the next-to-leading pixel, provides a good charge measurement for true hits and excellent noise suppression. Further refinements led to the IERF (improved extended row filter) [6], for which the noise suppression performance at 5 MHz is indicated in Fig. 24. With the pixel threshold needed for 99% min-I detection efficiency (~ 250 e^-) the noise is suppressed by approximately a factor 1000, resulting in only a handful of hits from a 3.2 Mpixel CCD. Of course, it is not trivial to design such complex functionality to run at 50 MHz, but this problem is well suited to pipeline processing, c.f. the ATLAS Level-1 trigger logic, in which valuable experience has been gained.

3.4 Data acquisition and software

The decision to adopt a modular architecture for the phase 1 test system will result in the maximum flexibility both in the UK and with our international collaborators. As the R&D programme evolves, we envisage being able to share designs and modules, as progress in one group leads to developments that may be useful to another. The plan is for the DAQ system to be VME-based, with analysis and display on workstations, which might run UNIX,

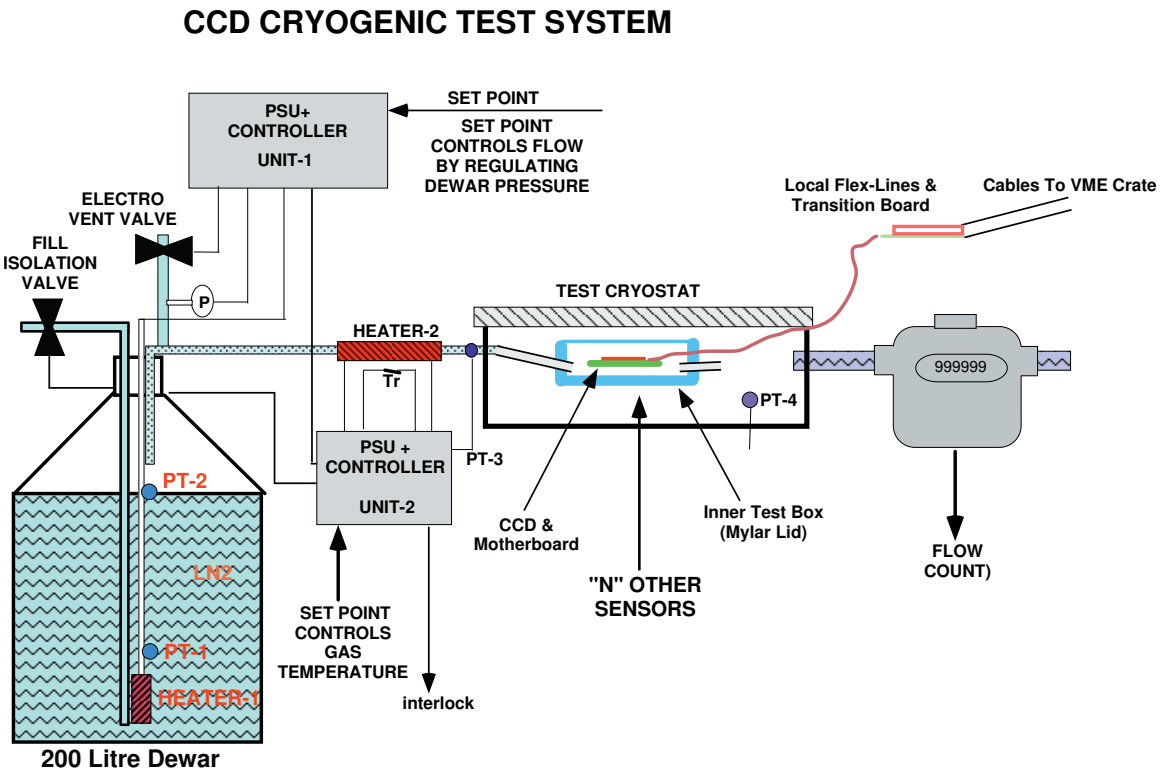

Fig. 25 Layout of proposed RAL cryogenic system for the CCD testing.

Windows or Mac operating systems, according to the preferences of the particular user group.

The data acquisition will be controlled by a commercial CPU board. The CES RIO is suitable. It has Ethernet, plus PMC PCI slots for daughter cards such as the CES GPIO, which provides FPGAs well suited to developing the CCD noise suppression algorithms.

Code development will be carried out on the host machine, using one of the IDEs (Integrated Development Environments) such as Code Warrior. The analysis system will run on the same host, running the same development software, as that used for the DAQ system.

3.5 Test system mechanics, cryogenics and controls

The group propose to build in total three cryogenic systems. Two of these are for studying the performance of individual CCDs, one in the temperature range offered by a liquid nitrogen based system, the other to the lower temperatures accessible using liquid helium, where data on CCD performance are sparse. The third system is designed to enable accurate study of the mechanical behaviour of the ladder structures proposed for the vertex detector.

The general layout of the first system is indicated in Fig. 25. It combines features of systems used previously in CCD test systems and experiments over the past 20 years. While it lacks the capability of running steadily round the clock for years (as is possible with the SLD system) it has the advantage of being inexpensive, compact and capable of rapid temperature cycling (very desirable in an R&D lab system). Furthermore, the temperature cycling can be controlled to limit the ramping rates to levels which are safe for the CCD assemblies.

The essentials of the system are a liquid nitrogen dewar fitted with level sensors and a resistor (HEATER-1) which controls the rate of boil-off. The gas passes through a foam-insulated pipe into the test cryostat. En route it is warmed by HEATER-2. Inside the cryostat, the gas is fed through the inner test box (sealed plastic with a mylar top window) which vents into the cryostat and then to the atmosphere. The flow rate and HEATER-2 settings are controlled by hardware controllers with set points from a dedicated PC. The system will be set up to provide an appropriate (maximal safe) rate of cooldown to the desired operating

temperature, and a similar rate of warmup when access to the detector is required.

The inner test box (with local flex-line) is taken into a clean room whenever it is to be opened for exchange of CCD/motherboard assemblies or other work with the CCD exposed. The mylar window permits irradiation with an X-ray or β-source, these sources being attached to thin rods and pushed into position over the CCD inside the test cryostat.

The test cryostat and its lid are made of thin plastic in a double-walled structure with foam-filled cavities, and are sealed using a gasket so that most of the cold gas exits through the vent pipe. Flow rates are sufficiently modest ($\leq$ 1 gm/s of nitrogen) that the vent gas, returned to room temperature, creates no measurable oxygen deficiency in a normal lab environment.

Using a 200 litre dewar, the system can run for a week continuously. For typical R&D operation, it would normally be permitted to warm up overnight, with a slow flow rate of nitrogen to preserve the non-corrosive atmosphere for the detector elements.

In contrast to the original and upgrade SLD detectors, there are no sliding contact or ZIF micro-connectors in the cold environment. Although the ZIF connectors of the upgrade detector were 100% reliable, the need for screened cables of constant impedance for the fast drive and readout now rules them out. Also, experience suggests that for the future detector with its mechanically more stable ladders, assembly of these ladders with pre-fitted flex-line 'pigtails' will be faster, safer and easier than one in which a high density of micro-connector insertions has to be made with the detector installed onto the beam-pipe and within the partly-assembled detector cryostat. In the future, all electrical connections made during assembly will be at convenient locations (the inputs to the local electronics on the SR masking cones).

Relative to the SLD vertex detector, this test system is simplified in that we do not envisage a microprobe system for studying electrical signals on the CCD. Such a system is of course restricted to room temperature operation with the lids of the cryostat and test box opened, hence requiring some additional environmental control, notably an enclosure and filtered laminar flow system for dust reduction. For SLD, this system was primarily needed for investigating discontinuities in connections induced by temperature cycling, such as sheared wire bonds in plastic-encapsulated surface-mount transistors. As a result of experience gained with these problems, they were completely eliminated in the upgrade detector. Similar precautions will be taken with the new system (e.g. regarding the line drivers on the flex-lines) and we can again hope to avoid the need for the microprobe facilities. They can of course be added later if necessary.

The second cryogenic system is to be constructed at Liverpool and will have an optical window permitting the use of the Liverpool BNC 1060 nm laser diode system for the stimulation of the CCD. This will allow precisely controlled studies of CTE effects over the full area of the CCD as a function of the various operating parameters. One of these parameters is the temperature, and it is proposed to make this second cryogenic system capable of running using helium, taking advantage of the Liverpool helium liquefier and the expertise developed there in the construction of the HERMES gas target system. This will allow a systematic study of the behaviour of CCDs down to about 40K, an area where good data are lacking. In the light of recent discoveries in the operation of heavily irradiated microstrip detectors at very low temperatures, the so-called 'Lazarus' effect, such studies have become particularly interesting in the context of investigations into the effects of radiation damage on CCD performance. The proposed setup will allow the group to make a fundamental contribution to our understanding of instrumentation in this area.

The second cryogenic system is illustrated schematically in Fig. 26. A helium dewar supplies gas to the cryostat via a controlled heater, the gas being pumped out of the cryostat through a warm-up coil using a diaphragm pump before being returned to the Liverpool helium liquefier. Computer control of the heater, using platinum thermometers in the heater and in the cryostat, allows the controlled warming and cooling of the test CCD. The optical window, chosen to be transparent to the 1060 nm laser light, is of diameter about 3 cm. This allows illumination of the complete width of the CCD, but not its entire length. The micrometer vertical moving device allows the CCD to be moved past the window, giving access to the whole area of the CCD

Cryogenic System for CCD Tests at Low Temperature

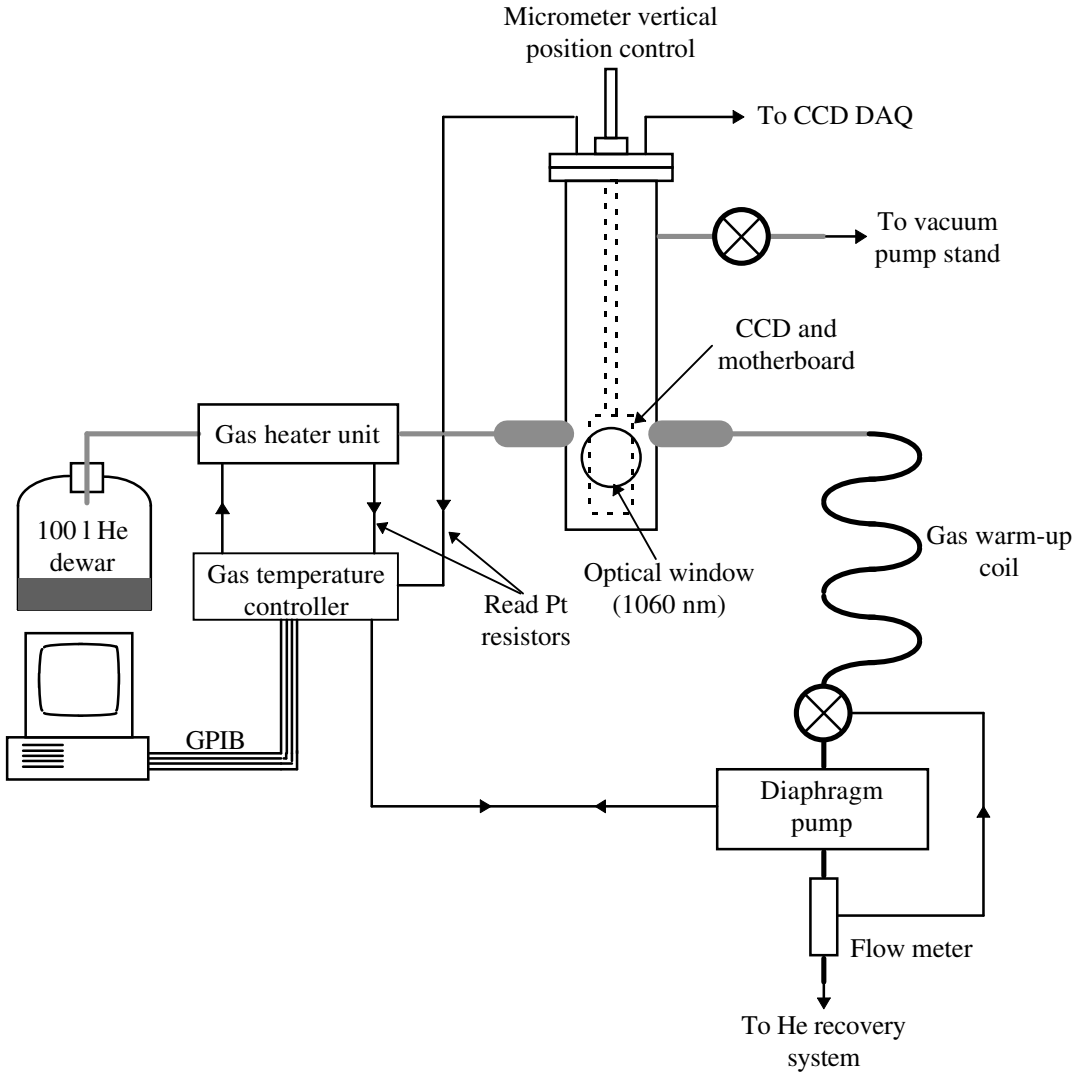

Fig. 26 Layout of proposed Liverpool University cryogenic system for the CCD testing

The third cold test system, to be used for studies of the mechanical stability of unsupported and supported ladders when temperature cycled, will also need an optical window made to a high standard. We observed problems due to imperfections in the glass, and due to differential expansion of the glass close to the 3 mm diameter plastic support pillars (a lensing effect) which will need to be eliminated and/or calibrated if the more precise aims of the future programme are to be achieved. There is a need for detailed design of this programme in conjunction with the instrumentation to be used for making the measurements. A first-generation system was used at Brunel University for the original SLD detector [20], and a more advanced system, the OMIS II programmable optical coordinate measuring machine [21] was used at MIT for the upgrade. Only in the first case was the detector surveyed cold, and the procedures followed there as regards the mechanical mounting within the cryostat as well

as the window will form the basis of the new system.

3.6 Test CCDs

The CCDs to be tested in the first instance will be setup-grade (i.e. giving somewhat defective images) from the EEV Company. These relatively inexpensive devices will be ideal for tuning up new readout systems with untested hardware and software. In this situation, the consequences of imperfections in the static precautions or in bias control systems will not be catastrophic. Furthermore, the Company can make available to us a variety of devices which (after exhaustive testing) will certainly guide us in designing custom CCDs close to our requirements for the actual detector. One of the most useful functions of our first stage R&D programme will be to make quantitative comparisons between a variety of device types in a single test system.

While our initial plans are focused on EEV CCDs, as previously explained, the test systems will be widely flexible as to bias, drive and readout conditions, and will certainly accommodate all probable architectures from other manufacturers. We look forward to learning about test results from our Japanese and American colleagues, and exchanging or lending each other devices as our programmes evolve.

The plan which has been provisionally developed with EEV (based on past experience) is to furnish them with bare motherboards equipped with local flex-line pigtails, housed in test boxes. We shall also supply a jig onto which they will transfer the motherboard, then attach the CCD and wire-bond, in their clean room. The assembly will then be returned to the test box, after which (making connections via the flex-line) the CCD will be DC tested, prior to delivery. Such testing will eliminate problems of mis-connected wire bonds or static damage, and should essentially guarantee that the device will image as it did in previous probe testing at the wafer or bare die level. Device types that have already been identified for our R&D programme are as follows:

- CCD 34
  This is the only EEV device that currently has a 2-phase I register, as is planned for the future LC detector.
- CCD42 2K×512N (N=1,8)
  Widely used in astronomy. Useful cross-check.
- 'Experimental CCD' 128×128
  Eight 2-stage outputs each end, plus dummy outputs that we may or may not use.
  Designed to run at 35 MHz; may go faster.
- EPIC CCD $(40\ \mu\text{m})^2$ pixels
  Very useful for cross-reference to X-ray astronomy. Open phase found to assist radiation resistance. Important to quantify the benefits. Charge injection to the imaging area is available and may assist the radiation resistance. If nothing else, charge injection should permit us to probe the details of the CTI mechanisms in these devices.
- CCD58 1K×1K
  2-stage output. Claimed to have achieved $\sim 150\ e^-$ rms noise at 40 MHz. 3-stage output was designed also for this device, but gave only marginal improvement.
- CCD63 4-phase device
  This architecture (with 9μm pixels) may be particularly robust with respect to local potential wells.
- *p*-channel CCD
  Manufactured to explore radiation resistance in the absence of the Si-E centre which dominates bulk effects for *n*-channel devices. Comparative radiation damage studies may be very interesting. Due to the high hole mobility at low temperatures, such devices may have the required speed performance if operated cold enough.

3.7 Radiation damage studies

The radiation hardness of a particular CCD obviously depends on the application to which it is being put. A loss of signal of say 10% from the remote end, which would be disastrous for spectroscopic applications, would be entirely acceptable for a tracking detector, where gain uniformity is only required locally, for cluster centroid determination. Given the spread in the min-I energy loss from a thin silicon sample, one is certainly tolerant of signal losses of 10-20%. Beyond that, the inefficiency may begin to be measurable. In this section, we focus only on radiation effects which can be of concern for CCD tracking detectors. Further details can be found in [22].

Regarding ionizing radiation, the effects are fixed positive charge within the dielectric layer and interface charge (negative for *n*-channel and positive for *p*-channel devices) at the

oxide/silicon interface. The net charge which causes flat-band voltage shifts is thus smaller in *n*-channel devices, one reason why they have been preferred in terms of their radiation resistance properties. However, with modern 'hard oxide' technology, one can produce CCDs with extremely small radiation-induced flat-band voltage shifts. Such devices can be operated at doses of 1 Mrad and beyond; this performance is entirely adequate for all CCD vertex detector applications contemplated to date.

As well as causing flat-band voltage shifts, the interface states produced by ionizing radiation act as sources of electron-hole generation, i.e. increased dark current. In HEP applications, there is no reason not to design the tracking detector for operation at cryogenic temperature, thereby reducing the dark current to completely negligible levels.

Turning to bulk damage, this refers to permanent radiation-induced changes to the crystalline structure of the bulk silicon. Most relevant for CCD particle detection are the changes to the channel (the region of the potential energy minimum) within which the signal charge is stored and transported.

Bulk damage can be caused by electromagnetic radiation, for electrons above a threshold energy of ~ 200 keV, determined by the minimum energy transfer of ~ 20 eV required to displace a silicon atom from the crystal lattice. Electromagnetic radiation always results in 'point defects', simple complexes of vacancies (V) and interstitial atoms (I). The interstitials are benign and immobile, but the vacancies diffuse through the crystal until they form a complex with some atomic inclusions. In the phosphorus-doped *n* layer, they nearly always form a Si-E centre, an acceptor-like phosphorus-vacancy complex which lies ~0.45 eV below the conduction band edge.

Bulk traps can adversely affect the dark current, charge collection efficiency, and charge transfer efficiency. Even in heavily irradiated CCDs, the excess dark current can normally be dealt with by modest cooling. Given the thin epitaxial layer (~ 20 μm) from which the min-I signal is collected, the requirements made on minority carrier lifetime are not severe, and there is essentially no problem with charge collection into the potential wells. However, once the electron charge packet starts its long journey to the output node (possibly several centimetres, ~ 2000 pixels), the situation is far more dangerous. At every location where the charge packet is momentarily stored (and there are three such locations for every pixel of a 3-phase CCD) there is a finite probability that some of the signal charge may be trapped, leading to loss of charge transfer efficiency. In order not to seriously degrade the signal-to-noise performance, the average CTI of a tracking detector using large CCDs should typically not exceed ~ 10^{-4}.

For hadronic irradiation, the situation is more complex, since cluster damage to the crystal can result in a large number of traps of different types and energy levels being generated throughout the band gap of the material. Due to the much greater non-ionizing energy loss (NIEL), the damage rates of hadrons in CCDs are much greater than for electromagnetic radiation.

Charged hadrons such as protons have a large cross-section for Coulomb-nuclear scattering, with sufficient energy transfer to the struck silicon atom to not only displace it but to generate a cluster of further displacements. Neutrons have smaller interaction cross-sections, but they induce nuclear disintegration which creates even larger damage clusters (having dimensions typically hundreds of angstroms in longitudinal and transverse dimensions). These clusters constitute highly disordered regions within the crystal, and may be a source of mobile vacancies, divacancies etc. In the heavily doped CCD *n* channel, after hadronic irradiation the majority of active defects are again Si-E centres, but there are additional significant traps at $E_c - 0.4$ eV, believed to be the divacancy (VV), and shallower traps at $E_c - 0.30$ and $E_c - 0.12$ eV.

Empirically, for electromagnetic irradiation, it is possible to cool a CCD to a sufficiently low temperature (~ 180 K) that the relaxation time for the Si-E trap becomes very long (seconds). Therefore the traps remain almost 100% saturated by some long preceding charge packets, and the effect on CTI even in large devices with I registers of several thousand pixels can be reduced to a low level. However, for hadronic irradiation, the same procedure is less effective. The CTI falls as the temperature is reduced to ~ 150 K, but thereafter it may remain constant at a level which becomes unacceptable even after modest doses.

The effect on CTI depends on numerous parameters, as well as on the detailed design of the CCD (pixel storage volume etc.). Most important operational parameters are the drive pulse amplitude, risetime and duration. The mean time t_p between charge packets strongly influences the condition of the traps (filled or empty) when a given signal packet is

transported, and hence controls the CTI experienced by that packet. In the simplest case of a continuously clocked CCD, t_p is determined by the hit density, but in devices with electronic charge injection, t_p is controlled precisely as the period (e.g. once per frame) of those injections. The CTI can clearly be quite different between the R and I registers, and can also be quite different in a given device, depending on the operating conditions.

Simple comparison between experiments measuring the effects of hadronic irradiation show considerable variations, which may be attributed partly to such differences in operating conditions. But beyond this, the measurements at low temperatures are subject to further complications. Reduced temperature is advantageous in 'freezing out' the effect of deep traps, while always exposing the charge packets to capture by shallow traps which are ineffective at higher temperatures. This applies equally to device defects, which may create shallow potential wells in the structure (e.g. due to small differences in thickness between layers of dielectric underlying gates). The effect of the drive pulse amplitude aided by the Poole-Frenkel effect (lowering of a potential barrier by a potential gradient) is usually sufficient to draw the charge out of these shallow wells, but this is clearly related to the device temperature. Some commercial CCDs have exhibited catastrophic loss of CTE below ~ 150 K [23], presumably reflecting such a problem.

These complications have led to some confusion as to the effects of hadronic irradiation. Devices irradiated with substantial doses of ionizing radiation (~ 1 Mrad) can be cured of CTE loss by operating at around 180 K, effectively disabling the Si-E traps well above the temperature where these other complications may set in. However, for hadronic irradiation the induced trap levels are more numerous (at least 4 distinct energy levels) and complex. Pushing to lower temperatures can cause other problems. Hence one is more sensitive to the device operating conditions (notably t_p) and comparisons between different experiments are difficult.

What is urgently needed is a systematic study of these effects over a wide temperature range, under background and readout conditions representative of those at the future linear collider. If necessary, electronic charge injection to saturate traps is a perfectly feasible option, one which would be completely ruled out in applications such as X-ray astronomy where extremely long signal integration times are obligatory. This systematic study will be one of the most valuable contributions the LCFI Collaboration can make to CCD detector technology. It seems likely that in gaining a true understanding of the phenomena involved, we shall enable advances to be made in the applications of these devices in all areas where hadronic radiation is relevant, whether terrestrial (e.g. nuclear engineering) or space-based.

Regarding the drive pulse voltages, there is clearly a strong incentive to reduce these, for reasons of power dissipation. In principle, this would also assist in reducing the variation in storage depth of signal packets being transported, and hence their susceptibility to capture by bulk traps. Against this, the reduced drift fields make signal packets more vulnerable to trapping in potential wells. The design of structures which combine supplementary channels with an orthogonal potential gradient to minimise storage volumes can help. What has so far been lacking are both the simulation tools and controlled experimental data for various ideas along these lines. Regarding the former, TCAD_ISE [15] will provide precisely the required simulation capability, and the flexible test facility having precise control of all operating parameters will enable us to make the relevant systematic measurements. In addition, ideas emerging from other areas of silicon detector technology may be extremely useful. The option of *p*-channel devices was tried long ago with some success [24], but its revival for CCDs is an example of the useful interaction between different detector disciplines.

This work will depend on device simulations, CCD design and manufacture, excellent test facilities, and on the availability of well controlled irradiation facilities. Fortunately, for CCD bulk damage, the effects are independent of the bias conditions, so it is sufficient to irradiate devices with all terminals grounded. As to the temperature, the possibility of short term annealing and long term reverse annealing has not yet been explored. It is possible that there will prove to be an advantage in continuous cold operation, as with microstrip detectors, and for similar reasons. We are fortunate in having well calibrated sources of ionizing radiation and neutrons available at Brunel University and RAL. In both cases, it will be possible to irradiate devices at any temperature in their cryostat (equipped with a portable cooler for the period when it is not connected to the main system) then reconnect to the main system for post-irradiation performance evaluation. It would obviously be more convenient to permit occasional warm-up of the sample, so one of the

first questions will be whether the bulk damage effects in CCDs which cause CTE loss are subject to either or both annealing and reverse annealing after irradiation.

Before leaving the question of radiation damage, mention should be made of the SLD experience, in which the upgrade vertex detector suffered significant damage soon after installation and before the electronics was commissioned, when SLC was operated in a non-standard mode (undamped e^- beam) for a short period. The enormous synchrotron radiation flux destroyed a nearby CCD camera, and the performance of the vertex detector (notably the inward-facing CCDs on the inner layer) could be restored only by operating 40° cooler than nominal. Fortunately there was sufficient flexibility in the detector design to permit this. Local radiation monitors gave no warning of problems during this period.

From this, several lessons can be learned, of relevance to the future linear collider. Firstly, non-standard beam conditions should be treated with extreme caution, starting always with much reduced intensity. Secondly, all obvious precautions should be taken to minimize the effects. For example, the beam to the detector must always be interlocked to having the solenoid field on. Thirdly, the beam must also be interlocked to the vertex detector running in background-monitor mode. This means charge sensing of a few rows transferred to the output node after each bunch train. The CCDs on the inner layer, which see the interaction region through a very thin beryllium window, are uniquely susceptible to soft radiation which will never be picked up by any external monitors. Each of these devices needs to be used as its own radiation monitor, and to be capable of shutting off the beam in hostile conditions. Since the beams at a linear collider are re-created on each pulse, there is no risk of a huge single burst of radiation when a massive stored charge is dumped, as is possible at a storage ring. On the contrary, the integrated background at a linear collider should be little more than that given by the tuned-beam conditions. This however requires vigilant monitoring and effective interlocks to be planned, implemented, and never overridden.

3.8 Other short-term R&D topics

The environment of the future linear collider will present additional possible complications for operation of the vertex detector. Two examples immediately come to mind, and more may emerge later.

Firstly, the detector will be operated in a magnetic field of approximately 4 Tesla, 7 times higher than previously for min-I detection. Effects to consider are that on the drift of signal electrons being collected, the post-collection transport in the R register (normal to the field direction) and stresses on the bond wires used for the drive pulses and (more seriously) the analogue pulsed power. All these need to be simulated and possibly subjected to experimental test. If the latter, the 4T test magnet at RAL can be used.

Secondly, the effects of pickup of the magnetic pulse from the passing bunch train need to be considered. The corresponding problem at SLD caused disruption to the digital links between the local electronics and the external controller. The local boards tended to self-reset and go into undesired control modes, due to beam interference affecting the decoded clock modulation and hence generating spurious control commands. The solution in SLD was to reset the local digital electronics to a standard condition after each bunch crossing. At the future machine, the first effect to consider is disturbance to the charge signals stored in the detector. Fortunately, static charge storage in potential wells in the buried channel (the condition throughout the bunch train) is extremely robust. Tests should be made, but one can be reasonably confident that the signal packets will remain undisturbed by pickup effects. The question then comes down to the local electronics, as in SLD. The sequencing (successive readout of part-frames from the outer layers over some number of bunch train intervals) can be entirely controlled from the external VME system, so (as in SLD) there is again the possibility to initialise all the local electronics after each bunch train. This should be designed in from the outset.

No doubt, other topics requiring lab tests and development will emerge as the project evolves. One area that has not begun to be addressed is interference with the novel laser-based beam-size and beam-position monitor equipment. There are also a number of issues related to the extreme mechanical stability required for the accelerator final focus system, to which the vertex detector including its cryostat and cold gas system (necessarily mounted off or coupled to the inner beam-pipe) is effectively a part. The plan to mount the front-end electronics on the face of the M1 masks (see Figs. 3, 4 and 17) raises the issue of vibration induced by water cooling. While much of the digital processing will benefit from advances in low-power CMOS, the drive pulse

generation (if unchanged in voltage from the SLD detector) could result in ~ 1 kW dissipation at each end. Vibration levels caused by the associated water cooling could be unacceptable to the final focus, where nanometre stability is required. This is an added incentive for achieving operation with much reduced drive pulse voltages.

4. Short-Term Goals, and Request for Support

Firstly, we plan to continue our physics studies, and be guided by them in refining the longer term goals for the detector design. In the short term, the goals of the phase 1 R&D programme may be summarised as follows:

- Establish a CCD/system architecture which shows the way to 50 MHz operation with LC-compatible performance parameters (power dissipation etc.).
- Establish a ladder design of thickness ~ 0.1% X_0 with the required mechanical stability.
- Understand the radiation damage characteristics of relevant devices under readout conditions appropriate to the LC. Establish CCD design details which show the way to the required radiation resistance in the LC environment.
- Evaluate the significance of other environmental factors such as 4 Tesla solenoid field and RF pickup from the beams.
- Respond to other design requirements which emerge from ongoing physics and detector studies by ourselves and our international colleagues.

This programme, which is expected to take approximately three years, and the longer term programme outlined in the next section, will be based on three complementary test facilities.

Firstly, we envisage a detector test system at RAL, consisting of a cryogenic system (Fig. 25) and readout system (Fig. 18), with signal injection by β- and X-ray sources. This will be used for system development (readout speed, crosstalk, noise performance) as well as device details (potential pockets, etc.). It is planned to house this test system, a somewhat similar one for astronomy/space science, and ongoing silicon microstrip R&D work in one laboratory. Sharing of people and ideas between these projects is likely to be generally beneficial.

Secondly, we are planning a detector test system at Liverpool University, to be used primarily for the study of radiation damage effects, an area in which the participating groups already have considerable expertise. This system (Fig. 26) will be similar to that at RAL, but with two important differences. The cryostat will be cooled with helium gas, and capable of operating at considerably lower temperatures. This is very important for investigating radiation damage effects, where the effects of shallow traps are currently poorly understood. It is even possible that a new temperature window for CCD operation (analogous to the 'Lazarus' effect in silicon microstrip detectors) may be revealed. Furthermore, this cryostat will be equipped with an optical window, to take advantage of the excellent BNC 1060 nm laser diode system at Liverpool. This facility will be extremely useful as a fine probe for CTE effects, which are the main cause for concern in cooled irradiated CCDs. Note that using components already available at Liverpool, such as the liquid helium dewar and the vacuum pump stand, and manufacturing others in the Liverpool workshops, reduces the cost of the system significantly.

Thirdly, we shall construct a mechanical structure test system, consisting simply of another cryogenic system (with a large optical window) to be used for studying the mechanical stability on thermal cycling of various prototype ladder assemblies. The costly part of this system is the precise coordinate measuring machine. We require an automated system with a limited working depth (3 cm would suffice) and high resolution (~2 microns) in the depth measurement. Here there are a number of options on which free time may be available, the most promising being the system proposed for measuring the ATLAS SCT modules during production. The system used at MIT for measuring the SLD upgrade detector could (with slightly modified optics) also do the job.

All members of our collaboration are contributing to the overall design of the phase 1 test systems. The responsibility for the engineering design will be mainly divided between our groups, and staff in the RAL Technology Department. In addition, we wish (as in the past) to have Technology Department staff provide some of their invaluable expertise in the assembly and evaluation of the test structures and modules, and in the overall system development. In total, we are requesting 0.8 SY (mechanical, Geoff Tappern's group)

and 1.8 SY (electronics, Richard Stephenson's group) for this, to be divided between the current and next financial year. We have made particular efforts to minimise the request for TD manpower, so as not to exacerbate the overload from the LHC GPDs. As a consequence, more work will need to be done in industry, somewhat increasing the equipment budget request. Wherever possible, university workshops will be used. Cost estimates are summarised in Table 2, with the spend again being divided between the two financial years. The total equipment budget request amounts to £127K. In addition, we request £5K per annum for running costs (liquid helium).

Regarding our entire R&D programme, we intend to maintain close links to those in Japan (existing) and in the USA (being planned). We envisage a sharing of ideas, hardware and software between them, so as to optimise progress on an international scale. In order to maintain these important links, we have already established a number of valuable contact methods. Through our current experimental activities, we are frequently present in SLAC and DESY. Through active participation in the ECFA/DESY and DOE physics and detector studies, we have been supported for travel to

Table 2 LCFI R&D Equipment Budget Request (£K inclusive of VAT)

Description	NRE/ Spares	Detector Test Systems		Mech Dev System
		RAL	L'pool	
EMLAB_ISE and TCAD_ISE (academic licence)	5.3			
Dewar		2.5	3.8*	2.5
Pipework, heaters, cryostat, test box	1.0	4.5	3.7	4.5
Optical window for cryostat	2.0		0.3	1.4
Vacuum pump			5.3*	5.3*
Vacuum fittings				0.5
Control hardware		4.4	2.7	4.4
Rod-mounted X-ray and β-sources		0.6*		
CCDs (setup grade)		7.5	7.5	
CCD motherboards, flex-lines, interface boards, transition cards and cables	7.3	6.5	6.5	
Bias module	2.6	0.6	0.6	
I-drive module	2.6	0.7	0.7	
R-drive module	2.6	0.7	0.7	
Amplifier/shaper	2.6	0.8	0.8	
VME crate (6U)		1.5*	1.5*	
CES RIO2 processor system		7.0	7.0+	
Desktop computer		1.5*	1.5*	
Programmable CCD readout sequencer	2.3	0.8	0.8	
ADC module (4-channel)	2.3	0.8	0.8	
CES GPIO mezzanine card (pipeline processor dev)		0.6	0.6+	
CES MFCC mezzanine card (frame-store memory)		1.4	1.4+	
CCDs (thick/thin sandwich, non-working)				8.0
Test substrates	1.5			7.4
Assembly jigs				2.5
Totals	32.1	38.8	25.1	31.2

* In hand, so not included in total

\+ Being purchased by Liverpool University, so not included in total

numerous workshops in Europe and the USA, and this will continue. In order to strengthen the links to our Japanese partners, three of us applied for, and have been granted, a very useful British Council Collaborative Research Project award. Conversely, the Japanese groups have applied for a Monbusho grant, so they will be able to visit our test facilities when we have them. Beyond these initiatives, we request support from the PPESP for a specific budget of £5K per annum for travel within the UK and abroad, to permit us to make full use of the proposed resources.

5. Overall Schedule and Long Term Programme

We envisage the phase 1 R&D programme continuing for approximately three years, to be followed by a second phase using full-custom CCD designs and re-engineered local electronics.

In practice, there will be some overlap between these phases. Ongoing development in CCDs, associated electronics and mechanical design will clearly be considered until the time when the design of the LC vertex detector needs to be finalised. Furthermore, there is considerable interest within the PPARC-supported astronomy community for devices with some of the performance requirements under discussion. It is therefore possible that a joint programme of CCD development will be undertaken somewhat in parallel with this phase 1 R&D work but if so, support for this will be sought from a PPARC inter-disciplinary funding source, not via the PPESP. It is also likely that we may gain access to custom devices from non-UK sources, funded by our US and Japanese colleagues. In any event, the design of custom devices specifically for this detector will clearly follow after the formation of the overall detector collaborations, perhaps four or five years from now.

As well as the CCD design, this second phase will include developments of local electronics

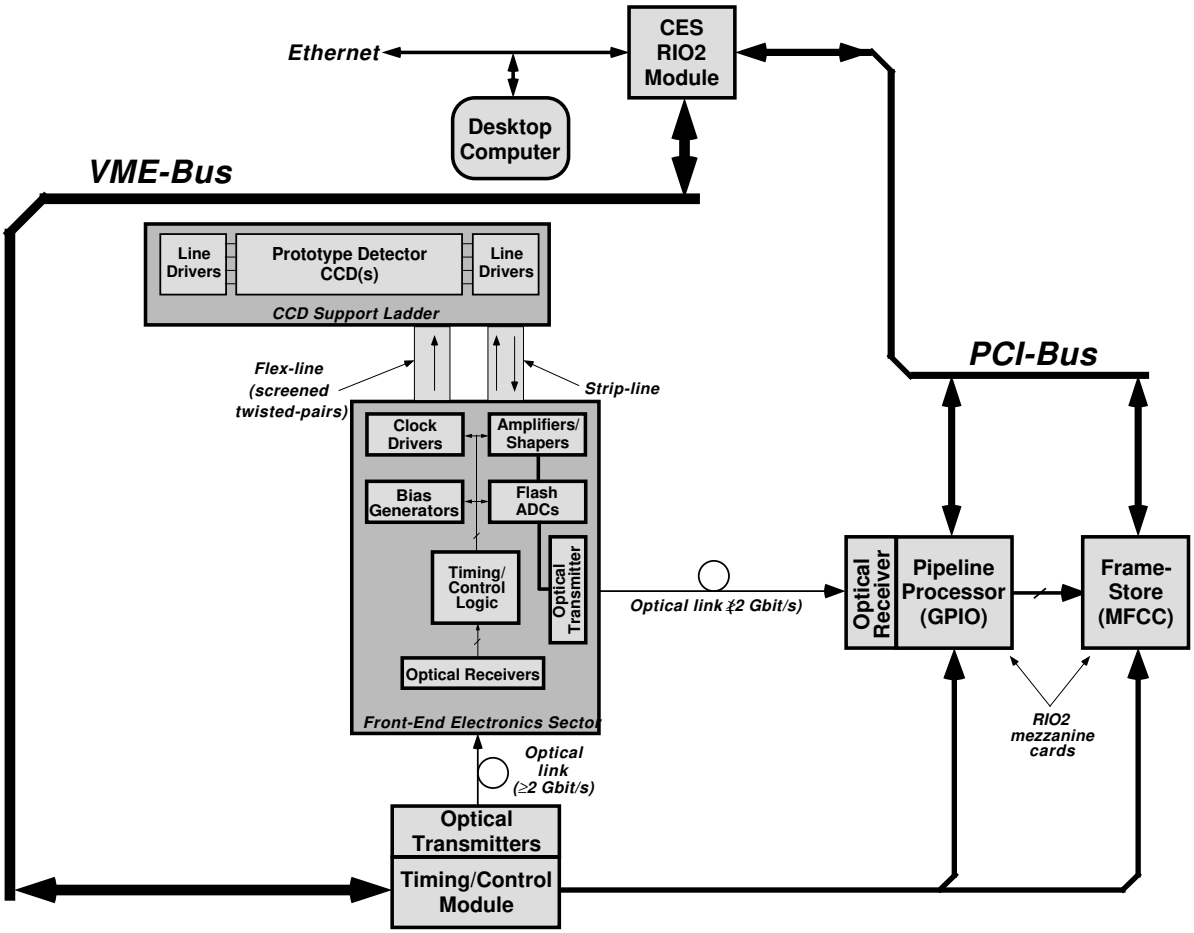

Fig. 27 Block diagram of suggested CCD test system readout electronics, phase 2. The components of this system will be fully representative of the vertex detector for the future linear collider.

suited to the requirements of the experiment. The physical layout is sketched in Fig. 17, and the corresponding functional block diagram is shown in Fig. 27. The aim is to develop a local detector system which requires only a few power tapes and optical fibres to connect it to the external digital processing and DAQ system. Note that only one optical fibre is required to link the Timing/Control Module to the front-end electronics either side of the IP. With present technology, 50 data fibres per side would be required, but even this modest number will be reduced as this technology is advancing rapidly. Conceptually the local electronics outside the cryostat will consist of multi-function boards serving some number of ladders. In practice, the fast R-drive may remain isolated and screened from the sensitive analogue electronics. Furthermore, the 'boards' will be multi-layer flex-circuits shaped to fit snugly onto the outer surface of the support cones, in the region of $|z| \sim 30$ to 60 cm, as suggested in Section 3.2. Particular attention will be given to the design of the local flex-lines that penetrate the cryostat. Very likely, the R-drive lines will be single screened twisted pair cables for each R register, with a sufficiently thin insulation layer to achieve the required characteristic impedance.

Efforts to reduce material in the important small-angle region, beyond the angular coverage appropriate to a vertex detector, will continue. Such efforts were already rewarded with considerable success in the evolution from the original to the upgrade SLD vertex detector. Taking advantage of current industrial trends, we can clearly envisage very compact drive and readout electronics using ICs bonded to flexible multi-layer copper-kapton substrates, attached to the surface of the conical shields. If necessary, shallow water-cooled channels can be incorporated in the shields beneath the electronics.

The system design will obviously be complicated by the requirements for compatibility with a variety of other equipment to be located in the interaction region, issues which have not yet begun to be addressed.

6. Conclusions

We wish to play a major role in the international collaborative effort that is gaining momentum and leading towards the design of a high energy e^+e^- collider and its detectors, for study of the origin of electroweak symmetry breaking. We propose to continue our strong participation in the ongoing physics, detector and accelerator studies, which will allow further development and refinement in the design of detectors for this environment. In particular, we propose an R&D programme to address the outstanding issues in the design of a CCD-based vertex detector for heavy-flavour identification, namely the ability to assemble a mechanically-stable system of thin, large-area CCDs with fast readout, adequately low power dissipation and noise, and the required degree of background and radiation tolerance. Based on over a decade of experience at the SLC, we believe that this technology offers the best possibility for the unprecedented flavour-tagging capability required to unravel the anticipated new physics processes, which manifest themselves in complicated multi-jet event topologies.

Wherever possible, we intend to collaborate in these studies with our colleagues in the USA and Japan. Furthermore, a number of aspects of the R&D programme will be of direct interest to the strong UK communities in astronomy and space-based earth observation, who also require thin, fast, large-area CCDs, and we intend to develop collaboration with these groups. We believe that our existing expertise, combined with the strong collaboration developed over the past 20 years with the UK CCD manufacturer EEV, offers a unique opportunity for the UK to play a major part in developing a powerful tool for exploiting the physics opportunities at the future linear collider.