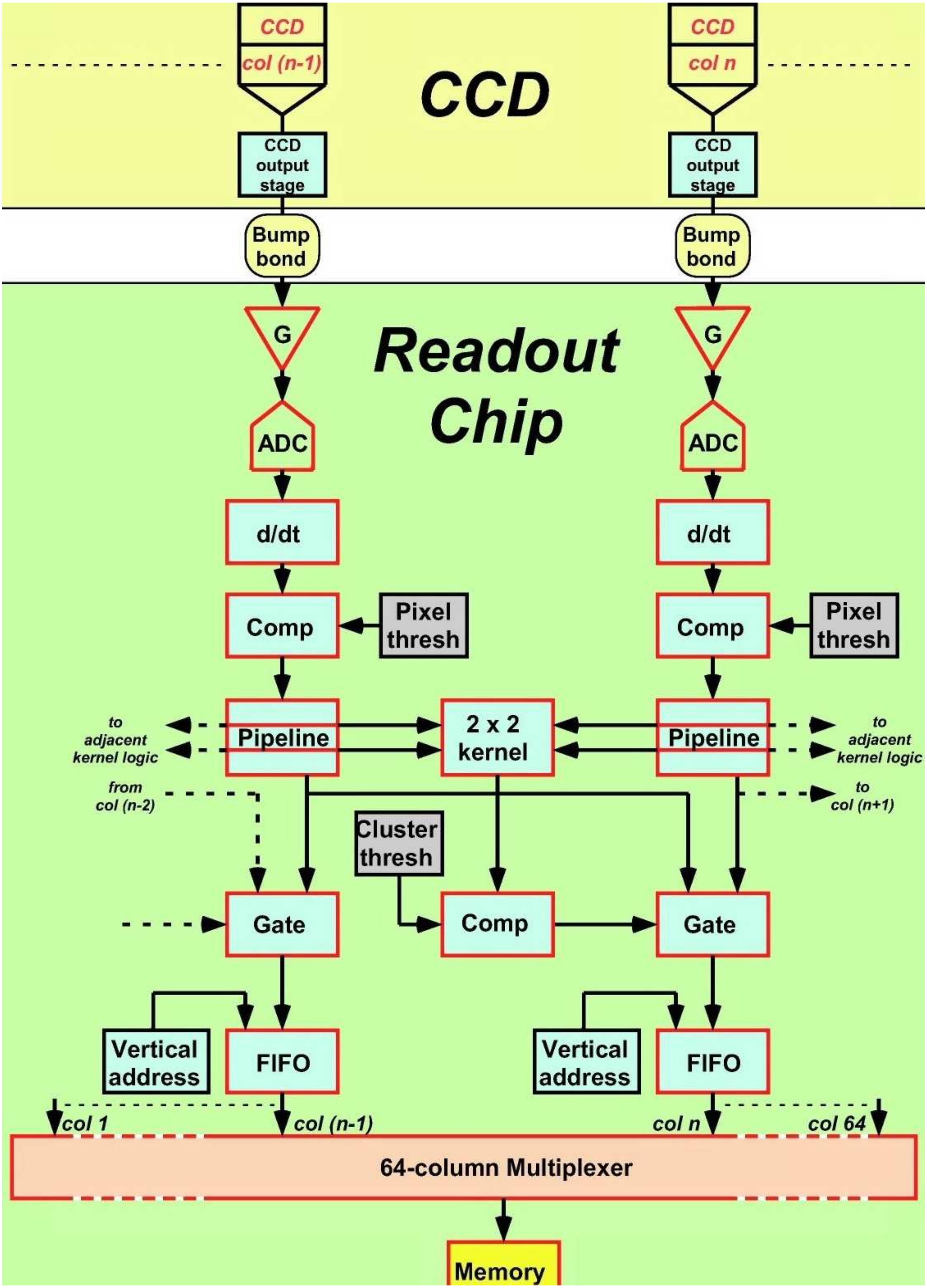
CCD
col (n-1)
CCD
col n
CCD
CCD
output
stage
CCD
output
stage
Bump
bond
Bump
bond
G
G
Readout
Chip
ADC
ADC
d/dt
d/dt
Comp
Pixel
thresh
Comp
Pixel
thresh
to
adjacent
kernel logic
Pipeline
2 x 2
kernel
Pipeline
to
adjacent
kernel logic
from
col (n-2)
to
col (n+1)
Cluster
thresh
Gate
Comp
Gate
Vertical
address
FIFO
Vertical
address
FIFO
col 1
col (n-1)
col n
col 64
64-column Multiplexer
Memory

Self-supporting CCDs