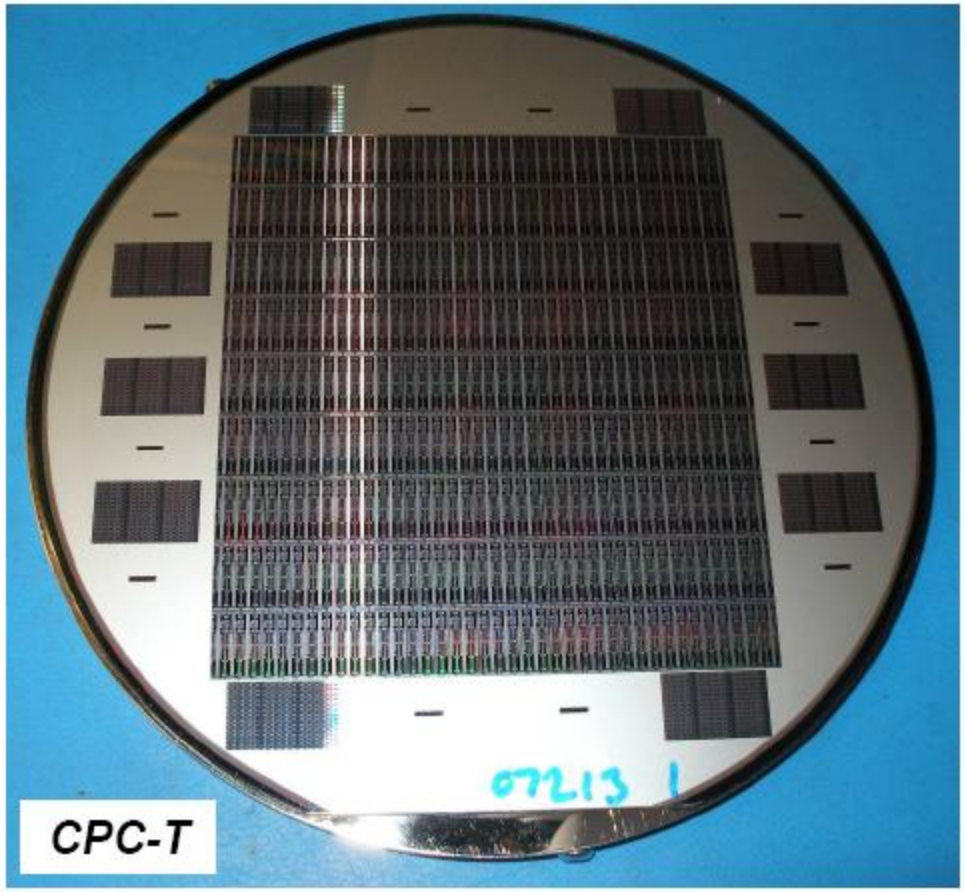
Update on Sensors and Testing

- News from e2v.
- ISIS2 status.
- Tests of ISIS1 with p-well.
- Test beam studies of ISIS1.
- Summary.



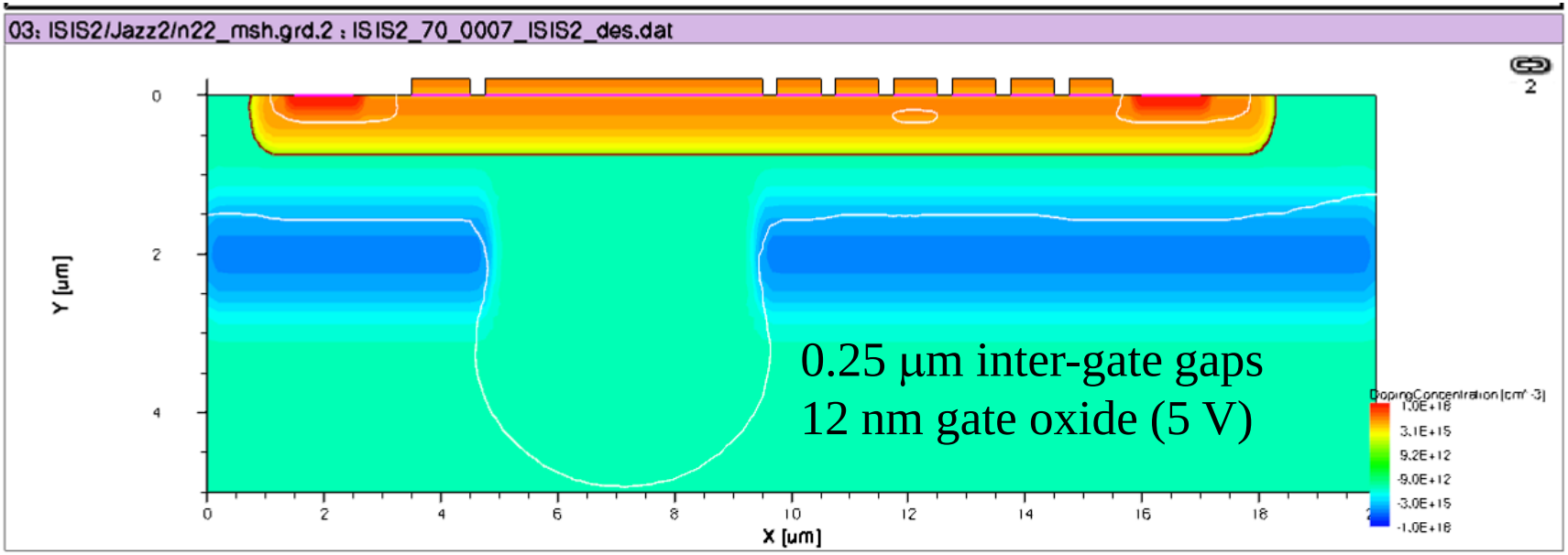
News from e2v

- CPC-T
- All CPC-T wafers now diced and (hopefully!) in our hands.
- We will do wire-bonding and packaging.
- Delays at e2v due to attempts to set up robotic handling of many small chips.
- Test board ready (Bristol).
- Will soon have 29 variants of CPC-T to test.

- CPC2
- Some good news: all 4 double level metal CPC2s have been DC probed by e2v.
- Some bad news: all but one failed DC tests.
- Some astonishing news: all the largest CCDs on the good wafer look IK!

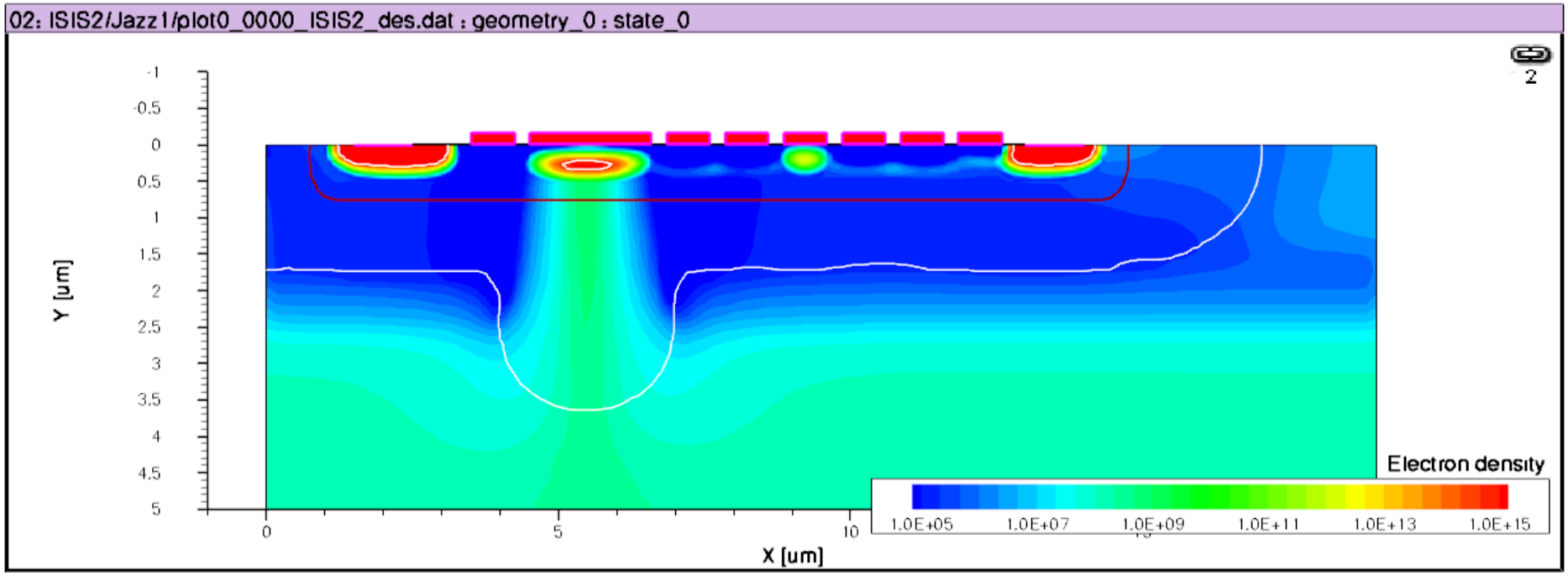
ISIS2 Status

- Jazz Semiconductor will manufacture ISIS2.
- Process is 0.18 μm dual gate oxide (1.8 V and 5 V).
- Wafers p++ with 25 μm epi layer, $\rho > 100\ \Omega$ cm.
- ¼ of MPW masks + 2 add. masks
- Five or ten wafers with process variations.
- Area 1 cm^2 (four 5 × 5 mm^2 tiles).
- Doping profiles calculated by Konstantin, Jazz will develop buried channel and deep p^+ implants.



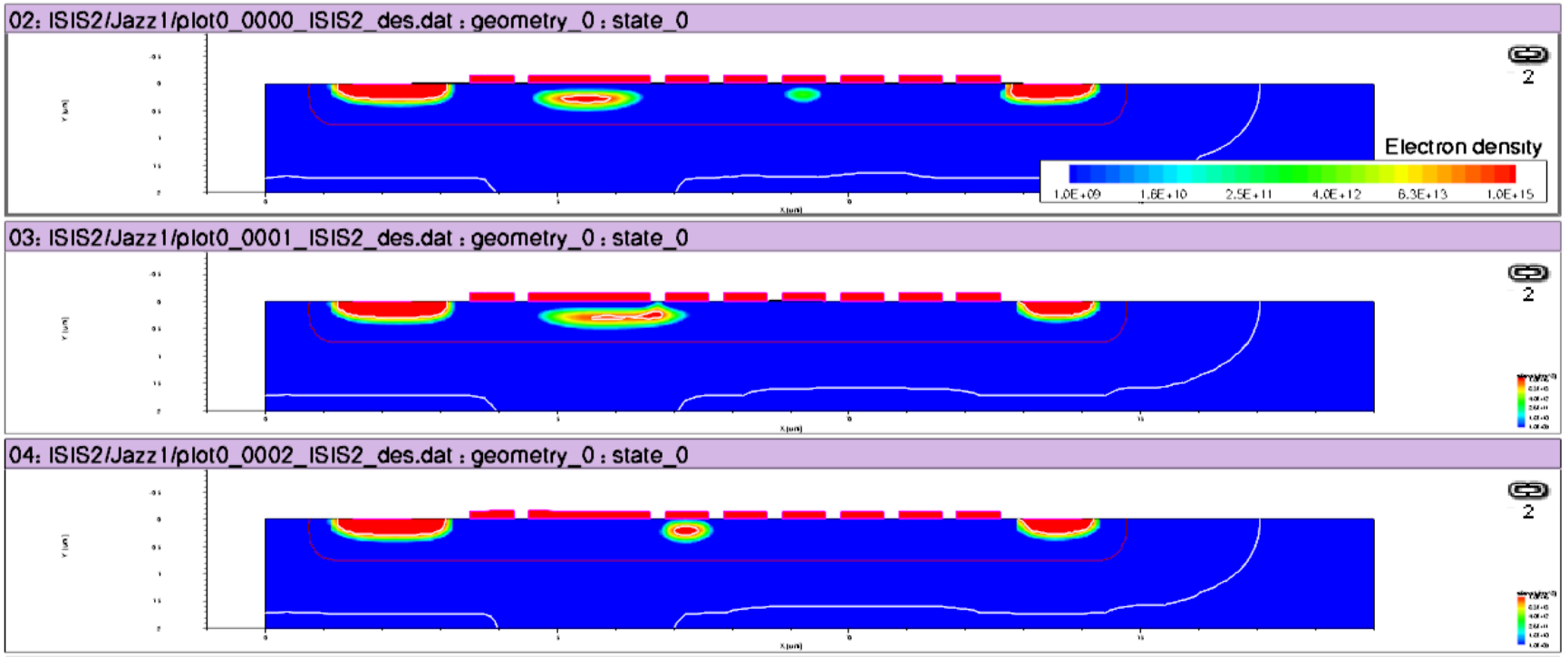
ISIS2 Status

- Konstantin has simulated charge collection,



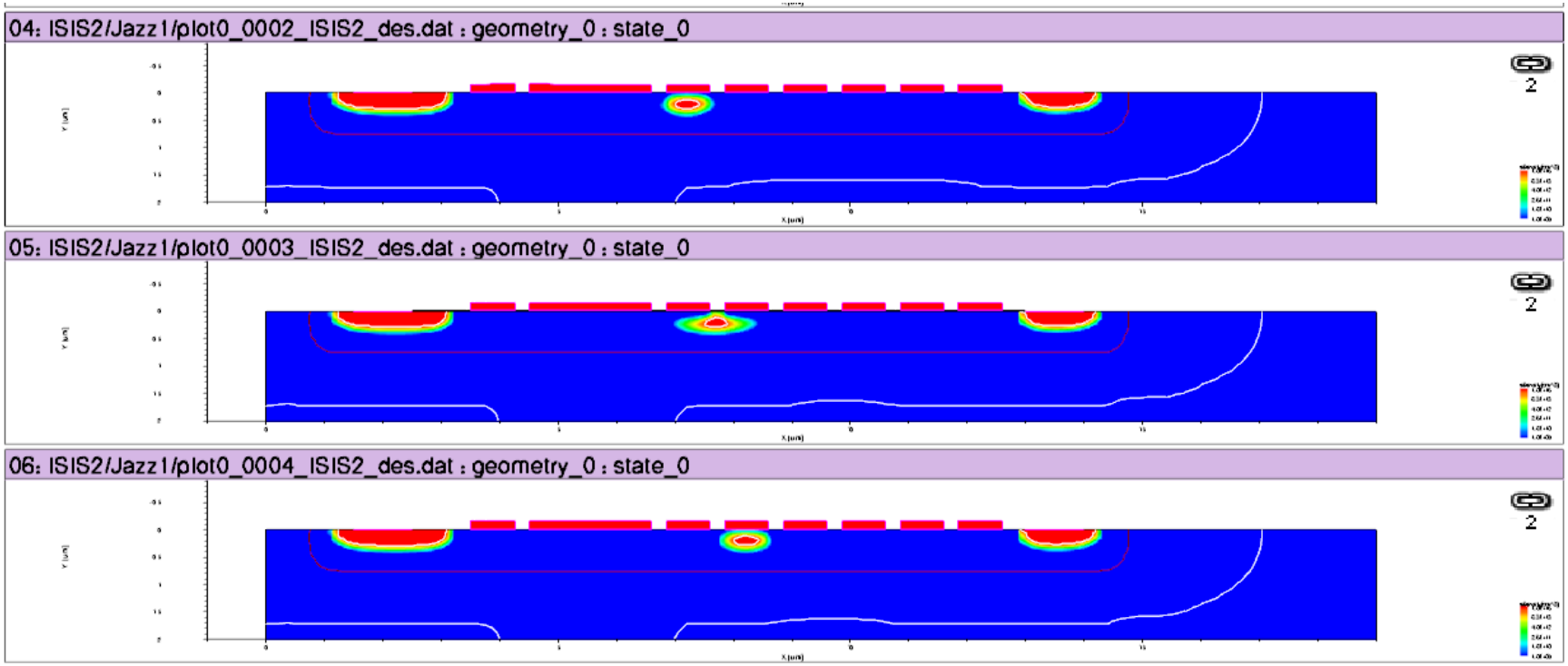
ISIS2 Status

- transfer from photogate to storage cell...



ISIS2 Status

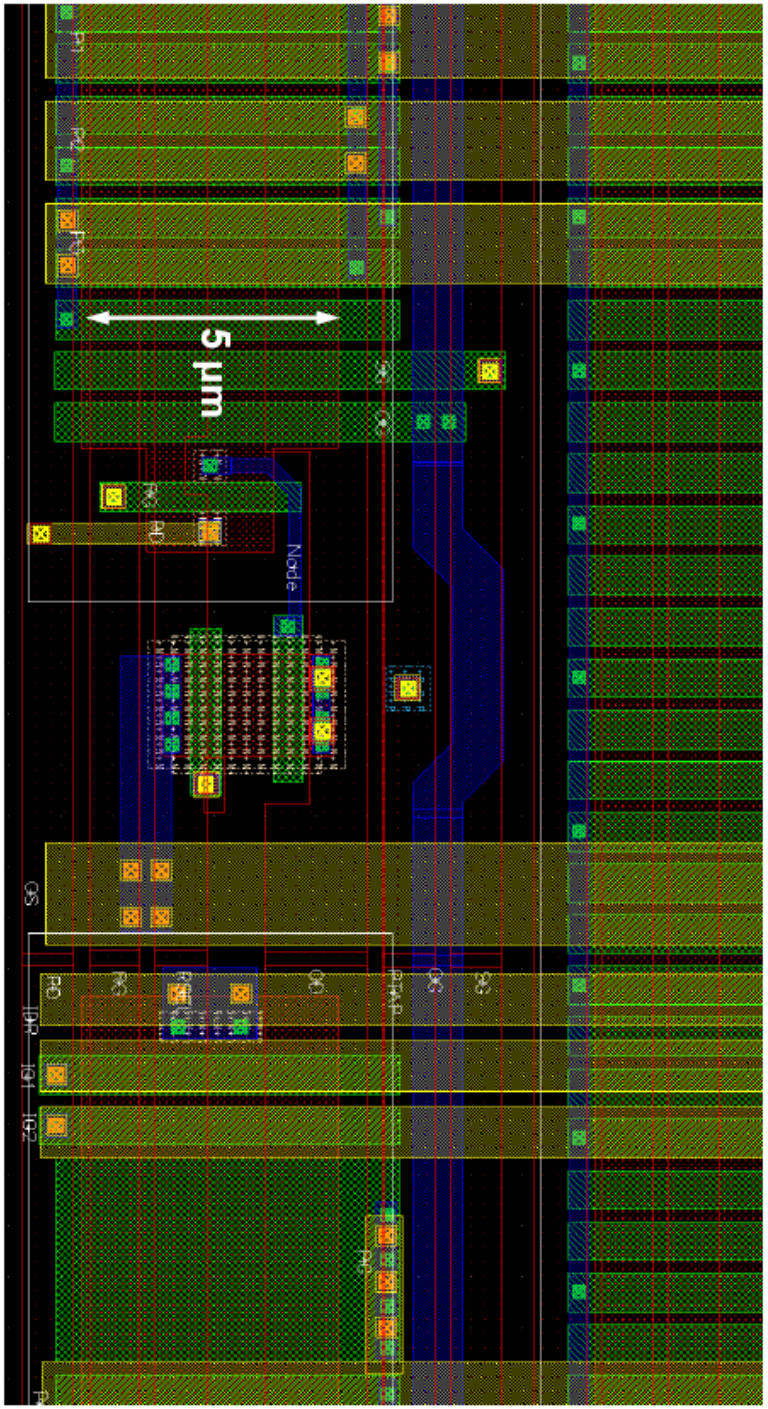
- and transfer between storage cells.



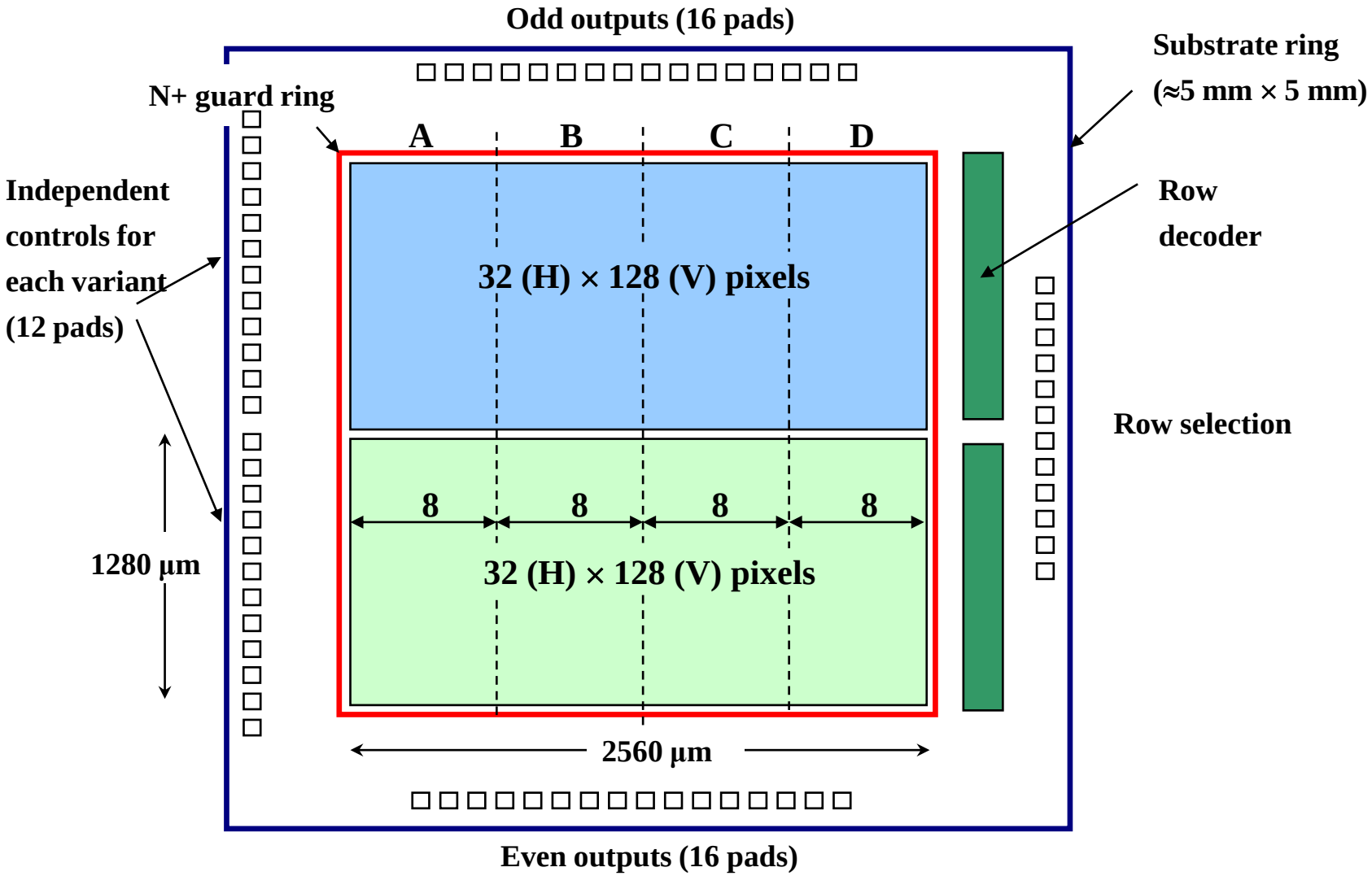
- All function with high efficiency.

ISIS2 Status

- Pixels 80 × 10 μm², buried channel 5 μm width, 3 metal layers (right).
- Konstantin has done some redesigning following discussions with Jazz and e2v about poly doping.
- Some test structures also included (transistors, short CCD), design now with Jazz engineers.
- Peter Murray has finished nearly all of top level design (logic, source followers...) using “custom” 5 V logic gates.
- Standard Jazz pads not what Peter needs?
- Target tape-out date 8th April.

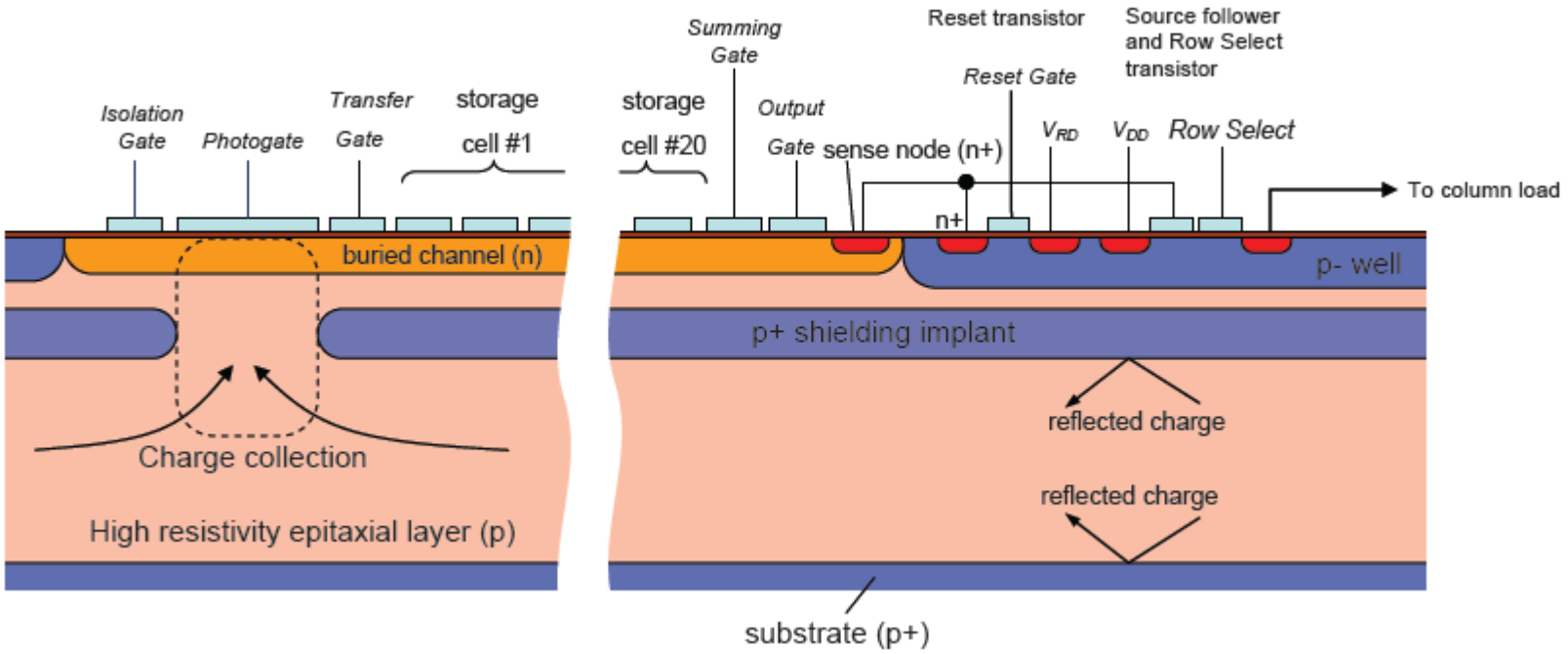


ISIS2 Tile Layout



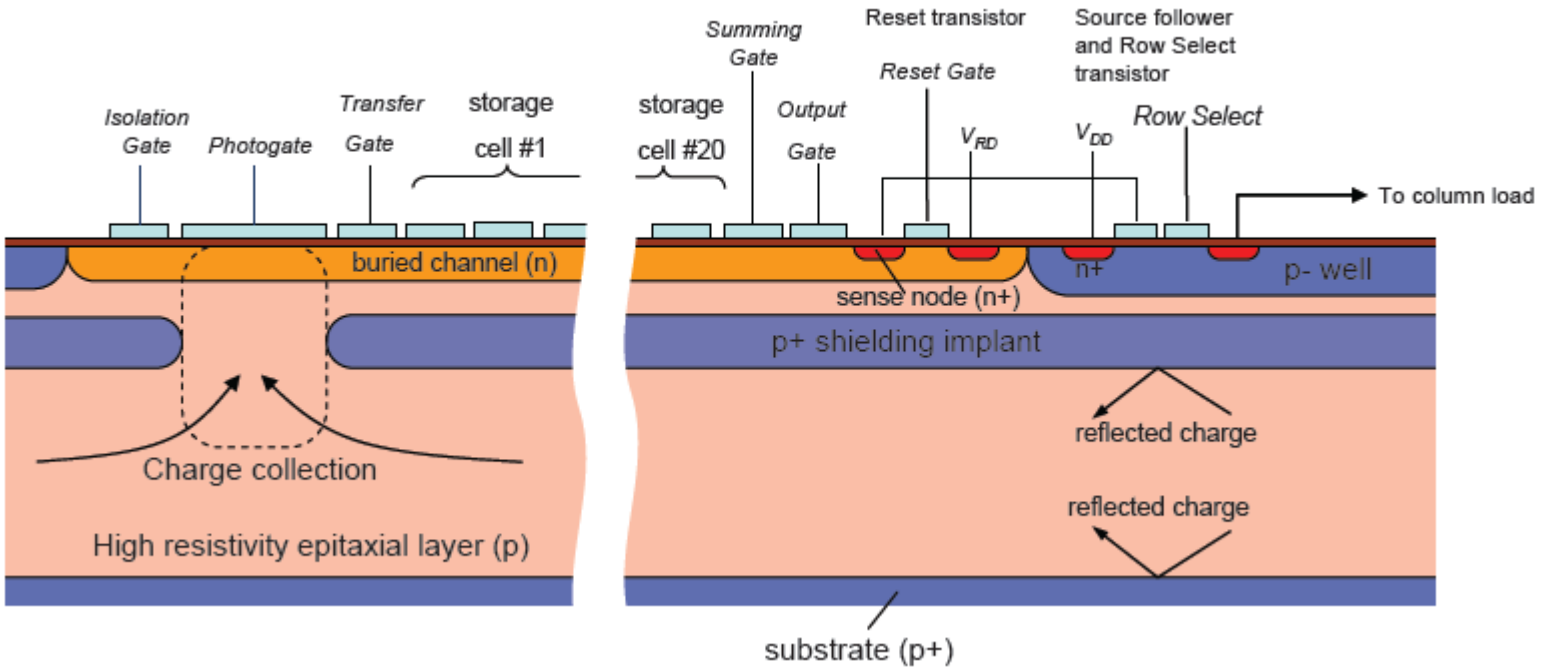
ISIS2 Variants

- Surface channel reset transistor...



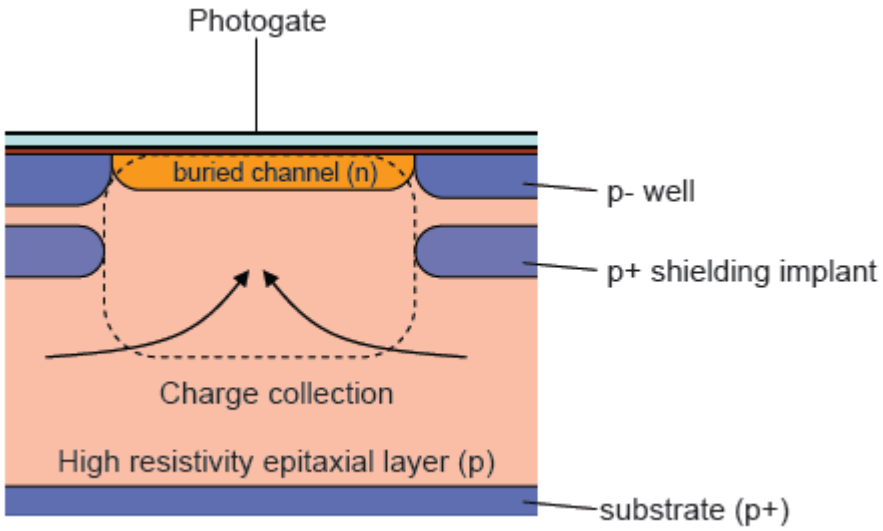
ISIS2 Variants

- Buried channel reset transistor...



ISIS2 Variants

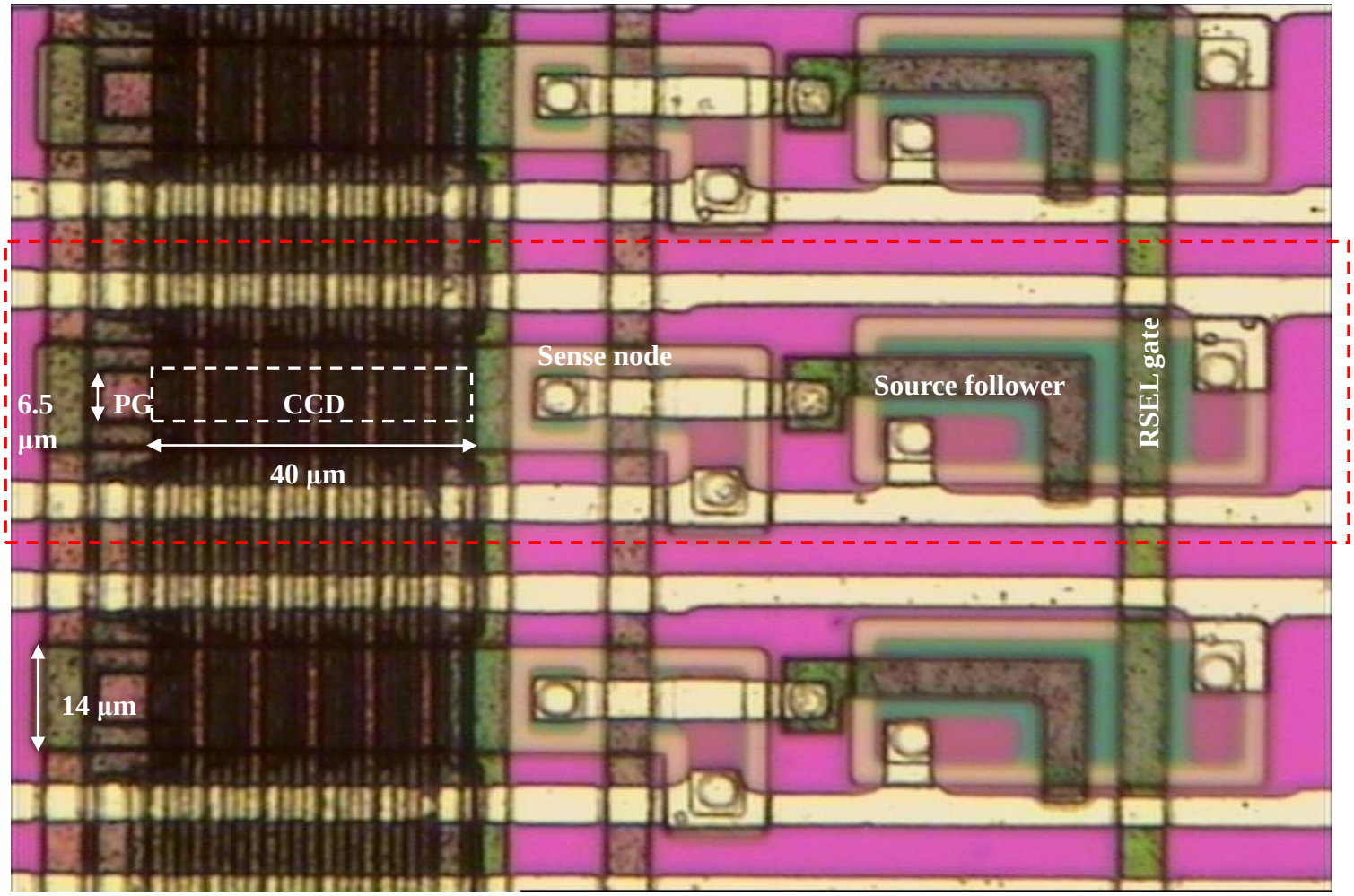
- Cross section under photogate for both previous variants:



- Further variations:
  - CCD gate pitch.
  - With deep p+.
  - Without deep p+.
  - With deep p+ but no charge collection “hole”.
  - Changess in dopant concentrations of ~20%.
- Running out of space!

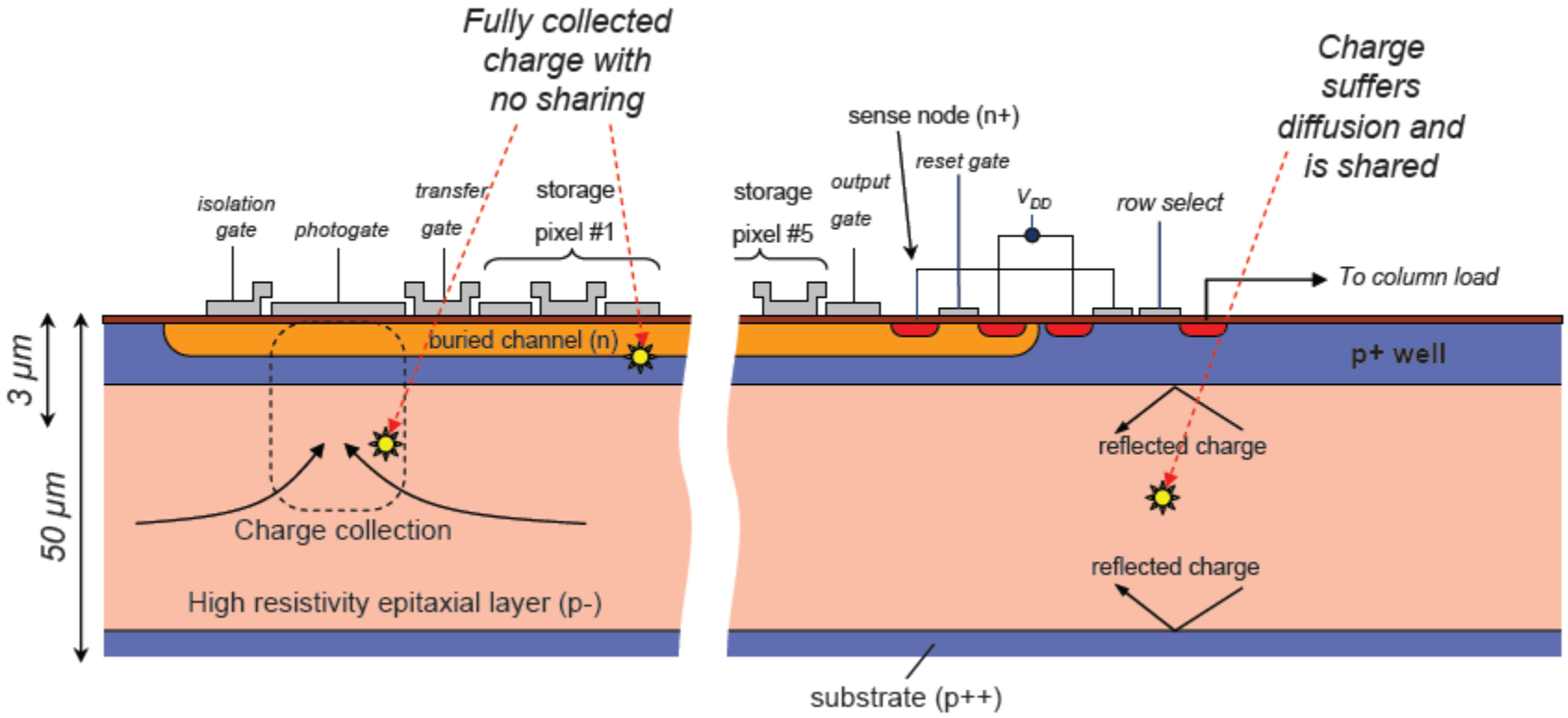
Tests of ISIS1 with p-well

- The ISIS1:



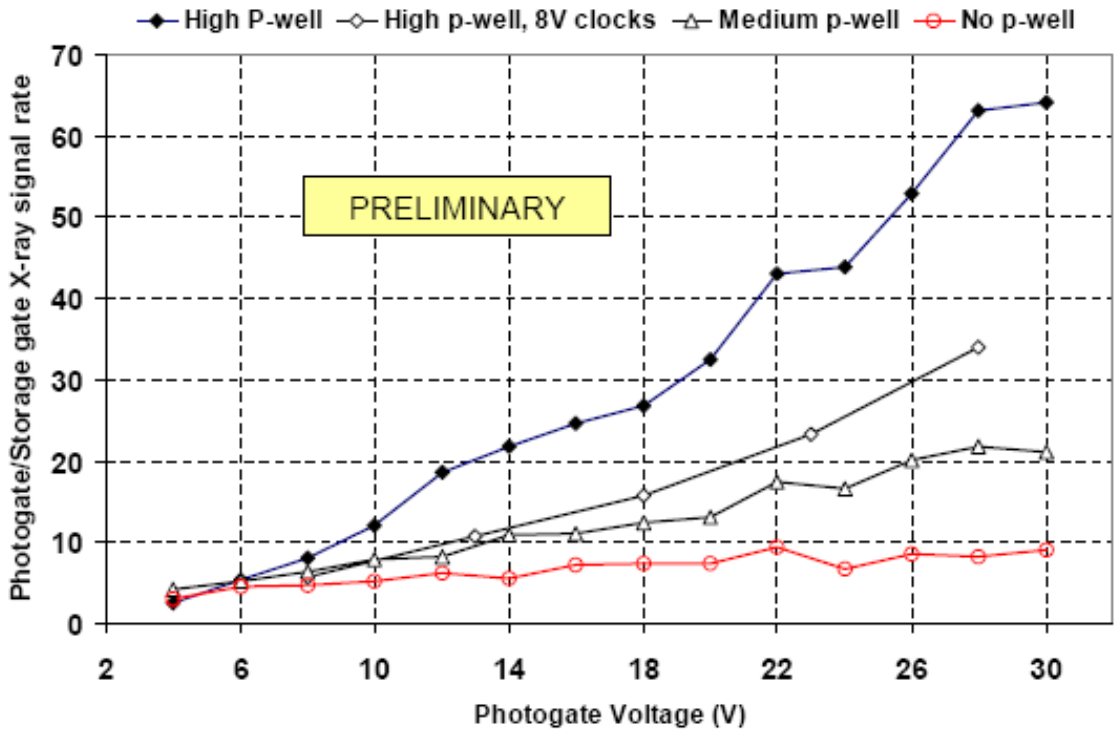
Tests of ISIS1 with p-well

- Does p-well reflect charge?
- Study using ^{55}Fe X-rays (5.9 keV, attenuattion length 30 μm, charge released in 1 μm sphere).
- Look at ratio of charge collected on photogate to charge collected on a storage pixel.
- Tests carried out by Gary.

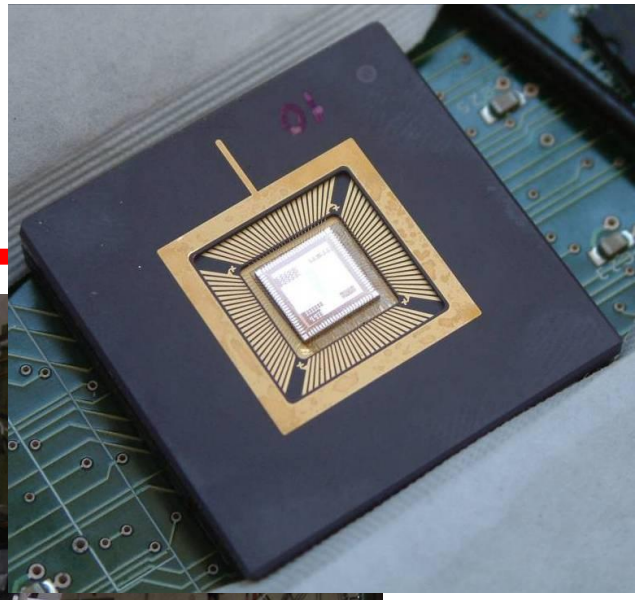


Tests of ISIS1 with p-well

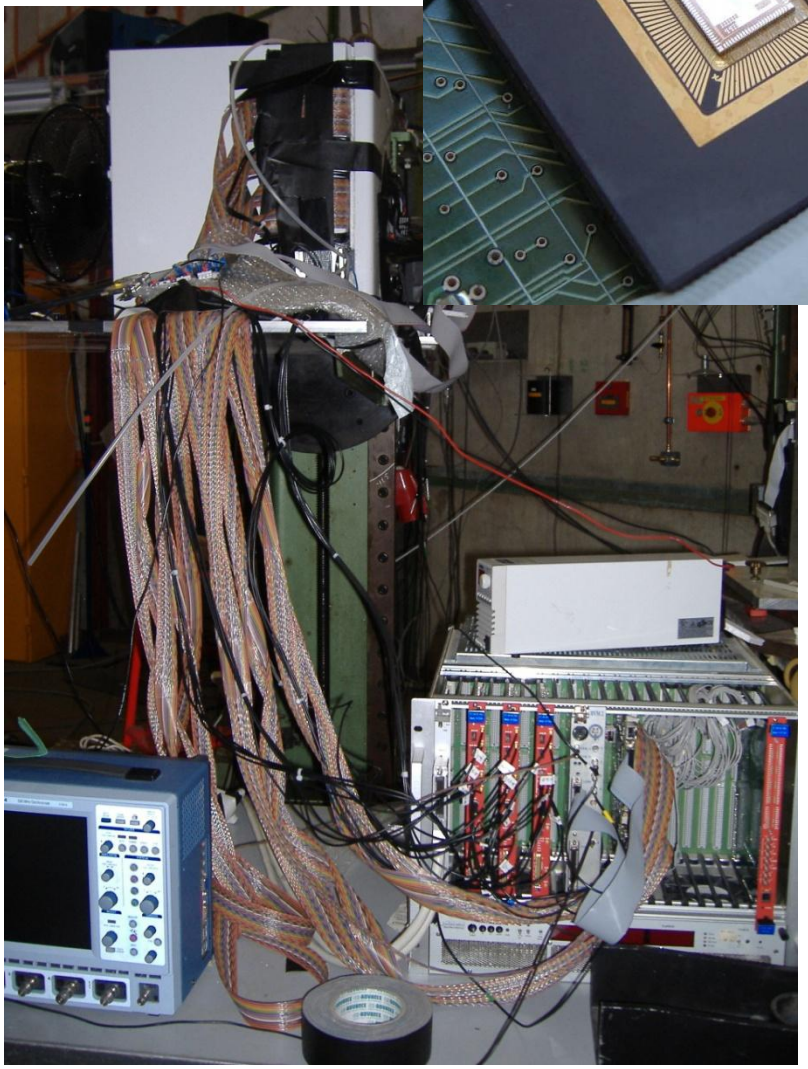
- High p-well doping, storage register protected, p-well works!
- If increase clock voltage, get punch through under in-pixel CCD, R drops.
- Lower p-well doping, charge reflection decreases.
- No p-well, R dependent on gate geometry and voltages.
- Publication being prepared.



Tests of ISIS1 in Beam

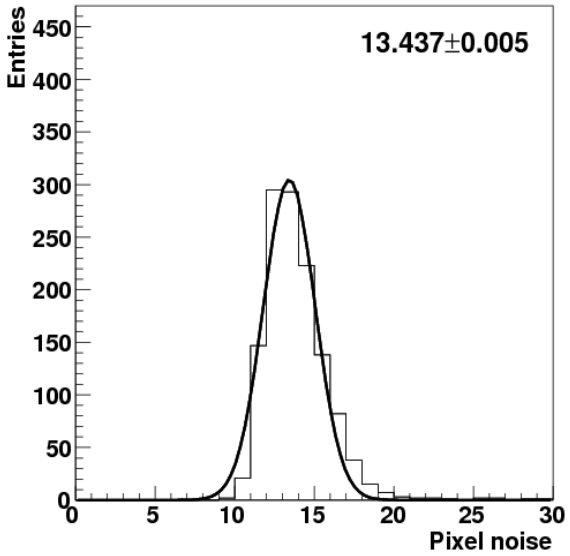


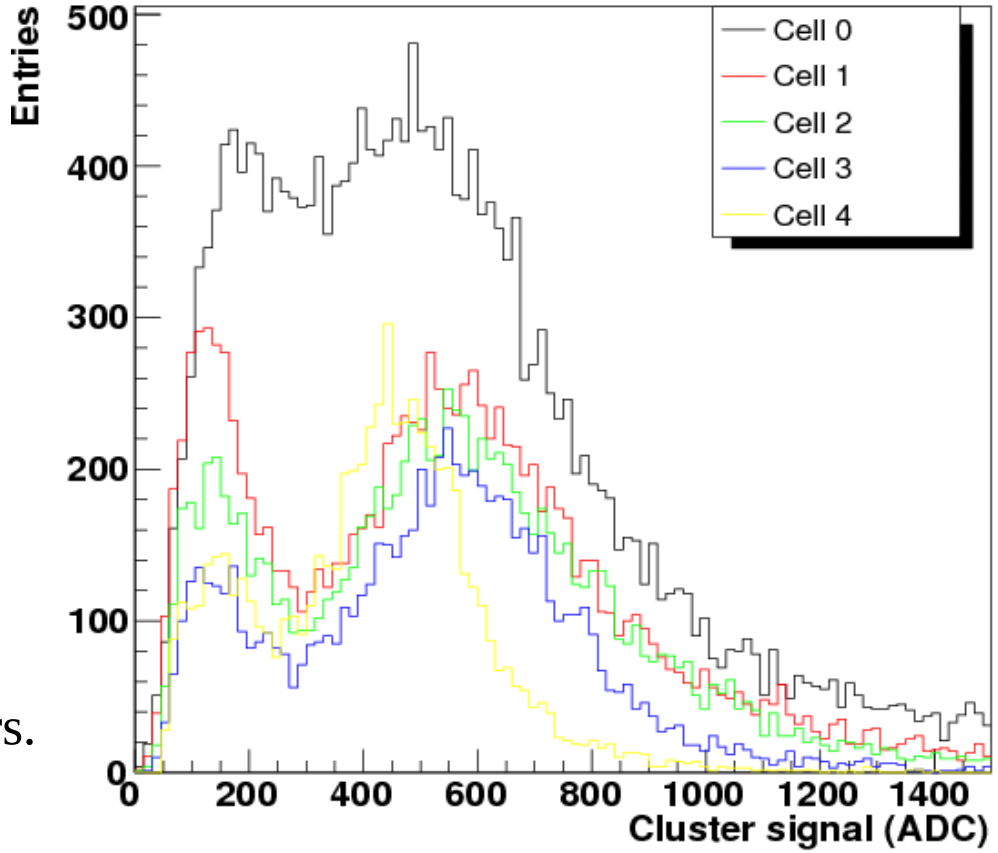
- Jaap has been analysing ISIS1 test beam data.
- Construct ISIS1 telescope with five ISIS1 chips.
- Sensors have:
- 16 × 16 pixels, each of 40 × 160 μm^2.
- Five storage cells per pixel.
- Active area 0.56 × 2.24 mm^2.
- Accurate alignment required!
- Tests performed in DESY 1...6 GeV e^- beam.
- Readout speed 2.5 MHz, (ILC needs 1 MHz).



Tests of ISIS1 in Beam

- Calculate pedestal for each pixel.
- Noise from standard deviation after pedestal subtraction.

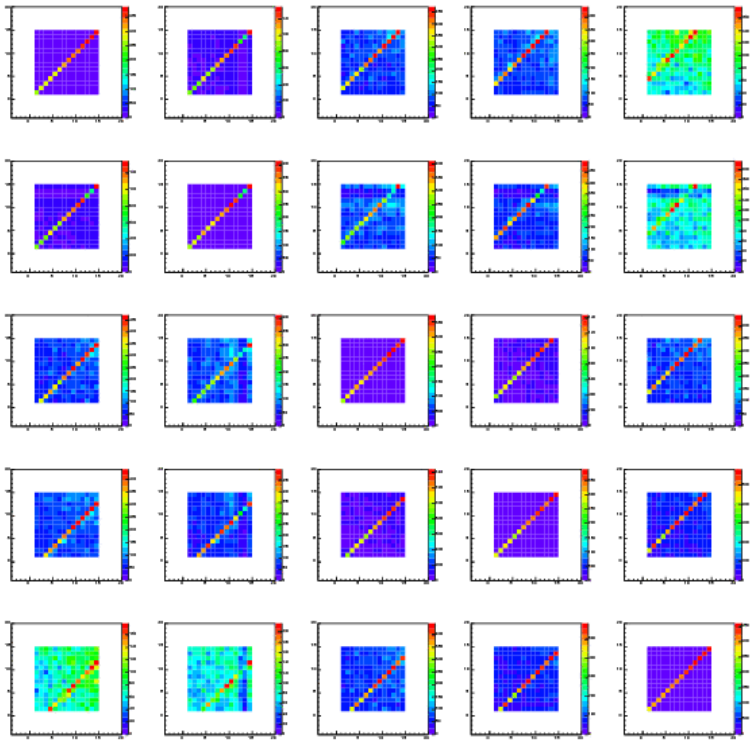




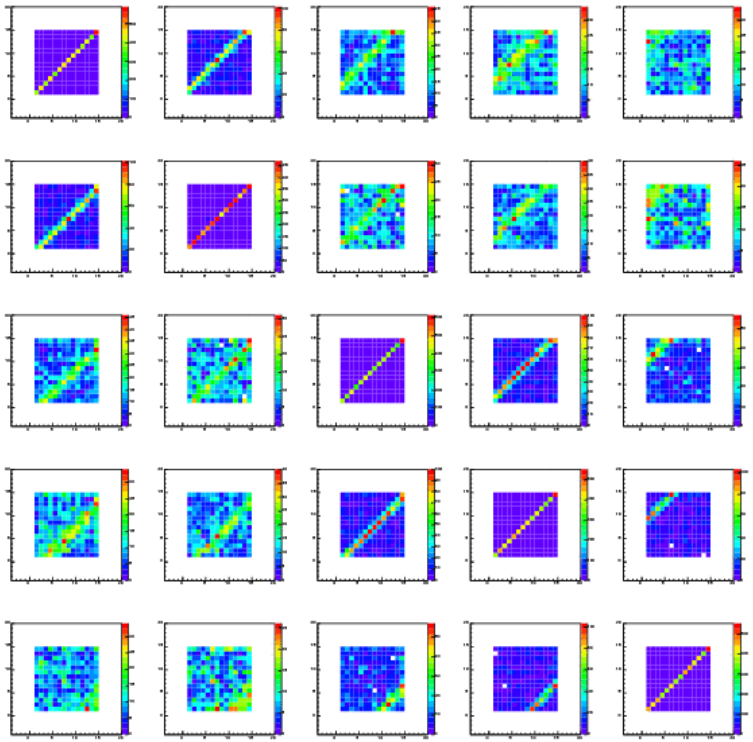
- Clusters 5σ seed, 2σ neighbours.
- Clusters small: little charge sharing in y (“long”) direction.
- S/N ~ 37.

Tests of ISIS1 in Beam

- x versus x (“short” direction).



- y versus y (“long” direction).



Tests of ISIS1 in Beam

- Use sensors 0, 1 and 3 to predict position of hit in sensor 2.
- Hence determine deviations and resolution.
- Problems where no charge sharing observed – deviation then typically zero!
- In x direction where sharing get $\sigma = 10.8 \pm 0.3$ μm.
- Compare with $60/\sqrt{12} = 17.3$ μm.
- Includes (large) multiple scattering effects.
- Results don't change with choice of memory cell (time slice).
- Next test beam planned for end August at CERN using high energy beam and EUDET telescope.
- Will include ISIS1 with p-well.
- Obtain more precise resolution numbers.
- Study parasitic charge collection.
- Publication to follow.

Summary

- CPC-T will be available for testing shortly.
- CPC2 and CPR2A/B also now available.
- ISIS2 design progressing well, but time tight!
- Functioning of p-well in ISIS1 demonstrated.
- Results from ISIS1 test beam starting to emerge.
- Further ISIS test beam planned at CERN for end August.
- Testing of CPR2A/B bump-bonded to CPC2 to come.
- Expect publications on CPC-T, on ISIS1 and CPC2 + CPR2A/B tests and also on design and performance of ISIS2.
- Negotiations with Janet Seed ongoing to ensure we have support for these studies.