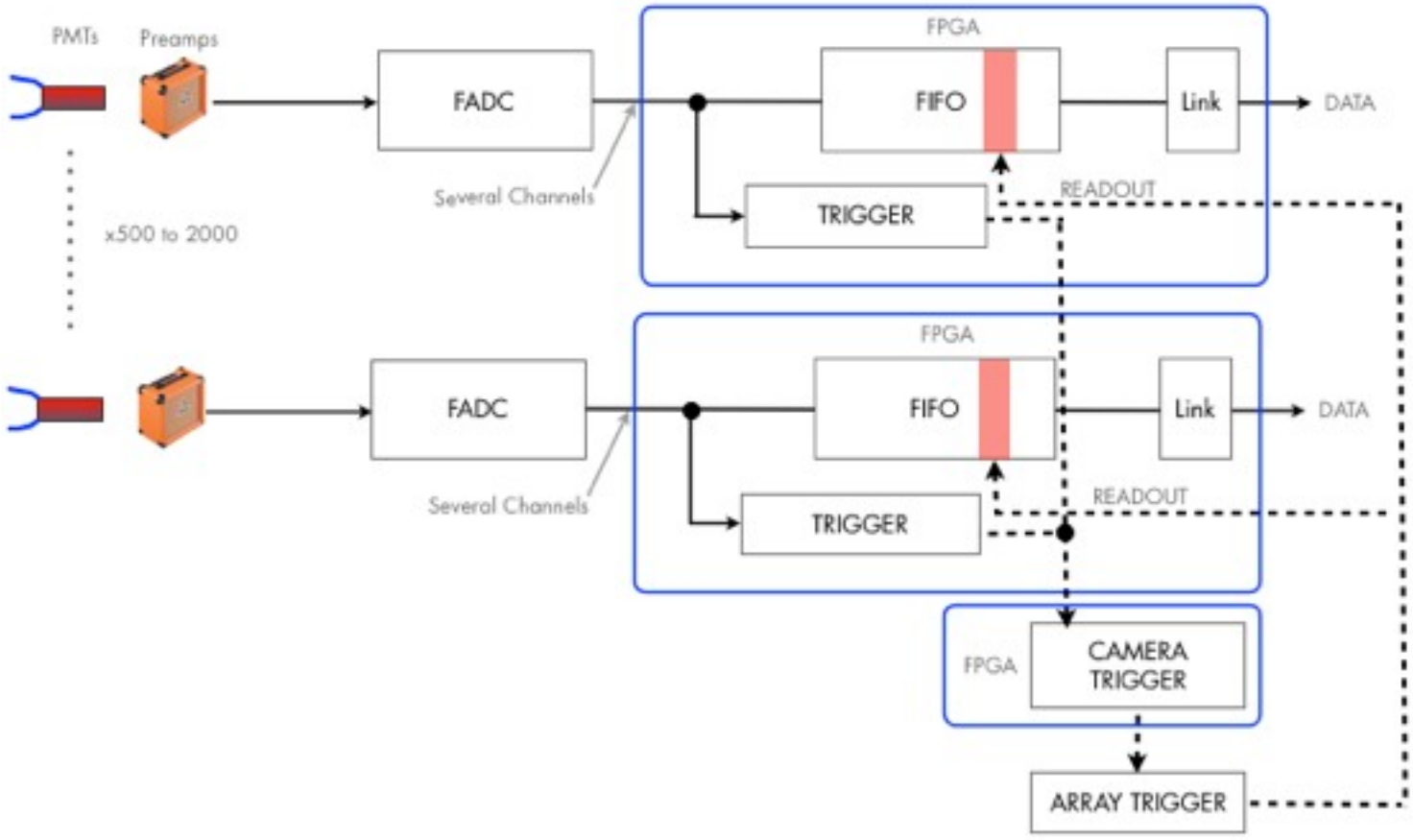
FLASHCAM

Richard White for the FLASHCAM team
SST Meeting, Liverpool, 7-8 Sep. 2010

Note that only 0.01% of this is my own work, most plots and points have been stolen directly from FLASHCAM talks in Zurich and Zeuthen.

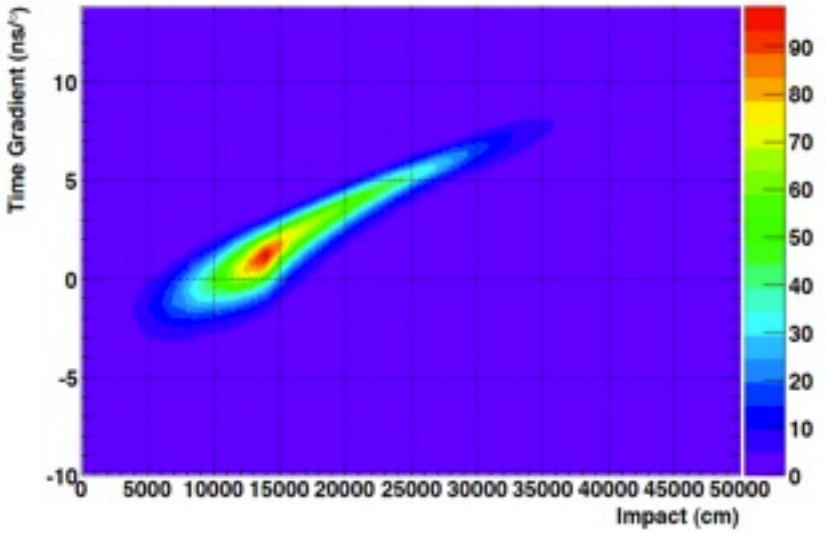
FRONT END ELECTRONICS

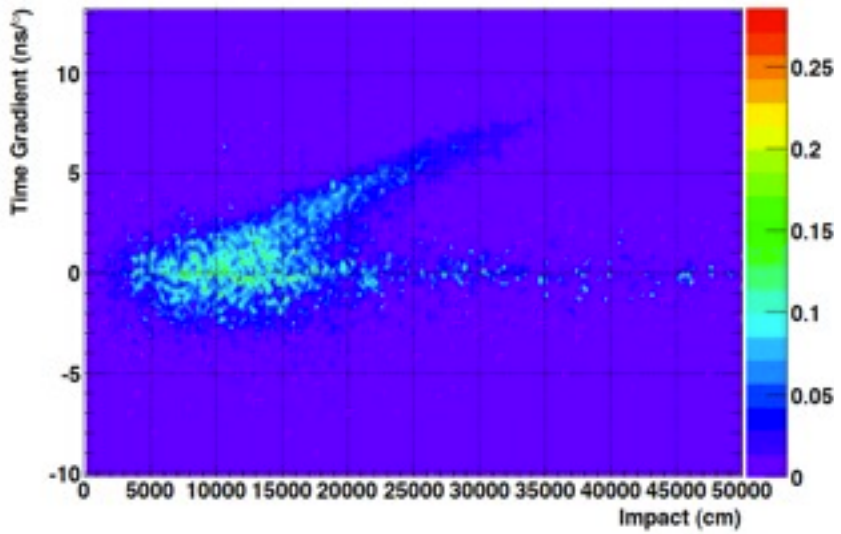
FADC



ImageTiming
High Energies (1 TeV – 100 TeV)

- Time gradient increases with impact distance.
- Length is also increasing
- At 1 km impact, we're looking at image durations of hundreds of ns.
- Sampling does not need to be in 0.5 ns or 1 ns slices!

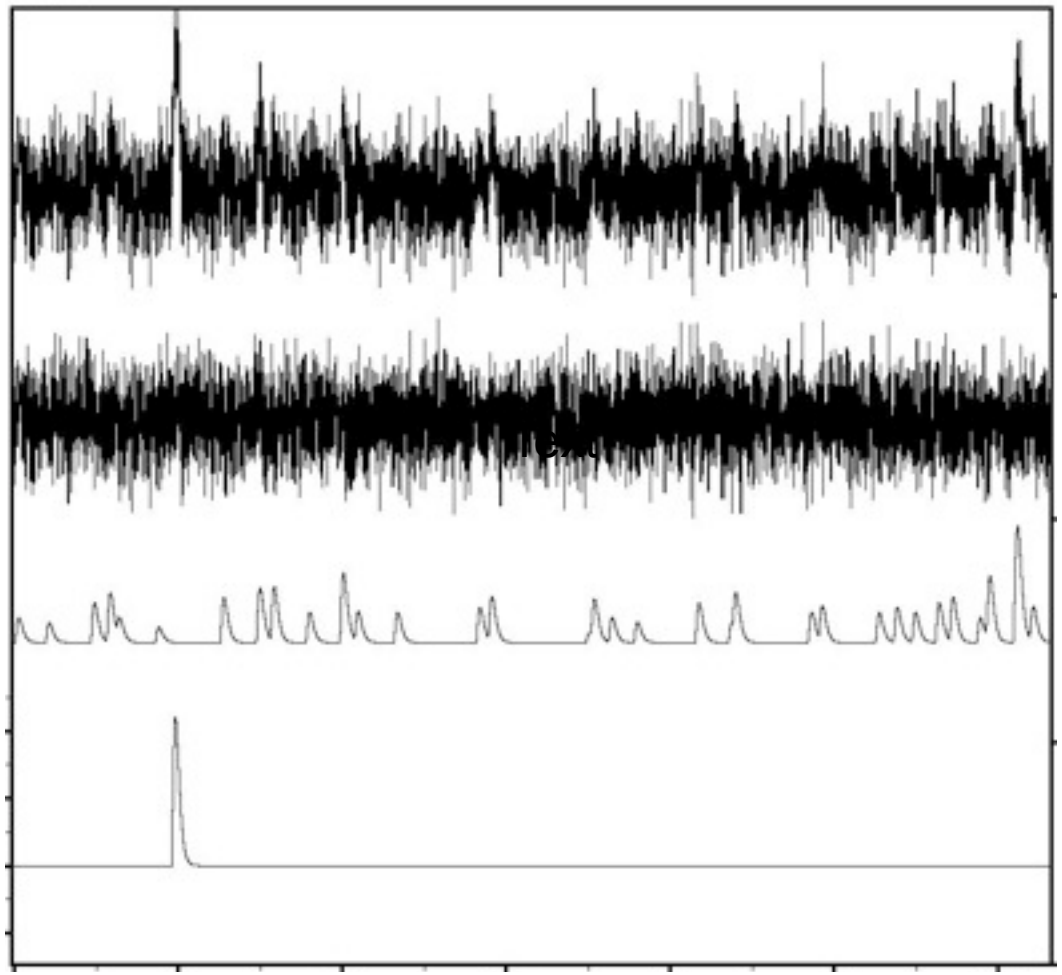




What is the minimum digitisation speed to maintain timing resolution and background rejection capability?

SIMULATIONS

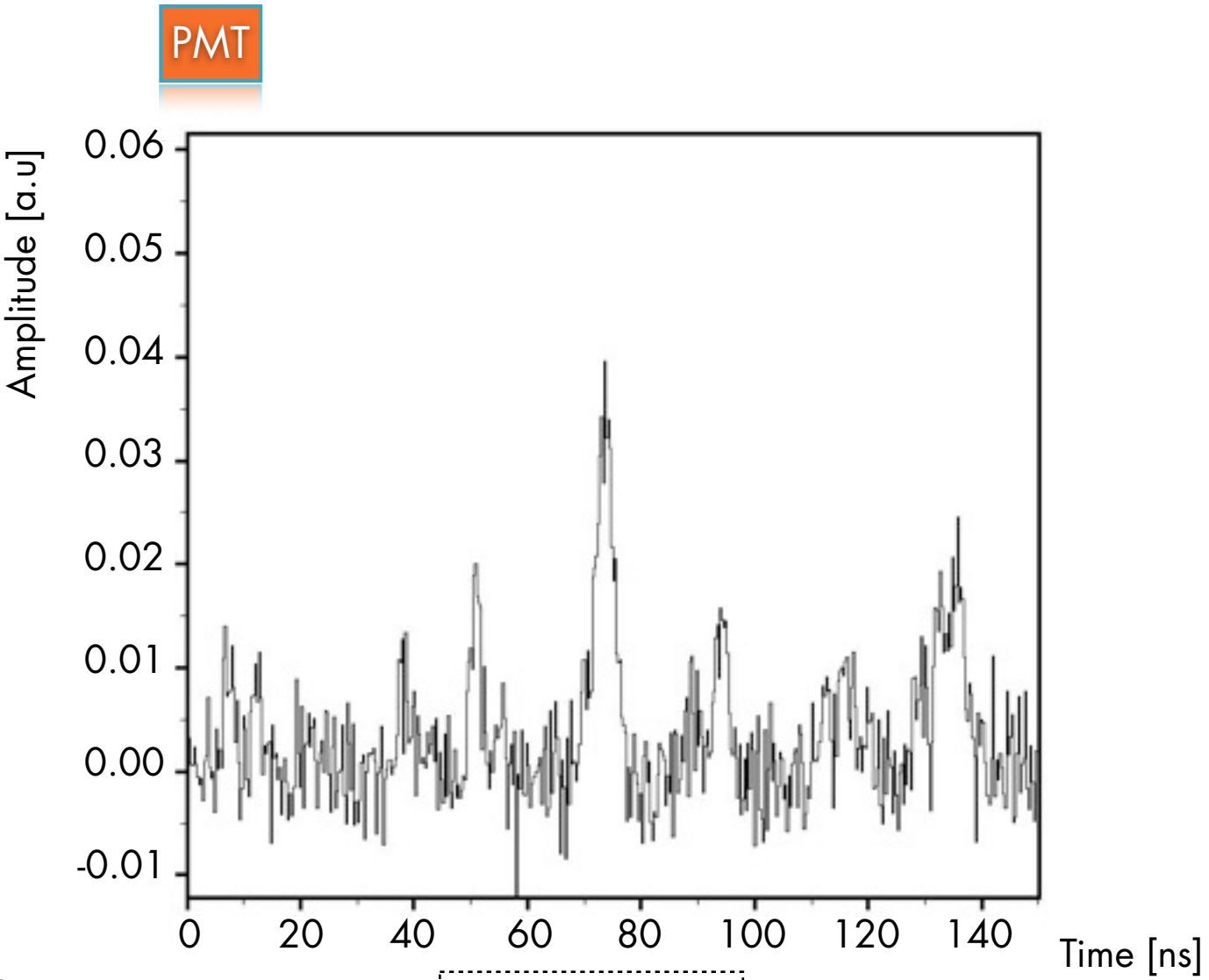
What is the optimum digitisation speed?



All Sims from MPIK

SIMULATIONS

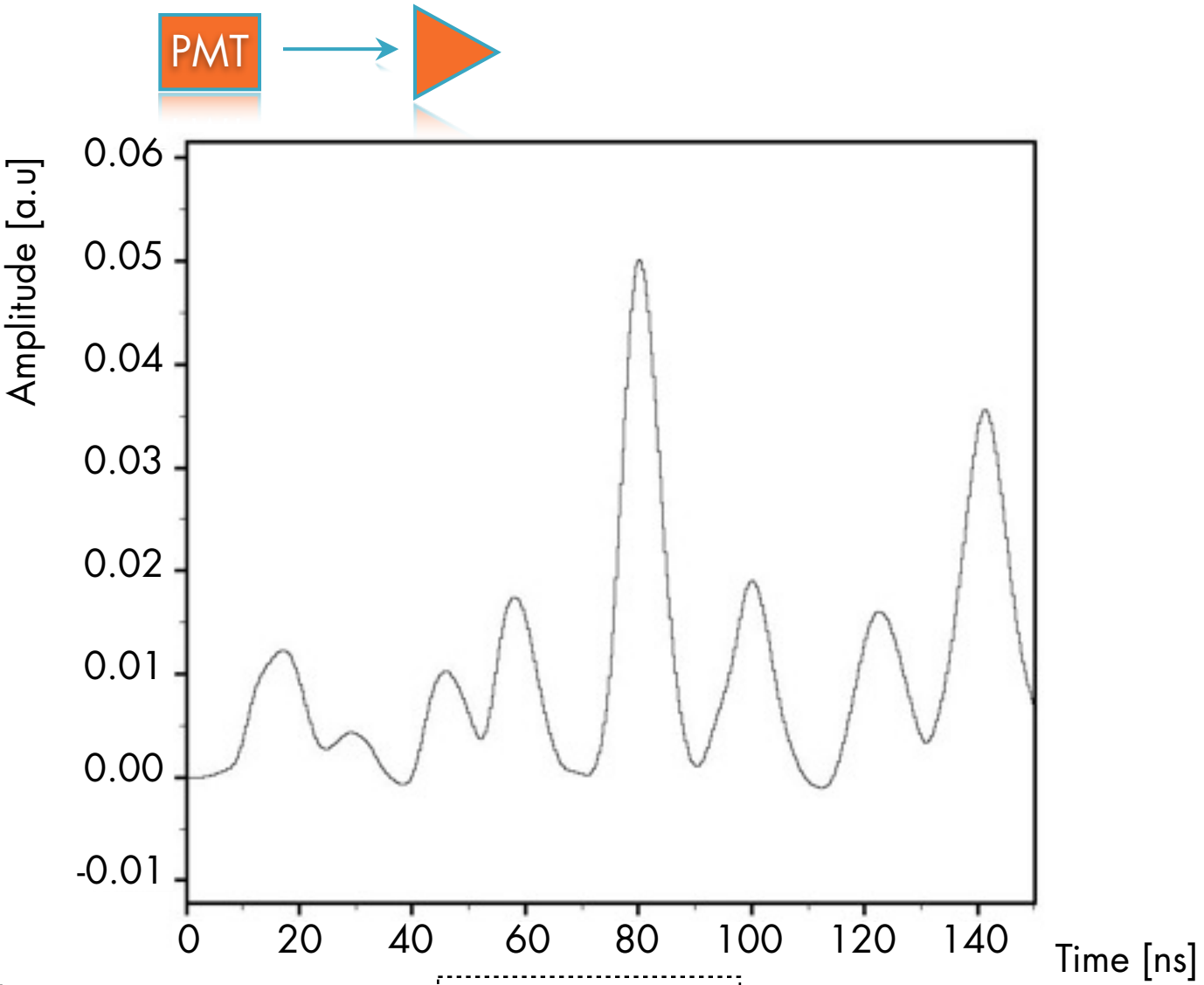
PMT: Signal simulation at 50 GHz (shown at 5 GHz)



All Sims from MPIK

SIMULATIONS

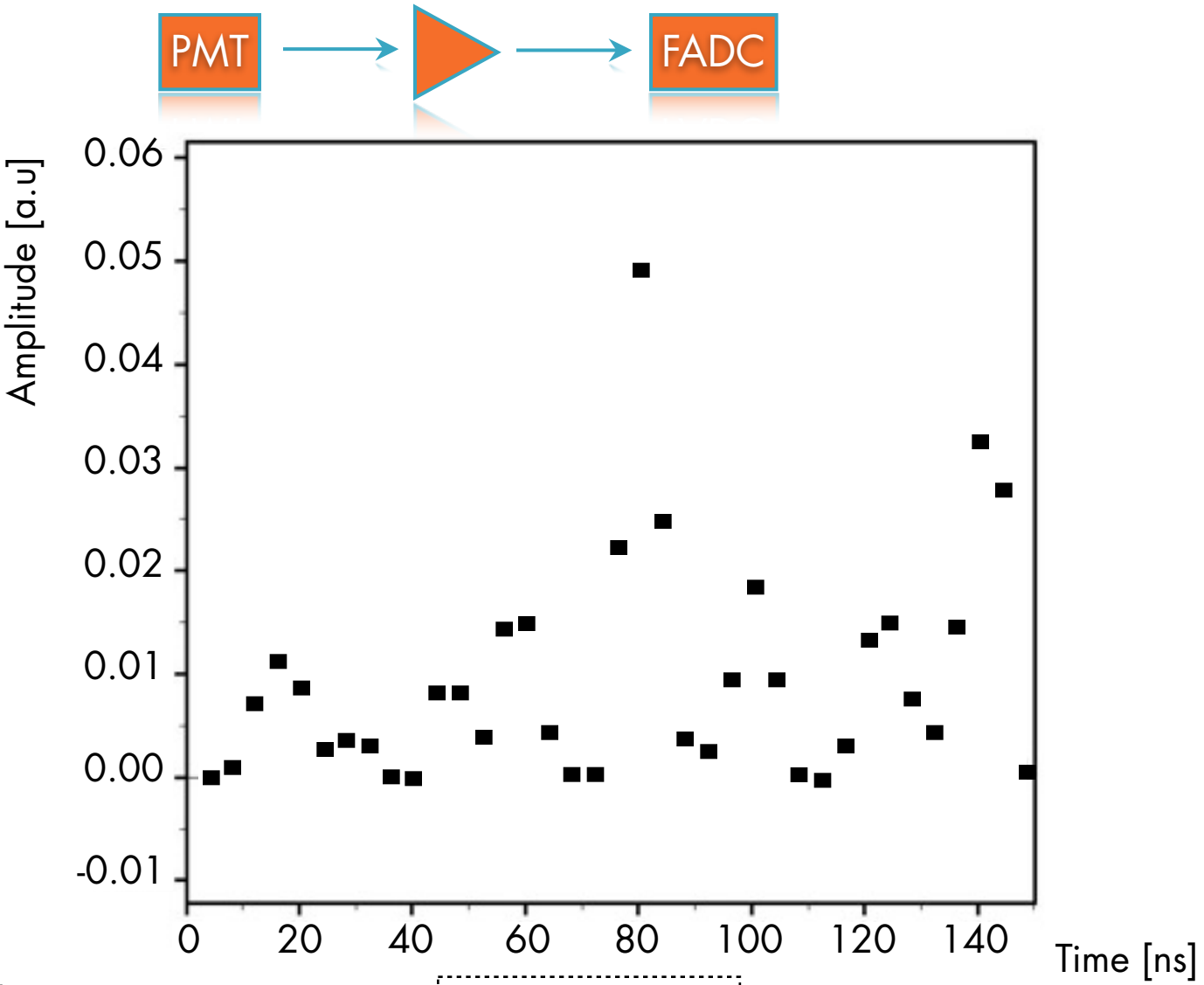
Pre-Amp: Signal after low-pass filter



All Sims from MPIK

SIMULATIONS

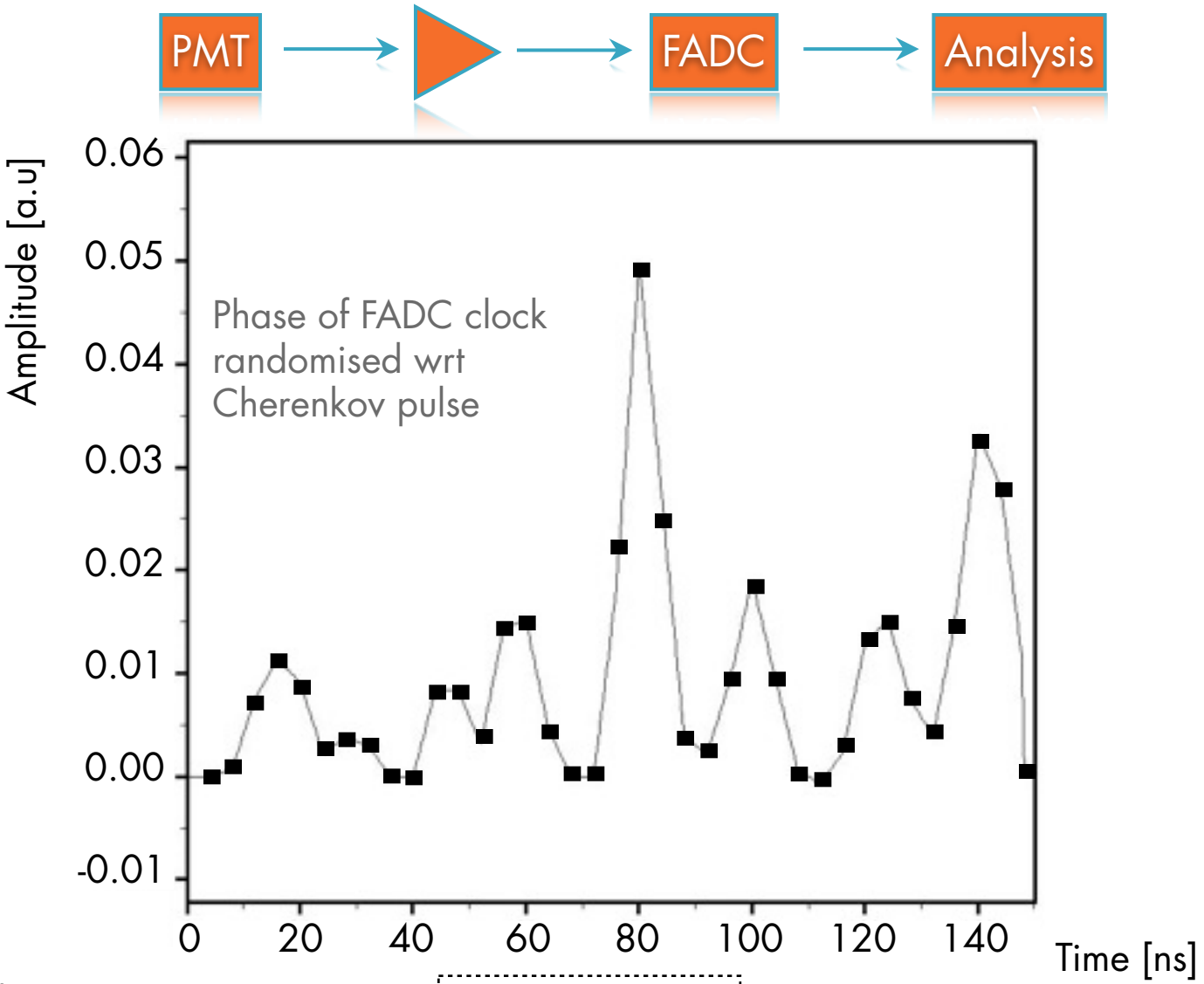
FADC: Digitised signal (250 MHz)



All Sims from MPIK

SIMULATIONS

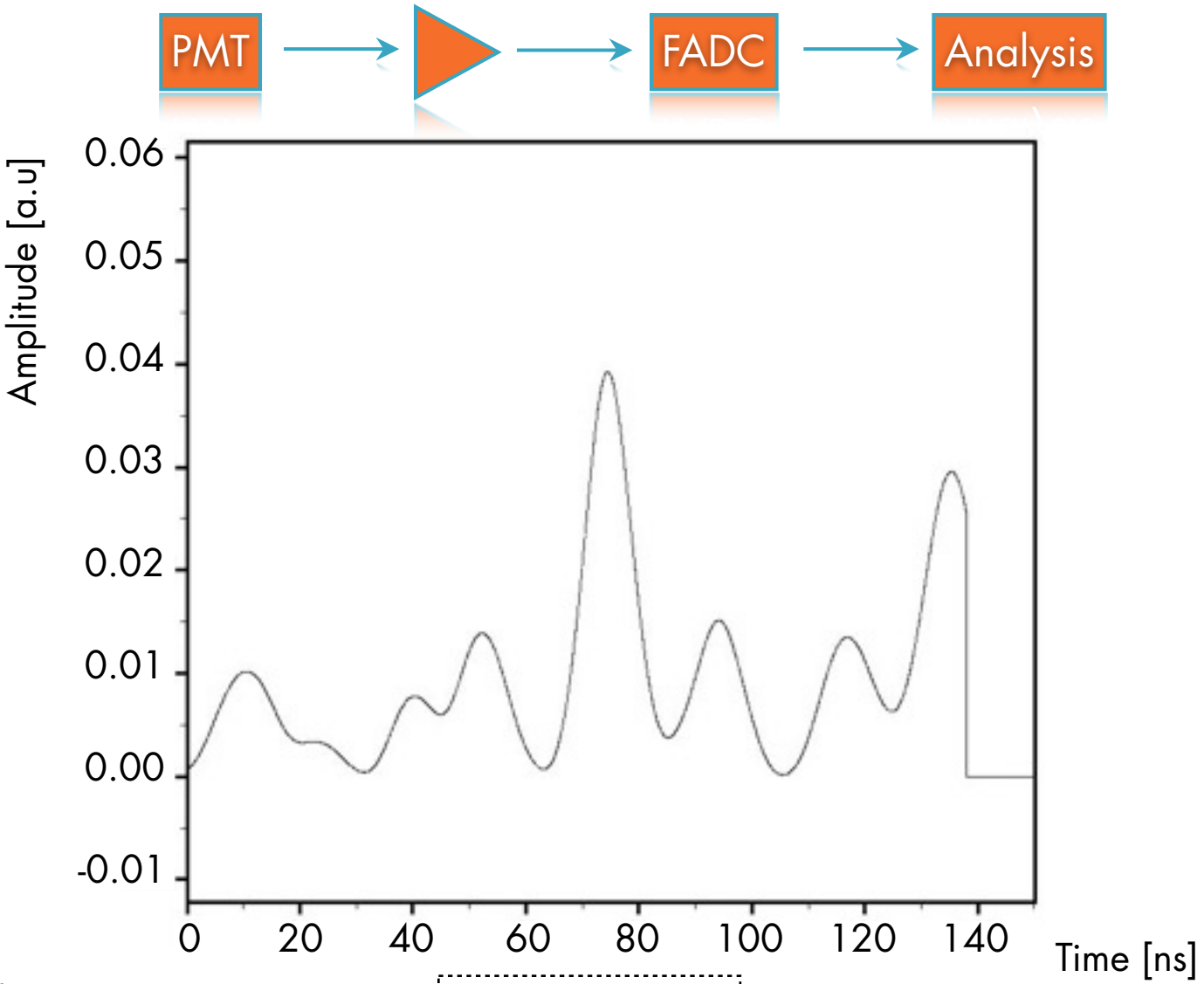
FADC: Digitised signal (250 MHz)



All Sims from MPIK

SIMULATIONS

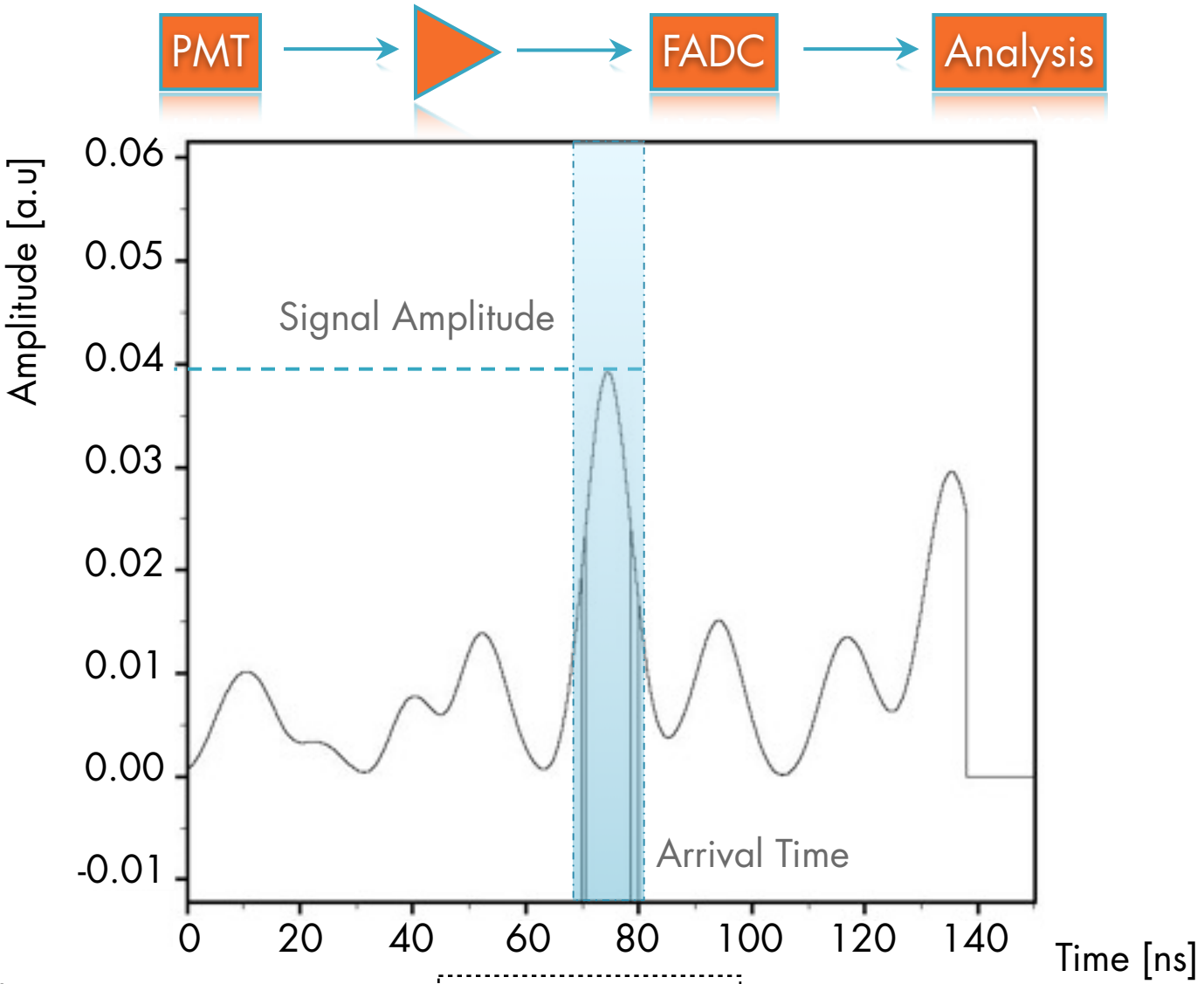
Analysis: Smoothing of interpolated signal



All Sims from MPIK

SIMULATIONS

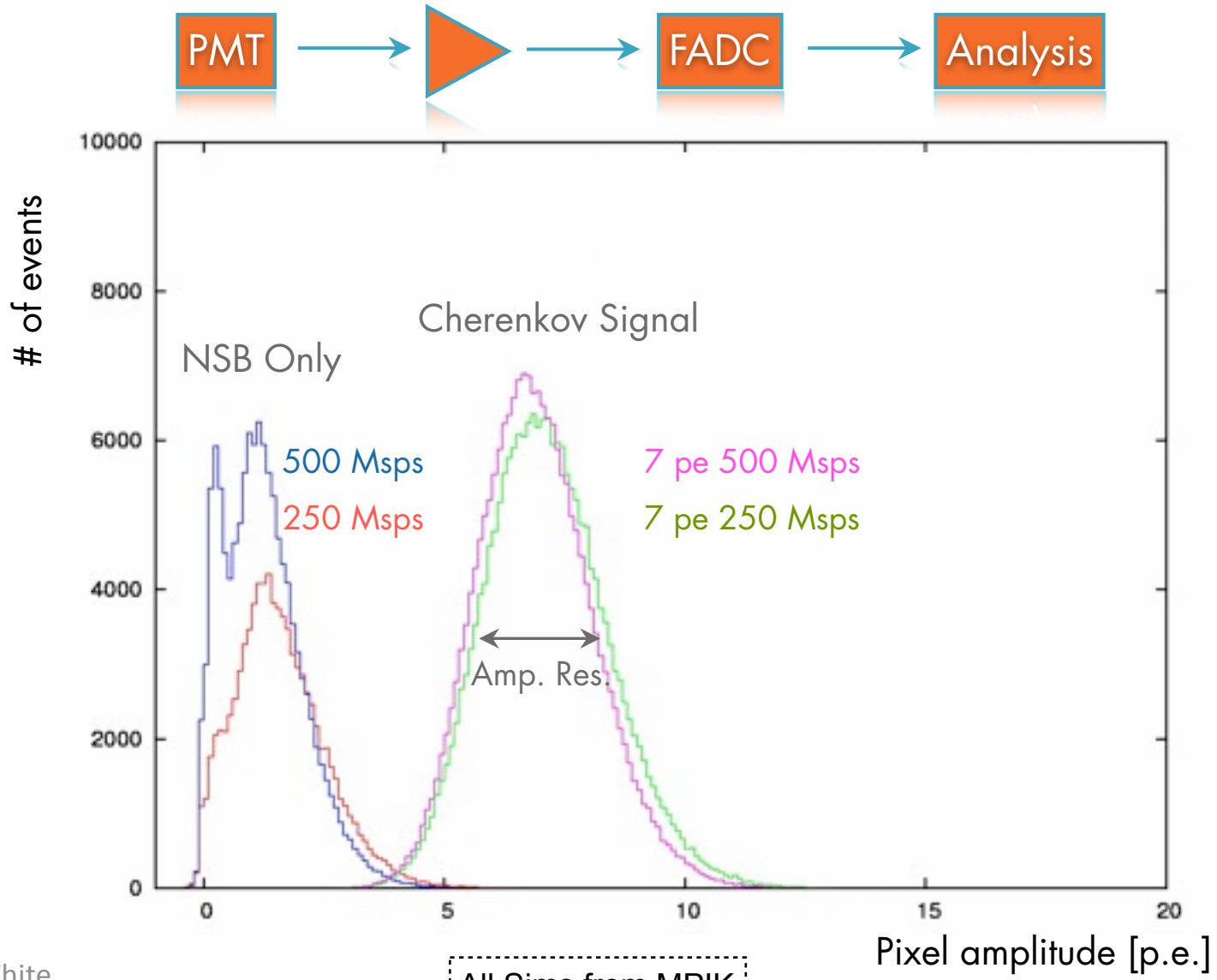
Analysis: Recover signal amplitude and arrival time



All Sims from MPIK

SIMULATIONS

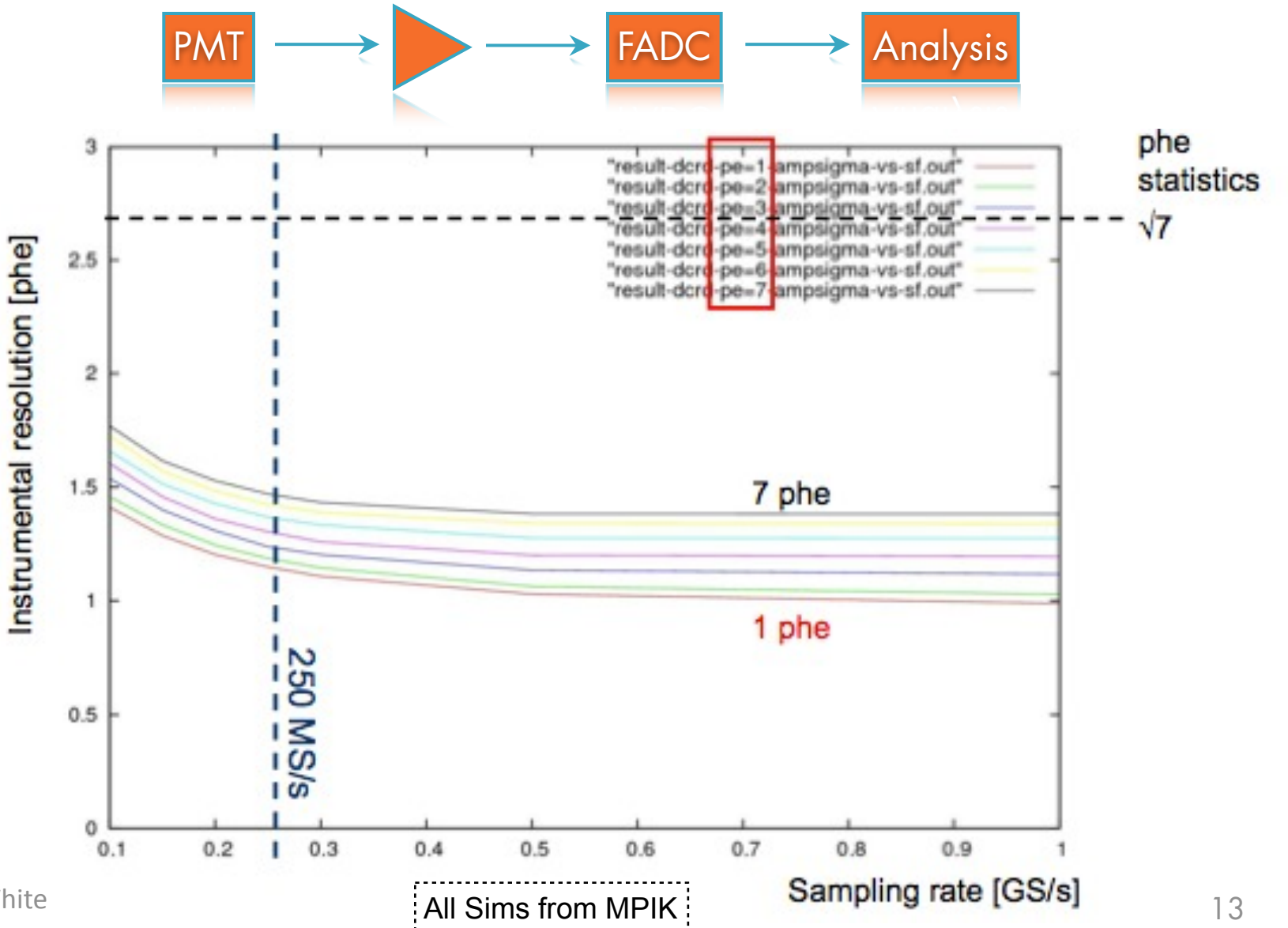
Analysis: Distribution of signal amplitudes (DC, MST)



All Sims from MPIK

SIMULATIONS

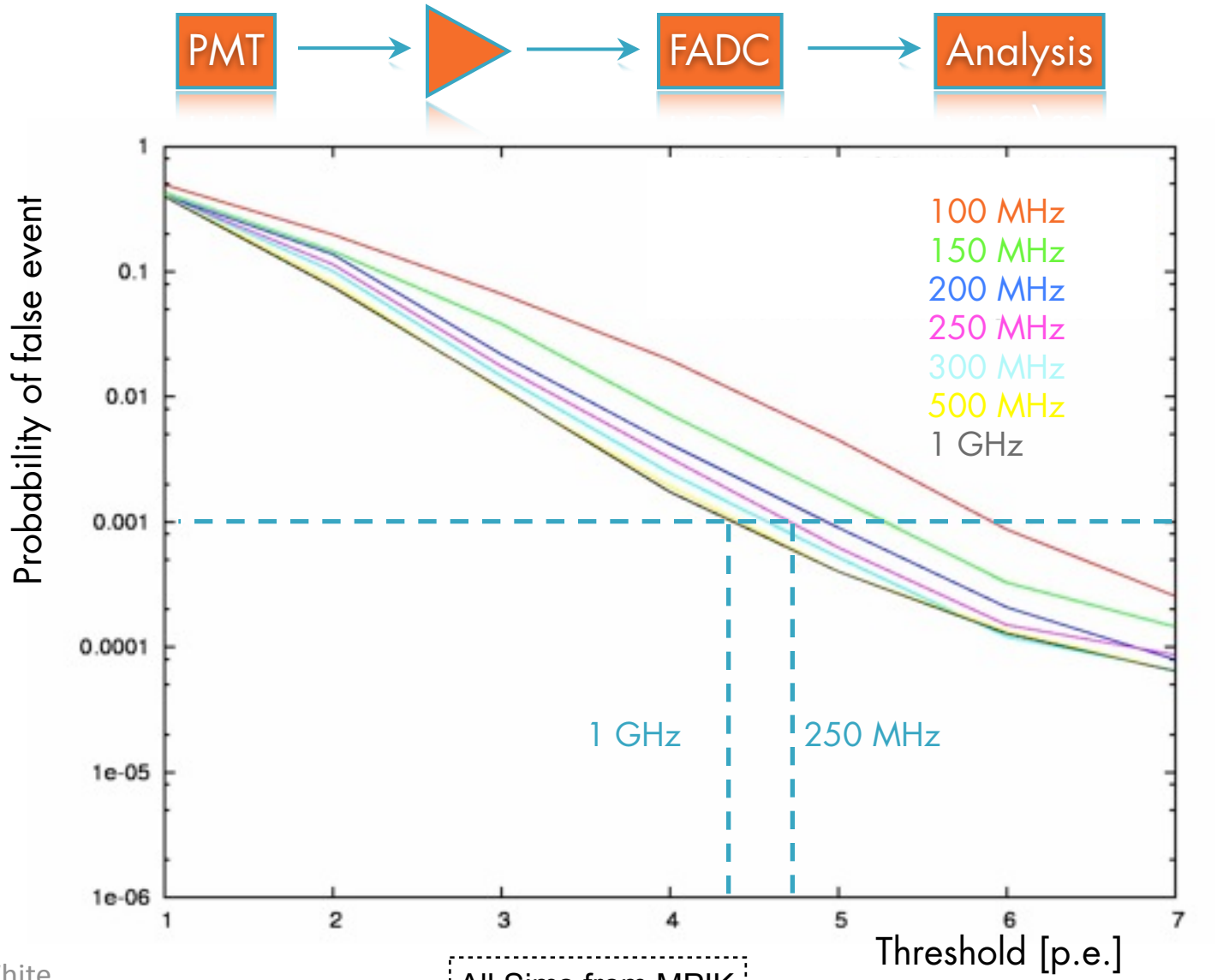
Analysis: Amplitude resolution vs. sampling frequency (DC, MST)



All Sims from MPIK

SIMULATIONS

Analysis: Background rejection (DC, MST)



All Sims from MPIK

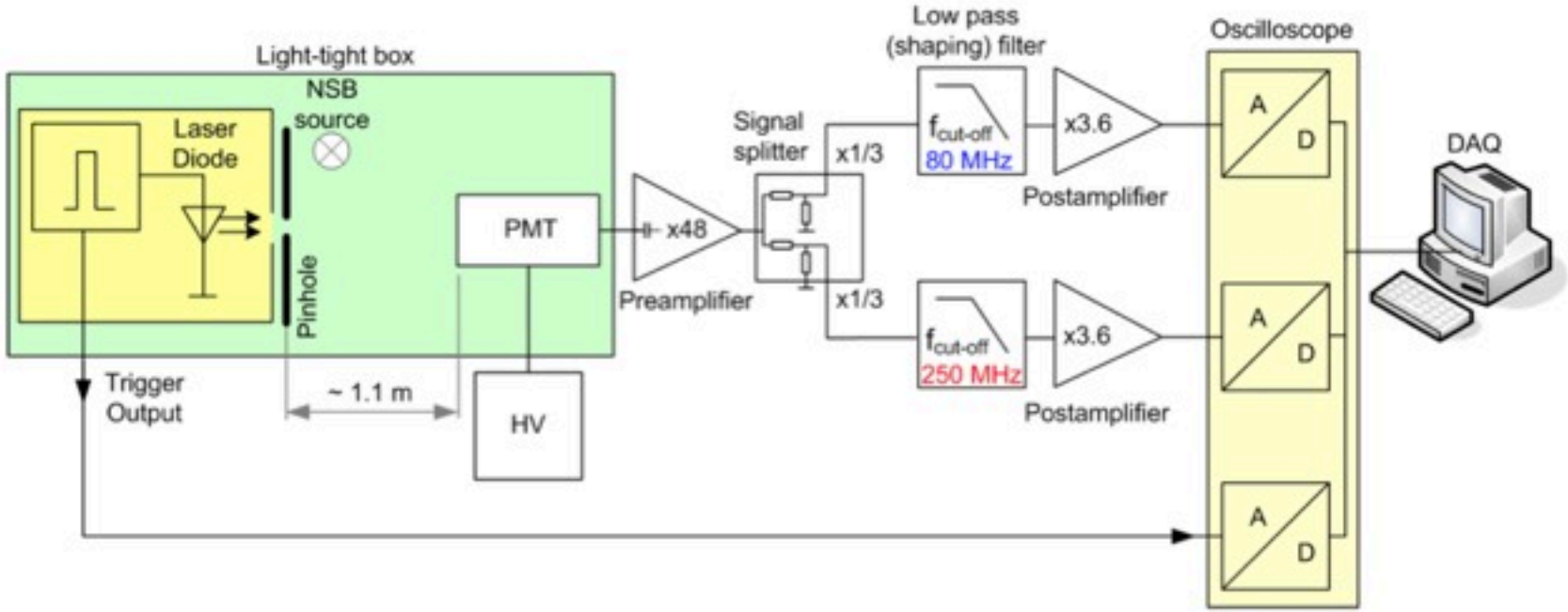
SIMULATIONS

Analysis: Background rejection

- Amplitude and time resolution do not improve significantly above 250 MHz, and there is no improvement at all >500 MHz.
- Amplitude Resolution: ~1.5 pe, only requires an increase of 0.3 pe in software threshold for a DC reflector.
- Time Resolution: ~1 ns (pixel signal >3 pe) and ~0.5 ns (pixel >7 pe).
- Don't need fast sampling for the SST.

MEASUREMENTS

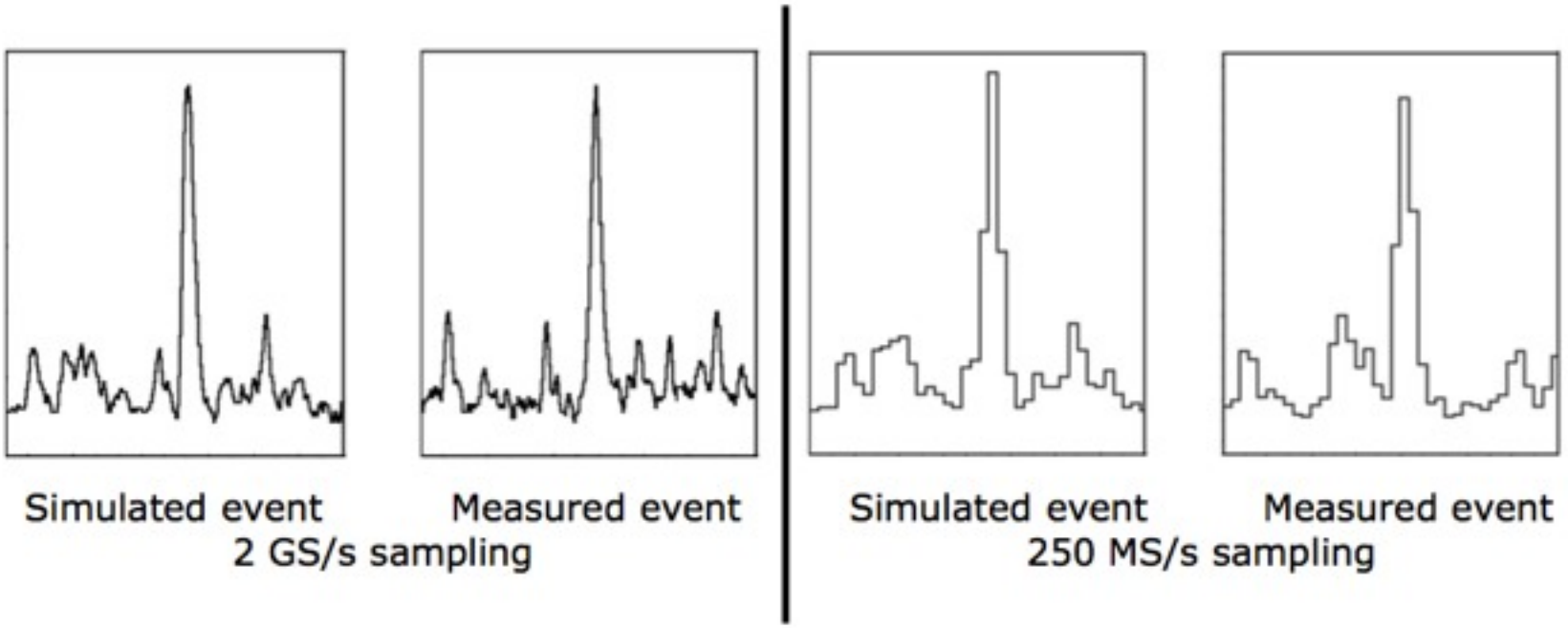
Test Setup



MEASUREMENTS

Results

- The simulations should be believed.



11.05.10, Arno Gadola
CTA Meeting Zeuthen

MEASUREMENTS
Results

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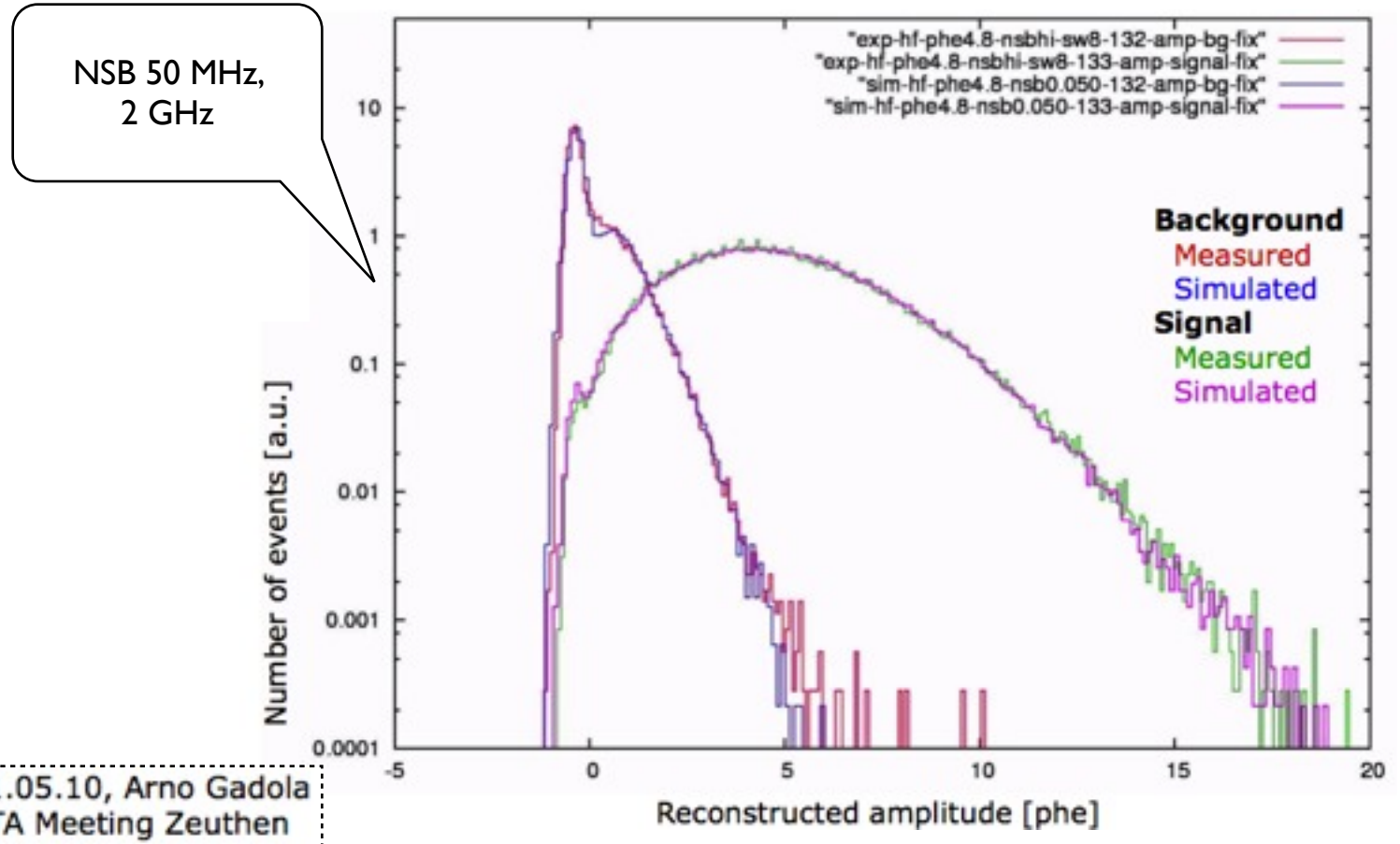
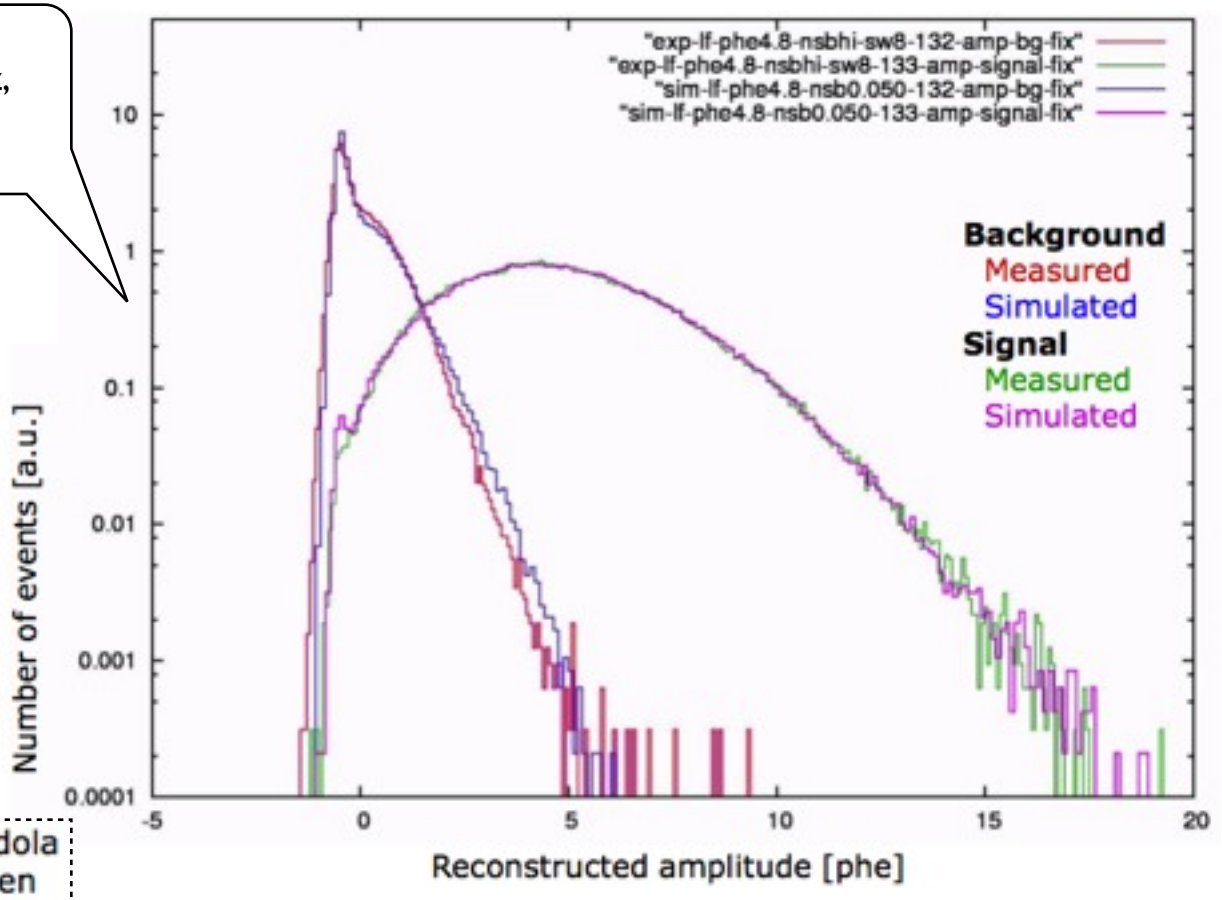


MEASUREMENTS
Results

- The simulations should be believed.

NSB 50 MHz,
250 MHz



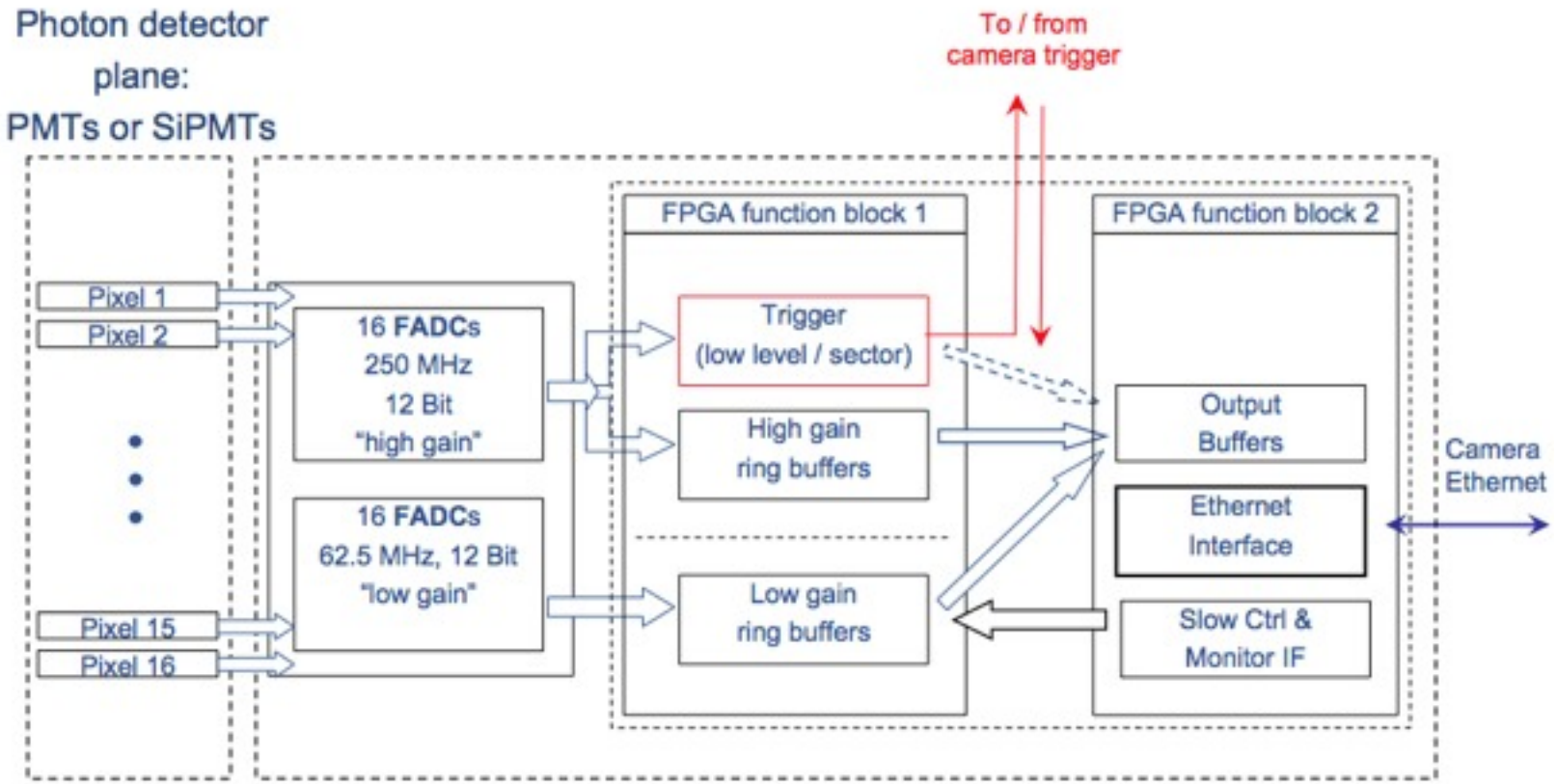
11.05.10, Arno Gadola
CTA Meeting Zeuthen

FLASHCAM

A fully digital camera

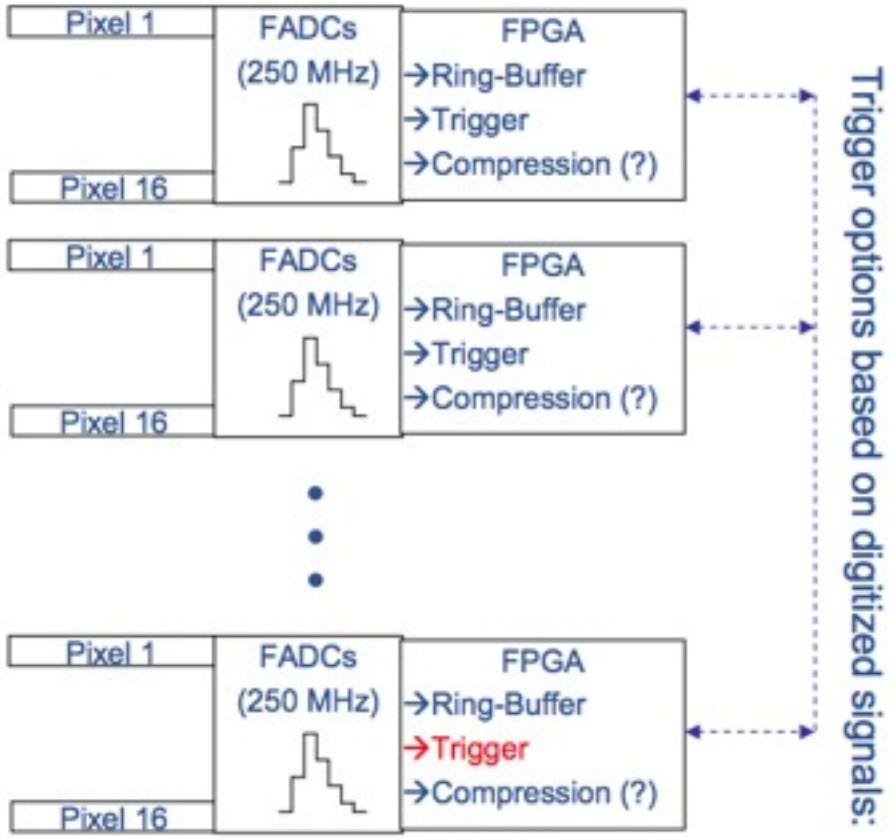
- Digitise the signals from a cluster of pixels (16) on a single board in the camera.
- Perform data buffering and trigger logic in a single FPGA on the cluster.
- Make it cheap (Hard, FADC is 20E for one-off).

FLASHCAM
Cluster Architecture



FLASH-CAM

Trigger Options: Cluster



a) Digital majority / threshold

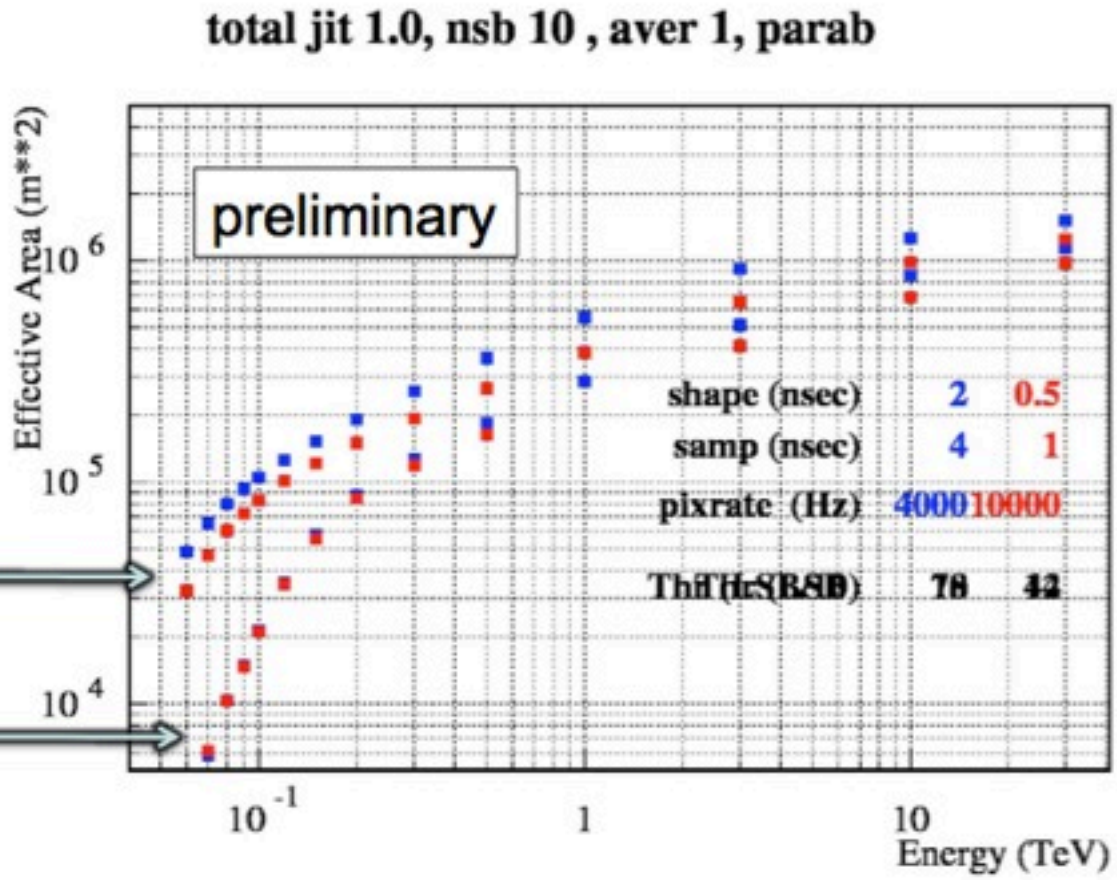
b) Digital sum trigger

c) Sum of clipped signals trigger

Triggering

The impact of different algorithms

1 GHz
250 MHz



Digital sum

Majority

MPI-K

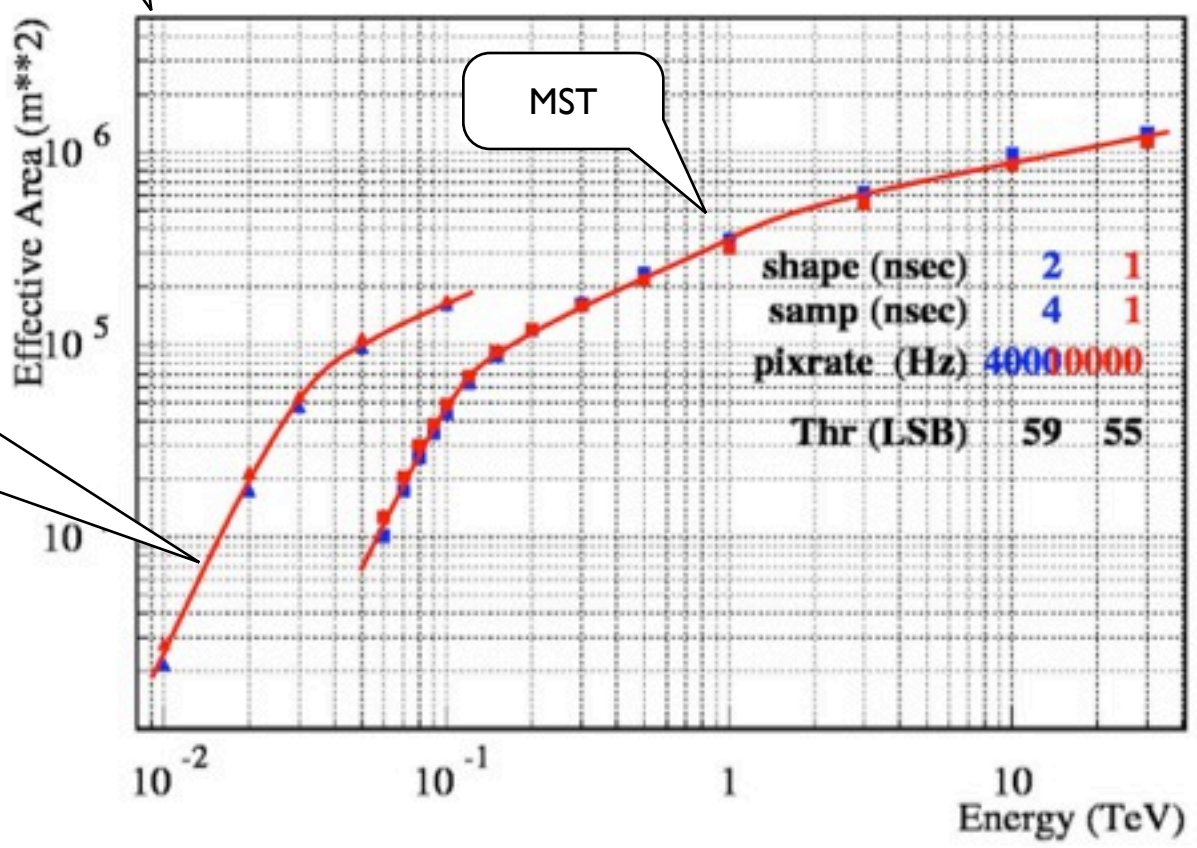
In turn, from Gerd's Zeuthen talk

Triggering

The impact of after-pulse rates

Rate: 10^{-5} > 5 pe

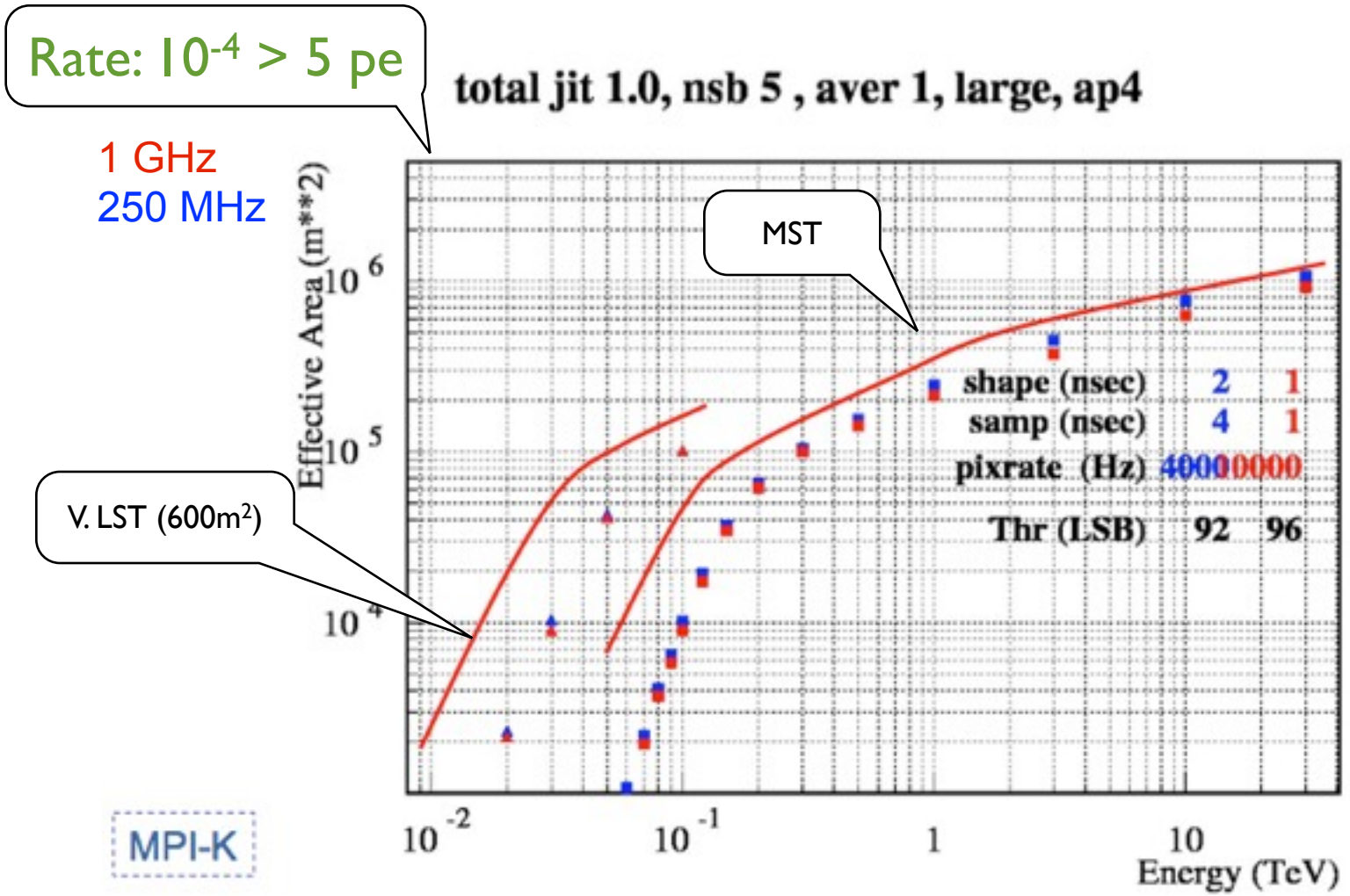
1 GHz
250 MHz



MPI-K

Triggering

The impact of after-pulse rates

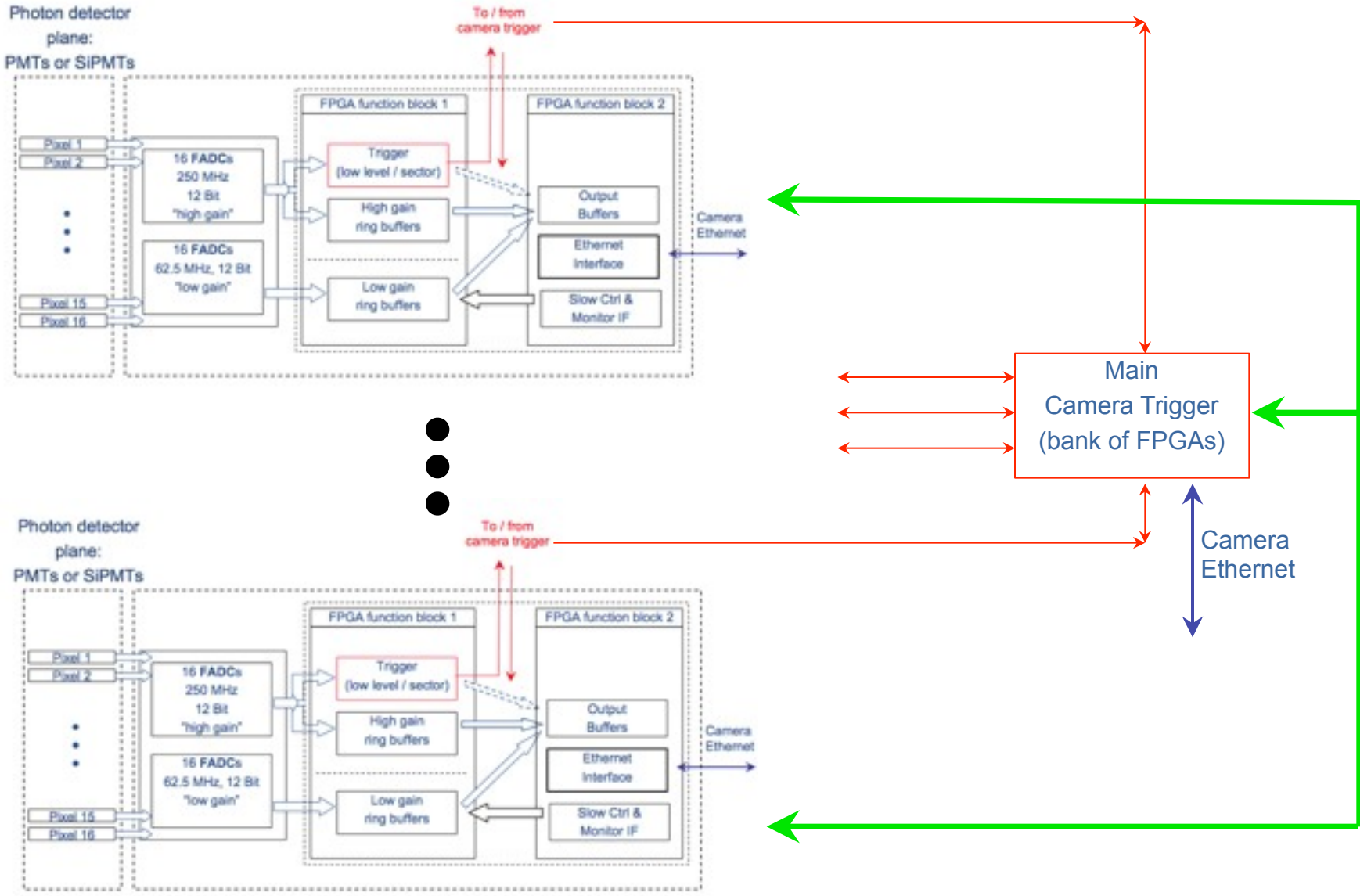


Triggering
Conclusions

- Digitial sum gives a higher area than majority… preliminary!
- Above ~150 - 200 GeV, 250 MHz gives more area than 1 GHz.
- If realistic jitter is included then 250 MHz is comparable to 1 GHz at these low energies.
- Even with 600 m^2, differences are not dominated by sampling speed.
- Photosensors need a low after pulse rate… this can not be traded for higher PDE.

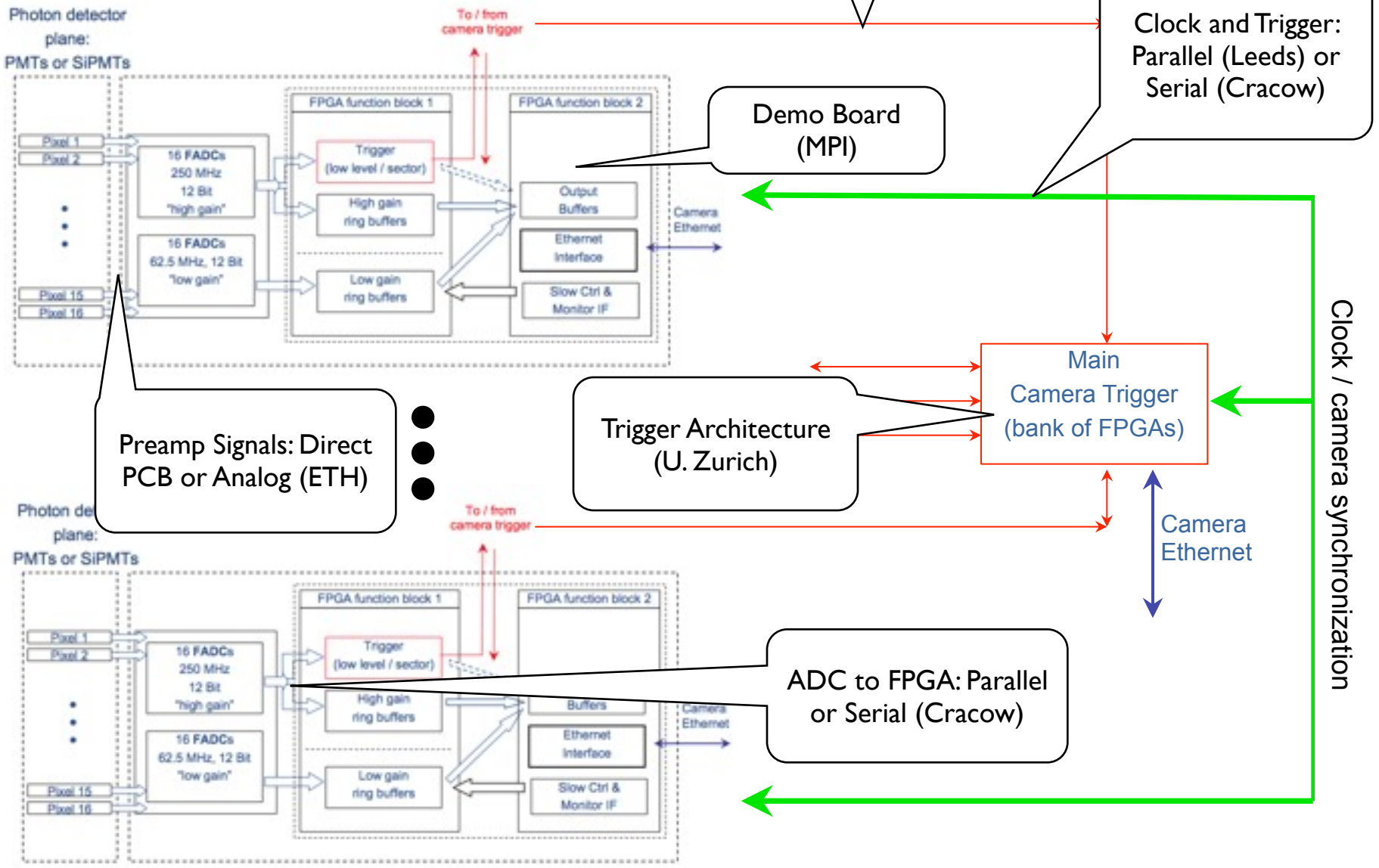
FLASH-CAM

Camera Architecture



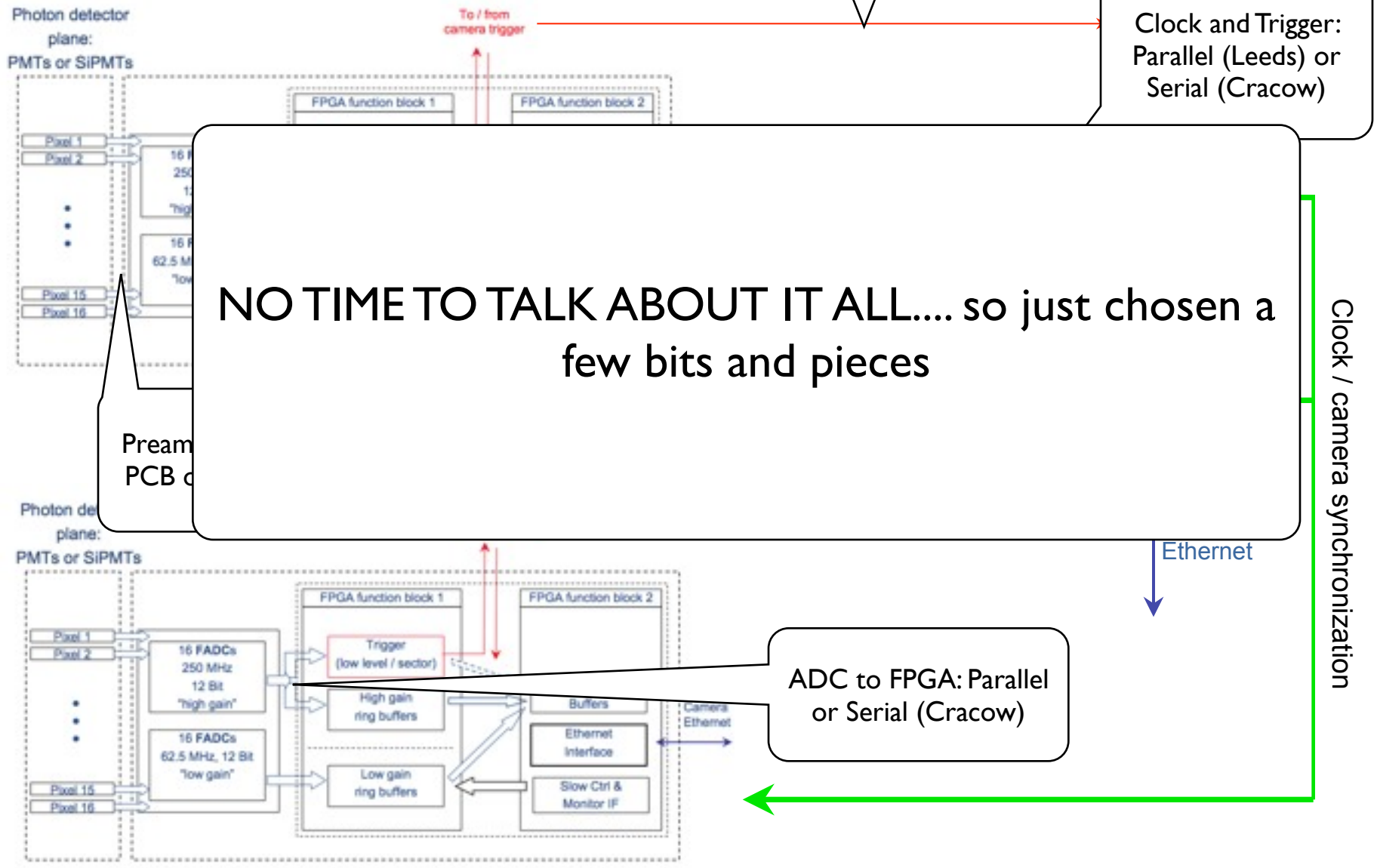
FLASH-CAM

Camera Architecture



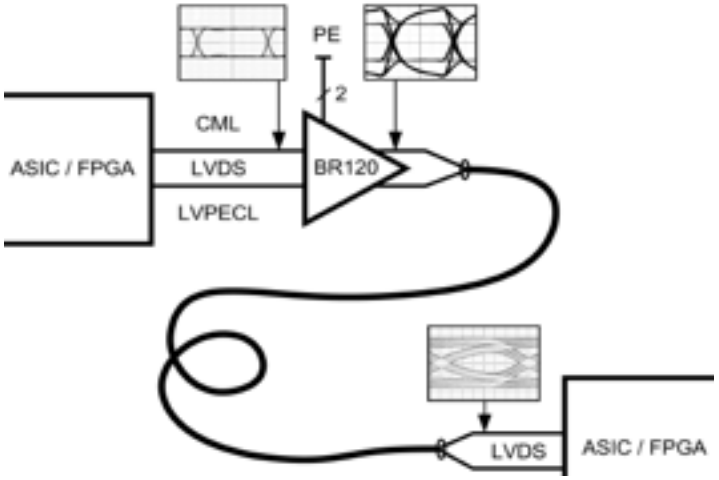
FLASH-CAM

Camera Architecture



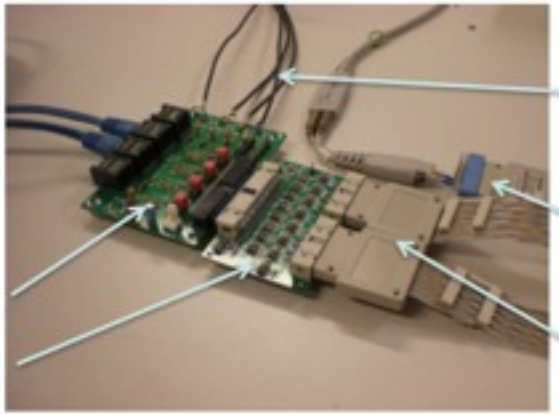
Signal Transmission
Digital Clock and Trigger in Parallel

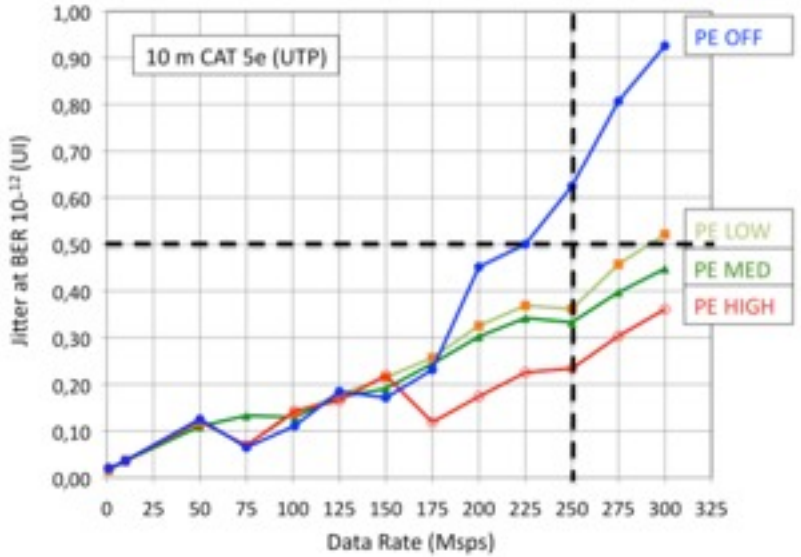
- Clock and trigger signals will be going at 250 Mbps, and will need to be differential.
- How can we transmit these over several meters cheaply? 3 bits in parallel, or more in serial (+ flexible, - faster clock).
- Cat5e? LVDS?

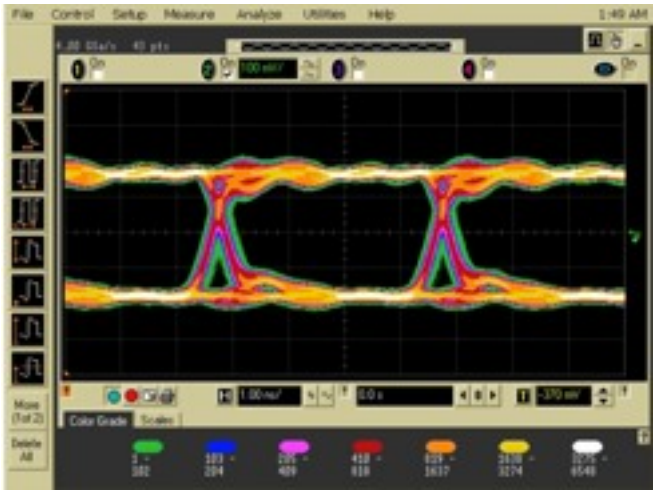


DS25BR120
3.125 Gbps LVDS Buffer with Transmit Pre-Emphasis

Signal Transmission
Digital Clock and Trigger in Parallel

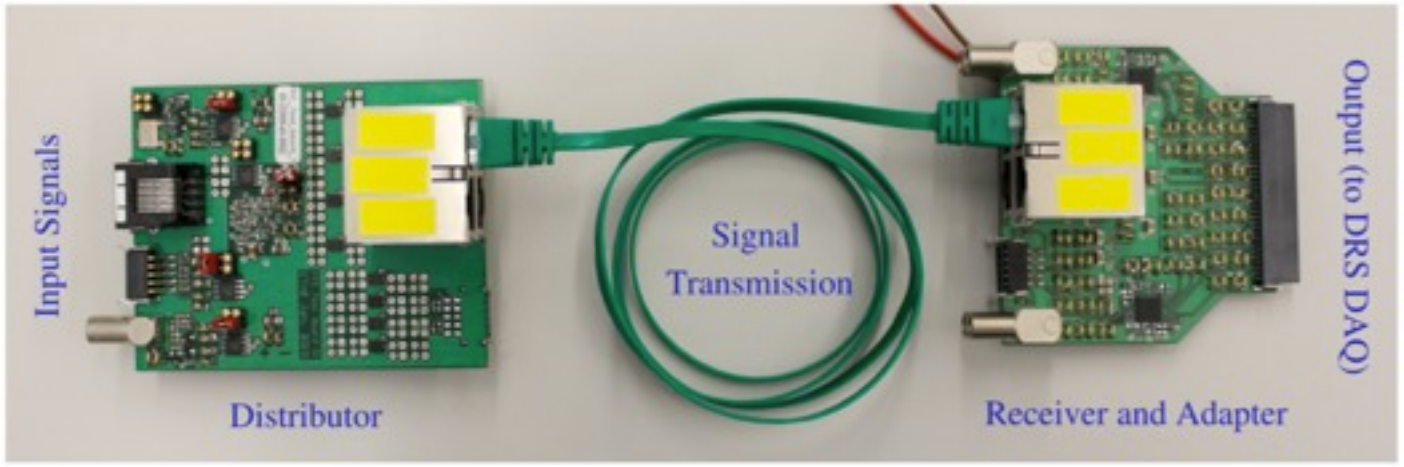


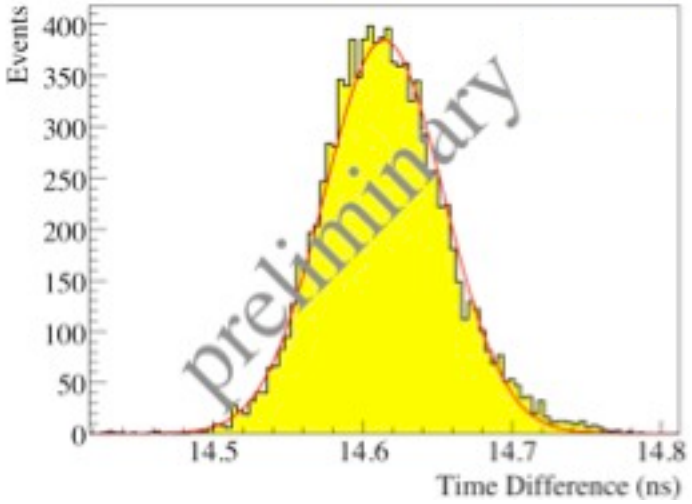




Signal Transmission

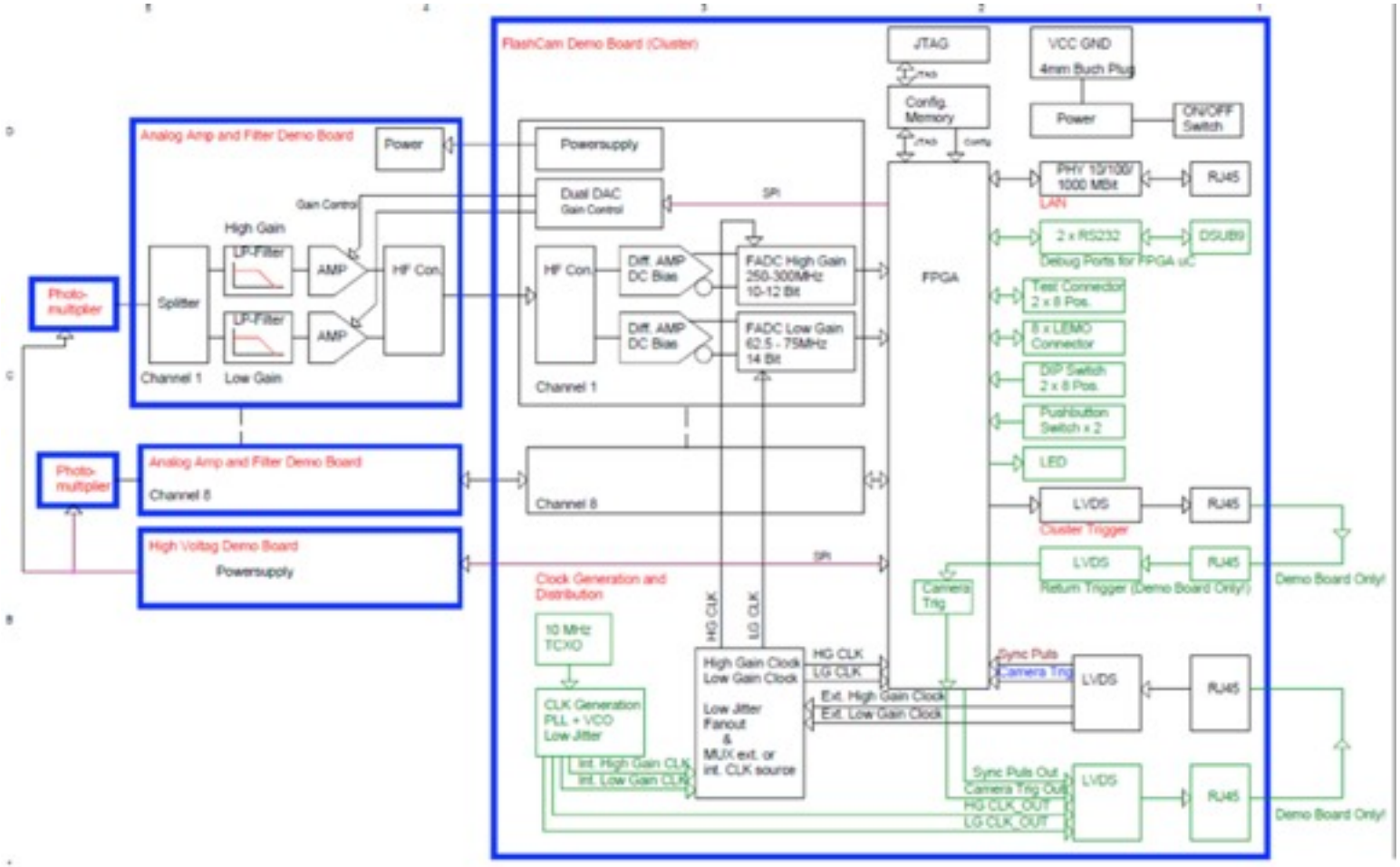
Limits of Clock Transmission





Demonstration Board

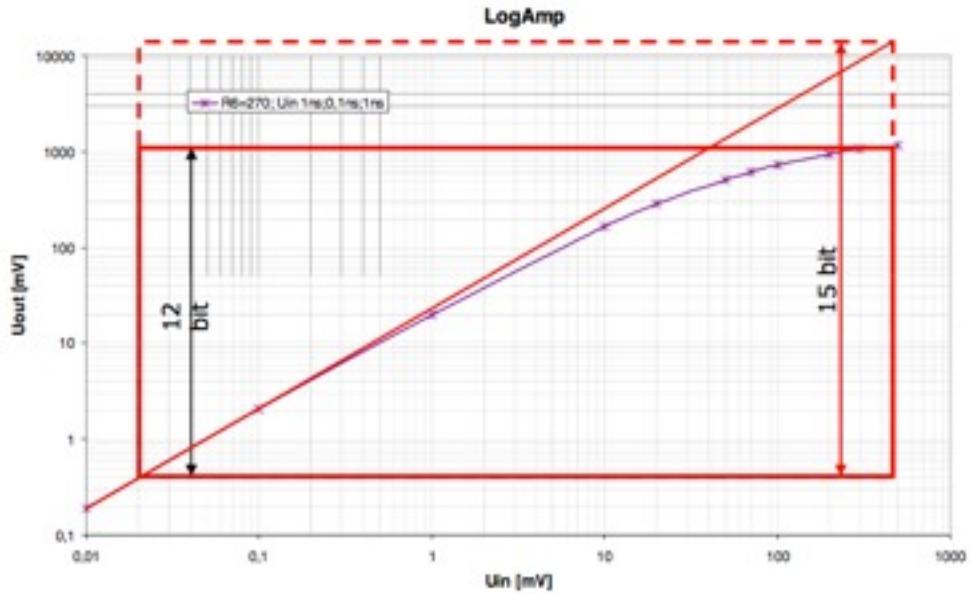
Overview

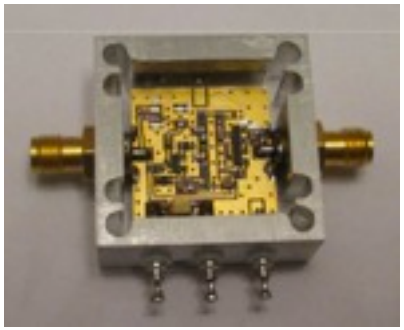


Demonstration Board

Preamps

- Linear and Logarithmic preamps under consideration at Cracow, MPIK.
- Linear: 2 channels with different gain, requires 12-bit & 8-bit ADC per pixel.
- Logarithmic: compress 15 bit to 12, only need one ADC.



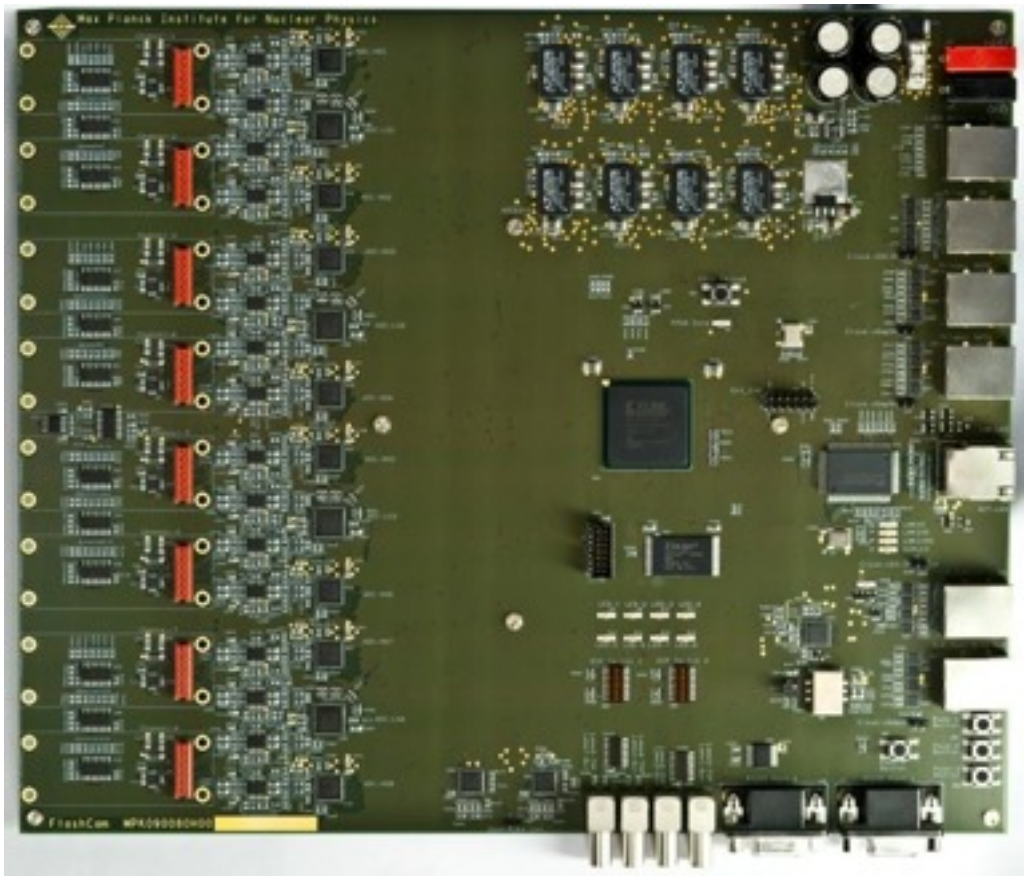


Cracow

Demonstration Board

The real thing…

- Now stuffed and being tested / debugged.



FLASHCAM for the SST

Questions

- Can we go even slower for the SST? - Simulations needed.
- If we go to, say 125 MHz, does it get cheaper?
- SO:
  - Can the design be adapted to fit in a compact focal plane?
  - Can the preamp signals be sent in analog to behind the primary?
- What happens with long readout windows? Or is it better to just run in dead-time free mode?
- Can the preamp be easily adapted for "alternative" photosensors?
- 64 channel version?