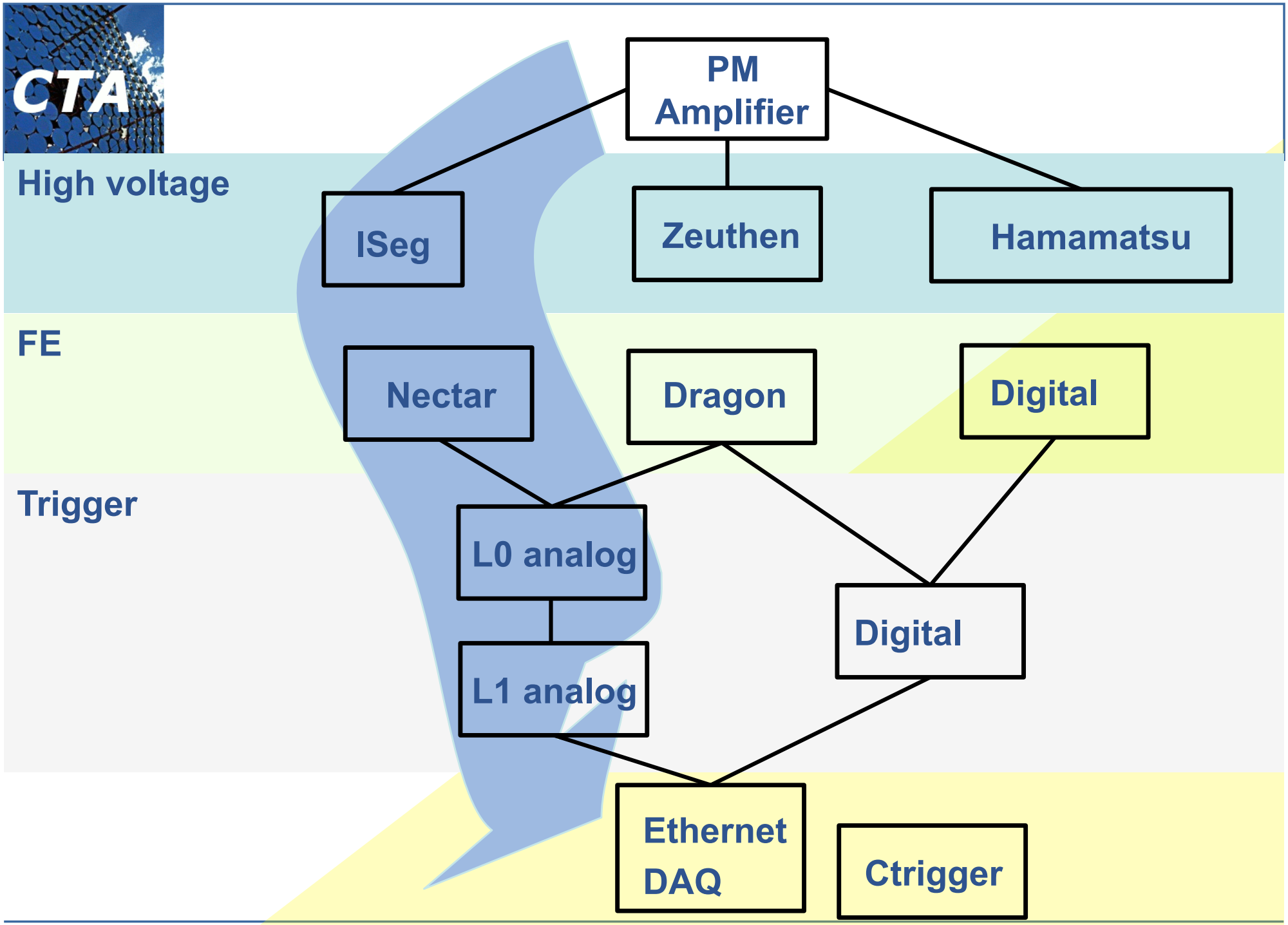
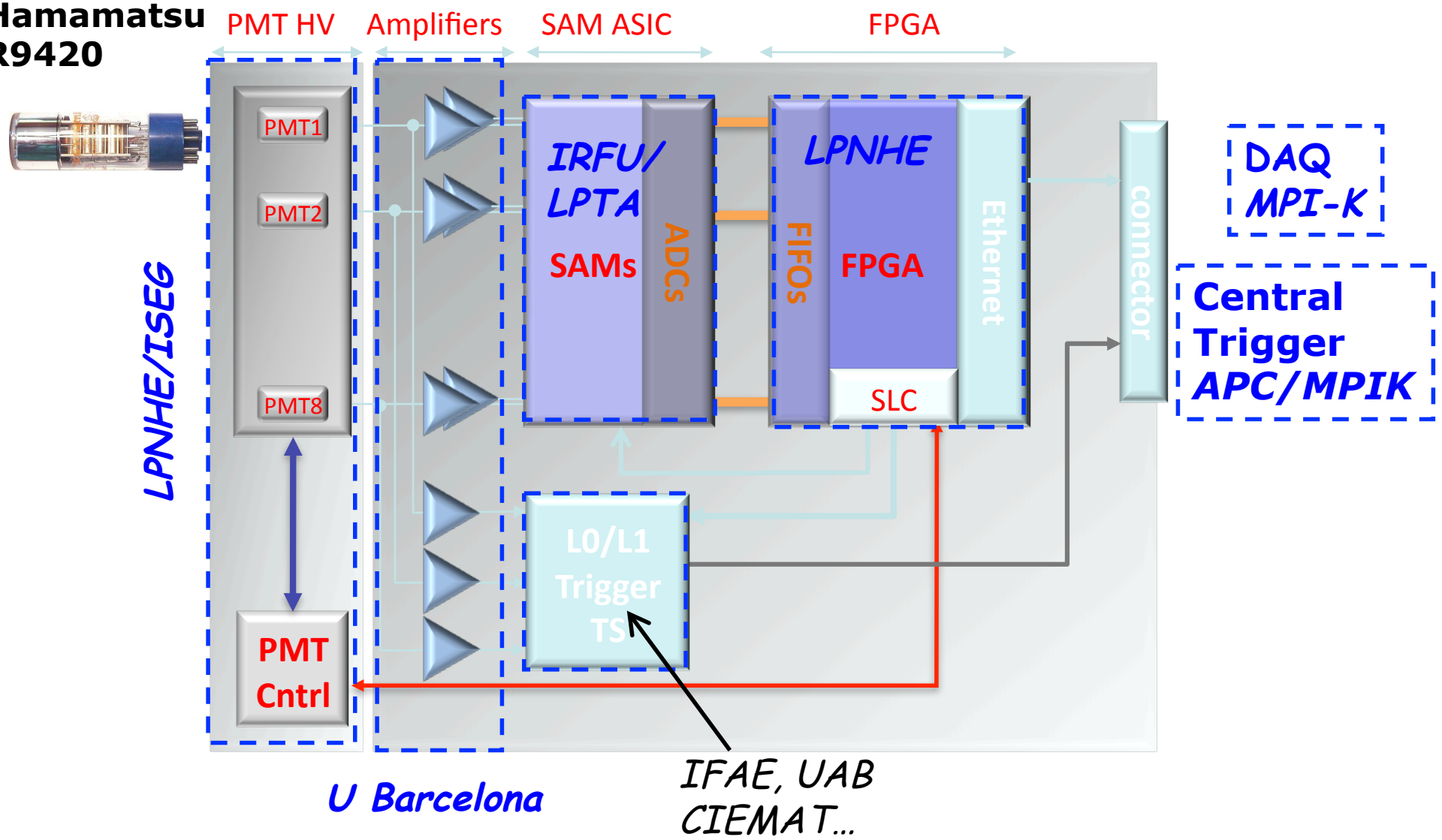
New Electronics for the Cherenkov Telescope Array

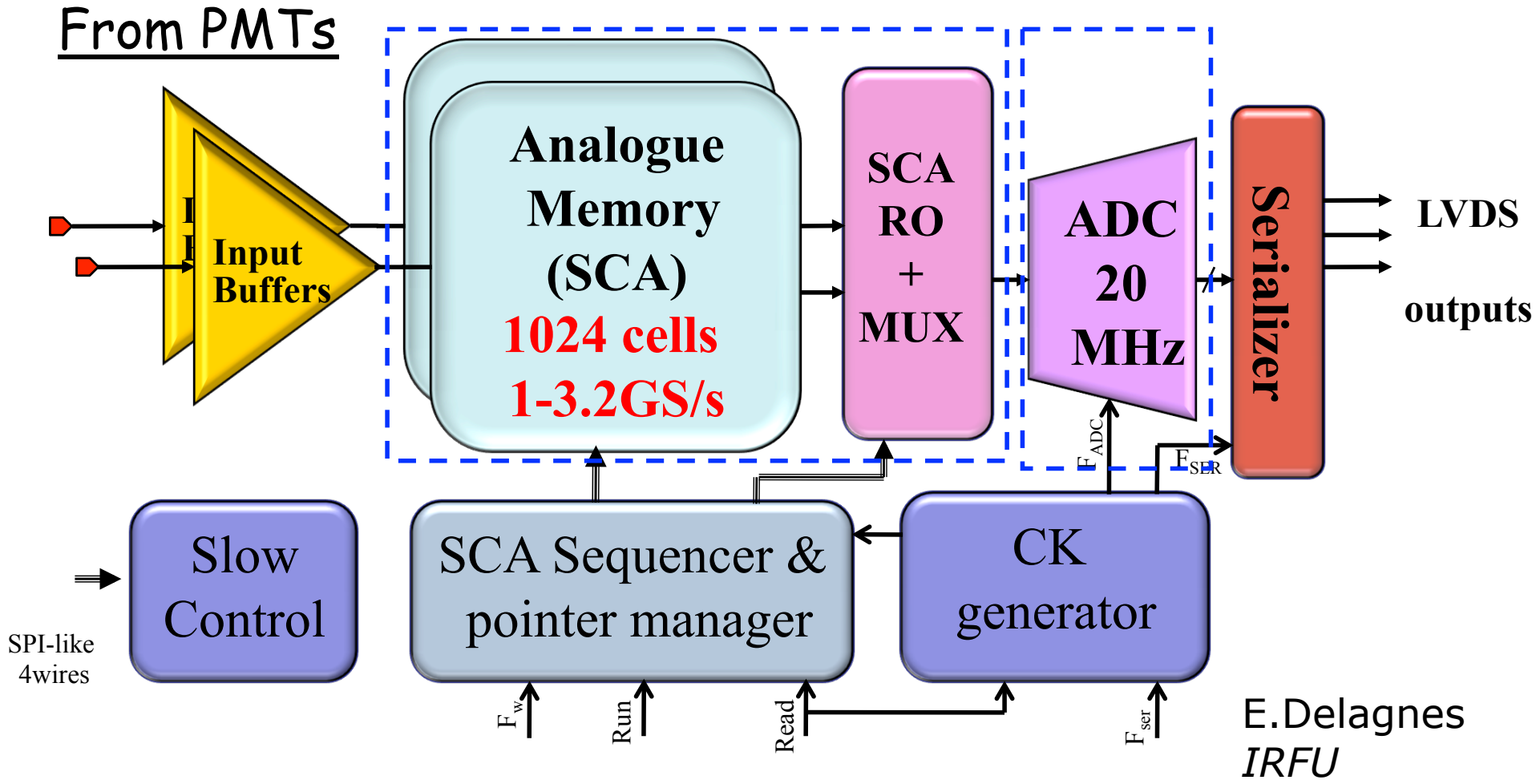
- Idea: use a front end board similar to those of HESS/HESSII
- FEB layout based on the use of analogue memories (ARS0 for HESS, SAM for HESS2)
- Analog trigger with comparators
- Collaborative efforts with french and spanish labs
- Special attention paid to price/power consumption reduction


CTA
High voltage
FE
Trigger
PM
Amplifier
ISeg
Zeuthen
Hamamatsu
Nectar
Dragon
Digital
L0 analog
L1 analog
Digital
Ethernet
DAQ
Ctrigger

Overview of the NECTAr based solution



NECTAR0 block diagram

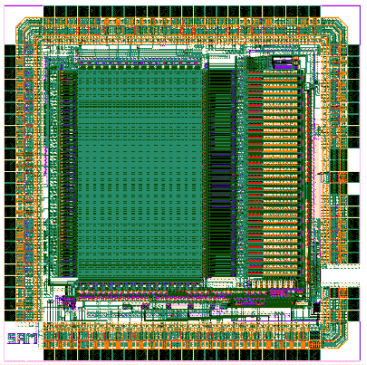


- Fast analog sampler/memory + digitizer.
- 2 differential channels (1024 cell memory each)

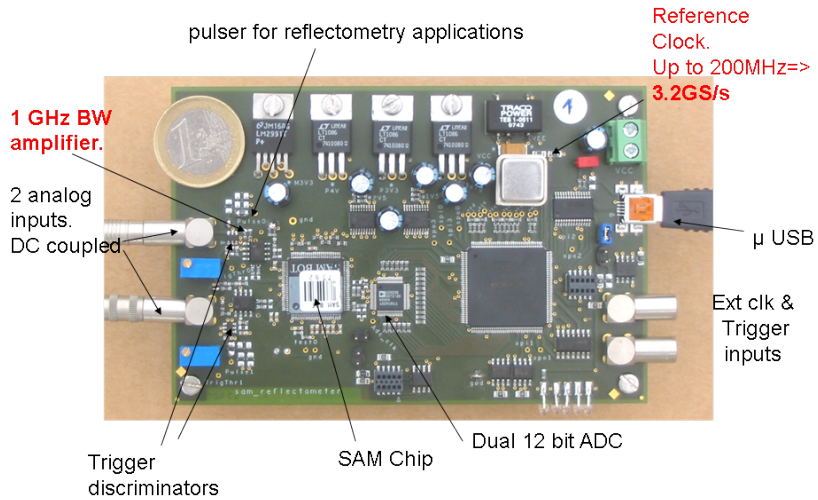
NECTAR requirements: almost identical to those of SAM.

NAME	SAM	Nectar0 (expected)	Unit
Power Consumption	300	150-300	mW
Sampling Freq. Range	<1to 2.5 (3.2)	1 to 3.2GS/s	GS/s
Analog Bandwidth	250-300 (450MHz	300 MHz	MHz
Read Out time for an event (2 gains 16 cells)	< 1.5	<2	µs
Fixed Pattern noise	0.4		mV rms
Total noise (constant with frequency)	0.65 (0.5mV if FPN cancelled)	<0.8	mV rms
Maximum signal (limited by ADC range)	2 (4)	2	V
Dynamic Range	>11.6 (12.6)		bits
Crosstalk	<3	<3	per mil
Integral non linearity	< 1	<1	%
Sampling Jitter	<15	<50	ps rms
memory depth	256	1024	cells

SAM chip

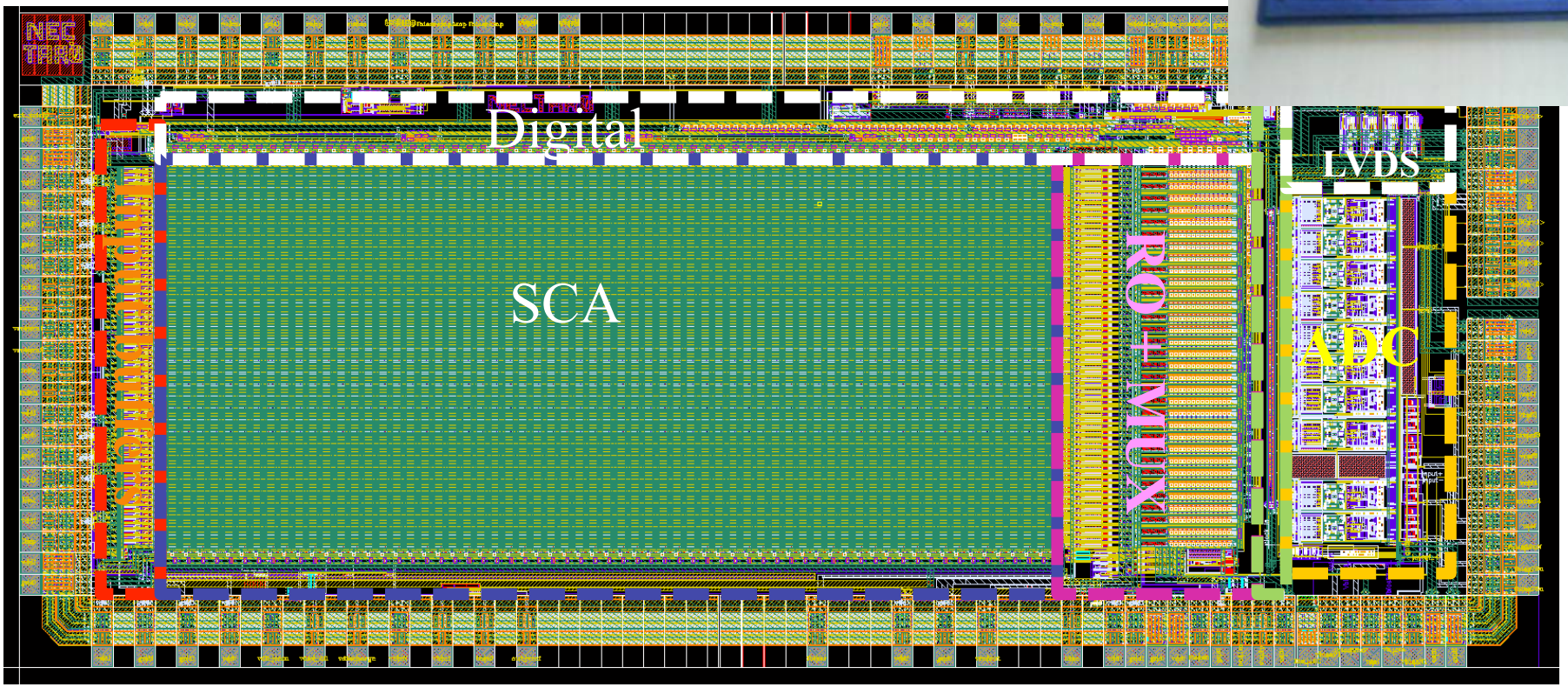


Blue: on HESS2 FE boards.
Red: on the USB test board



Nectar 0 chip Layout

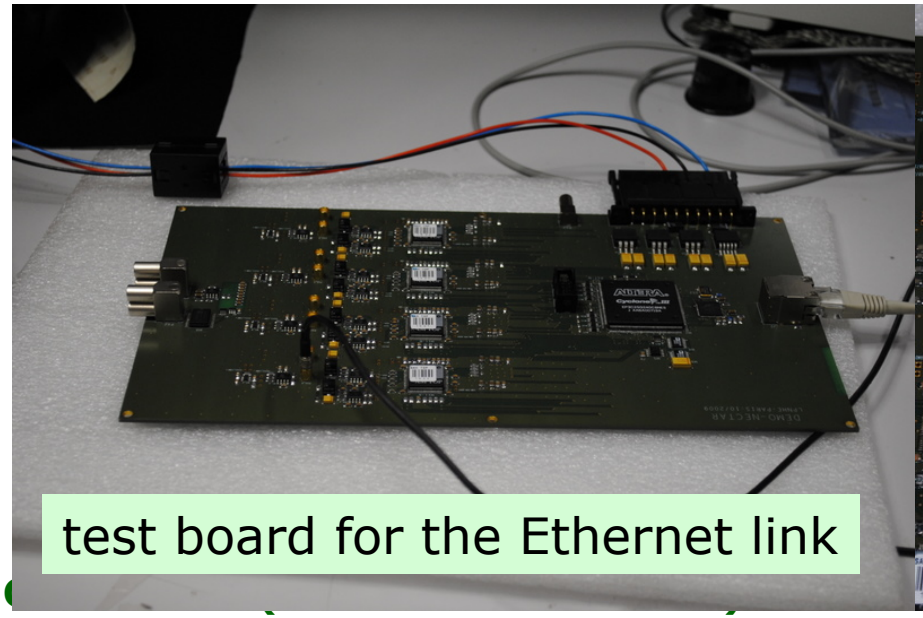
- CMOS AMS 0.35µm technology.
- 3x7mm chip size
- final chip could integrate 4 diff channels on a 5mm*7mm chip
- chip returned from foundry in July, is tested right now .



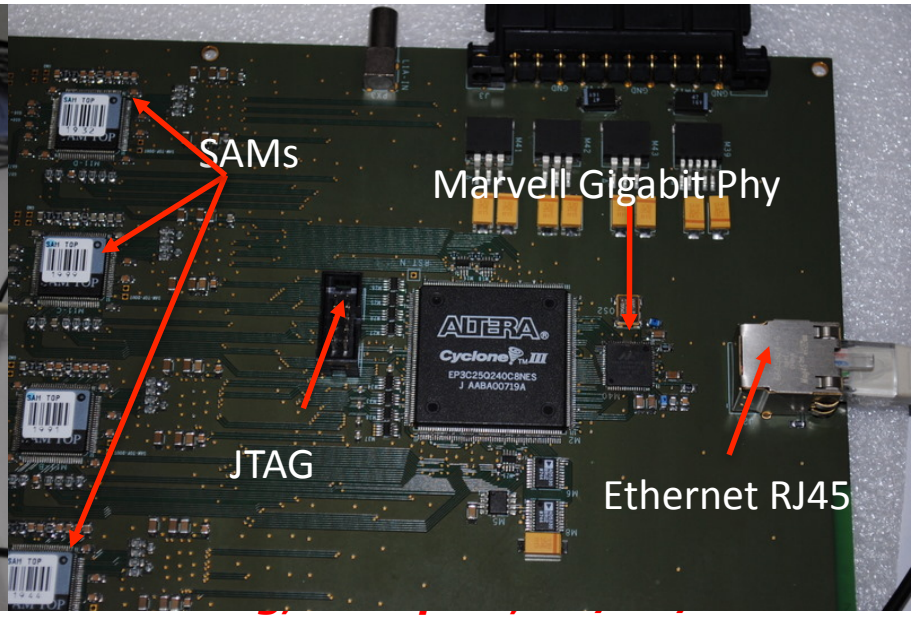
Front-end FPGA

- Integrates:
  - FE control
  - Event FIFOs
  - Ethernet Interface
- Ethernet Interface:
  - 100 Mbits/s or 1 Gbit/s
  - in a low cost FPGA (~ 30 €)
  - uses UDP protocol instead of TCP
  - commercial IP

P.Nayman
LPNHE

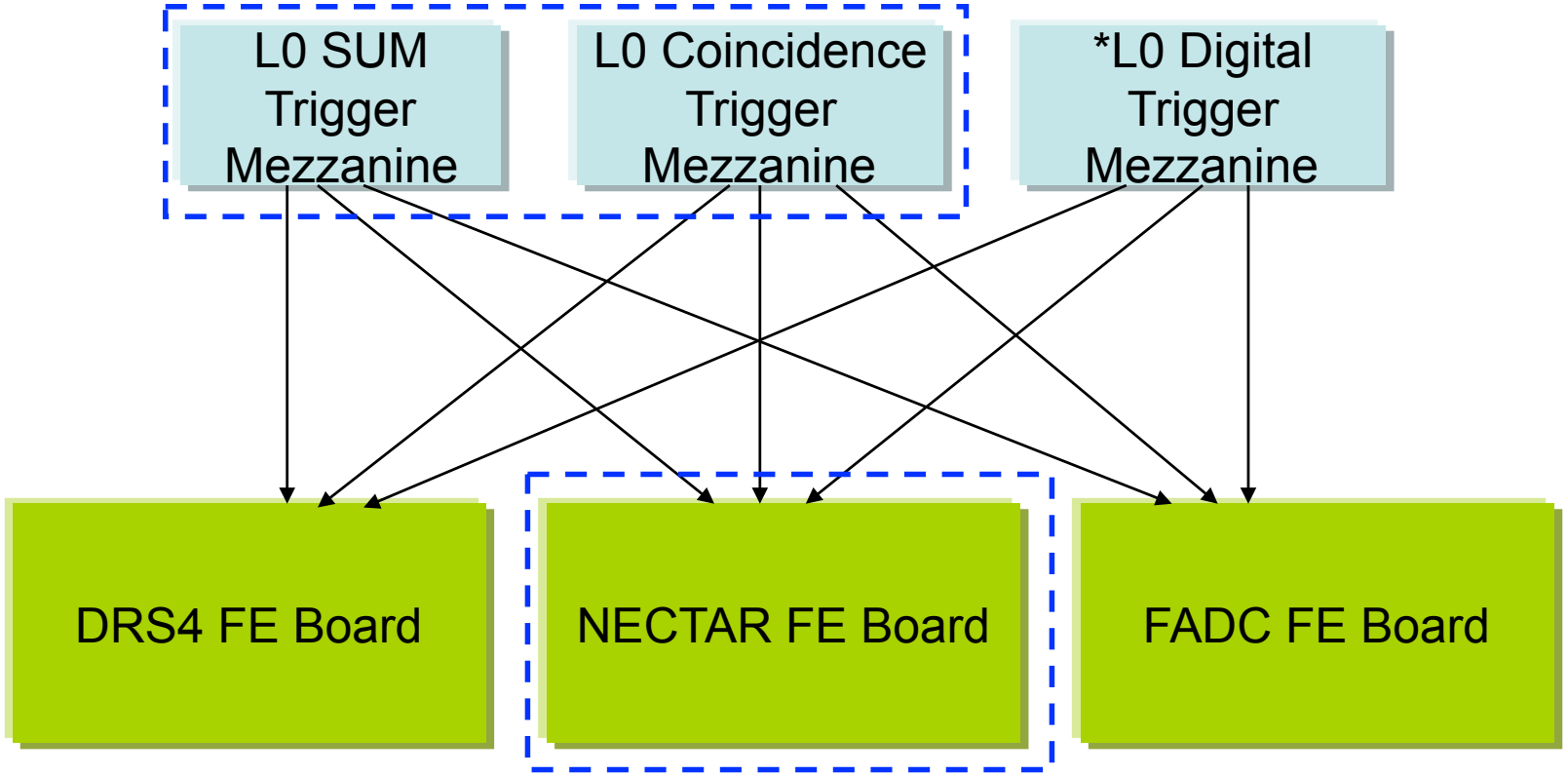


test board for the Ethernet link

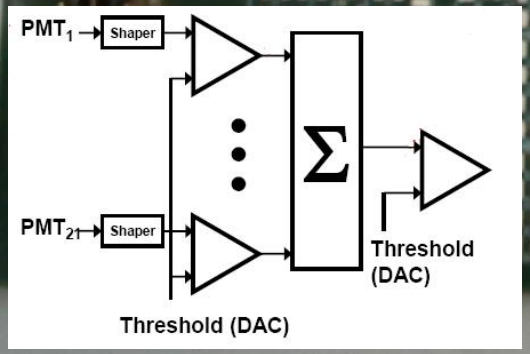


L0 trigger (analog)

- Prototypes designed at IFAE
- Well known Trigger concepts:
  - Coincidence of Pixels above threshold (HESS)
  - SUM Trigger (MAGIC)
- Built two Trigger mezzanines for tests with Front End Board

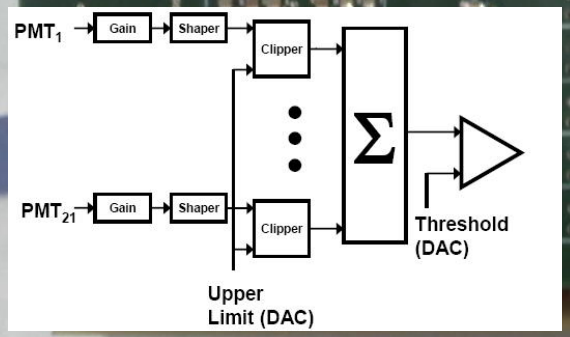


coincidence trigger prototype (IFAE)

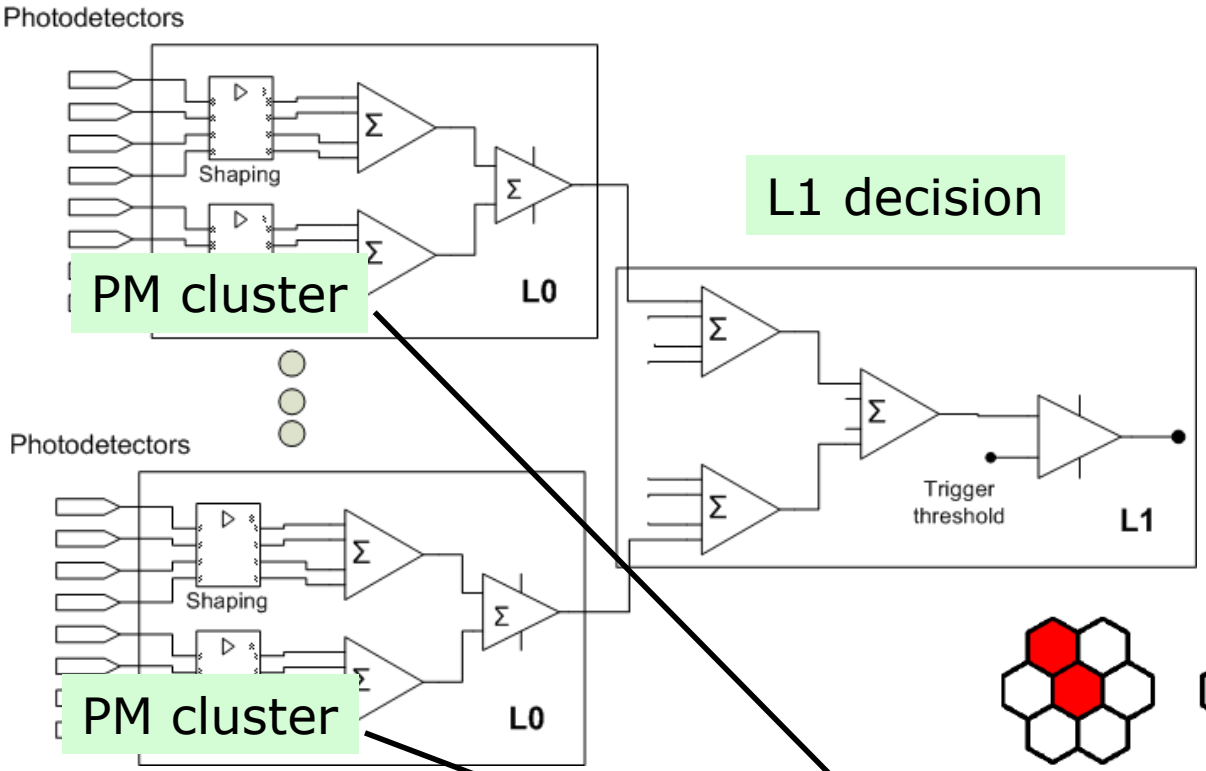


sum trigger prototype (IFAE)

M.Barcelo
O.Blanch
J.Boix
IFAE+..

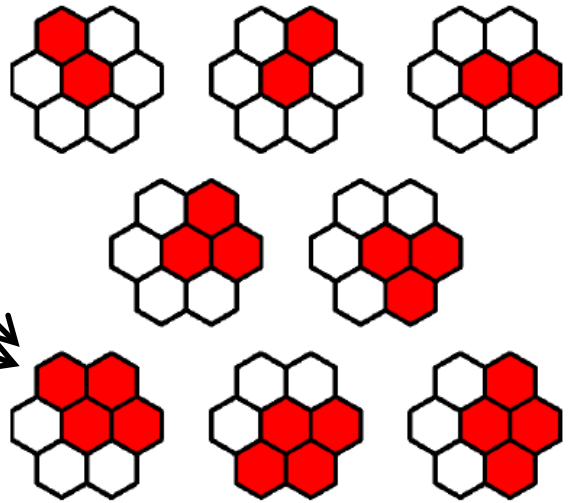


L1 trigger



L1 decision

trigger topology



G. Martínez, C. Delgado
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L1 trigger implementation

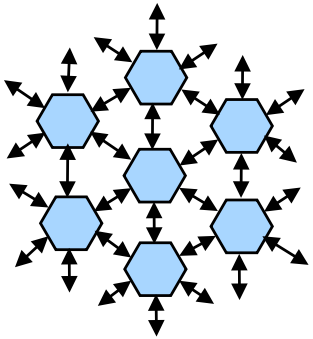
Two approaches for the L1 logic and distribution:

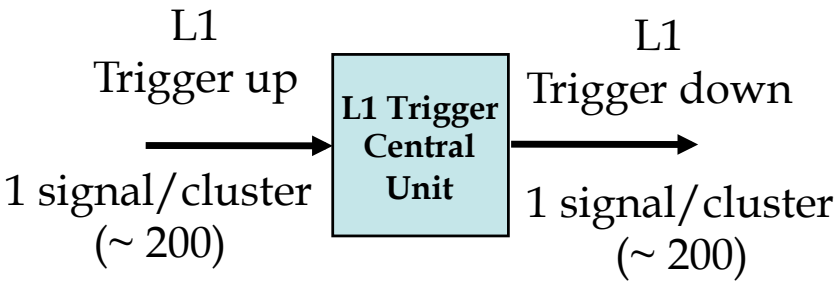
Without central unit:

Any cluster can start the distribution of L1 trigger to a certain region of interest or the whole camera

With central unit:

A central unit collects L1 outputs from all cluster and distributes L1 trigger down to a certain region of interest or the whole camera





The L1 decision can be forwarded to a ROI or the whole camera.

G. Martínez, C. Delgado
Ciemat

Conclusions and outlook

- HV design: design by ISEG expected in October
- Amplifier (UCB), NECTAr0 returned from foundry in July
  - tests started, results are promising
- FPGA ethernet readout OK
- L0 Trigger mezzanines prototypes available

- If all of the above OK, full camera module built
  end 2010/beginning 2011