AGIS Camera Front-end Electronics Development

Stefan Funk for the CTA-US Camera group

SLAC NATIONAL ACCELERATOR LABORATORY

KIPAC

Sep, 8-9, 2010
Liverpool, SST Meeting

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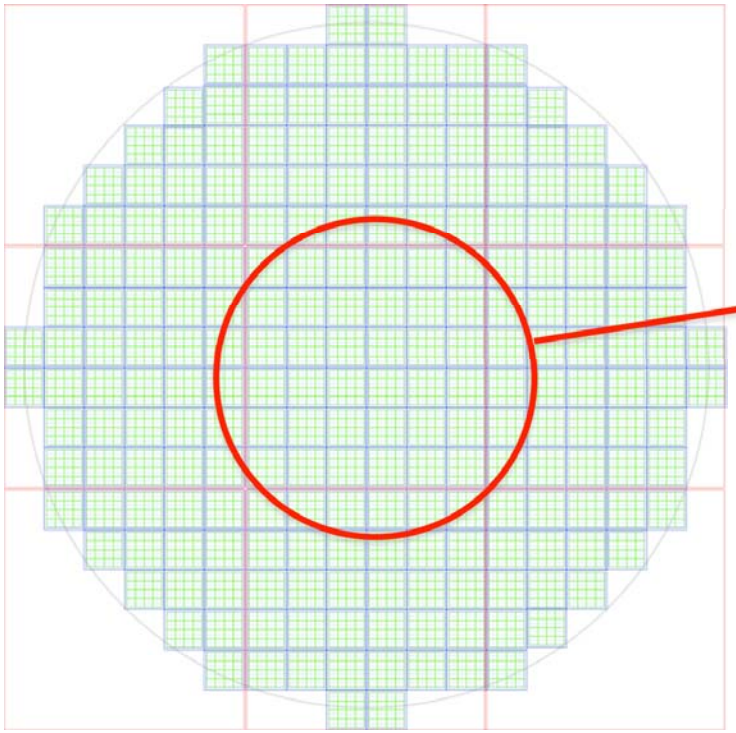
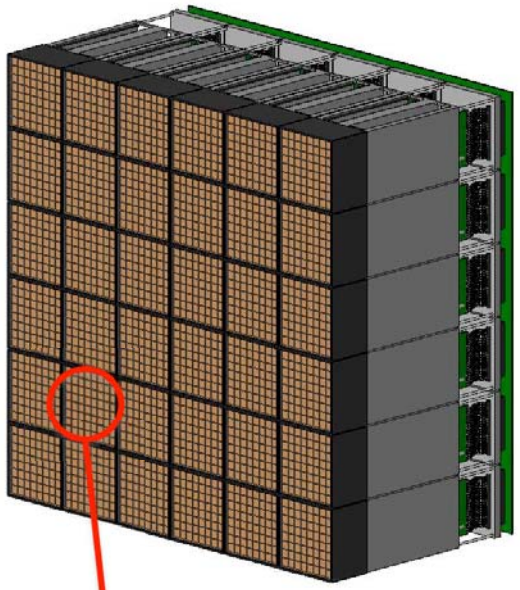
AGIS Camera design

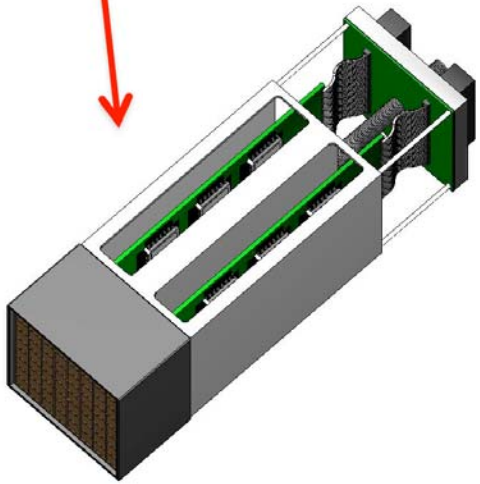
9 “subfields”
each with 36, 32, or 15 camera modules:



Example subfield
with 36 camera modules:

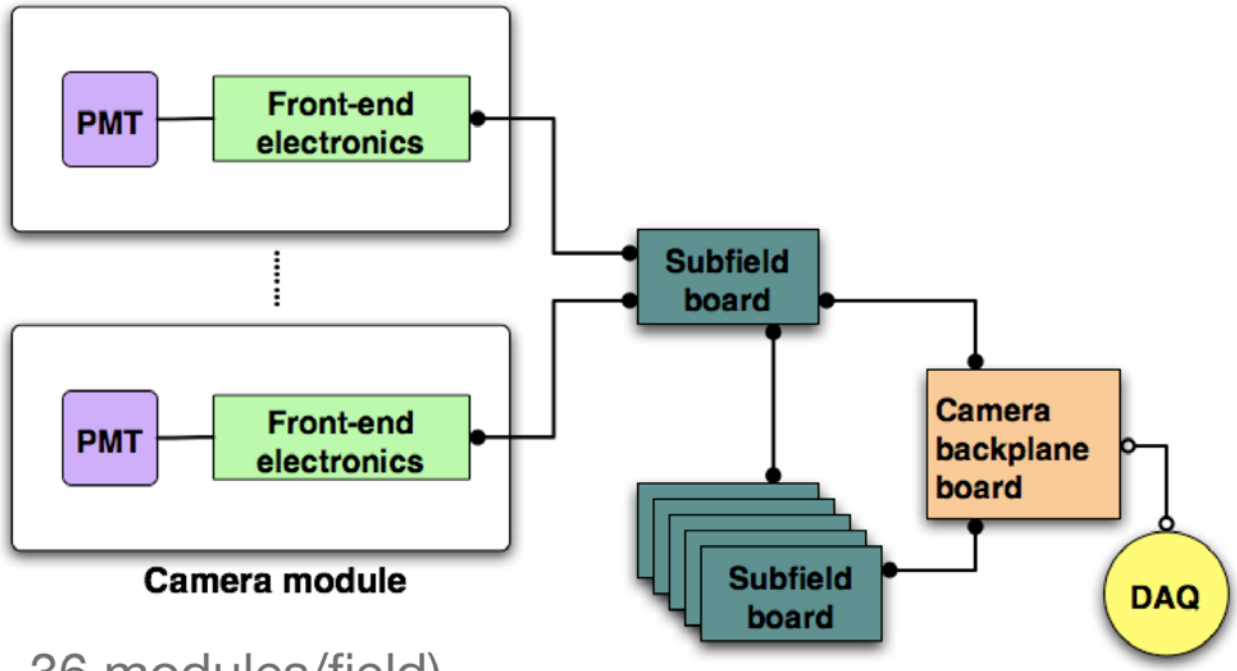


Camera module:
- 2” multi-anode PMT
- readout electronics
- 64 pixels per MAPMT
- each pixel is 0.05-0.1°



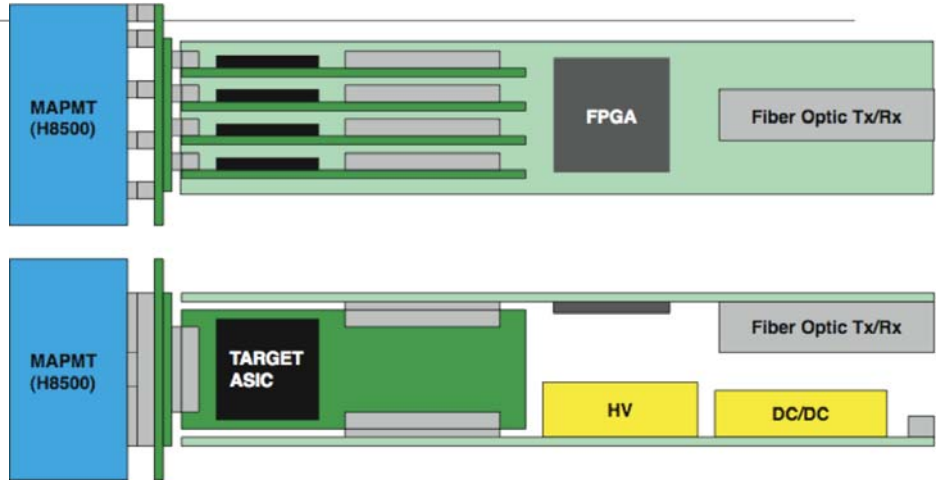
36 telescopes x 224 modules x 64 pixels
= ~500k channels total for AGIS

Camera Electronics Overview

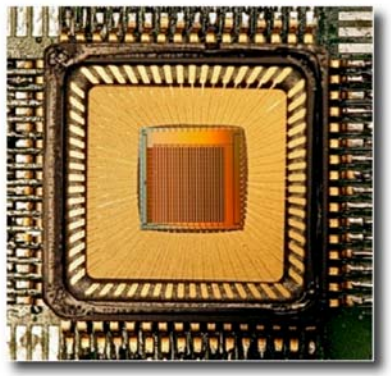


- Camera electronics consists of:
  - Camera modules: ~200/camera (~13k pixels)
    - Waveform sampling and digitization, 16 triggers
  - Subfield boards: ~10/camera (~36 modules/field)
    - Cross-link trigger information
    - Subfield trigger
  - Camera backplane board:
    - Camera trigger
    - Gb ethernet link to outside (or any other commercial solution)

Camera module: general idea

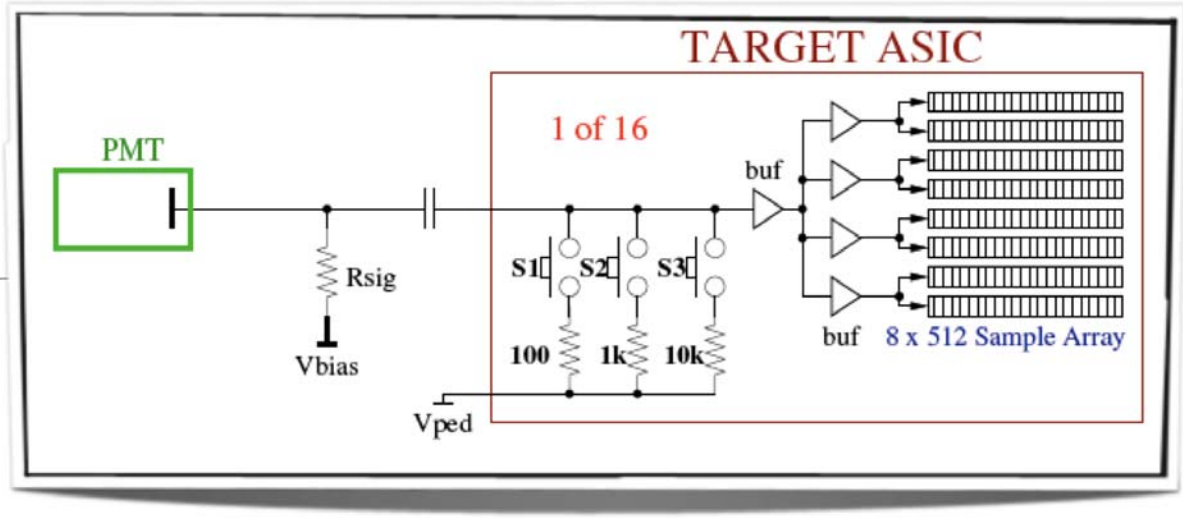


- Increase ~3k to ~500k total channels requires
  - Low cost, power per channel
  - Robust design: modular
- Goal: $20/channel (electronics + Ma PMT)
  - Current generation is ~$1k/channel
- Main cost saving through:
  - (1) MaPMT
  - (2) TARGET readout (ASIC) chip
    - “TeV Array with Gsa/s sampling and Experimental Trigger”



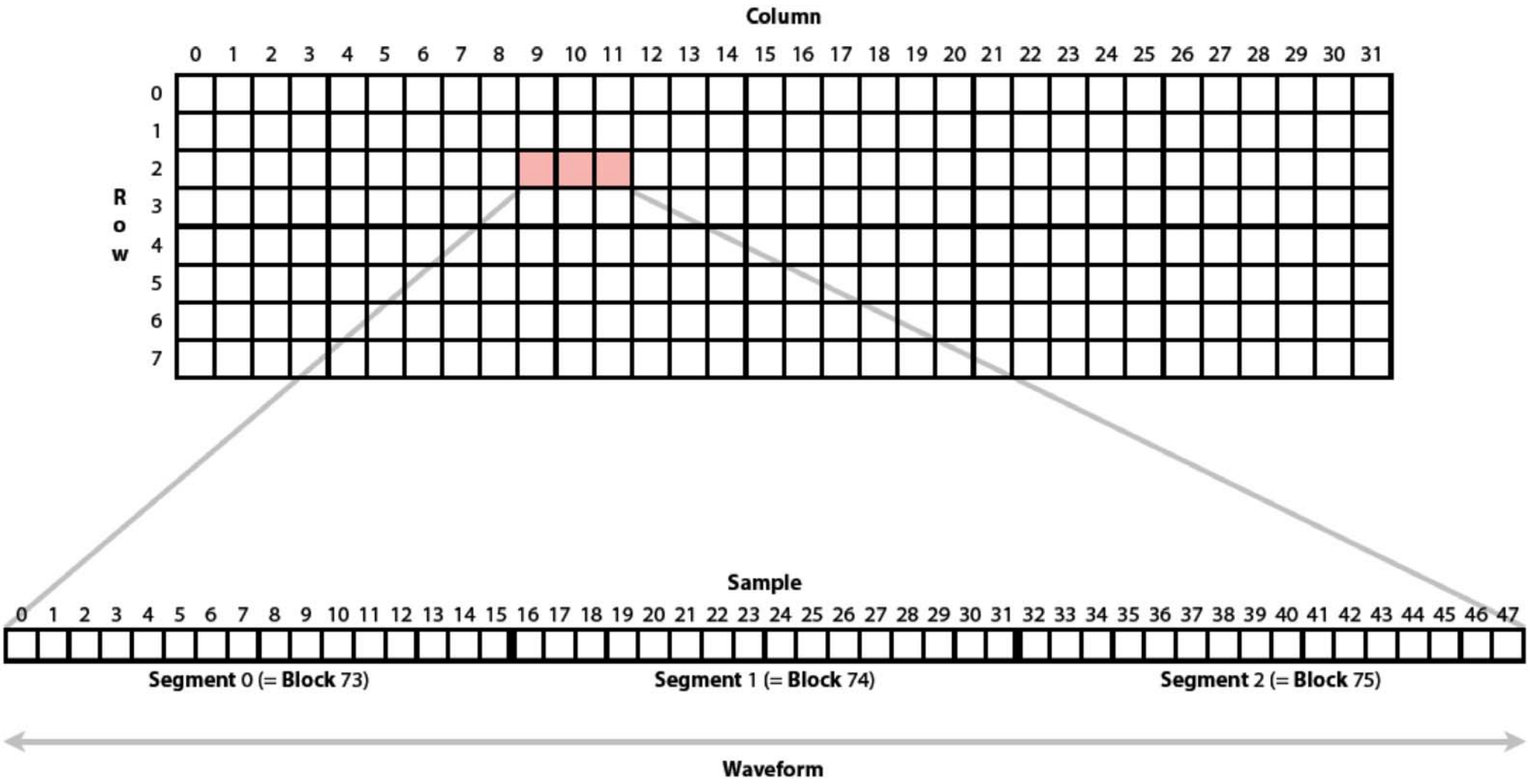
- TARGET based on LABRADOR (ANITA) and BLAB-(1-3) chips (Super-B factory)

TARGET

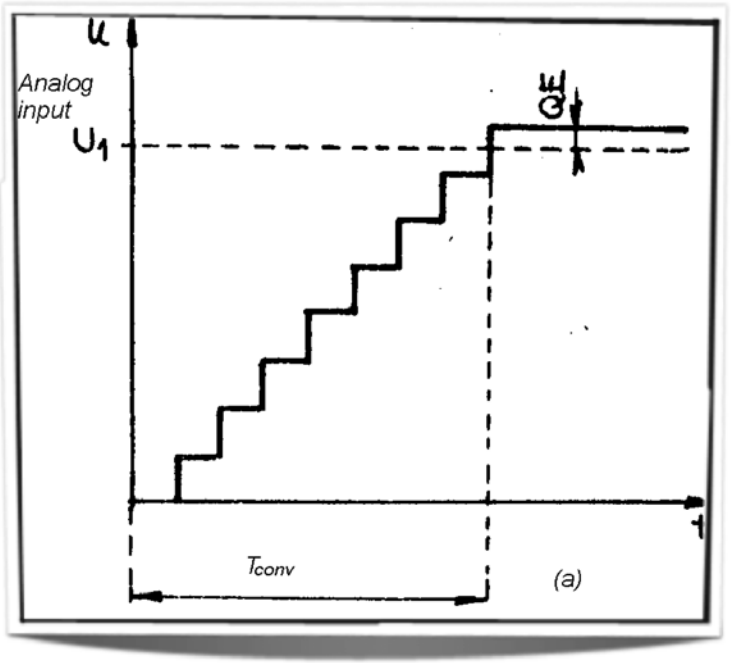


- 16 channels per TARGET chip
  - i.e. 4 TARGET digitizer ASIC per 64-channel MaPMT
- Properties:
  - Switched capacitor array consisting of 4096 capacitors per channel
  - 1 GSample/s sampling of each channel (i.e. 4 µs buffer depth)
    - Sampling rates from 0.5 GSample/s to 3.5 GSample/s possible
  - Digitization via Wilkinson-type ramp (12 bit encoding, 10 bit range)
  - Trigger on-board (currently OR of 16 channels. Will be analog sum of 4)
  - Multi-hit buffer (8 independent rows)

Buffer layout



At occurrence of trigger (internal or external)



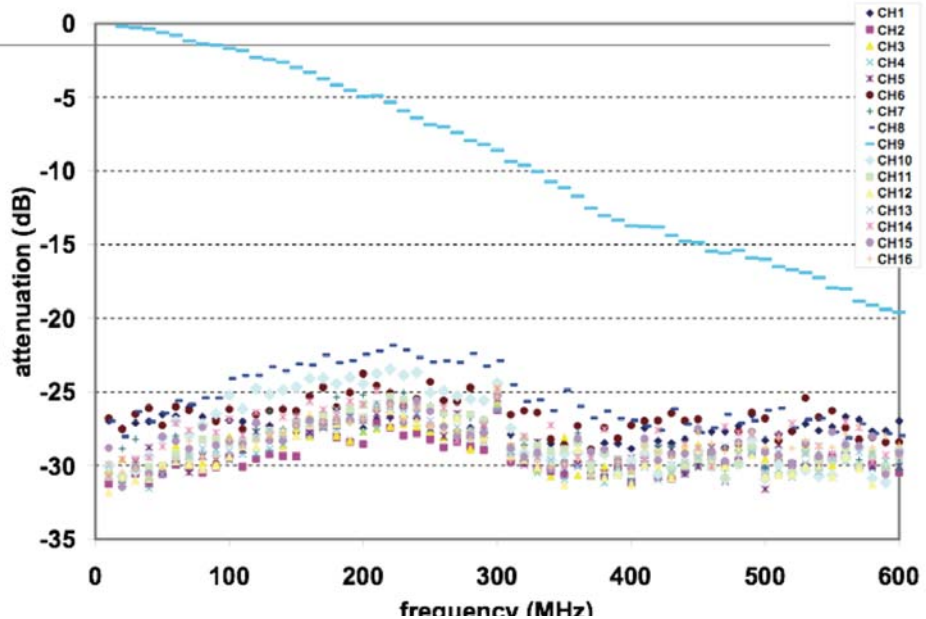
- Digitization:
  - Wilkinson-type ramp (counting time-steps until comparator matches V_{sample})
  - 12-bit gray code counter currently on FPGA, will be on ASIC in next version (effectively 450 MHz)
  - Digitization is done for atomic blocks of 16 in 2 channels simultaneously
  - Rows are independent, digitization can be done deadtime-free

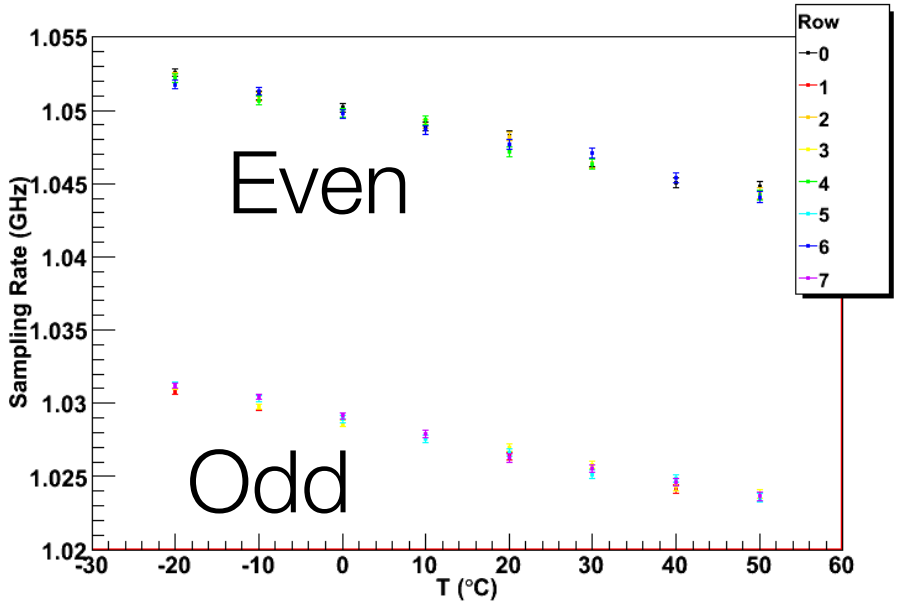
Summary of digitization

Spec	TARGET 1
Dynamic Range	12-bit (4096)
Channels	16
Sampling Capacitors	4096
ADC Clock Speed	223 (445 effective) MHz
Samples per Digitization	16
Channels per Digitization	2
Ramp Time	4096 / (223MHz x 2) = 9.3 µs
Ramps per Channel	64/16 = 4
Totals Ramps	16/2 x 4 = 32
Channel Digitization Time	4 x 9.3 µs = 37 µs
Total Digitization Time (16 channels)	32 x 9.3 µs = 290 µs

TARGET Performance

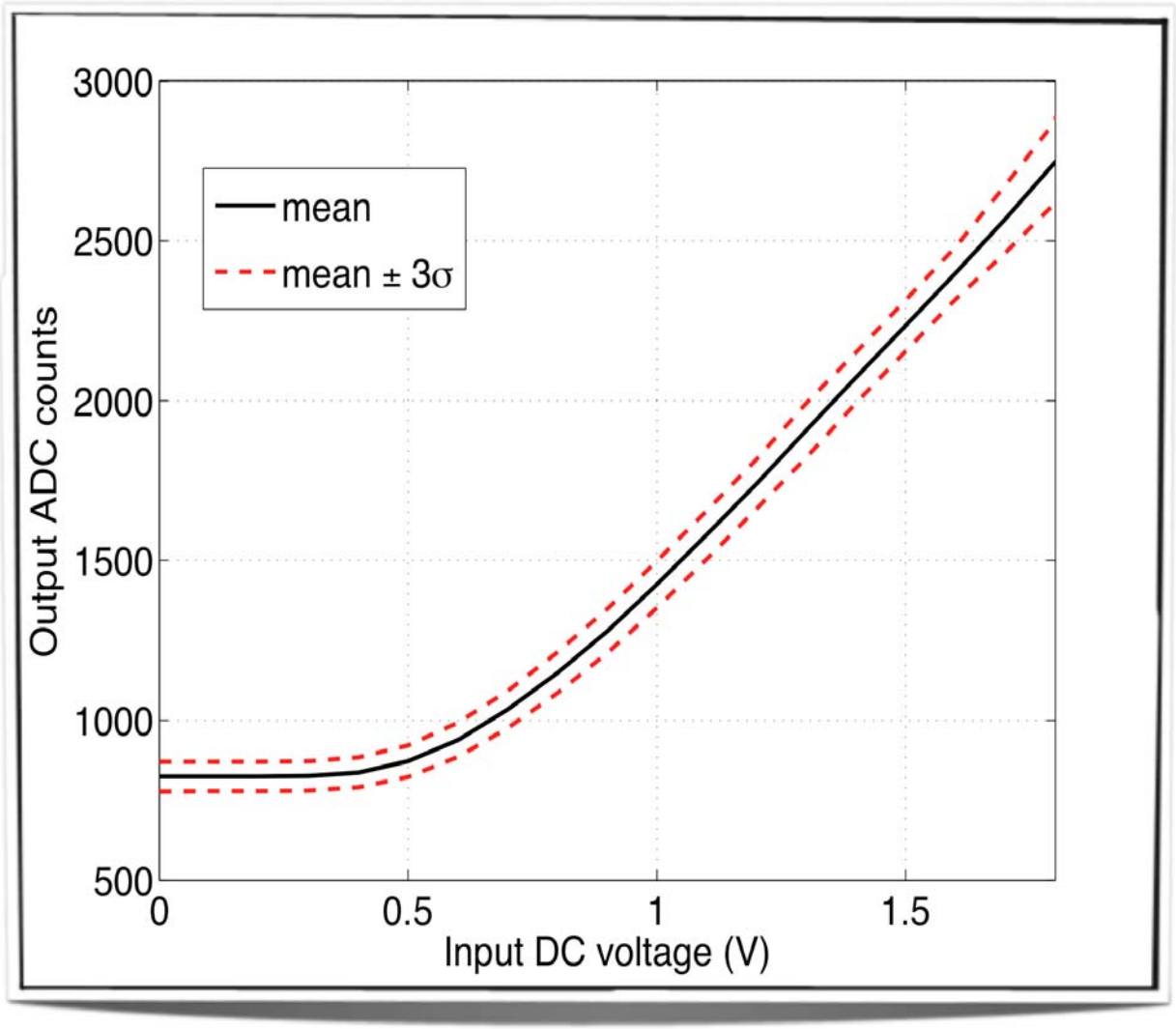
- Dynamic range: ~1 V with ~1 mV noise level, 10 bit, therefore effective 9 bits
- Bandwidth (150 MHz) and crosstalk (~5% at 400 MHz)
- Sampling rate stable
  - Sampling rate different between even and odd capacitor rows (2% level)
  - Temperature dependence: 10^{-4}/K (stabilized by a feed back circuit)
- Power consumption: 7.1 mW/channel for TARGET only, 70mW/channel including everything (FPGA, fiber optics etc.)



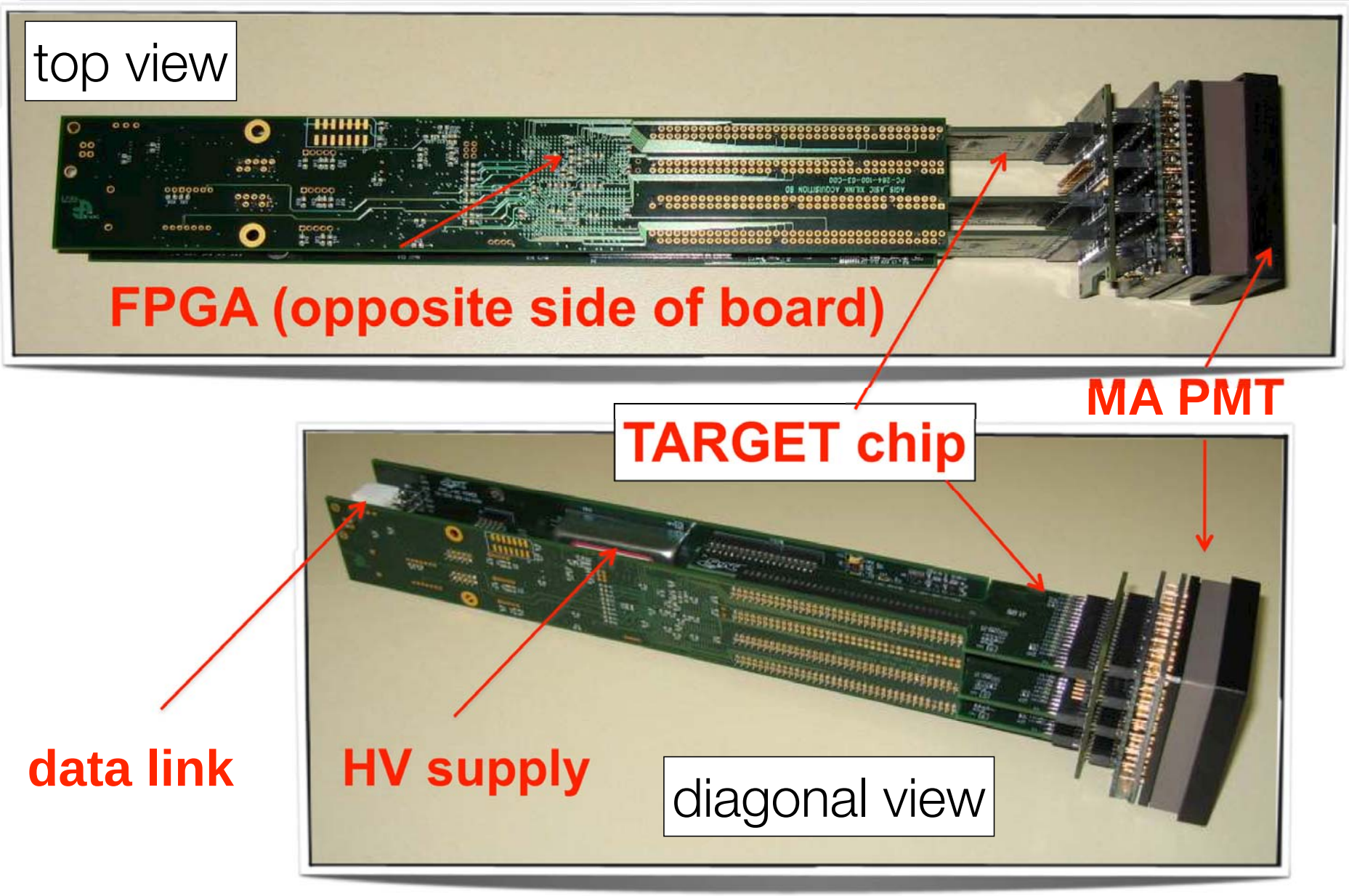


Transfer function

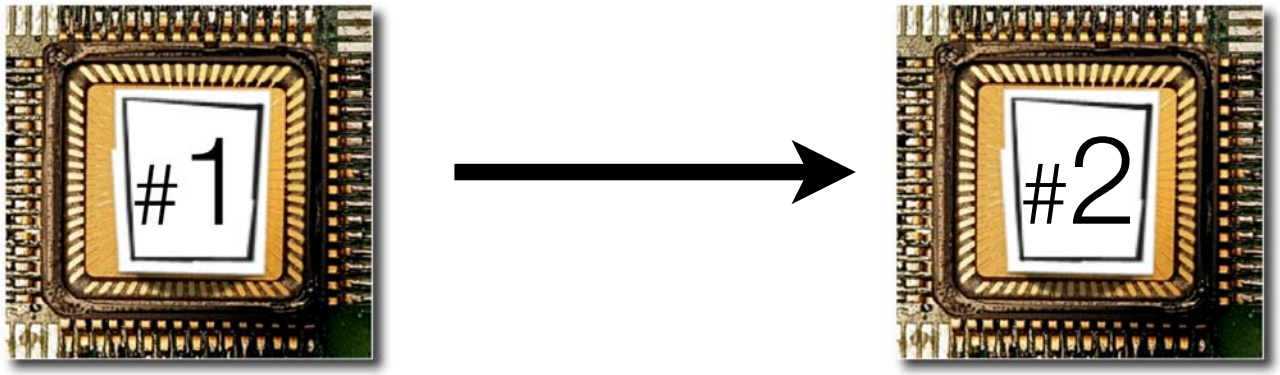
- Correlation between input voltage and output ADC counts
- Standard deviation due to variation from capacitor to capacitor (but shape is the same)
- Residuals to 4th order polynomial fit within capacitor smaller 1 ACD count



Status of work



Going from TARGET 1 to TARGET 2



- TARGET 2 design well underway (production run in the fall)
  - Trigger on analog sum of 4 channels
  - Longer look-back time for buffer (4μs → 16 μs)
  - Faster readout (16 μs → 2 μs) or more dynamic range
  - Higher bandwidth (150 MHz → 380 MHz), lower cross-talk (1%)
  - More trigger outputs (1 → 4)

Summary of digitization for TARGET 2

Spec	TARGET 1	TARGET 2
Dynamic Range	12-bit (4096)	12-bit (4096), 10 bit effective
Channels	16	16
Sampling Capacitors	4096	16384
ADC Clock Speed	223 (445 effective) MHz	700 effective MHz
Samples per Digitization	16	32
Channels per Digitization	2	16
Ramp Time	4096 / (223MHz x 2) = 9.3 μs	1024 / (650 MHz) = 1.5 μs
Ramps per Channel	64/16 = 4	64/32 = 2
Totals Ramps	16/2 x 4 = 32	16/16 x 2 = 2
Channel Digitization Time	4 x 9.3 μs = 37 μs	2 x 1.5 μs = 3 μs
Total Digitization Time	32 x 9.3 μs = 290 μs	2 x 1.5 μs = 3 μs

- In case of TARGET 2, the deadtime will be dominated by transfer time from chip

Cost Estimate for Front-End Module

- No labor for testing and calibrations included

- Numbers in **blue** are based on real quotes

Item	13,000 channels		640,000 channels	
	Unit price	Cost/ch	Unit price	Cost/ch
ASIC	**$65**	**$4.06**	**$15**	**$0.94**
FPGA (XC5VLX30T)	$235	$3.67	$176	$2.75
HV module	$140	$2.19	$105	$1.64
Connectors		$1.17		$0.88
FPGA board components		$2.42		$1.82
PS board components		$1.14		$0.85
PCB fabrications	**$9~38**	**$1.70**	**$5~22**	**$0.91**
Board loading	$10~40	$2.44	$8~30	$1.76
Total		**$18.70**		**$11.54**

The next steps

- TARGET 2 ASIC development
  - Testing and characterization of next-generation chip
- Board development
  - Provide a TARGET-board, similar to DRS-4, so that people could add their own triggering, HV system, ... to the readout channel
  - In discussion what needs to be done to redesign for SST
- Backplane development
  - Develop backplane for CTA-US camera that takes the different pixel trigger channels and combines them into a camera trigger.