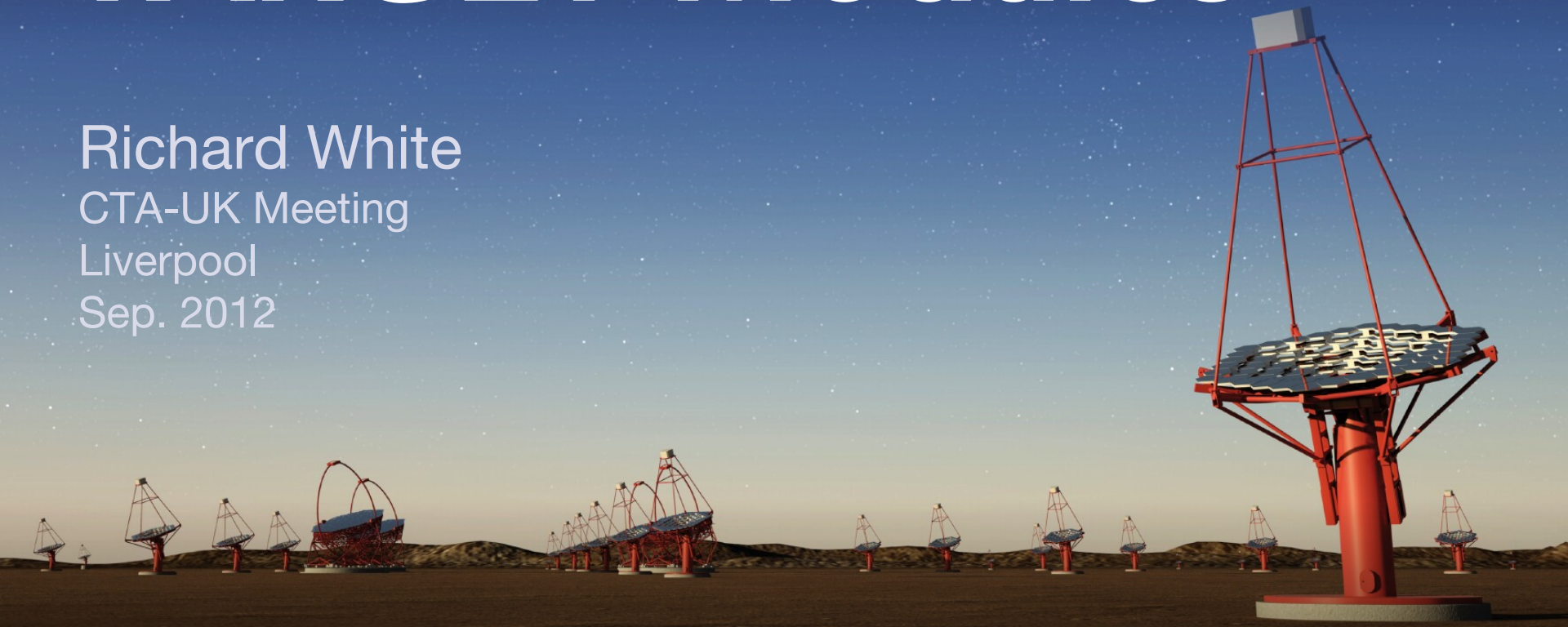
TARGET Modules

Richard White

CTA-UK Meeting
Liverpool
Sep. 2012



Most material here is stolen from Justin's talk in Amsterdam and this note:

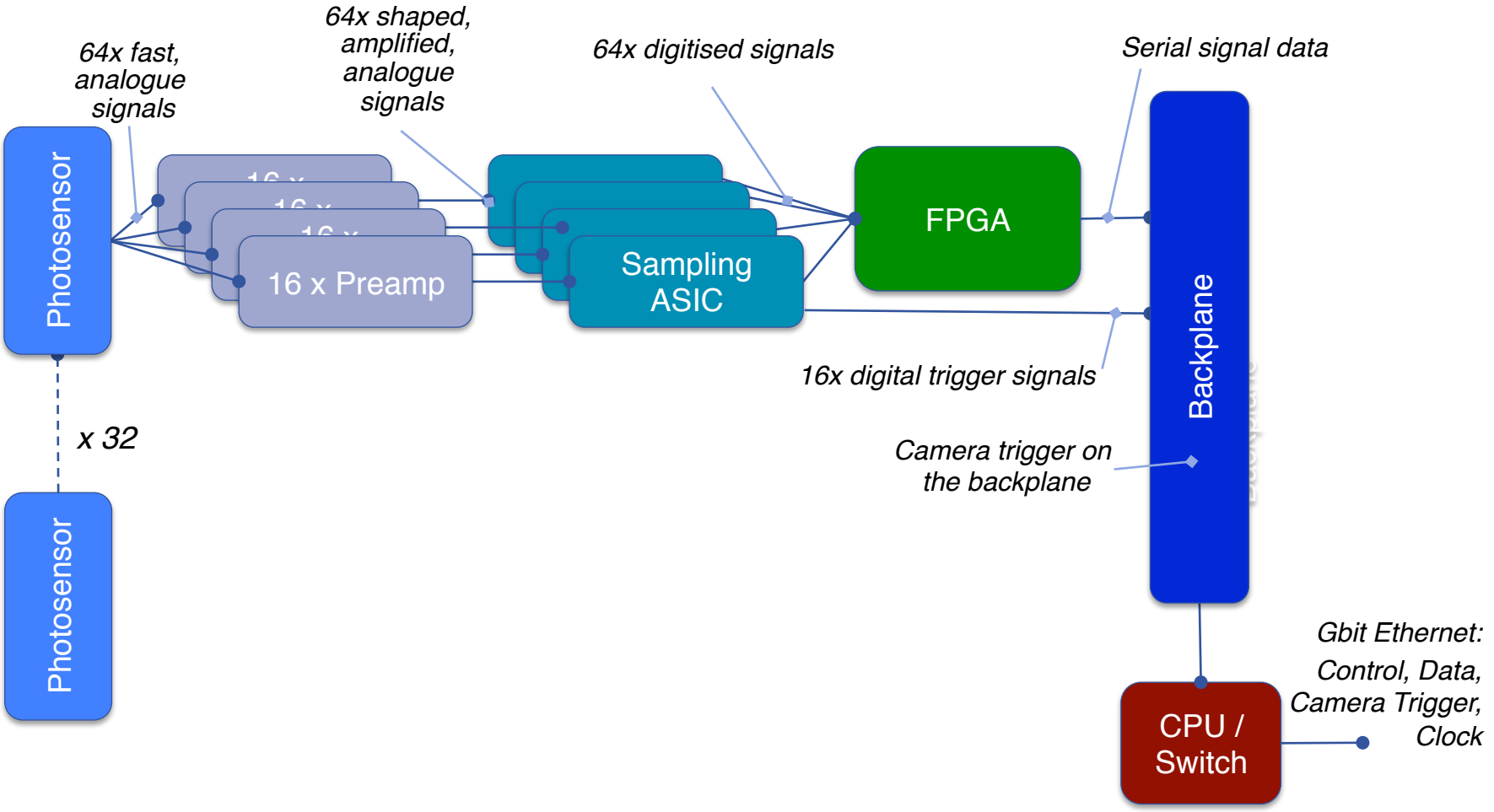

Characterization and Optimization of the TARGET 4 chip for the Cherenkov Telescope Array

Margaret C. Murphy*

University of Leicester

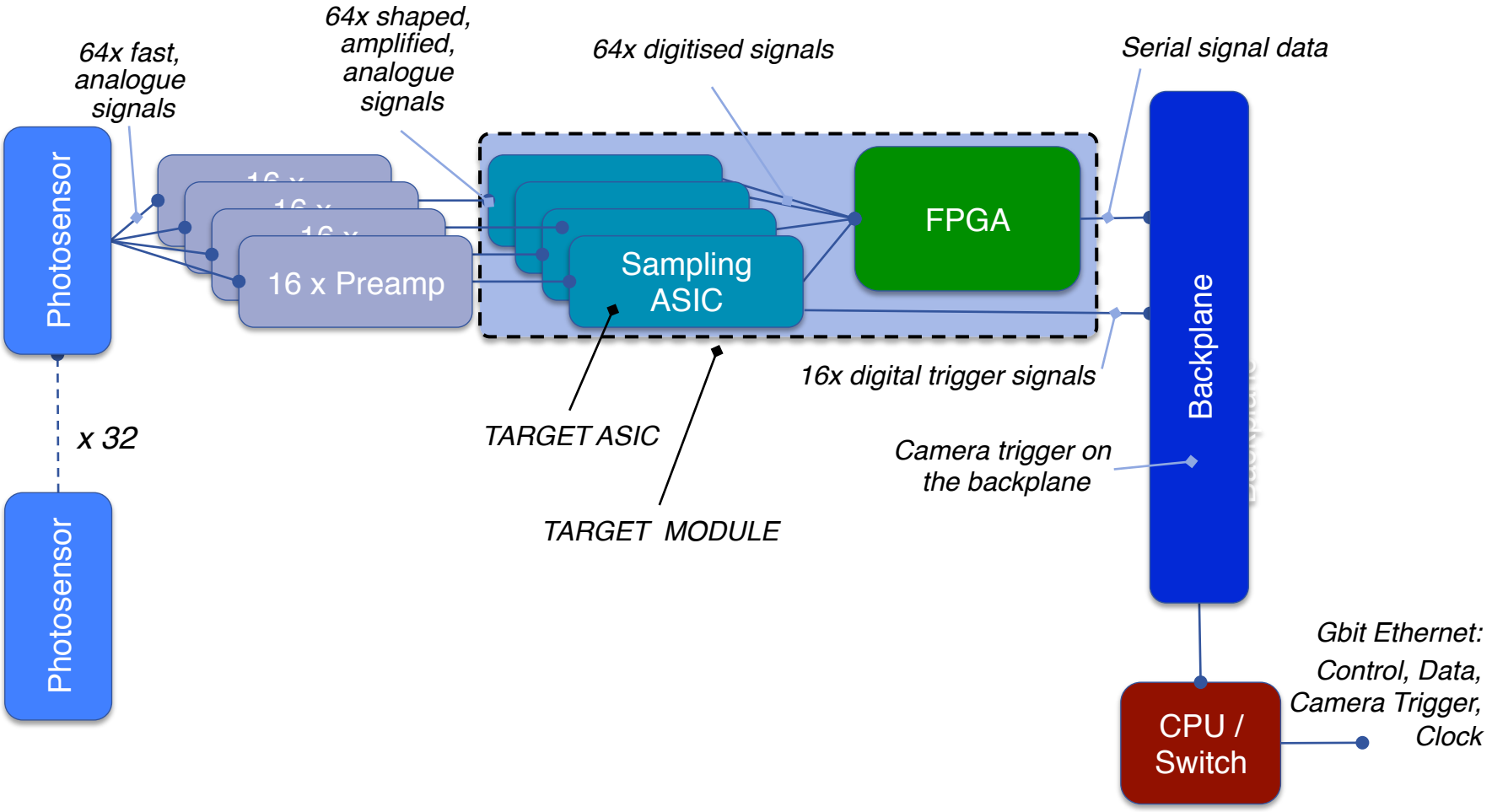
Introduction

TARGET and CHEC



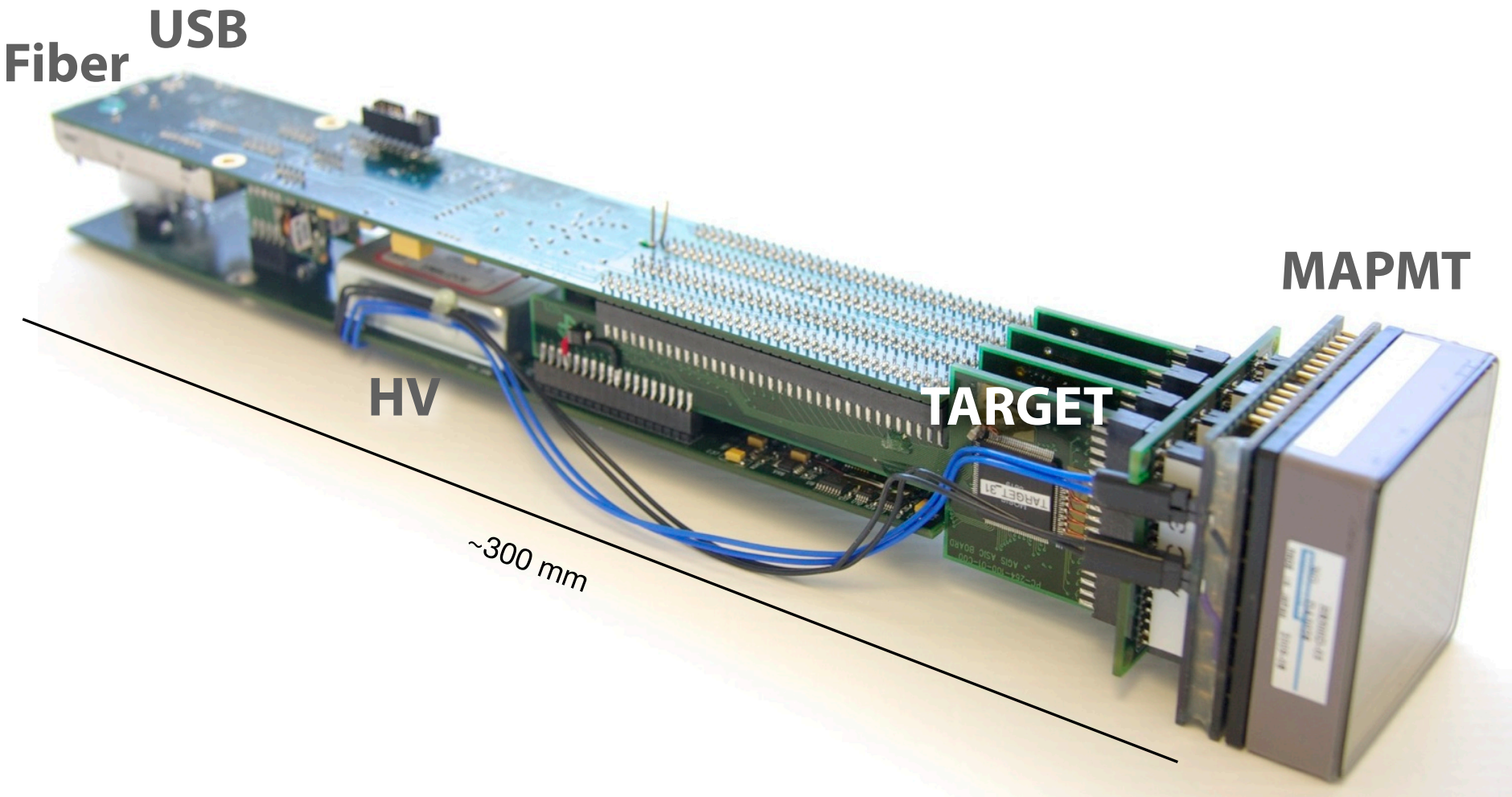
Introduction

TARGET and CHEC



The TARGET Module

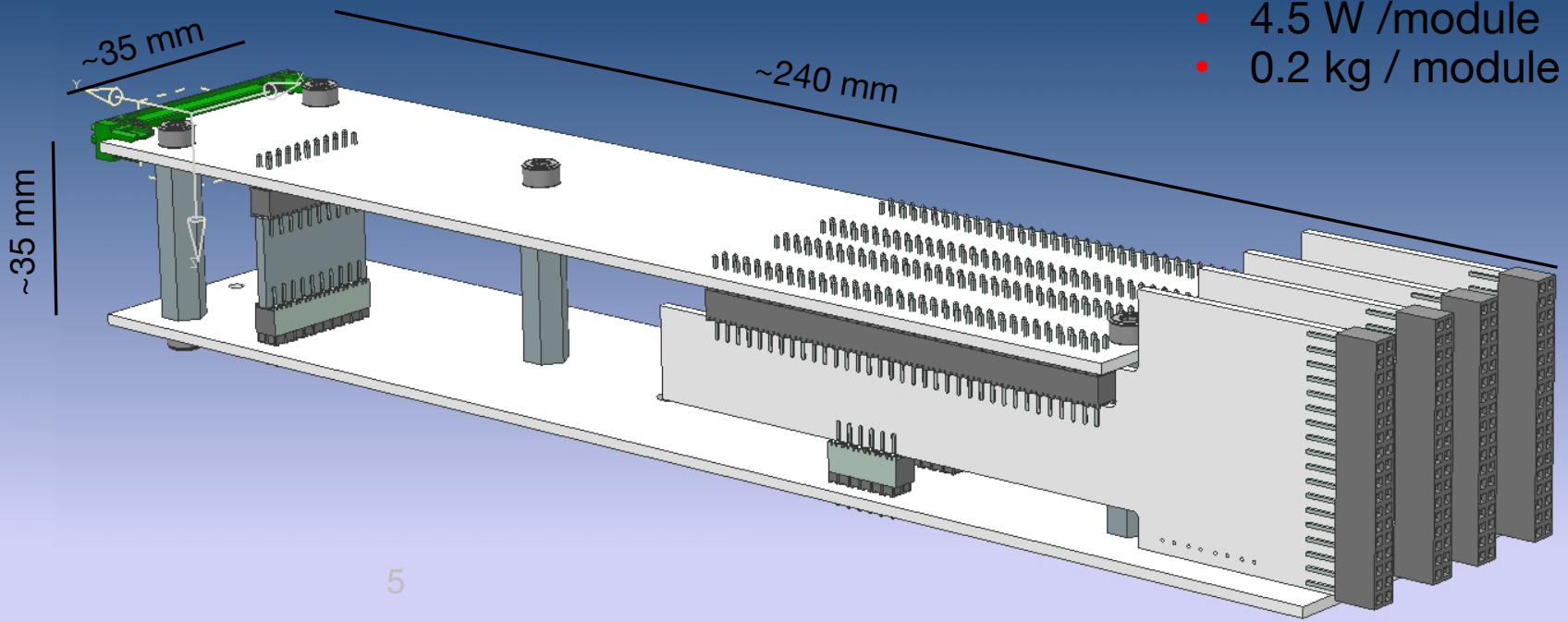
Version 1



The TARGET Module

CHEC Adaptations

- Shorter
- Parallel trigger output
- Height constrained
- Keep-out regions for rails
- +5 V feed through for preamps

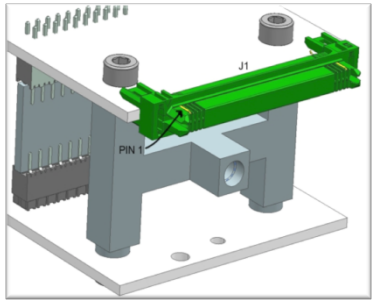


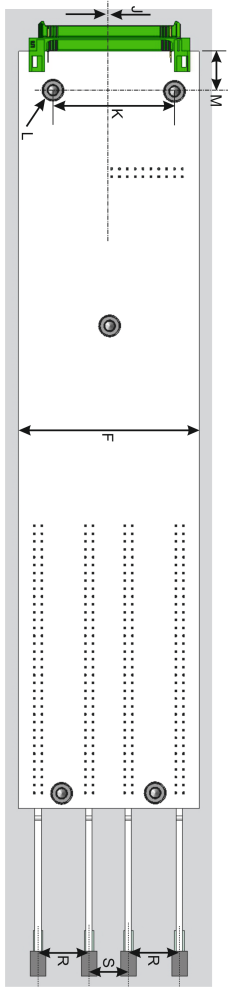
- 4.5 W /module
- 0.2 kg / module

5

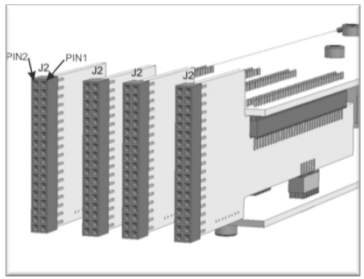
The TARGET Module

Interface Control





- Mechanical tolerances defined.
- Input pinning and connector from preamplifier module defined.
- Output pinning and connector to back plane defined.
- TARGET input coupling defined.
- Preliminary environment defined.
- Preliminary HV connector defined.
- Preamplifier output pulse shape and range defined, but not fixed yet.
- Outstanding issues:
  - Preamplifier power consumption and acceptable noise on power supply
  - Final HV connector
  - Final preamplifier output pulse shape
  - More TARGET specs: transfer function, noise, operating temperature range, power consumption



http://wiki.gamma-ray.co.uk/images/e/e7/SRC-RS-00001-00_DRAFT-CTA_Target_module_Interface_Specification_Control_Document.docx

The TARGET ASIC

Versions

- TARGET 1: characterized
  - Works well
  - 4k sample buffer per channel; simple trigger (OR of 16 channels)
- TARGET 2/3: characterized
  - 16k buffer depth; improved trigger (OR of 4-channel analog sums)
  - Fixed AC linearity problem of TARGET 1
  - Suffered problems in shift register that provides configuration voltages, prevented bias voltages necessary for data taking from reaching comparators
- TARGET 4: characterization in progress / nearly done
  - Most of shift register problem fixed
  - Small problem remains (prevents sampling slower than 2.3 GSa/sec)
- TARGET 5: chips now in hand
  - Designed to fix remaining shift register problem,

TARGET	1	5 (4 is similar)
Channels	16	16
Storage cells per channel	4096	16,384
Pre-amplifier?	No	No
Single-ended or (pseudo) differential?	SE	SE
Bandwidth (MHz)	150	>300
Cross-talk @ 3 dB frequency	<4%	1%
AC saturation?	Yes	No
Int/ext control voltages	Ext	Int
Trigger	OR of 16	4x OR of 4 analog sums
Wilkinson ADCs (ch x samples)	2x16	16x32
Dead time for 10 bit, 16 ch, 48 samples (µs)	48	10
Sampling frequency (GSa/sec)	0.7-2.3	0.2-1.2

The TARGET ASIC

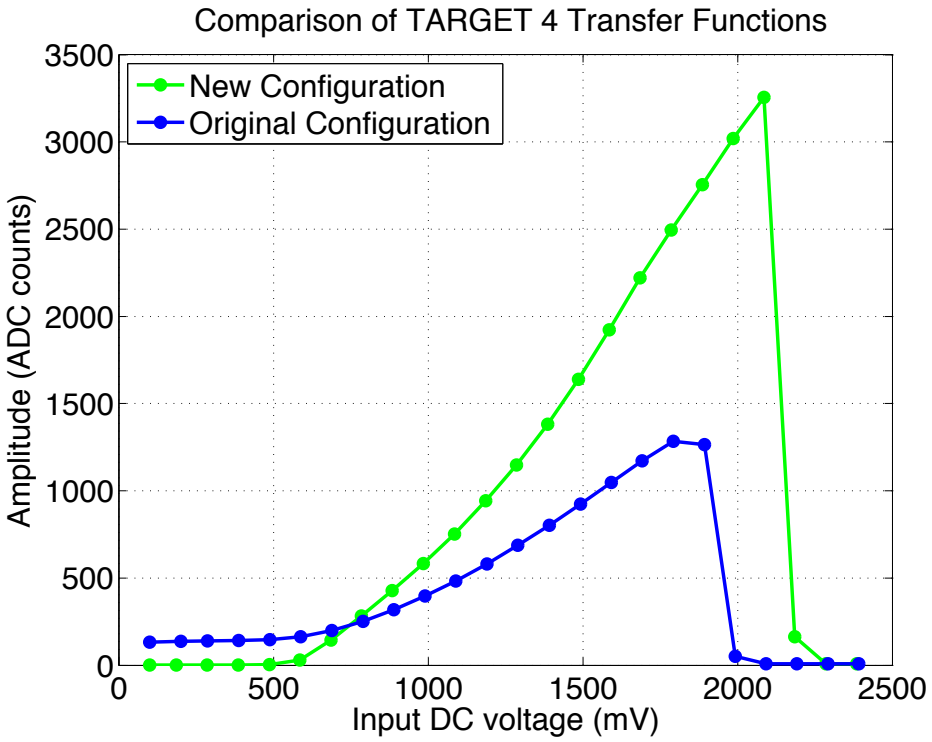
CHEC Requirements / Wish List

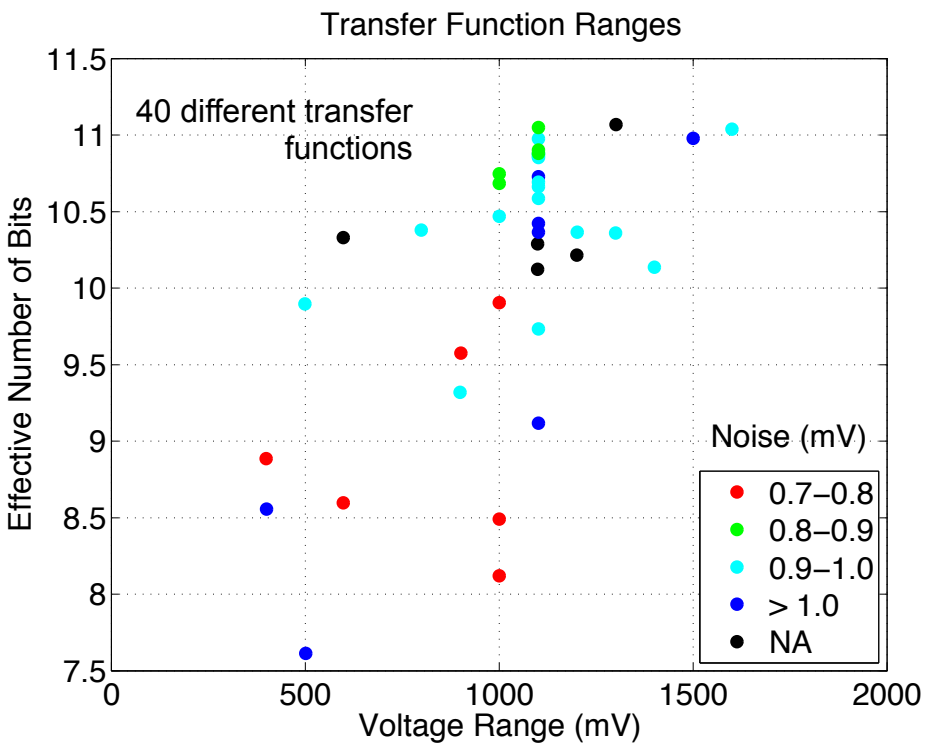
- Effective range: 1000 p.e. (ENOB = 10 bits).
- Noise & V range:
  - we don't really care as long as the ENOB is high and we can get the preamp to work in that range with a noise that doesn't dominate the chain.
  - Restriction: preamp noise < 4 mV would not be easy.
- Sampling Rate & Bandwidth: go down ~500 MSPS, 150 MHz if it helps with noise.
- Readout window: at least 100 ns would be good, we don't mind if the dead time is slightly higher…
- Trigger:
  - Analogue sum of 16
  - 4 x Analogue sum of 4
- Preamp: gain 1-2, to correct for pixel-pixel gain differences in 1 unit.
- Pedestal injection / forced readout

The TARGET ASIC

TARGET 4 Test Results

- Optimised transfer function: range up to 1.5 V.
- ENOB = $\log_2(ADC_{range}/ADC_{noise})$ up to 11 bits achieved.
- Noise: Higher than 0.4 mV expected, but upper limit.





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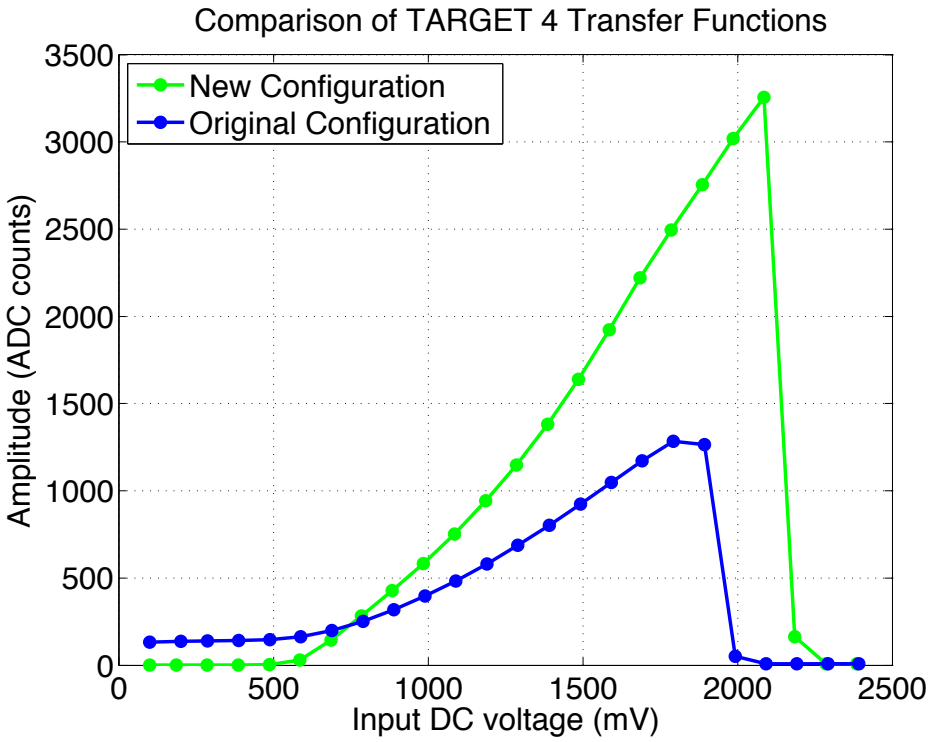
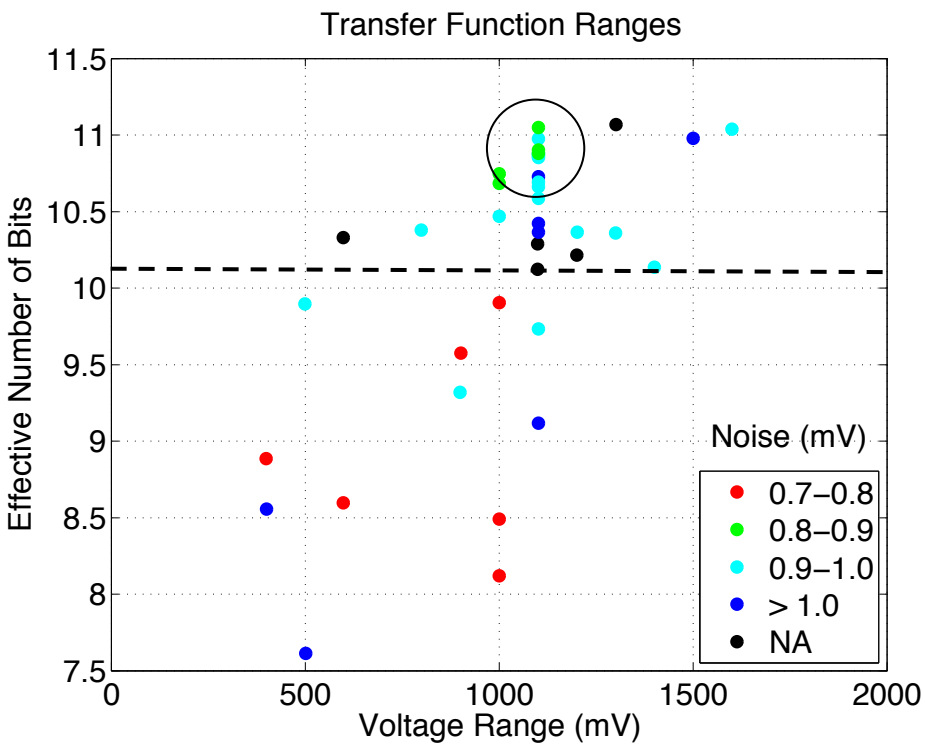
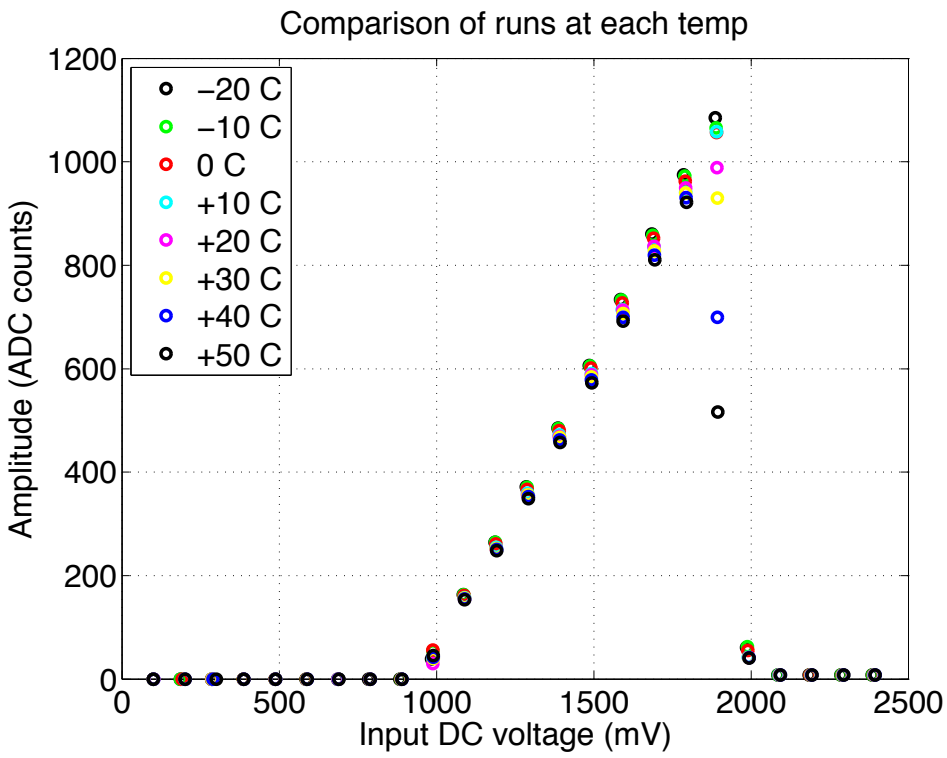


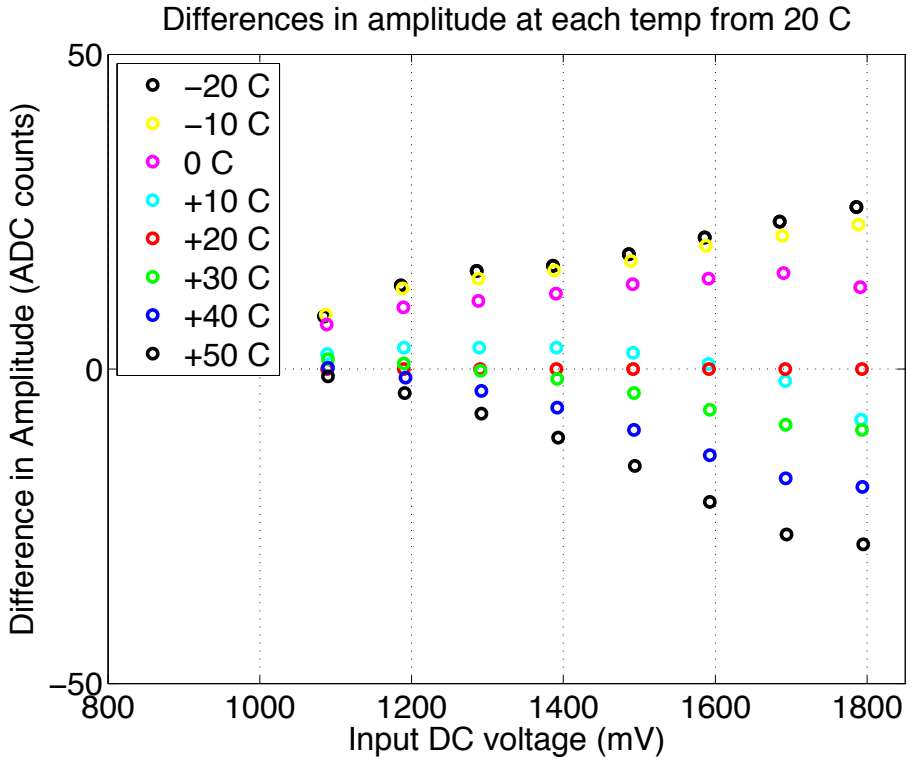


The TARGET ASIC

TARGET 4 Test Results

- Temperature dependence
- Probably due to shift in the 5 voltages that must be set to configure the transfer function, which affect things like ramp frequency.





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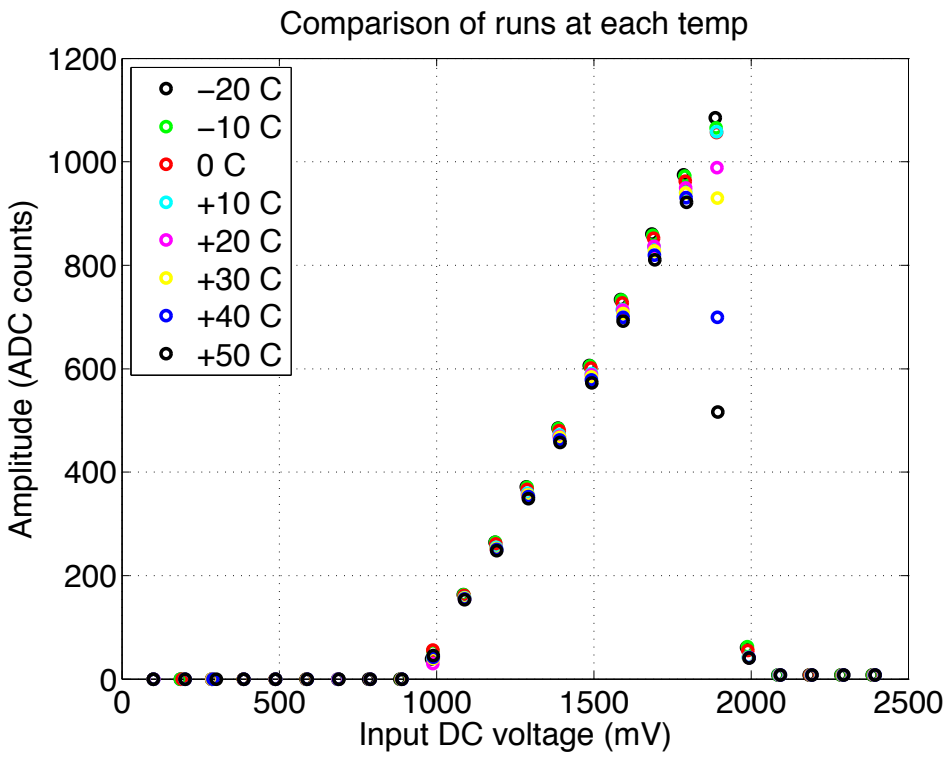
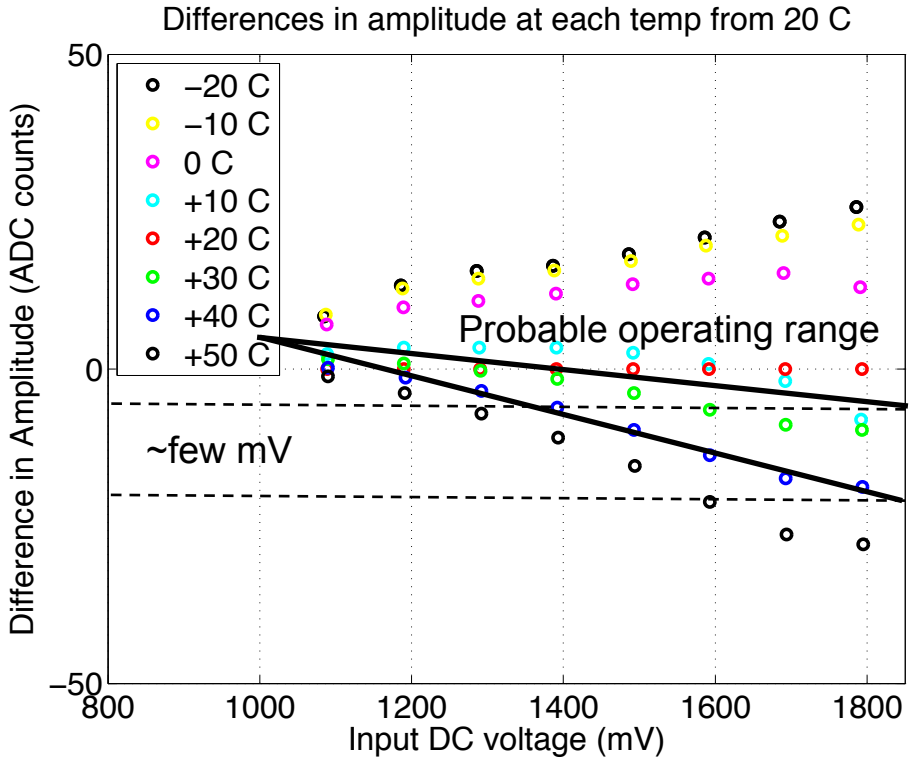
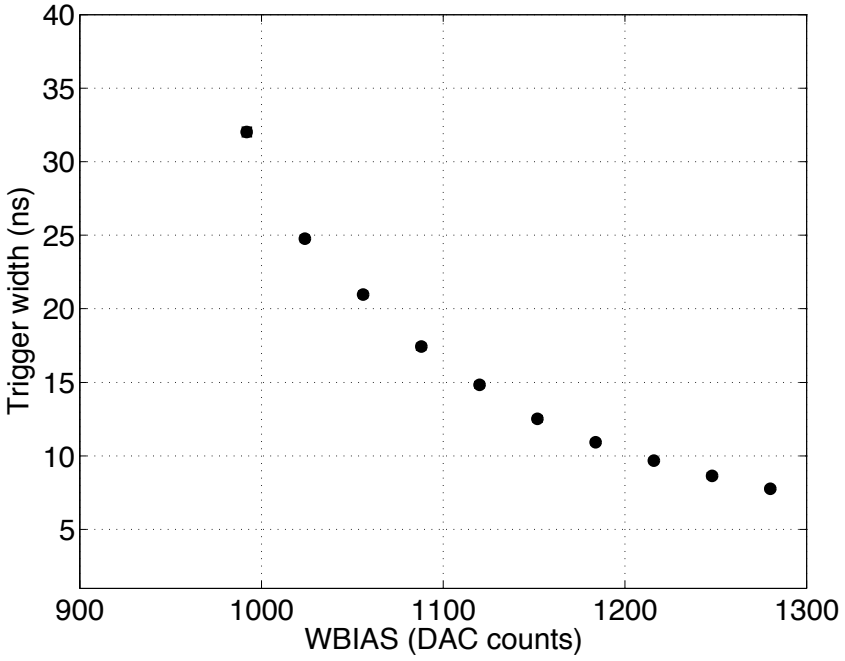


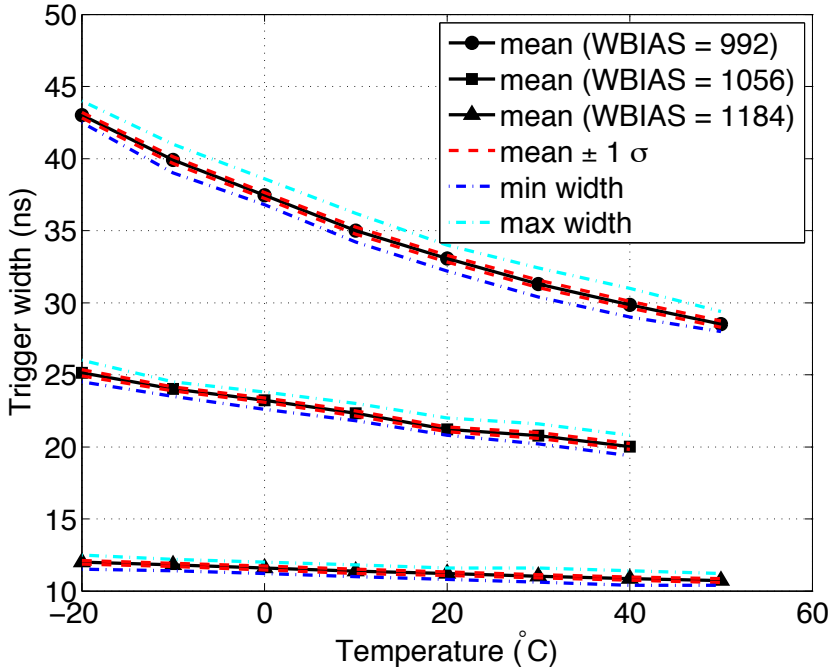


The TARGET ASIC

TARGET 4 Test Results

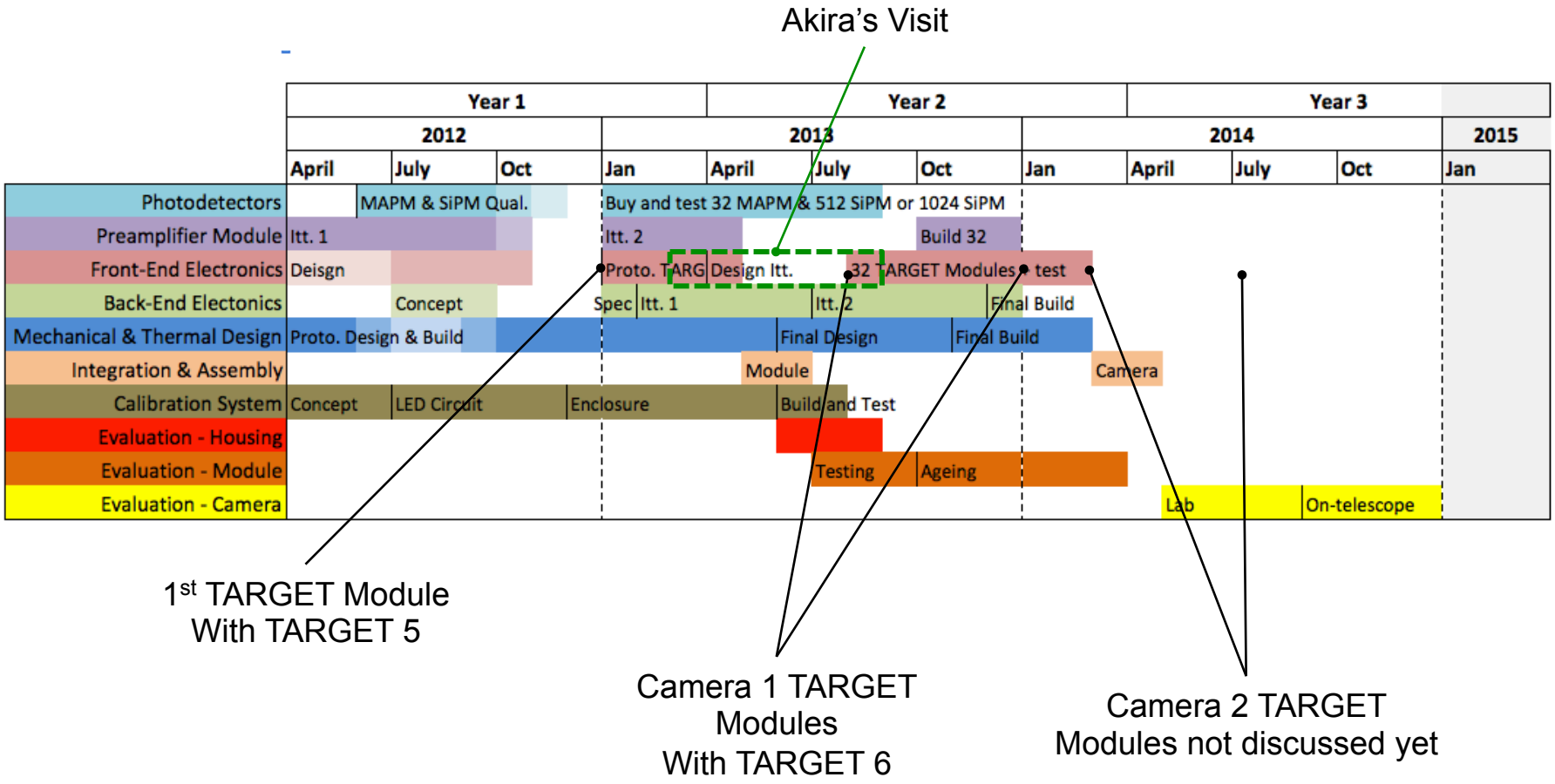
- Triggering:
- Digital output adjustable from 4-30 ns, <<1 ns jitter when properly synchronised to FPGA.
- We expect to operate with output pulse widths 6 – 12 ns… depends on preamp output. Little change with T at these widths.





Timescale

TARGET & CHEC



Conclusions

- The original TARGET module has been adapted for CHEC.
- A draft CHEC-TARGET IDC exists, only a couple of outstanding items.
- TARGET ASIC versions progressing well.
- TARGET 4 ASIC achieves 11 bits… our preamp spec will need to be updated.
- TARGET 5 ASIC will be tested soon.
- TARGET 6 ASIC design is still open to our “wish list”.
- No in depth discussions yet about delivery timescales.
- No in depth discussions yet about SiPM TARGET module.