Back-End Electronics

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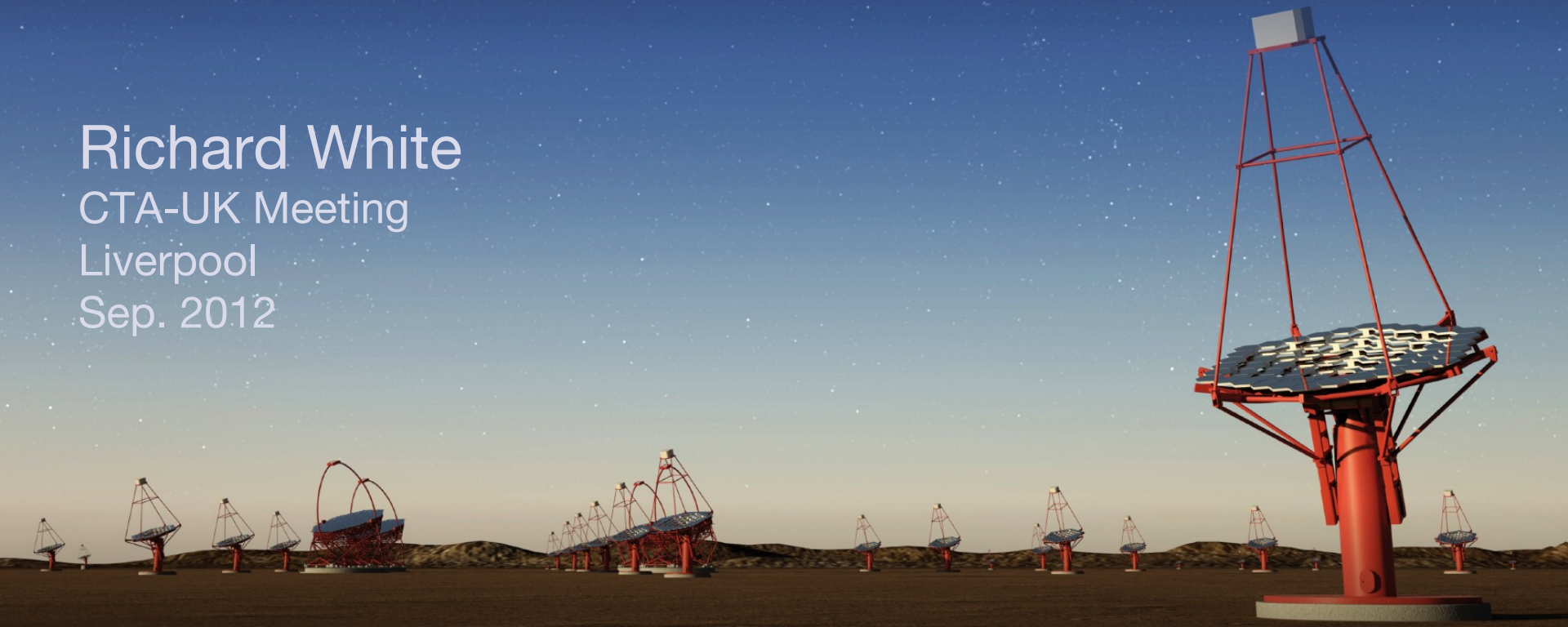
CTA-UK Meeting

Liverpool

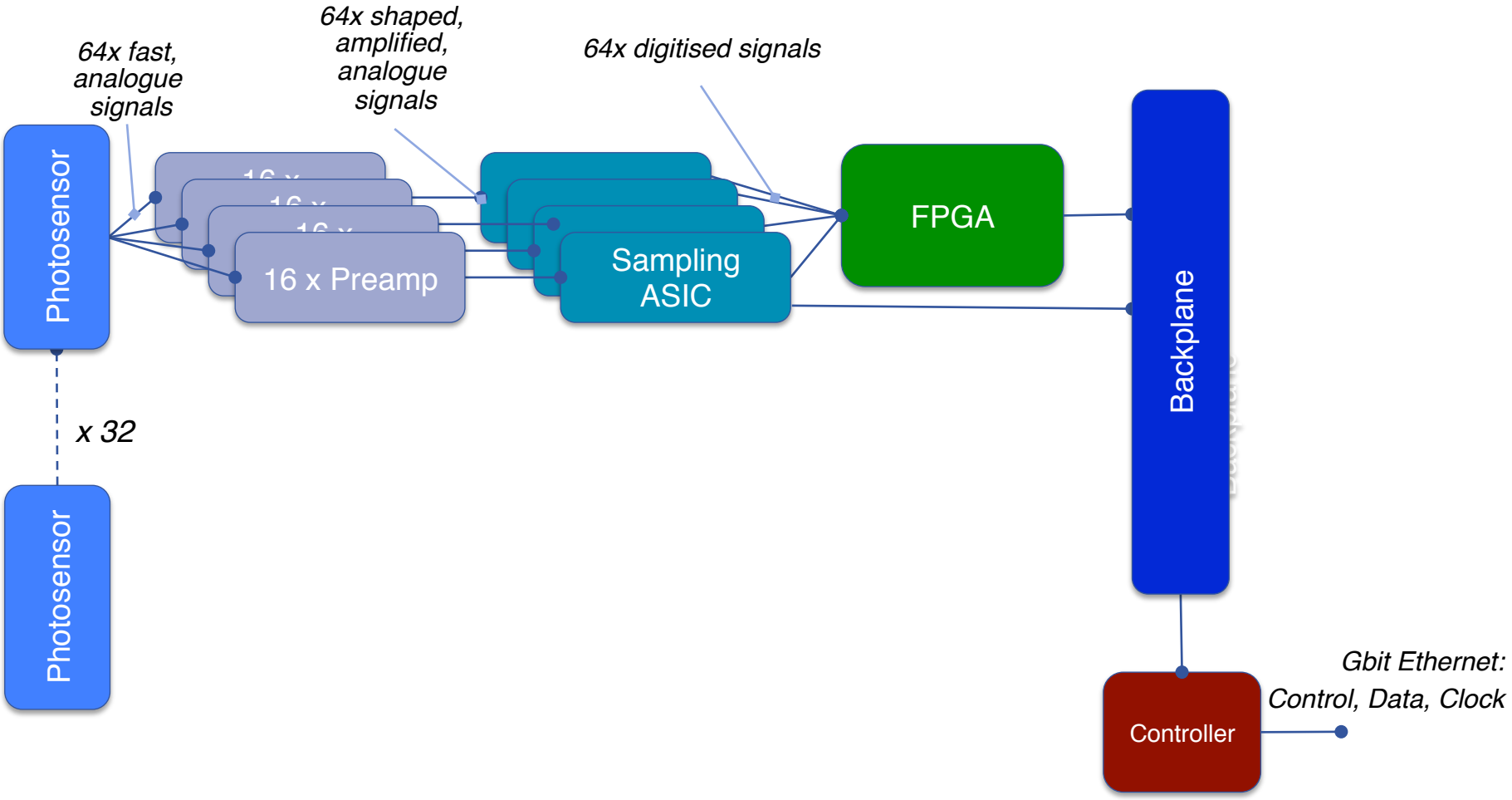
Sep. 2012



University *of* Leicester

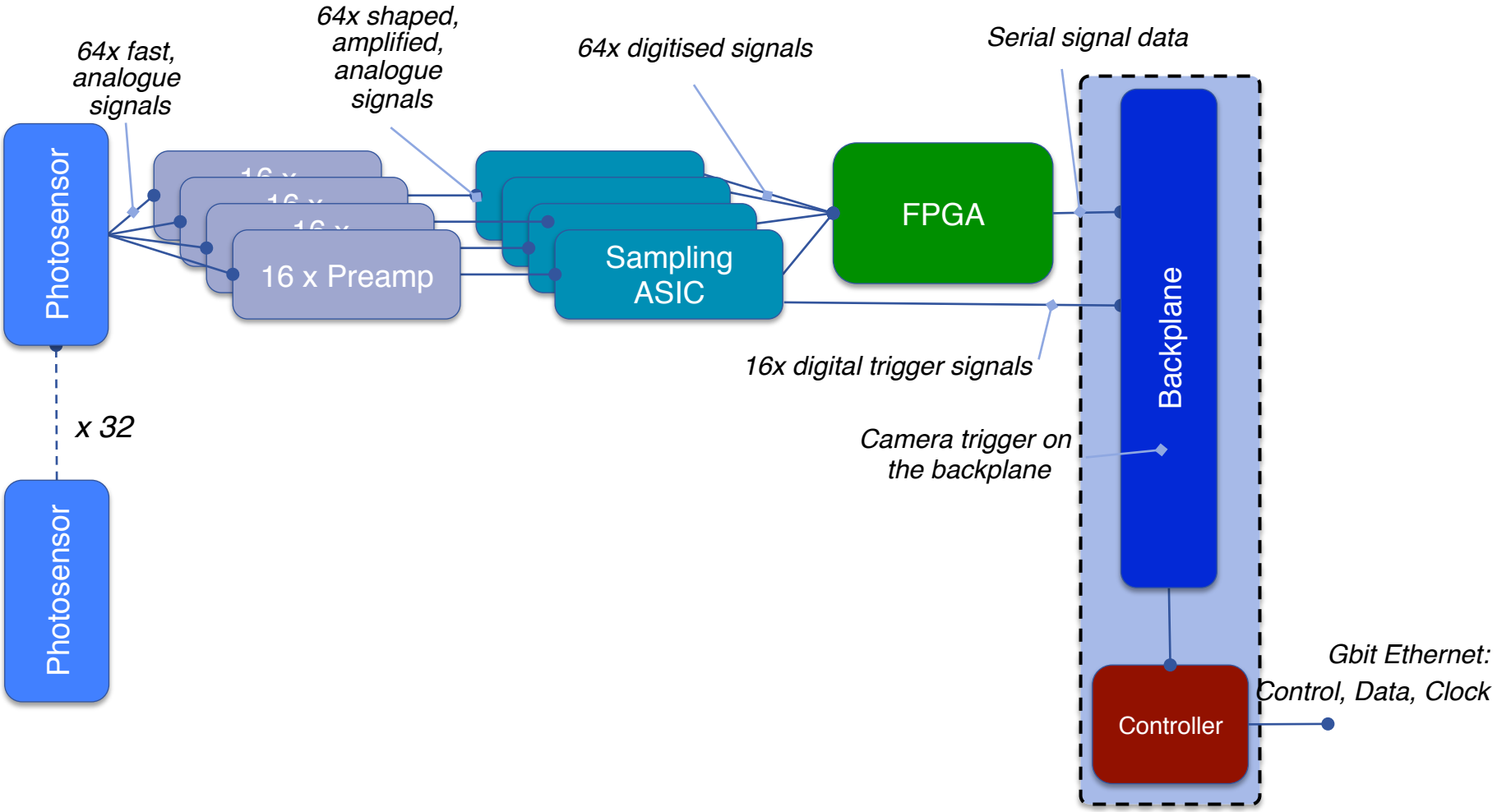
Introduction

The CHEC Back-End



Introduction

The CHEC Back-End



Introduction

Operational Concept

- The backplane receives trigger signals from all TARGET modules and produces a camera trigger signal.
- The camera trigger signal is sent back to the TARGET modules and they are read out.
- The backplane processes events and sends them to the camera controller.
- Time stamping can occur at various points along this path… I assume in the controller.
- All events that reach the controller are converted to the “CTA” protocol and transmitted to a central location.
- There is no hard-wired array trigger. All events are sent to a central location with nanosecond time stamps and compared to other telescopes before writing to disk.

The Backplane

Concept

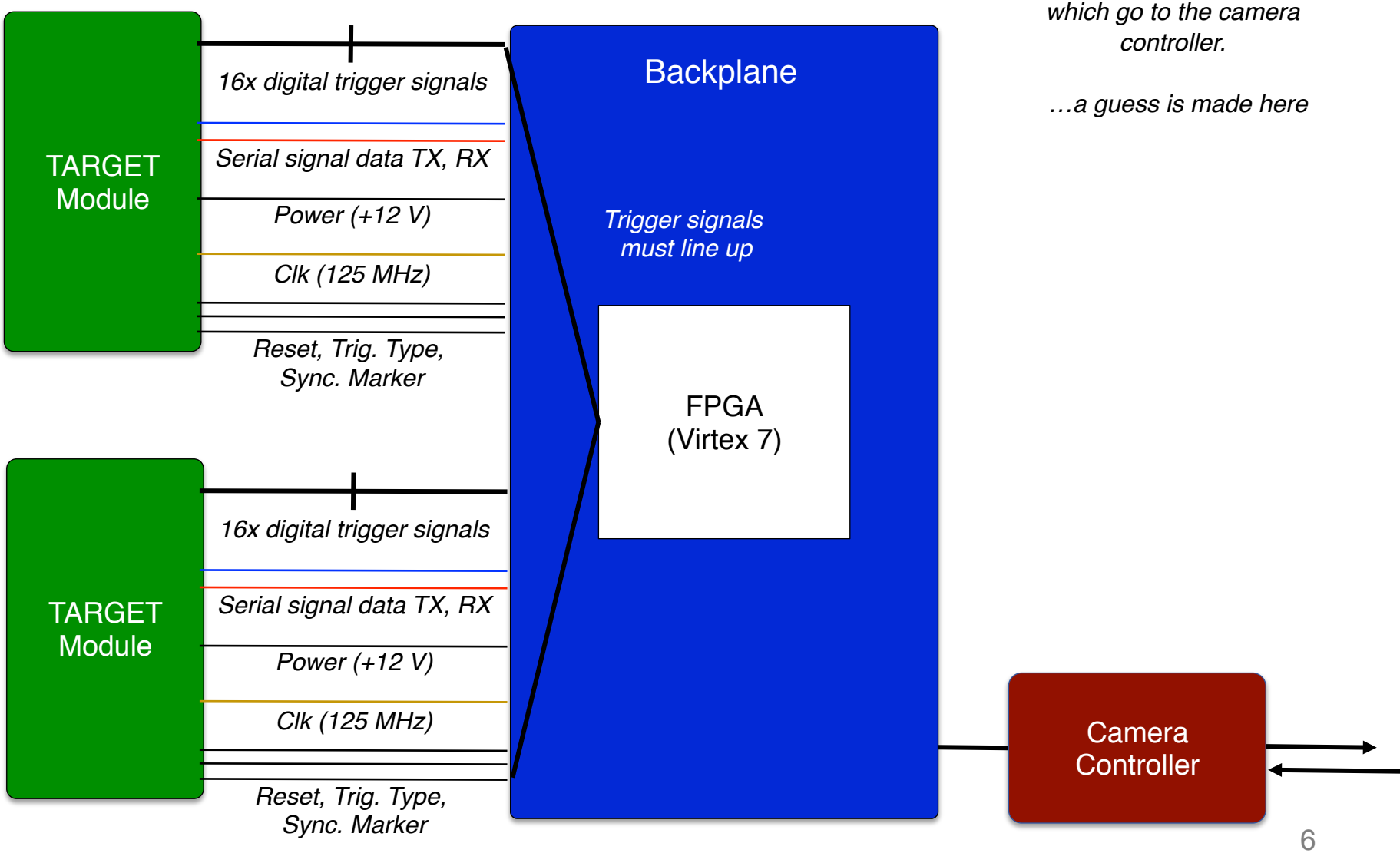
- Functional Requirements:
  - Combine trigger signals from TARGET modules to form a camera trigger.
    - Next neighbour logic
  - Send the camera trigger signal back to the TARGET modules when needed.
  - Interface clock between TARGET modules and camera controller.
  - Interface serial data signals from TARGET modules to camera controller.
  - Interface control and monitoring signals from the TARGET modules to camera controller.
  - Provide power to the TARGET modules.

The Backplane

Concept

Not clear yet exactly which signals go to the FPGA and which go to the camera controller.

…a guess is made here



The Backplane

Implementation

- Implemented as a single PCB with 1 very large FPGA.
- Wash. U. need to something very similar for the US camera.
- We have now agreed that their board will have a 6 x 6 TARGET module capability.
- There will be 2 physically different versions, with identical FPGA layouts and similar routing.
- We will pay $25k for a professional company to layout and manufacture this extremely large and complicated board.
- Wash. U. will deliver the PCB with some basic firmware.
- CHEC–specific firmware will probably be needed, and we hope that Oxford can help with this.

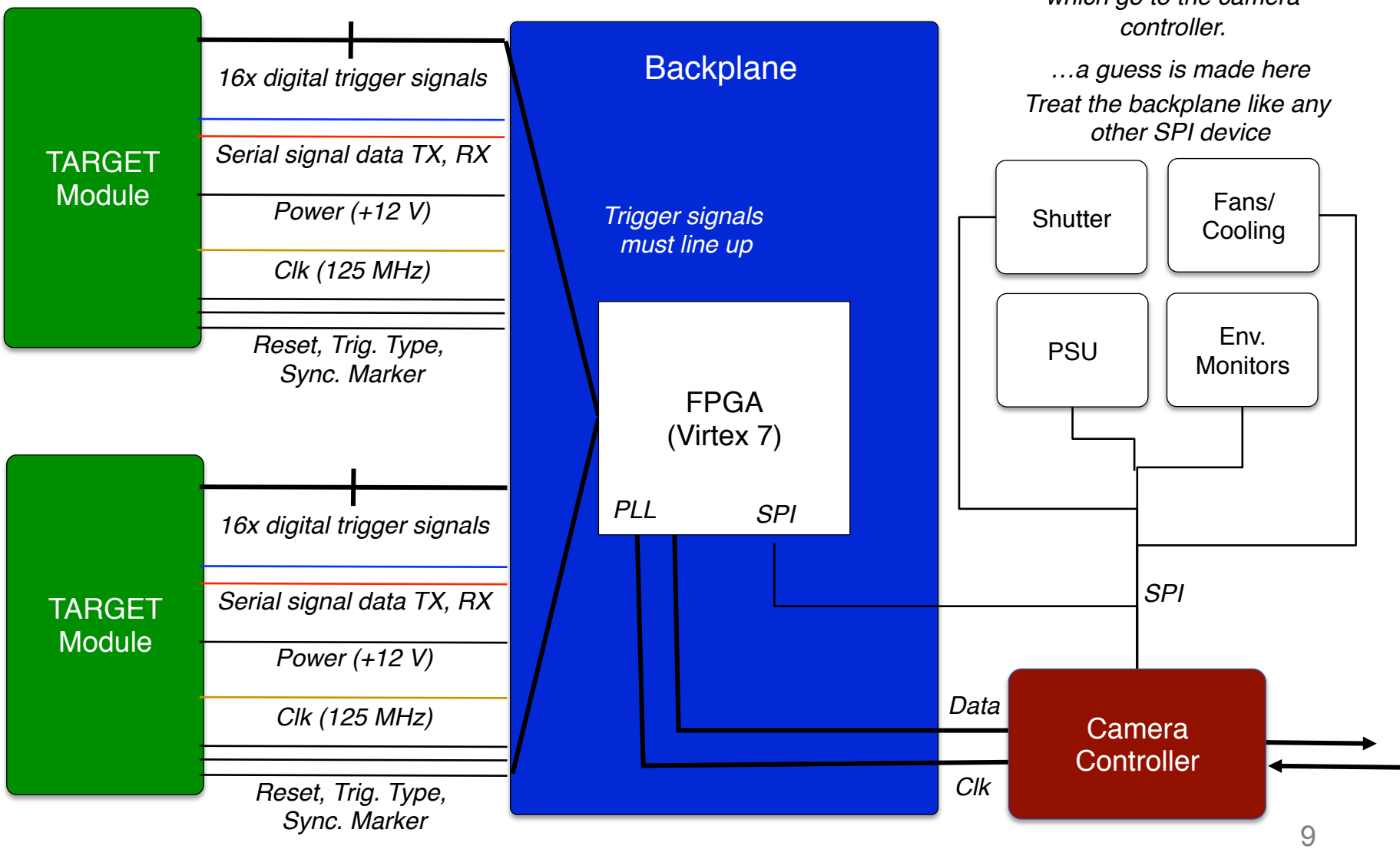
The Camera Controller

Concept

- Functional Requirements:
  - Time stamp events from the backplane.
  - Transmit events from the camera to central location.
  - Provide a clock for time stamping synchronised to the backplane and the other cameras to ~2 ns.
  - Provide control and monitoring of the backplane and camera peripherals (shutter, power supplies, cooling system) via a serial interface (eg SPI).

The Camera Controller

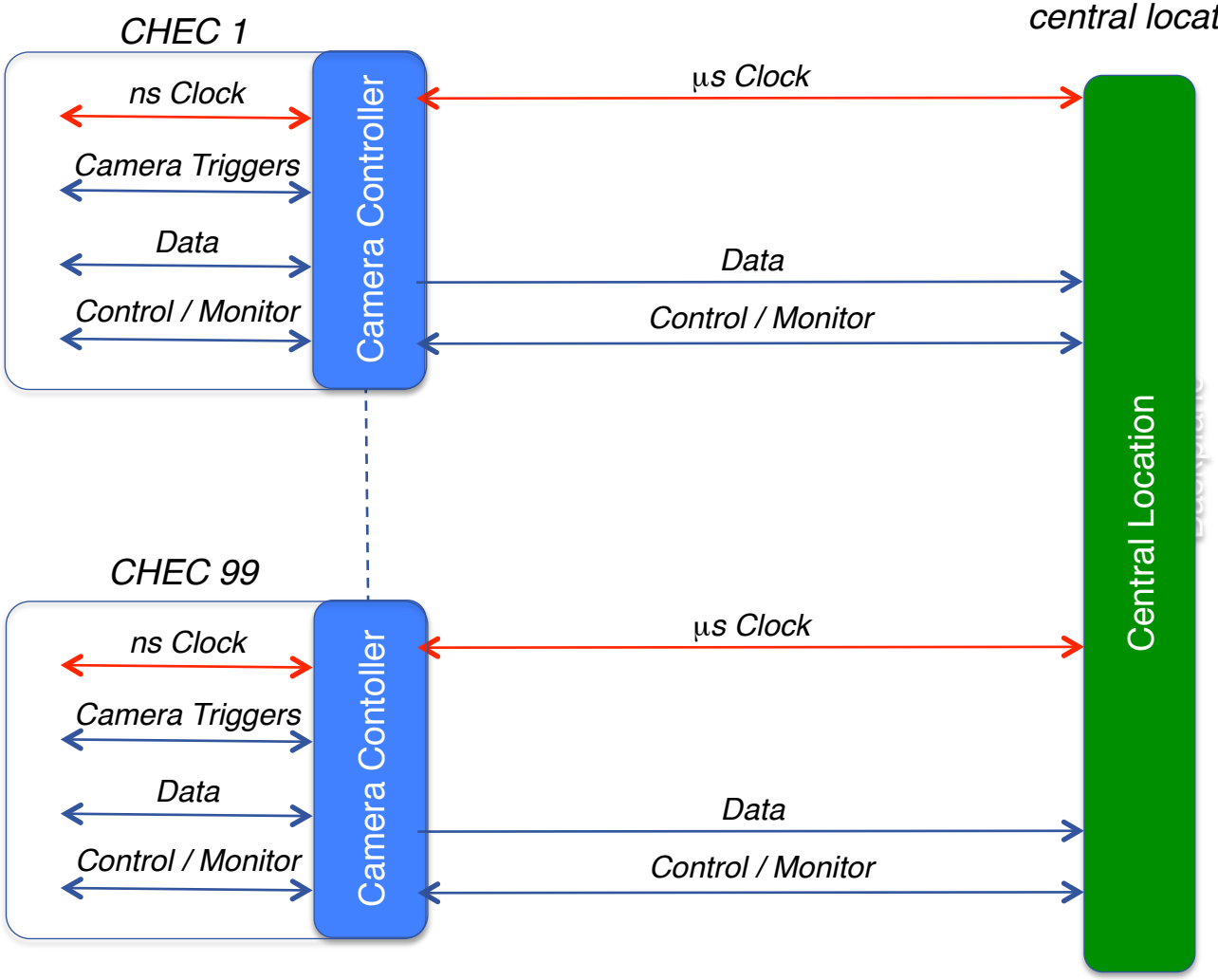
Concept



The Camera Controller

Concept

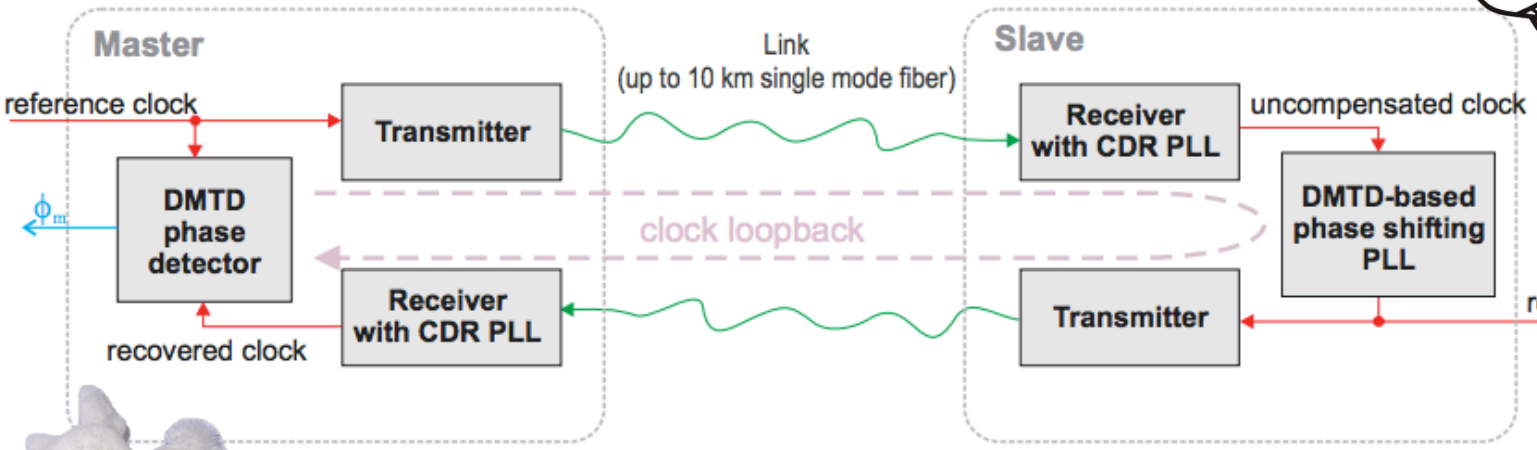
SST rate low enough to perform array trigger in central location

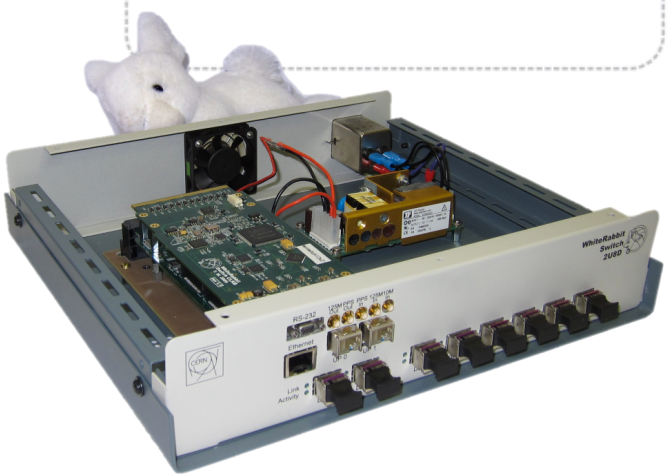


The Camera Controller

Clock Distribution

- White Rabbit:





A deterministic timing and data link

- 1 ns accuracy and 20 ps jitter
- 10 km fiber links
- Up to 2000 nodes

A successful open collaboration

- Fully open development
- Involving institutes and companies
- Full system commercially available mid-2012

The Camera Controller

Concept

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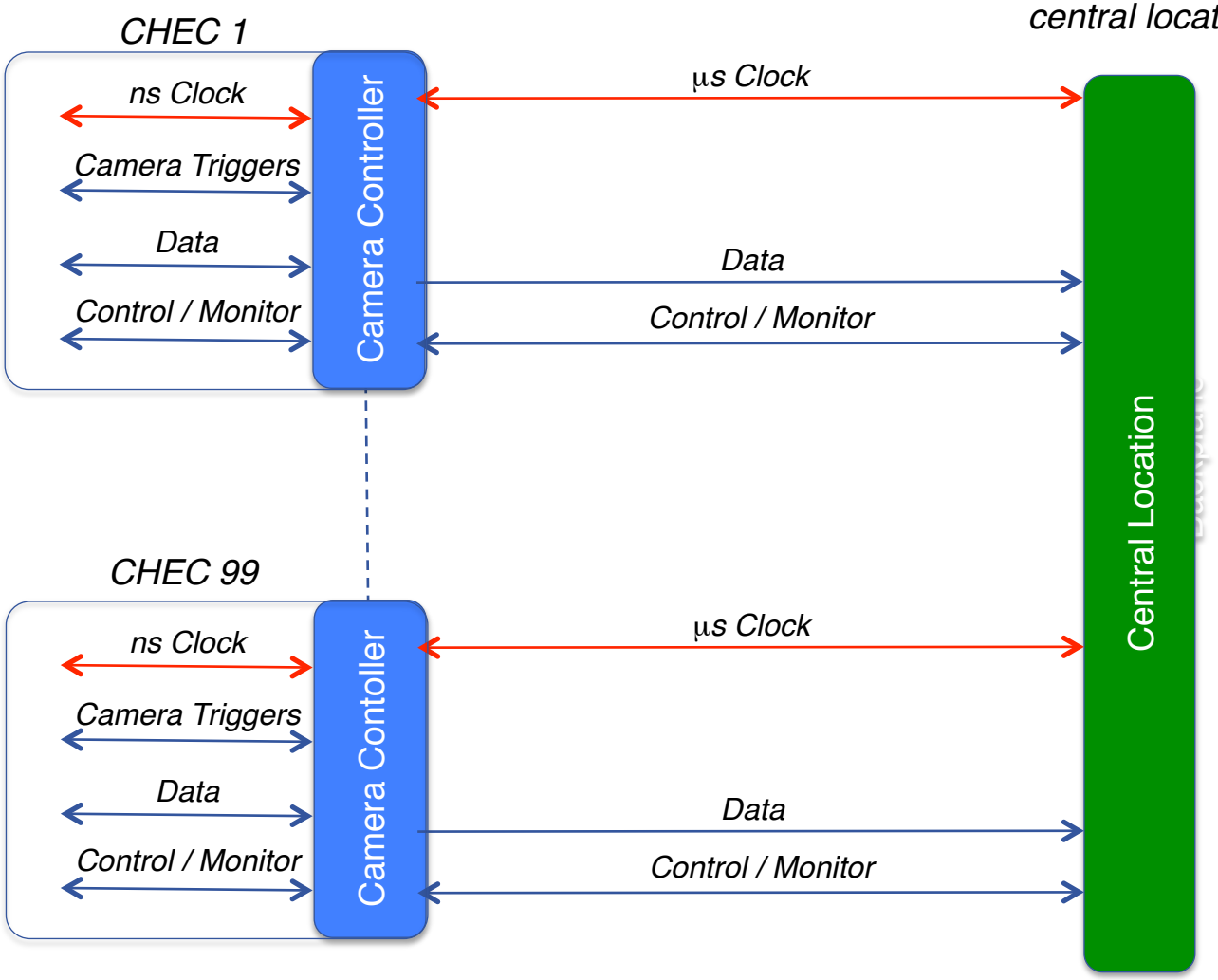

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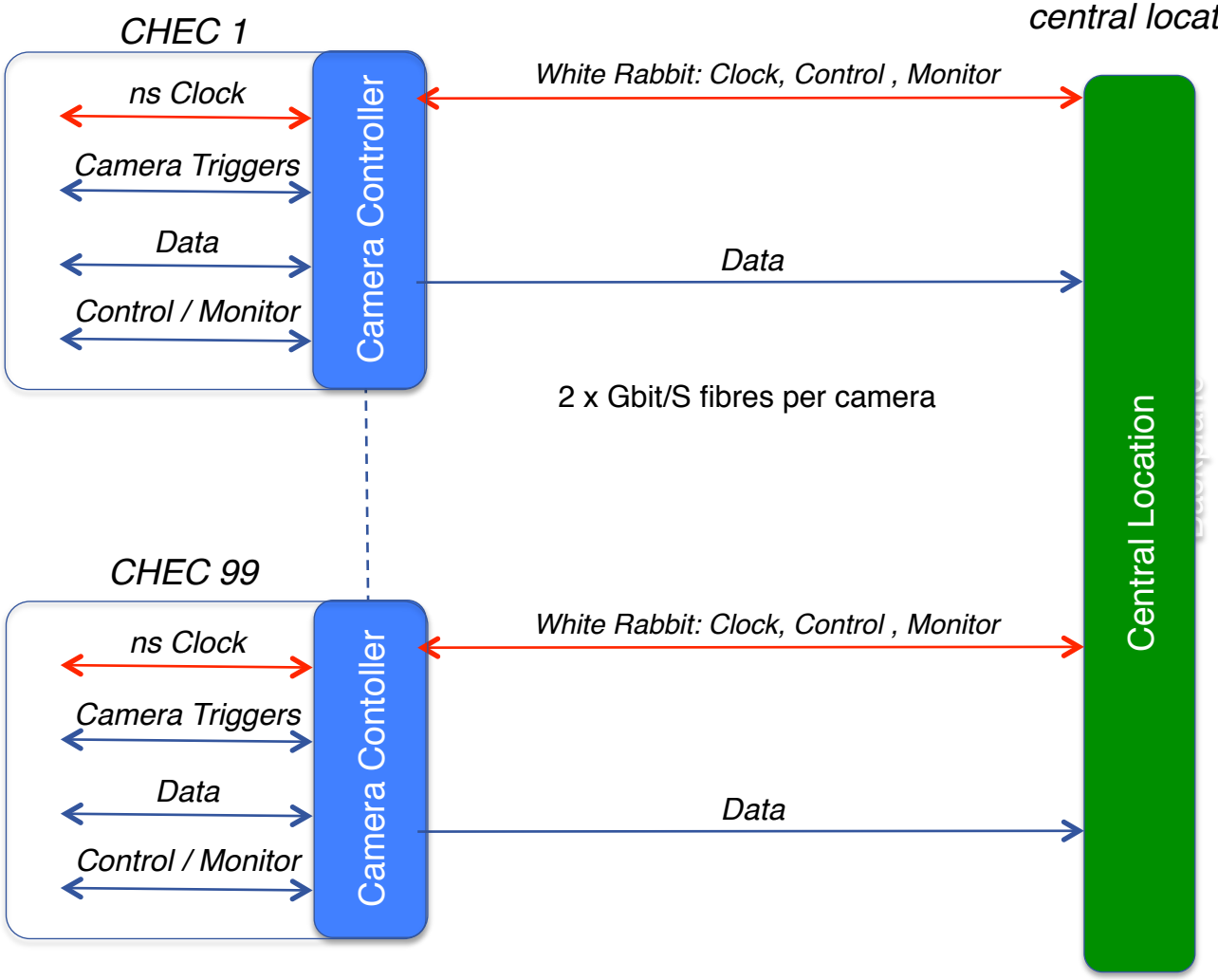
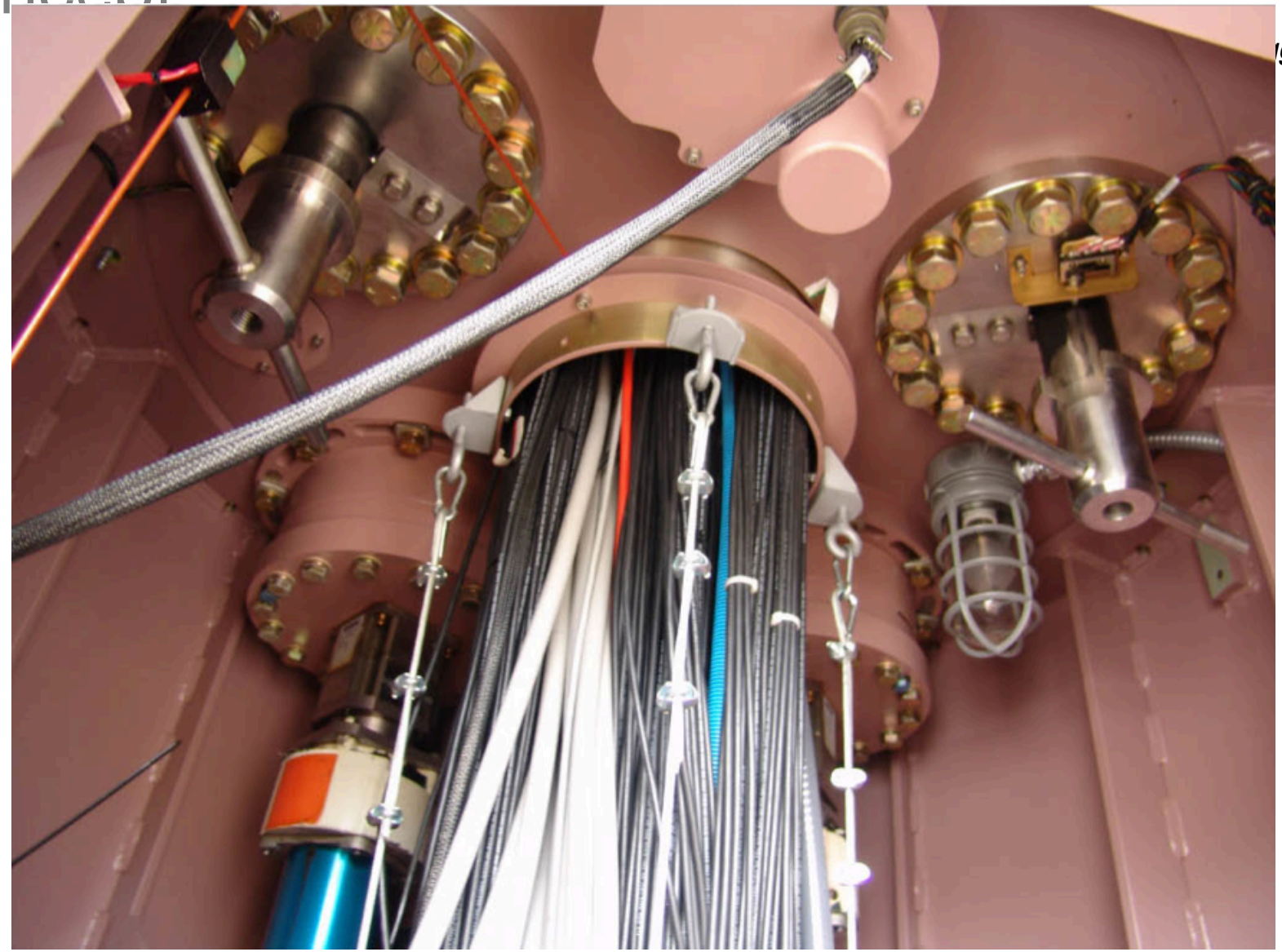


The Camera Controller

Concept



…ger in

The Camera Controller

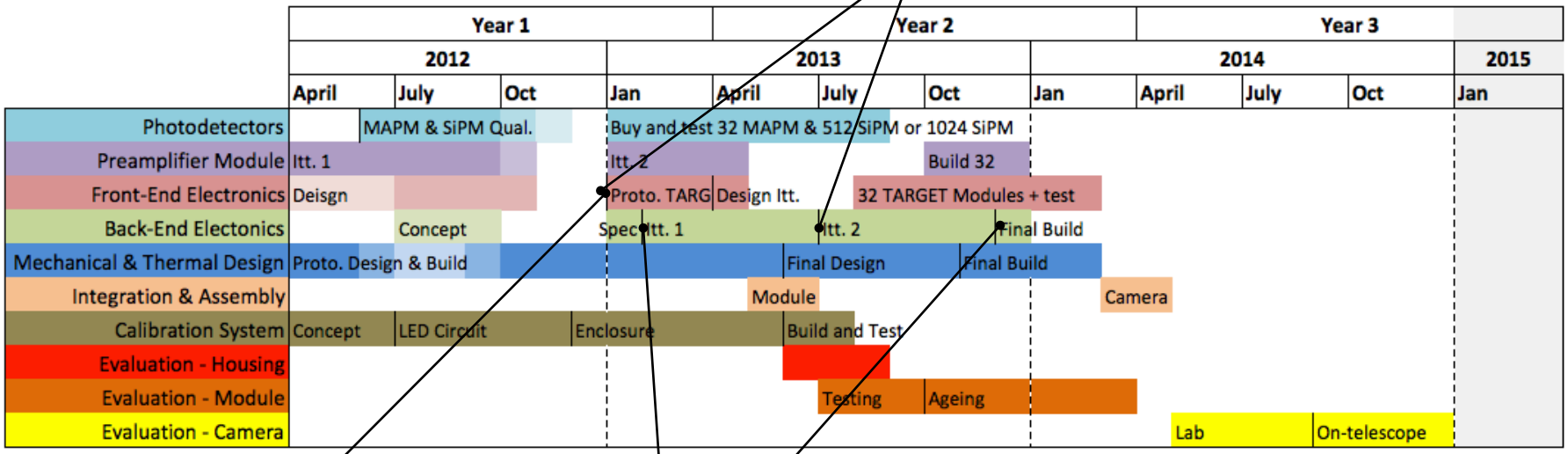
Implementation

- Either a mezzanine board on the backplane or a stand alone unit.
- David Berge will start in Amsterdam in Jan 2013 and will apply for funding to design and build the camera controller.

Timescale

Wash. U., Amsterdam & CHEC

Dutch funding wouldn't start until mid 2013, but work could start in Jan.



What to do with a single TARGET module? FPGA demo board?

Backplane development at Wash U. # iterations not set… could start with a "segment".

Conclusions

- Backend concept is underway.
- Wash. U. have agreed to build the backplane.
- Firmware development will be needed for CHEC.
- David Berge will apply (tomorrow) for camera controller development funds.
- With 3 groups involved, the concept must be clear, and ICDs will be needed.

Additional Information