

## Chapter 2. Basic Features of Silicon Detectors

This chapter presents some results from semiconductor physics that are relevant for the study of silicon detectors, on the basis of the theory exposed in [2.1], [2.2].

### 2.1 General principles

The electrons bound to atoms or molecules in a solid occupy energetic levels with a well-defined energy gap between them. The Pauli principle prohibits more than two electrons to occupy the same level. In a solid, because of the large number of electrons, the energy levels are so close to each other that they are arranged in band with continuous values of energy. The valence band contains the electrons bound to a single nucleus of the solid: for example, in silicon, they form the covalent binding, which produces the inter-atomic forces of the crystal. The conduction band contains free electrons that can contribute to the electrical conductivity of the material. Between the valence and the conduction bands there is a region of energy where no levels are allowed; this region is called the forbidden gap. The width of this region determines if a material is an insulator or a semiconductor. In an insulator, the forbidden gap is  $> 5$  eV and it is very unlikely that an electron excited by thermal collision jumps from the valence to the conduction band. In a semiconductor such as silicon, this band gap is  $\approx 1$  eV and the electrons excited by the thermal collision can jump from the valence to the conduction band. The electron leaves behind, in the valence band, an unoccupied place, called hole, with a positive charge. Both carriers, the electron and the hole, are able to move in the electric field applied to the semiconductor, although with a different mobility. The charge density of electrons ( $n$ ) and of holes ( $p$ ) is proportional to the thermal agitation and therefore to the temperature:

$$n = N_c \exp\left(-\frac{E_c - E_F}{kT}\right) \quad (2.1)$$

$$p = N_v \exp\left(-\frac{E_F - E_V}{kT}\right) \quad (2.2)$$

where  $N_c$  and  $N_v$  are the effective density of states in the conduction and valence band respectively,  $E_c$  the bottom energy of the conduction band,  $E_v$  the top energy of the valence band and  $E_F$  is the Fermi level of the semiconductor. The Fermi level is defined as

$$E_F = \frac{E_c + E_v}{2} + \frac{kT}{2} \ln\left(\frac{N_v}{N_c}\right) \quad (2.3)$$

and for intrinsic semiconductor lies very close to the middle of the bandgap. At thermal equilibrium, the product between the charge carrier densities is always constant and it is given by

$$np = n_i^2 \quad (2.4)$$

$n_i$  is called intrinsic carrier concentration, i.e. the carrier concentration in a pure semiconductor. Its value in silicon is  $1.45 \cdot 10^{10} \text{ cm}^{-3}$  [2.1]. The introduction of impurity atoms with three valence bonds (B), or with five valence bonds (P, As) in the silicon crystal changes the electrical properties of the semiconductor. Silicon atoms have four valence bonds. If a pentavalent impurity atom substitutes a silicon atom in its lattice position, four valence electrons of the impurity participate to the covalent binding, but the fifth electron can easily be released in the conduction band, leaving behind in the semiconductor bulk a positively ionised fixed atom. On the contrary, the impurities with three valence bonds capture an electron from the valence band, giving a hole for the conduction and becoming negatively ionised. This situation is schematically depicted in Fig. 2.1, where the impurity effect results in the introduction of energetic levels in the band gap. The energetic levels introduced by impurities of the third and the fifth groups are called shallow levels, because they are situated very close to the conduction band or to the valence band, respectively: in Table 2.1 are reported some values of shallow energy levels. The energy gap between the conduction (valence) band and the shallow donor (acceptor) level is so small that at room temperature all the dopants are ionised. If the doping concentration is larger than the intrinsic carrier concentration, the carrier type introduced by the doping dominates the conductivity. The free carrier concentration in a silicon crystal doped with donor atoms is  $n \approx N_D$ . The majority carriers are electrons and the material is called n-type silicon. Similarly, a silicon crystal doped by acceptor atoms is called p-type

silicon, and the concentration of free carriers (holes) is  $p \approx N_A$ .  $N_D$  and  $N_A$  are the concentrations of donor and acceptor atoms, respectively.

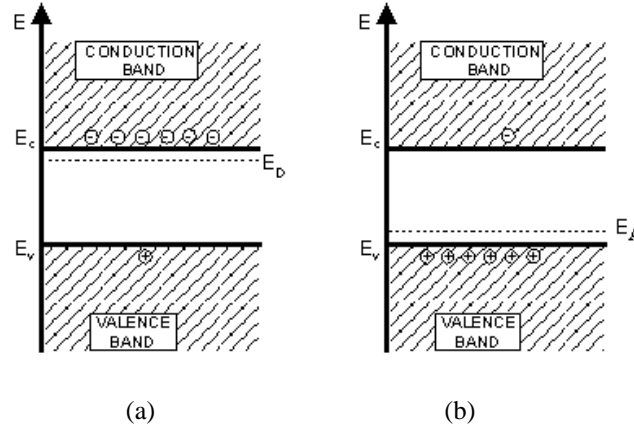


Fig. 2.1 Schematic band diagram for (a) n-type and (b) p-type semiconductor.  $E_D$  = energy level of the donor impurity;  $E_A$  = energy level of the acceptor impurity.

Atom	$E_L - E_V$ [eV]	$E_C - E_L$ [eV]	Conductivity type
Boron (B) – III group	0.045		p
Phosphorus (P) – V group		0.045	n
Arsenic (As) – V group		0.054	n

Table 2.1 Difference between the bottom of the conduction band ( $E_C$ ), the top of the valence band ( $E_V$ ) and the impurity level ( $E_L$ ) for the most important donors and acceptor in silicon.

When an n-type or p-type doping is introduced, the Fermi level must adjust itself to preserve charge neutrality. The displacement of the actual Fermi level in a doped semiconductor ( $E_F$ ) from the intrinsic position ( $E_{Fi}$ ) can be calculated as follows

$$E_F - E_{Fi} = kT \ln \left( \frac{n_0}{n_i} \right) \quad (2.5a)$$

$$E_{Fi} - E_F = kT \ln \left( \frac{p_0}{n_i} \right) \quad (2.5b)$$

where  $n_0$  and  $p_0$  are the carrier concentrations in the thermal equilibrium conditions. The Fermi level moves up in the bandgap when the impurity atoms introduce n-type carriers and down when the impurities introduce p-type carriers.

## 2.2 The p-n junction

The fundamental structure of most of the silicon detectors is the p-n junction, or silicon diode. Figure 2.2 represents the band diagram of n-type and p-type silicon separately and after the junction formation. The strong gradient of carriers across the junction causes diffusion of electrons in the p-type region and holes in the n-type region. The unbalanced fixed charges left behind by the diffusing carriers constitute the space charge region (SCR): positive ions in the  $n$  region and negative ions in the  $p$  region. A potential drop due to the space charge takes place and an electric field appears across the junction, causing a drift current in the opposite direction of the diffusion current. The equilibrium will be reached when the potential drop prevents further charge transfer across the junction. This potential is called built-in potential ( $V_{bi}$ ), and it is about 0.6 V for silicon. Very few free carriers of both signs are present in the SCR, therefore it is called the depletion region.

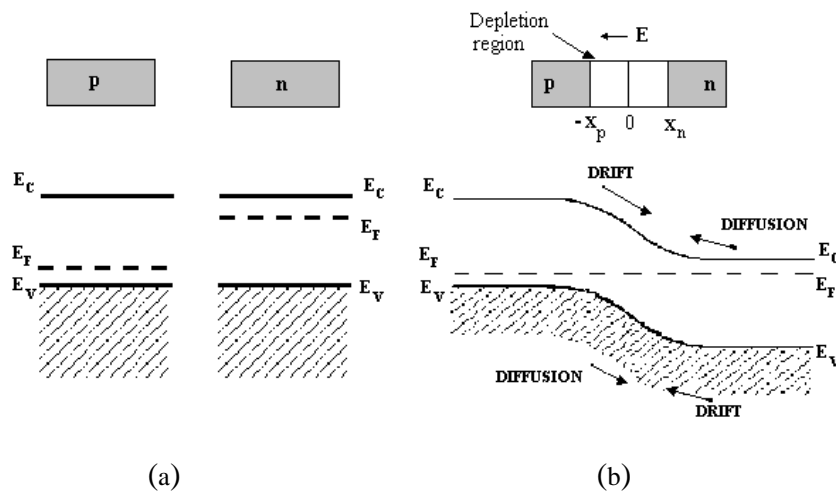


Fig. 2.2 Band diagram of (a) uniformly doped p-type and n-type silicon (b) after the junction formation.

The electric field and the potential in the depletion region can be calculated solving the one-dimensional Poisson equation

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\epsilon_r \epsilon_0} = -\frac{\rho}{\epsilon_{Si}} \quad (2.6)$$

where  $\epsilon_0$  is the permittivity of the vacuum,  $\epsilon_r$  is the silicon dielectric constant and  $\epsilon_{Si}$  is the

permittivity of silicon. The charge density  $\rho$  is given by the spatial charge and, in doped semiconductors, is about equal to the impurity concentration. In the following it will be assumed that the density of doping atoms changes sharply from the p-side ( $\rho = qN_A$ ) to the n-side ( $\rho = qN_D$ ). This is called abrupt junction. In practice, the change between the two regions occurs gradually over a finite distance. The abrupt junction is a good approximation as long as the depletion layer width is large compared to the transition depth [2.2]. This is the case of silicon detectors.

The electric field in the depletion region is

$$E = -\frac{dV}{dx} \quad (2.7)$$

The integration of eq. 2.7 with the boundary condition  $E = 0$  at the limit of the depletion region ( $x = -x_p$ ) gives

$$E = -\frac{qN_A}{\epsilon_{Si}}(x + x_p) \quad (2.8)$$

The electric field reaches the maximum value  $E_M$  at the junction, in  $x = 0$ , where

$$E_M = -\frac{qN_A}{\epsilon_{Si}}x_p \quad (2.9)$$

Similarly, in the n-type side, assuming  $E = 0$  at  $x = x_n$

$$\frac{dE}{dx} = \frac{\rho}{\epsilon_{Si}} = \frac{qN_D}{\epsilon_{Si}} \quad (2.10)$$

and

$$E = \frac{qN_D}{\epsilon_{Si}}(x - x_n) \quad (2.11)$$

The maximum electric field at the junction is

$$E_M = -\frac{qN_D}{\epsilon_{Si}}x_n \quad (2.12)$$

By comparing eq. 2.9 and 2.12, we obtain

$$N_A x_p = N_D x_n \quad (2.13)$$

If the doping density in one side is larger than the density in the other side, the junction extends deeper in the less doped side. Asymmetric junctions are often used in detector technology. We will refer as a p<sup>+</sup>-n junction when the density of doping in the p region is much larger than the

doping in the n-side. In this case, the extension of the depletion region in the p<sup>+</sup> side can be neglected.

Integrating eq.2.8 and 2.11 with the boundary condition for the potential  $V_p(0) = V_n(0) = 0$  we obtain

$$V_p(x) = \frac{qN_A}{\epsilon_{Si}} \left( \frac{x^2}{2} + x_p x \right) \quad (2.14)$$

$$V_n(x) = \frac{qN_D}{\epsilon_{Si}} \left( x_n x - \frac{x^2}{2} \right) \quad (2.15)$$

The potential of the junction is the difference between the values of the potential at the boundaries of the depleted region,  $x_n$  and  $-x_p$ . The *built-in* potential,  $V_{bi} = V_n - V_p$ , is

$$V_{bi} = \frac{q}{2\epsilon_{Si}} (x_n^2 N_D + x_p^2 N_A) \quad (2.16)$$

If  $w = x_n + x_p$  is the width of the junction, by eliminating  $x_n$  and  $x_p$  using eq. 2.13 we obtain

$$w = \left( \frac{2\epsilon_{Si} V_{bi}}{q} \right)^{\frac{1}{2}} \left[ \frac{1}{N_D} + \frac{1}{N_A} \right]^{\frac{1}{2}} \quad (2.17)$$

### Junction under external bias

When a bias of the same sign than  $V_{bi}$  is applied to the junction, the depletion region grows and the junction is called reverse biased. If the bias has the opposite sign than  $V_{bi}$ , the depletion region narrows and the junction is called forward biased. The two situations are shown in Fig 2.3. The forward bias allows the passage of current through the junction whereas the reverse bias prevents the passage of large currents. The ideal current characteristic for a junction is expressed by

$$J = J_p(x_n) + J_n(-x_p) = J_S \left( e^{\frac{qV}{k_B T}} - 1 \right) \quad (2.18)$$

$$J_S \equiv \frac{qD_p p_{n0}}{L_p} + \frac{qD_n n_{p0}}{L_n} \quad (2.19)$$

where  $D_n$  ( $D_p$ ) is the electrons (holes) diffusivity and  $L_{n,p} = (D_{n,p} \tau_{n,p})^{1/2}$  is called the diffusion length of electrons or holes. The quantity  $\tau_{n,p}$  is the carriers lifetime.  $J_S$  is called the saturation current density. Figure 2.4 shows the ideal current voltage (I-V) characteristic. In reverse bias,

the current is  $\approx J_S$  until the junction breakdown takes place and the reverse current increases dramatically.

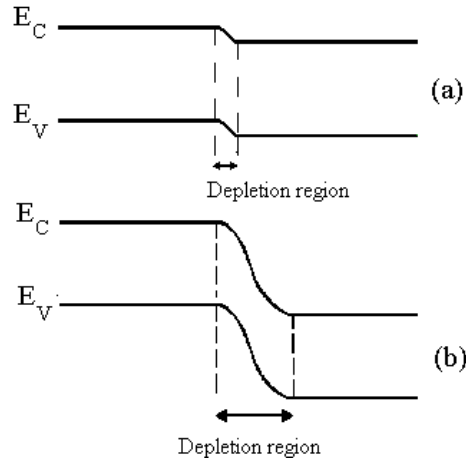


Fig. 2.3 Schematic energy band diagram of a p-n junction under external bias (a) forward bias (b) reverse bias.

Relevant departures from the ideal characteristic are found in silicon, because of the generation-recombination process. The presence of deep levels close to the middle of the band gap, due to impurities or crystal defects, always present in silicon, allows the processes schematically described in Fig. 2.5. Process (a) involves generation of an electron and a hole, and it provides carriers for the conduction. Process (b) involves recombination of an electron and a hole, and it removes a carrier from the conduction. In reverse bias, the free carrier density is poor, and the recombination process is negligible.

The generation is the dominant process and the resulting generation current contributes to the total current in a fraction proportional to the defect concentration. The reverse current  $J_R$  for a p<sup>+</sup>-n junction, where the depletion region extends mainly in the n-type side, can be expressed by

$$J_R \approx q \sqrt{\frac{D_p}{\tau_p} \frac{n_i^2}{N_D} + \frac{qn_i w}{\tau_g}} \approx \frac{qn_i w}{\tau_g} \quad (2.20)$$

The quantity  $\tau_g$  is the generation lifetime and accounts for the generation centre density, the cross section of the generation process and the energy level of the centre.

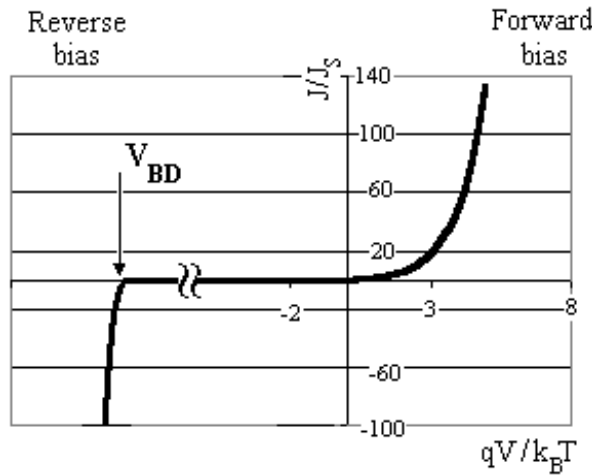


Fig. 2.4 *Ideal I-V characteristic of a silicon diode.*

In forward bias, the electron and hole densities exceed their equilibrium concentration, and the recombination process becomes efficient. The expression for the forward current,  $J_F$ , for a  $p^+n$  junction is

$$J_F \approx q \sqrt{\frac{D_p}{\tau_p} \frac{n_i^2}{N_D}} e^{\frac{qV}{k_B T}} + \frac{qn_i w}{2\tau_r} e^{\frac{qV}{2k_B T}} \quad (2.21)$$

In general, the experimental results can be represented empirically by

$$J_F \approx \exp\left(\frac{qV}{\eta k_B T}\right) \quad (2.22)$$

The factor  $\eta$  is called the ideality factor. If the ideal diffusion current dominates,  $\eta = 1$ , whereas if the recombination current dominates,  $\eta = 2$  and when both contributions are comparable,  $\eta$  has a value between 1 and 2.

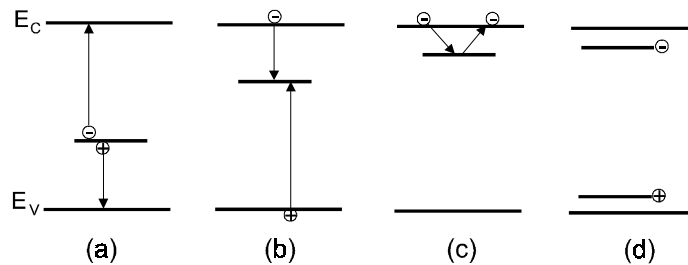


Fig. 2.5 *Processes at an intermediate defect level: (a) generation (b) recombination (c) trapping (d) compensation.*

In both, forward and reverse biases, the current is strongly dependent on the temperature. In



the present study, most of the experimental measurements have been performed with reverse biased junctions, where the generation current dominates. The reverse current dependence on the temperature can be expressed by

$$J_g \propto T^2 e^{-\frac{E_g}{2k_B T}} \quad (2.23)$$

## Breakdown

In a reverse bias situation, the breakdown is defined as the rapid increase of the current when the reverse bias goes above a certain limit ( $V_{BD}$ ), as shown in Fig. 2.4. The high current flowing in the breakdown regime makes the silicon detector unusable and could destroy the device if the bias is not rapidly decreased below  $V_{BD}$ . Therefore, it is very dangerous to operate a detector close to  $V_{BD}$  and it is important to keep  $V_{BD}$  as high as possible. The breakdown limit depends on the detector design and on the fabrication technology. Actually, electrode geometry, number and size of the guard rings, oxide quality and junction fabrication can influence  $V_{BD}$  [2.3].

The radiation damage increases the reverse leakage current and obliges to operate detectors at high voltages, increasing the chance of the occurrence of breakdown. Therefore, the detector breakdown is one of the limits to the operation of silicon detectors after irradiation. This problem of irradiated detector can be faced by design solutions or by reducing the radiation damage of the silicon itself.

## C-V characteristic of a reverse biased junction

The capacitance of a reverse biased junction is given by

$$C(V_d) = \frac{dQ}{dV} = \frac{dQ}{dx} \frac{dx}{dV} \quad (2.24)$$

If the diode is p<sup>+</sup>-n,  $N_A \gg N_D$  and the depletion region develops mainly in the n-side. This situation is called *asymmetric* or *one-sided junction*. In eq. 2.17 we can neglect the term  $1/N_A$ .

In the n-region, we define the effective doping concentration,  $N_{eff}$ , as it follows

$$N_{eff} = |N_D - N_{A,n}| \quad (2.25)$$

where  $N_{A,n}$  is the acceptor concentration in the n side region of the junction which partially compensates the dominant donor concentration.  $N_{eff}$  is related to the resistivity,  $\rho$ , of the material by

$$\rho \approx \frac{1}{q\mu N_{eff}} \quad (2.26)$$

The depth  $d$  of the depleted region is, similarly to eq. 2.17

$$d = \left( \frac{2\epsilon_{Si}V}{q} \right)^{\frac{1}{2}} \cdot \left( \frac{1}{N_{eff}} \right)^{\frac{1}{2}} \quad (2.27)$$

where  $V$  is the applied reverse voltage. The built-in voltage is neglected, because  $V \gg V_{bi}$  is assumed, which is the case in the operation of silicon detectors. The depleted region increases linearly with the square root of the bias. The proportionality constant depends on  $N_{eff}$ . Assuming a homogeneous distribution of  $N_{eff}$ , we can estimate the quantity

$$\frac{dQ}{dx} = qN_{eff}A \quad (2.28)$$

where  $A$  is the surface of the diode. Differentiating eq. 2.27, with  $x = x_n \gg x_p$ , we obtain

$$\frac{dx}{dV} = \sqrt{\frac{\epsilon_{Si}}{2qN_{eff}}} \cdot \sqrt{\frac{1}{V}} \quad (2.29)$$

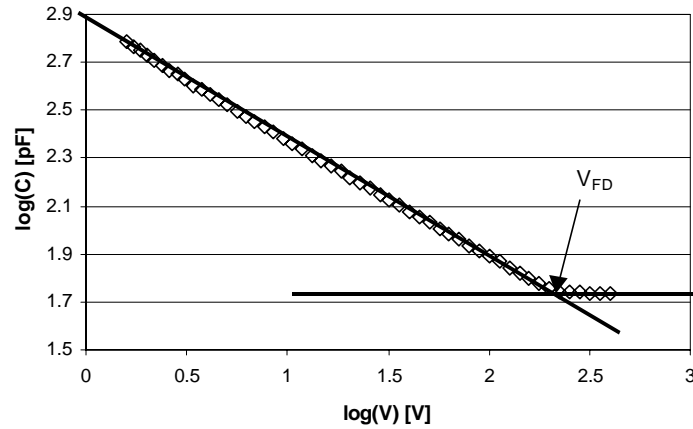


Fig. 2.6 The capacitance-voltage characteristic of a  $p^+$ -n junction.

A reverse biased diode can be assimilated to a parallel plate capacitor. The diode capacitance as a function of the applied reverse bias,  $V$ , is obtained by substitution of eq's. 2.28 and 2.29 into 2.24:

$$C(V) = \frac{\epsilon_{Si} A}{x} = A \sqrt{\frac{q \epsilon_{Si} N_{eff}}{2}} \cdot \sqrt{\frac{1}{V}} \quad (2.30)$$

Figure 2.6 illustrates the C-V curve of a one-sided junction. The capacitance decreases proportionally to the square root of the bias voltage until the depletion region extends to the entire volume (full depletion) of the diode (Fig. 2.7). The value of the bias at full depletion is called full depletion voltage ( $V_{FD}$ ). For bias voltages higher than  $V_{FD}$  the capacitance is constant

and the value,  $C_{FD}$ , corresponds to the geometrical capacitance of the diode considered as a plane plate silicon capacitor:

$$C_{FD} = \frac{\epsilon_{Si} A}{w} \quad (2.31)$$

where  $w$  is the thickness of the diode.  $N_{eff}$  can be evaluated combining eq. 2.30 and 2.31 to obtain

$$N_{eff} = \frac{2 \epsilon_{Si}}{q w^2} V_{FD} \quad (2.32)$$

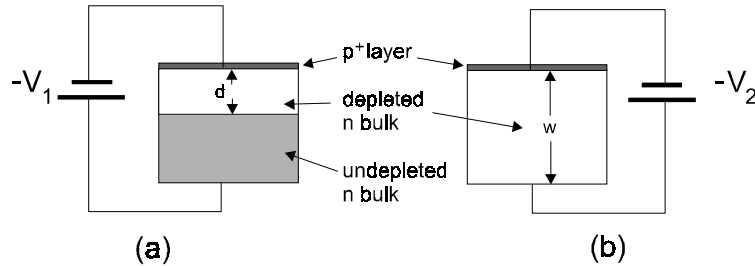


Fig. 2.7 Depletion region of a  $p^+-n$  junction: (a)  $V_1 < V_{FD}$ , (b)  $V_2 \geq V_{FD}$ .

## 2.3 Silicon mono-crystal fabrication and detector manufacturing

The silicon wafer is the fundamental structure for the device fabrication. It is a disk of single crystal silicon with a diameter ranging from 1 to 5 inches and thickness between 200 and 2000 micrometers. It can be obtained by cutting a single-crystal ingot or by silicon atom deposition on a single crystal substrate (epitaxial growing). A single-crystal silicon ingot can be manufactured by refining a polycrystalline silicon rod obtained after distillation and reduction of  $\text{SiO}_2$  (quartzite). The refinement methods, briefly described here, are the Czochralski (CZ) and Float-Zone (FZ) techniques [2.4, 2.5].

The approach to the radiation hardening of silicon detectors followed in the RD48 project consists of the engineering of the starting material by the deliberate introduction of impurities in the silicon crystal. The introduction of impurities can be performed at different stages of the wafer production: during the production of the polycrystalline silicon material, during the ingot growth before the wafer cutting, during the epitaxial growth or by diffusion in the wafer itself. For the engineering of the material tested in the present work, the impurities have been introduced during the ingot growth or by diffusion into the wafer.

### **2.3.1 Crystal growth methods**

#### **The Czochralski (CZ) method**

The starting polycrystalline silicon is placed in a fused silica ( $\text{SiO}_2$ ) crucible surrounded by the susceptor of a furnace. A rotation mechanism makes the system rotating clock-wise. All the system is in an inert atmosphere (argon or nitrogen). The silicon is heated at a temperature above its melting point. A seed-holder containing a single-crystal seed of the suitable orientation (e.g.  $\langle 111 \rangle$ ) is introduced into the melt and it is then slowly lift up. The progressive freezing at the solid-liquid interface yields the formation of a large single-crystal with the same characteristic than the seed. A typical pull rate is a few millimetres per minute. High concentrations of impurities are introduced into the melt from the crucible wall. In particular, oxygen atoms form thermal donor states when it occupies lattice substitutional sites. Oxygen becomes partially activated during the cooling of the crystal and makes impossible to achieve high resistivity with the CZ technique [2.6]. The typical resistivity of CZ wafer is  $\leq 50 \Omega \text{ cm}$ , therefore the CZ material is not suitable for the detector production, which requires high resistivity silicon. Other impurities diffuse from the crucible into the melt. The typical concentrations of the most common impurities, O and C, are  $1 \cdot 10 \cdot 10^{17}$  and  $1 \cdot 5 \cdot 10^{16}$  at.  $\text{cm}^{-3}$ , respectively.

#### **The Float Zone (FZ) method**

Purer and higher resistivity single-crystal silicon can be obtained using the FZ technique. A

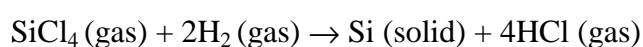
high-purity polycrystalline rod with a single-crystal seed at the bottom is held in the vertical position and rotated. A radio-frequency heater melts a small zone (few centimetres) of the rod, called *floating-zone*. Surface tension between the melting and the growing solid silicon retains the molten silicon. As the radio frequency coil moves up, single-crystal silicon freezes below the floating-zone. This process is performed in an inert atmosphere and allows the production of high resistivity and high purity material. The resistivity of the growing silicon depends on the doping atom (P,B,As) concentration in the polycrystalline material. The fluctuations of the resistivity value in a high resistivity silicon FZ wafer are  $\approx 30\text{-}40\%$ .

It is possible to introduce some impurities during the melting phase of the process, by flowing gases on the floating zone. This technique has been used for the production of single-crystal materials with addition of oxygen, nitrogen and carbon. The concentration achieved varies very much following the impurity type and the gas injection technique. Other ways to introduce impurities into the growing FZ silicon are drilling holes into the polycrystalline rod and to fill them with the required impurity (Sn, Ge, C) or soldering a single CZ crystal with high concentration of the required impurity between the seed and the silicon rod. The impurities can diffuse from the holes or from the CZ silicon into the growing single crystal during the FZ refinement.

### **The epitaxial growing**

This technique consists in the growth of a silicon layer on a single-crystal silicon substrate. The resulting grown layer is an exact crystalline extension of the substrate [2.7]. Silicon atoms are suitably released from a source over the substrate and some of them become part of the growing film. The transfer of silicon from the source to the substrate takes place via direct or indirect process. In the direct process the transfer is realised with no intermediate chemical reactions, using vacuum deposition, evaporation, sublimation or sputtering. In the indirect process, the silicon atoms are obtained by the decomposition of a silicon compound at the substrate surface. This second technique is the most widely used for the epitaxial silicon production. Examples are the hydrogen reduction of silicon tetrachloride ( $\text{SiCl}_4$ ), dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ), trichlorosilane ( $\text{SiHCl}_3$ ) and silane ( $\text{SiH}_4$ ) followed by its pyrolysis. These

techniques involve the vapour deposition of the silicon atoms released by the reactant molecules on the substrate layer in controlled condition (atmosphere, pressure, temperature, flux of the reactant...) and are called vapour phase epitaxial (VPE). The substrate is generally a CZ wafer 600  $\mu\text{m}$  thick, for mechanical strength reason. The substrates are introduced in a graphite susceptor of a furnace. The temperature of the silicon wafer during the process depends on the specific reaction involved and ranges from 1000  $^{\circ}\text{C}$  to more than 1200  $^{\circ}\text{C}$ . The overall reaction of the most used reactant, the silicon tetrachloride, that results in the growth of silicon layer is:



An additional competing reaction takes place reducing the solid silicon growth



The ratio between the two competing reactions depends on the concentration of silicon tetrachloride. Suitable concentrations of this gas are used to optimise the solid silicon growing rate. The dopant is introduced at the same time as the silicon tetrachloride during the epitaxial growth. Gaseous diborane ( $\text{B}_2\text{H}_6$ ) is used as p-type dopant, while phosphine ( $\text{PH}_3$ ) or arsine ( $\text{AsH}_3$ ) are used as n-type dopants. The impurity doping atoms are incorporated into the lattice while the layer is growing. It is possible to control the doping level with  $\pm 10\%$  accuracy. The growing rate can be controlled: the epitaxial materials used in this thesis have been grown at a rate of 0.5 or 1  $\mu\text{m}/\text{min}$ . The thickness of the epitaxial layers of wafers examined in this work ranges between 100 to 200  $\mu\text{m}$ . Thicker epitaxial wafers can hardly be produced.

During the crystal growing, impurities diffusing from the Czochralski (CZ) substrate are incorporated into the epitaxial layer. The oxygen and carbon concentrations in the substrate are often of the order of  $1 \cdot 10^{18} \text{ cm}^{-3}$  and  $1 \cdot 5 \cdot 10^{16} \text{ cm}^{-3}$ , respectively. Subsequently, it is possible to find higher concentrations of these impurities into the epitaxial wafers than into the cleaner Float-Zone (FZ) processed ones.

### **The silicon wafer**

The ingots produced with the FZ or the CZ techniques are cut into thin slices (400 – 1000  $\mu\text{m}$ ), then lapped and polished on both faces, in order to obtain final silicon wafers with the suitable

thickness and low damaged surfaces. The polishing of the surfaces is necessary for the alignment of the masks used for the photolithography stages during the detector processing. The total thickness of an epitaxial wafer is the thickness of the high resistivity epitaxial layer (100-200  $\mu\text{m}$ ) plus the low resistivity CZ substrate (600  $\mu\text{m}$ ). The thickness of the FZ wafers used for detector applications ranges between 200  $\mu\text{m}$  to 300  $\mu\text{m}$ . The diameter of the wafers could be two, three or four inches.

One disadvantage of the epitaxial wafers is the thickness of the substrate, which constitute a non-sensitive layer in the final detector. The LHC detectors require as small as possible amount of material into the inner part. The possible polishing of the epitaxial substrate to make it thinner is a difficult and expensive step in the production. Moreover, the suitable thickness of the sensitive layer to optimise the signal over noise ratio is  $\approx 300 \mu\text{m}$ . Therefore, the epitaxial silicon does not represent an attractive material for the LHC inner detectors, but can provide information about the influence of the included impurities (O, C) on the silicon radiation hardness.

### **2.3.2 Detector manufacturing**

The radiation hardening of silicon detectors can be approached through different ways. The detector design (electrode geometry, number of guard-rings, optimisation for under-depletion operation...) can improve the detector operation after its exposition to high fluence. This approach to the radiation hardening requires device simulation tools and the manufacturing and test of quite sophisticated silicon detectors. The study of the silicon bulk properties, on the contrary, can be performed using the simplest silicon detector: the single pad diode. In the present study, 25-100  $\text{mm}^2$  diodes have been used. They have been manufactured from silicon wafers using two different techniques: planar or mesa technologies (see below).

The planar technology applied for the production of simple diodes is essentially the same as used for the production of the more sophisticated high resolution segmented detectors conceived for high energy physics experiments (pixel detectors, micro-strips,...). The mesa process is a faster and cheaper technique compared to the planar one, and therefore has been used with the purpose to study new silicon materials with shorter production time and low cost.

As a fact, we have found that the diode manufacturing technique affects the radiation hardness properties of the detectors.

### The planar detector processing

The silicon devices are manufactured by successive placements of layers or patterns of insulators, doping and metallisation contacts. Masks or photomasks are used to define the geometry of the different placements. Fig 2.8 shows the CERN2 mask-set, produced for RD48 by CANBERRA [2.9.] and used by CANBERRA and SINTEF [2.10] for diode production. The masks are used to transfer the pattern onto the silicon. Several masks and then process steps are needed to realise complex structures. A mask contains the pattern for a layer of the device. It is generally a glass or quartz plate covered by a thin film of chrome or other opaque film. A thin layer of photoresist is deposited on the chrome. The photoresist is a material sensitive to the radiation (generally U-V light). If it is partially exposed to the radiation, the exposed part can be etched out after development of the film. The remaining photoresist covers partially the chrome layer, reproducing the required pattern. An etching of the chrome is performed and the remaining photoresist prevents the chrome etching of the covered parts: in this way, it is possible to reproduce the required pattern on the chrome coating the plate.

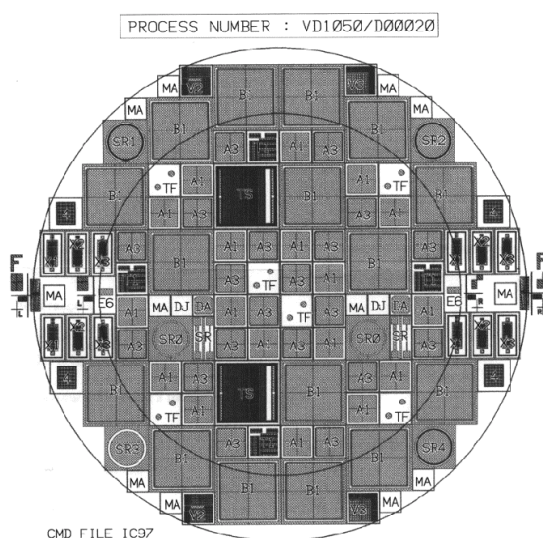


Fig. 2.8 CERN2 mask for planar device production. This mask is adapted to process 3” or 4” wafers (internal and external circles respectively).



A photolithographic process transfers the pattern from the mask to the surface layer of the wafer. The surface layer can be oxide, metal or silicon, depending on the step of the device fabrication. The first step of the planar process is oxidation and the first mask is designed to open windows into the oxide layer. For this purpose, a film of photoresist is deposited on the oxide. The photoresist is illuminated through the mask and then developed to allow the chemical etching of the illuminated part. The pattern is then transferred on the photoresist covering the oxide. A chemical or plasma etching is performed on the wafer, to remove the oxide from the region not protected by the photoresist. The remaining photoresist is removed with a process called stripping. The diffusion or the implantation of the junction and ohmic contact patterns is realised through the oxide windows on the wafer. The electrical contacts are insured by metallisation. The metal deposition is obtained by vapour deposition or sputtering. Figure 2.9 shows the main steps of the planar process. Each step of this process requires a specific mask. The planar process is then a complex and expensive technology that allows the creation of sophisticated structures on a silicon wafer.

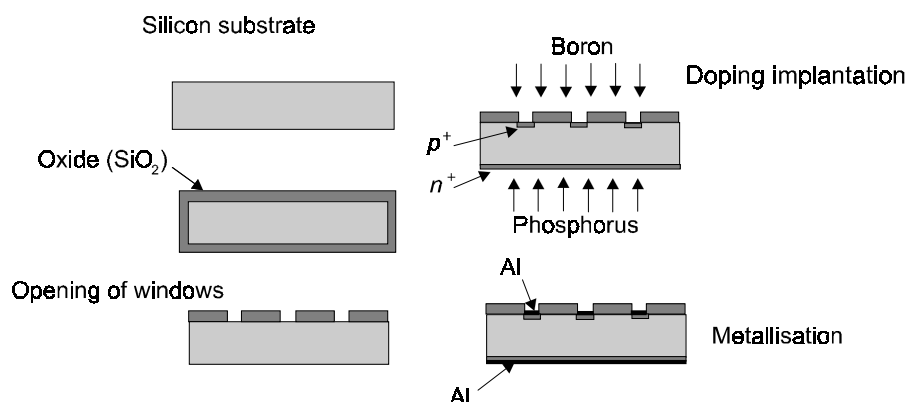


Fig. 2.9 Basic steps for the planar fabrication of a  $p^+-n-n^+$  detector.

### The mesa process.

The mesa process, described schematically in Fig.2.10, is a technique used for the production of single pad  $p^+-n-n^+$  diodes, which does not require oxidation or masking, and therefore is considerably simpler and cheaper than the planar process [2.11].

The junction and the ohmic contact of mesa diodes are realised with the simultaneous diffusion

at 1200 °C for three hours of boron and phosphorus, released by a paper impregnated of a B or P compound. The wafers are arranged in a sandwich structure in special SiO<sub>2</sub> holders, pressed by thick silicon disks on the top of the pile and then put in the furnace for the diffusion. After the diffusion, the metallic contact is realised by chemical deposition of gold on a coat of nickel previously deposited on the wafer.

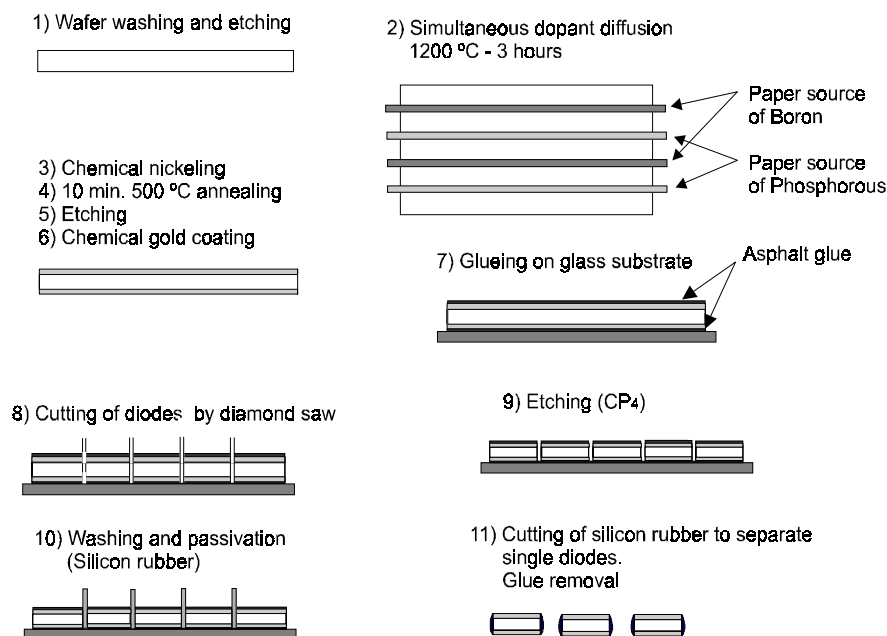


Fig. 2.10 Basic steps for the mesa fabrication of diodes.

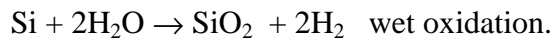
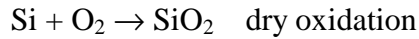
The fast diffusion of gold [2.7] in silicon introduces deep acceptor levels in the silicon band gap, resulting in a modification of the original  $N_{eff}$  [2.12, 2.13], in a reduction of the carrier lifetime and in an increase of the leakage current. The nickel coat prevents the diffusion of gold in silicon.

The final detector is a basic  $p^+ - n - n^+$  structure. The lack of guard-ring and the extension of the junction area to the device edge result in large surface-related leakage currents.

### Oxidation

The first step of the planar process is the oxidation of the silicon wafer to protect it during some production steps and to insulate the electric contacts (e.g. interstrip, guard ring or pixel

insulation) of the final detector. The oxide is grown by a chemical reaction between oxygen and silicon. The silicon wafers are placed inside a quartz tube into a furnace. A flux of pure oxygen gas or water vapour is provided into the tube. The process is called dry oxidation for pure oxygen and wet oxidation for water stream. The two possible reactions are:



The oxidation reaction takes place at the Si-SiO<sub>2</sub> interface, and the growing rate depends on the diffusion of oxygen in the silicon dioxide layer already present. The temperature of the processes is between 900 to 1200 °C and the oxidation time is of the order of hours. The wet oxidation is faster, but the choice of the oxide growth technique and of the parameters of the diffusion (temperature and purity of the gas atmosphere) is important in order to determine the quality of the oxide. Atmospheres containing nitrogen or chlorine are used to slow down the oxidation rate or to influence the oxide quality. Some ions can be trapped into the oxide layer, leaving it charged. Generally the oxide layer becomes positively charged. An excess of trapped charge at the Si-SiO<sub>2</sub> interface states influences negatively the detector performance, causing for example larger leakage currents or reducing the value of the breakdown voltage.

## 2.4 Operation of silicon detectors

This section describes the operation of silicon diodes as particle detectors. The principle is that a depleted diode is able to collect the charge deposited by an ionising particle. A current signal is induced by the charge moving inside the detector. The signal is proportional to the charge released by the ionisation caused by the passage of the particle through the detector.

Some departures of a real device from the ideal behaviour described previously are discussed. Furthermore, the charge collection properties of silicon detectors excited by various types of ionising radiation will be examined.

### 2.4.1 Biasing features

The basic silicon detector is a diode operated with a reverse bias to achieve full depletion. For a p<sup>+</sup>-n-n<sup>+</sup> detector, the reverse bias is applied by a positive voltage to the ohmic contact side (n<sup>+</sup>)

or a negative one to the junction side ( $p^+$ ). A protection resistor is in series between the biased contact of the detector and the power supply and an RC network connects the other contact to the ground. The read-out is performed through an AC coupling to charge or current amplifiers. Appendix A illustrates various set-ups used in this work. The development of the depleted volume as a function of the reverse bias in an ideal diode has been described in §2.2. Some departures from the ideal situation found in real devices are introduced below. They affect the electrical measurements (C-V, I-V) used to characterise the detector properties.

### Lateral extension of the depletion region

The surface of a  $p^+$ -n diode is defined by the area of the  $p^+$  contact. This surface does not coincide with the surface of the device (Fig. 2.11). The bulk of the diode extends laterally as regards to the normal projection of the  $p^+$  contact. In planar diodes, the structure includes the guard-ring (G-R) implants and some extension of the bulk externally to them. As a consequence of this structure, the depleted volume can extend laterally to the volume underneath the junction surface.

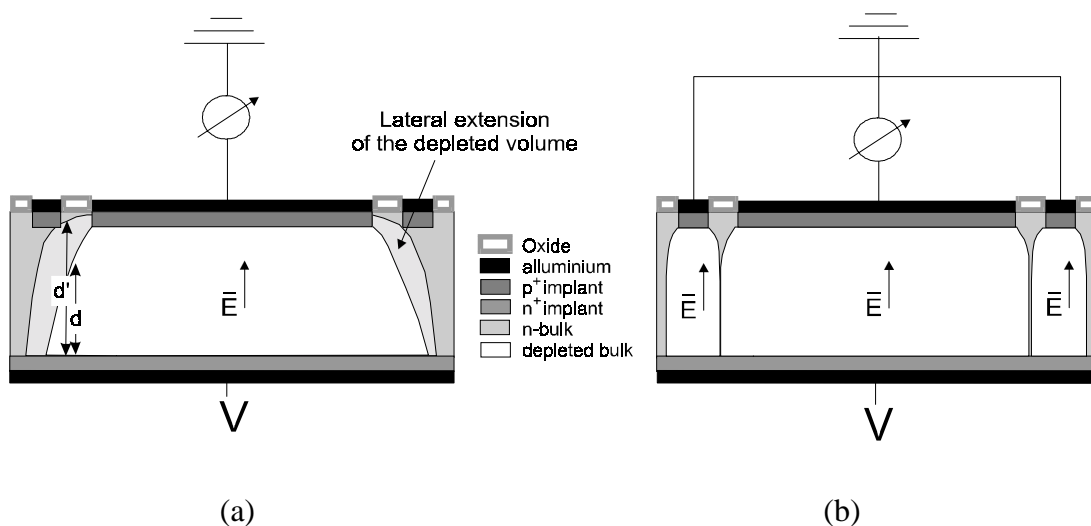


Fig. 2.11 Effect of the guard ring (G-R) contacting on the delimitation on the electric field region (a) G-R floating (b) G-R biased.

The amplitude of this extension is different whether the G-R is biased or unbiased. Figure 2.11(b) illustrates the effectiveness of the G-R on the settlement of the depletion volume (and the electric field region). Measurements of the field extension over the junction area have been performed using the micro-beam technique [2.14] and revealed that the field extension with the G-R contacted was  $\approx 1\%$  and five times larger when the G-R was kept floating.

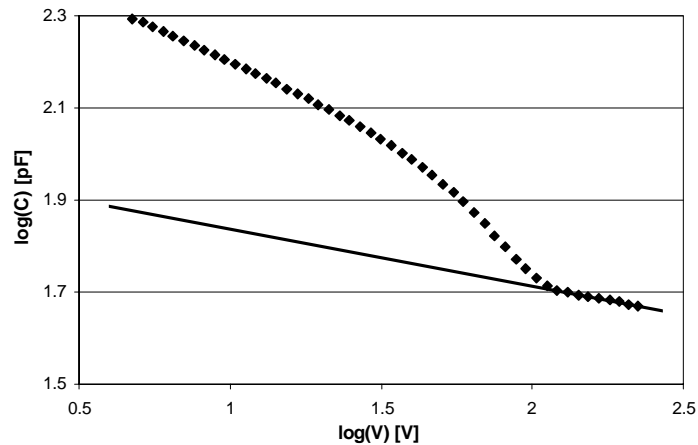


Fig. 2.12 *C-V characteristic of an irradiated planar diode. The decrease of the capacitance above full depletion is due to the lateral extension of the depleted volume.*

The lateral extension of the depleted volume can explain the decrease of the value of the capacitance for bias voltages above full depletion. In fact, the measured capacitance is sometimes found to decrease slightly above full depletion and to reach lower values than the geometrical capacitance. The depleted volume, above full depletion, extends laterally and also expands as a bulb. The increase of the effective surface of the depleted region results in an increase of the capacitance, according to eq. 2.31, but the expansion of the depleted volume towards the edge of the detector reduces the contribution of the external region to the capacitance value. Actually, the increase of the thickness of the outer depleted region ( $d' > d$  for  $V' > V > V_{FD}$ ) finally results in the decrease of the measured capacitance. Figure 2.12 shows this effect in an irradiated planar diode. A similarly irradiated mesa diode does not exhibit the same decrease, because the junction surface extends almost till the detector edges (Fig. 2.10) and a limited lateral extension can take place.

## Extra current sources

In § 2.2 it was emphasised that the current of a reverse biased diode is dominated by the generation processes in the bulk. However, various sources can cause extra current flowing through the edges of the device. Humidity or moisture on the oxide around the diode or the guard-ring (G-R) contact could conduct the bias over the oxide layer. The electrons of the neutral semiconductor are repelled and a depleted channel appears, which can inject free carriers, generated by imperfections at the edge of the device, into the semiconductor active region. Moreover, minority carriers can be injected into the depleted volume from the dangling bonds. Sawing cracks can reach the depleted region and inject charge carriers, especially in mesa diodes where the junction area goes close to the device edge, or in irradiated planar diodes with floating G-R. Local peak of the electric field, due to irregularity in the junction or to local fluctuations in the doping, can cause avalanche breakdown. This could be an explanation of the so-called soft breakdown often found in irradiated devices [2.15].

### 2.4.2 Particle detection

The operation of a fully depleted silicon diode as a particle detector relies on its ability to collect the charge generated by ionisation. The passage of an ionising particle creates electron-hole (e-h) pairs, which separate moving in the detector electric field. The absence of free carriers avoids recombination processes of the generated charge. The collection of holes or electrons appears as a current pulse, the integration over time of which equals the total charge deposited in silicon. The time needed to detect the whole signal depends on the drift length and on the strength of the electric field. The LHC interaction rate imposes very low collection time, which can go as low as 10 ns. The average energy necessary to create an e-h pair in silicon is 3.6eV. The number of created pairs is proportional to the energy lost by the ionising particle in the detector. The energy loss,  $dE/dx$ , by charged ionising particles is given by the Bethe-Bloch equation [2.17] and for a given material depends only on the particle's charge, mass and momentum. Above a given momentum, the energy loss, expressed in  $\text{MeV g}^{-1} \text{cm}^2$ , reaches a minimum independently on the medium. These particles are called minimum ionising particles (MIPs). MIPs traverse completely silicon detectors losing only a fraction of their energy,

which is uniformly distributed along the particle track. The total energy deposited is therefore proportional to the length of the particle path in the silicon detector, thus to the thickness of the sensitive volume of the detector.

The most suitable thickness for a silicon detector depends on various parameters. The signal induced by an ionising particle appears as a current pulse on top of the DC leakage current of the detector, which constitutes a noise. Other sources of noise come from the electronic read-out network. Safe operation of detectors requires a good signal over noise (S/N) ratio, in order to allow a good discrimination of the signal from the ambient variation of the current. Thick silicon detectors allow highest total charge deposition by MIPs. The noise is also associated to the detector capacitance, namely low capacitance correspond to lowest noise. This is another argument favourable to the use of thick detector.

On the other hand, the detectors are operated in over-depleted mode, to allow total and fast charge collection.  $V_{FD}$  is proportional to the square root of the detector thickness; therefore thicker detectors require higher bias voltages, which results in the increase of the leakage current. The leakage current itself is proportional to the volume of the detector. Also, the smallest amount of materials is requested in the inner region of the LHC experiments, in order to avoid multiple scattering from the particle emerging from the interactions.

A good compromise is reached using 250-300  $\mu\text{m}$  thick silicon detectors.

High resistivity silicon is required to keep a low value of the full depletion voltage. The radiation damage influences  $V_{FD}$  and the leakage current, making these parameters depending on the fluence. The optimal choice of the silicon should therefore take into account the changes foreseen over the planned operation time of the detectors.

## **Sources of noise**

Noise can be described as the variation of the ambient signal from a detector when there is no ionisation from a traversing particle. The noise limits the ability to detect the particle induced signal. It can be originated by the detector, by the biasing source and by the read-out electronic network. Sources of noise attributable to the detector are the fluctuation in the bulk generated leakage current (shot noise), fluctuation of the surface leakage current and Johnson noise associated with the series resistance or poor electrical contact to the detector. The leakage

current contribution to the noise is the most important source from the detector.

The leakage current is found to increase by many orders of magnitude under irradiation, then reducing sensitively the S/N ratio and making problematic the particle detection for heavily irradiated detectors [2.18].