Detectors for sLHC

G. Casse
University of Liverpool Group
6th December 2007

- Proposed Tracker Layout and Simulations (Radiation and Occupancy)
- Sensor and FE Electronics R&D
- Microstrip Module and Engineering Concepts
- Power, DCS, Opto-electronics, Services, Cooling, …
- Conclusions

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- **Proposed Tracker Layout and Simulations (Radiation and Occupancy)**
- **Sensor and FE Electronics R&D**
- **Micro-strip Module and Engineering Concepts**
- **Power, DCS, Read-out, Services, Cooling, …**
- **Conclusions**

The European strategy for particle physics

http://council-strategygroup.web.cern.ch/council-strategygroup/

"The LHC will be the energy frontier machine for the foreseeable future, maintaining European leadership in the field; *the highest priority is to fully exploit the physics potential of the LHC, resources for completion of the initial programme have to be secured such that machine and experiments can operate optimally at their design performance*. A subsequent major luminosity upgrade (SLHC), motivated by physics results and operation experience, will be enabled by focussed R&D; *to this end*, ***R&D for machine and detectors has to be vigorously pursued now and centrally organized towards a luminosity upgrade by around 2015***."

Why Discuss Upgrading the LHC Already?

Because we have to start the R&D now

Trigger Electronics:

- Most front-end electronics can probably stay but need faster clock speed and deeper pipelines
- Extensions to trigger capability required
- Need to maintain L1 output rate (more data per event)
  - Must upgrade detector backend electronics
    - increase bandwidth to deal with more data per event
  - Modify trigger algorithms to deal with high occupancy (and increase thresholds)

L-Ar:

- Performance degradation due to high rates in EndCap.
  (High ionisation gives big voltage drops, electronic is inaccessible, L-Ar boiling!)

TileCal:

- Some radiation damage of scintillators
- Challenging calibration with strong increase in pile-up

Muon systems:

- Degradation in performance due to high rates, in particular in the forward regions:
  - Will need additional shielding for forward region
  - May need beryllium beampipe
  - Aging/radiation damage needs confirmation for SLHC operation
- Huge expense and disruption if chambers need replacement

Inner Detector tracking systems:

- **The entire Inner Detector will have to be rebuilt**

ATLAS Inner Detector Replacement

To keep ATLAS running more than 10 years the inner tracker will have to go ...
(Current tracker designed to survive up to 730 fb^{-1} ≈ 10Mrad in strip detectors)

For the luminosity-upgrade the new tracker will have to cope with:

- **much higher occupancy levels**
- **much higher dose rates**

To build a new tracker for 2015, major R&D programme already needed.

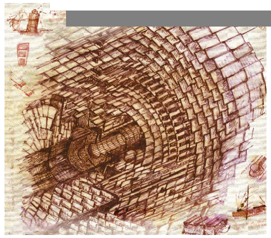
Timescales:

- **R&D leading into a full tracker Technical Design Report (TDR) in 2010**
- **Construction phase to start immediately TDR completed and approved.**

The intermediate radius barrels are expected to consist of modules arranged in rows with common cooling, power, clocking and cooling.

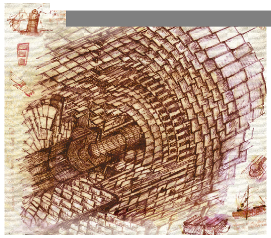
The TDR will require prototype super-modules/staves (complete module rows as an integrated structure) to be assembled and fully evaluated

All components will need to demonstrate unprecedented radiation hardness



The challenge…

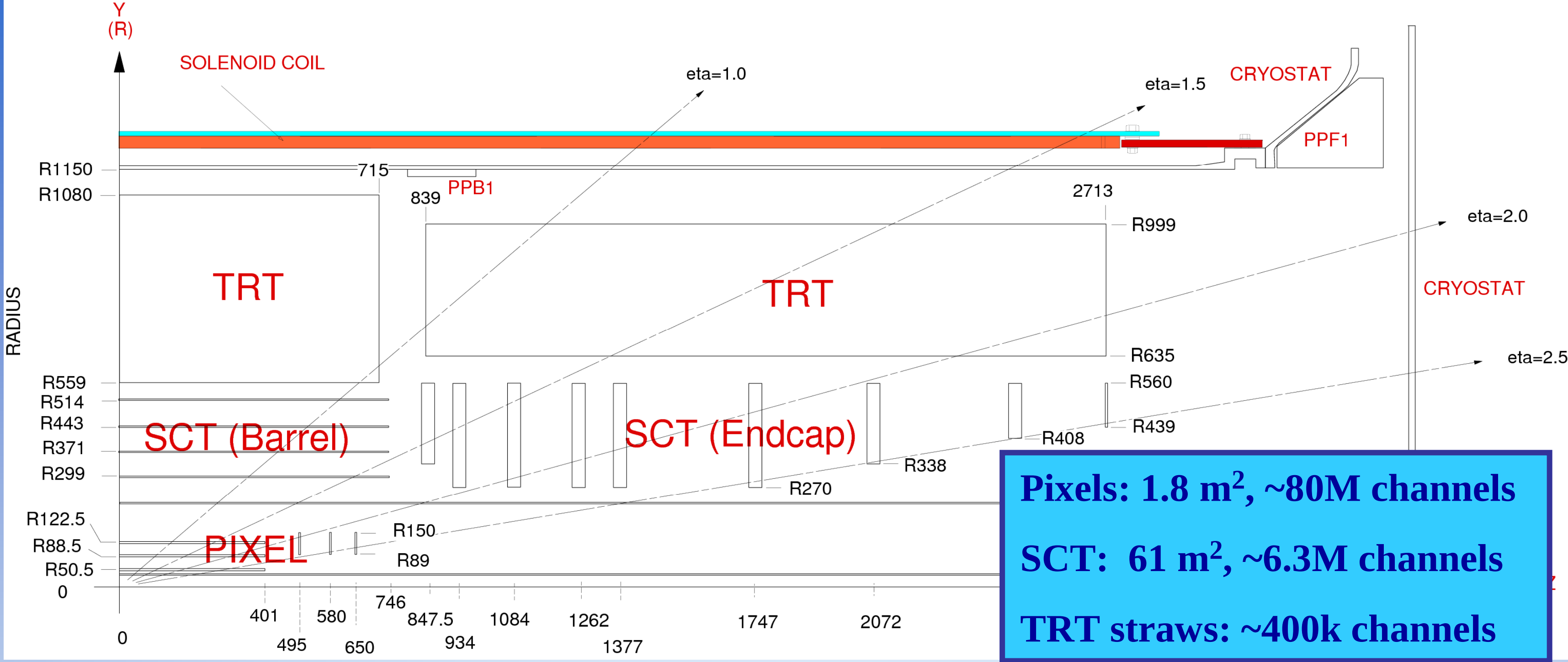
- **Build a replacement tracker for $\mathcal{L} = 10^{35}$ cm^{-2}.s^{-1} with equal or better performance, AND L1 Trigger Capability**
- **To do so, solve several very difficult problems**
  - **deliver power - probably requiring greater currents**
  - **develop sensors to tolerate radiation fluences ~10x larger than LHC**
  - **construct readout systems which can also contribute to the L1 trigger using tracker data**
  - **…and so on…**
- **It is probably as difficult a challenge as the original LHC detectors were in 1990**
  - **or possibly harder…**



Planning an Upgrade Project

- **To define the project scope we need (to iterate to establish)**
  - …some idea of timescale
  - …assessment of resources expected to be available, and those needed
    - Including - importantly- likely effort
    - with time profile
- **Planning assumption: ~10 years - from now - to operational upgraded tracker, with possible breakdown:**
  - 5 years R&D
  - 2 years Qualification
  - 3 years Construction
  - 6 months Installation and Ready for Commissioning
- **NB experience tells us that system approach and attention to QA are important considerations from a very early stage**

Current ATLAS Inner Tracker Layout

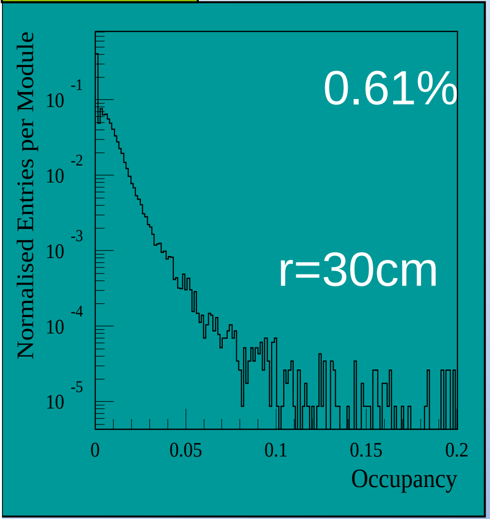


Pixels: 1.8 m^2, ~80M channels

SCT: 61 m^2, ~6.3M channels

TRT straws: ~400k channels

ID TDR



Mean Occupancy in Innermost Layer of Current SCT

Pixels (50 μm × 400 μm): 3 barrels, 2×3 disks 5cm < r < 15cm

- Pattern recognition in high occupancy region
- Impact parameter resolution (in 3d)

Radiation hard technology: n$^+$-in-n Silicon technology, operated at -6°C

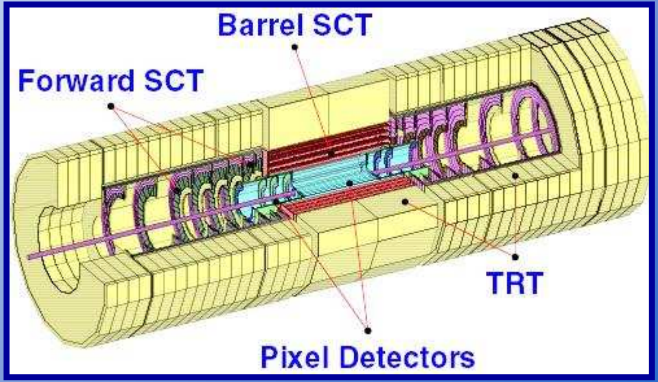
Strips (80 μm × 12 cm) (small stereo angle): “SCT” 4 barrels, 2×9 disks

- pattern recognition 30cm < r < 51cm
- momentum resolution

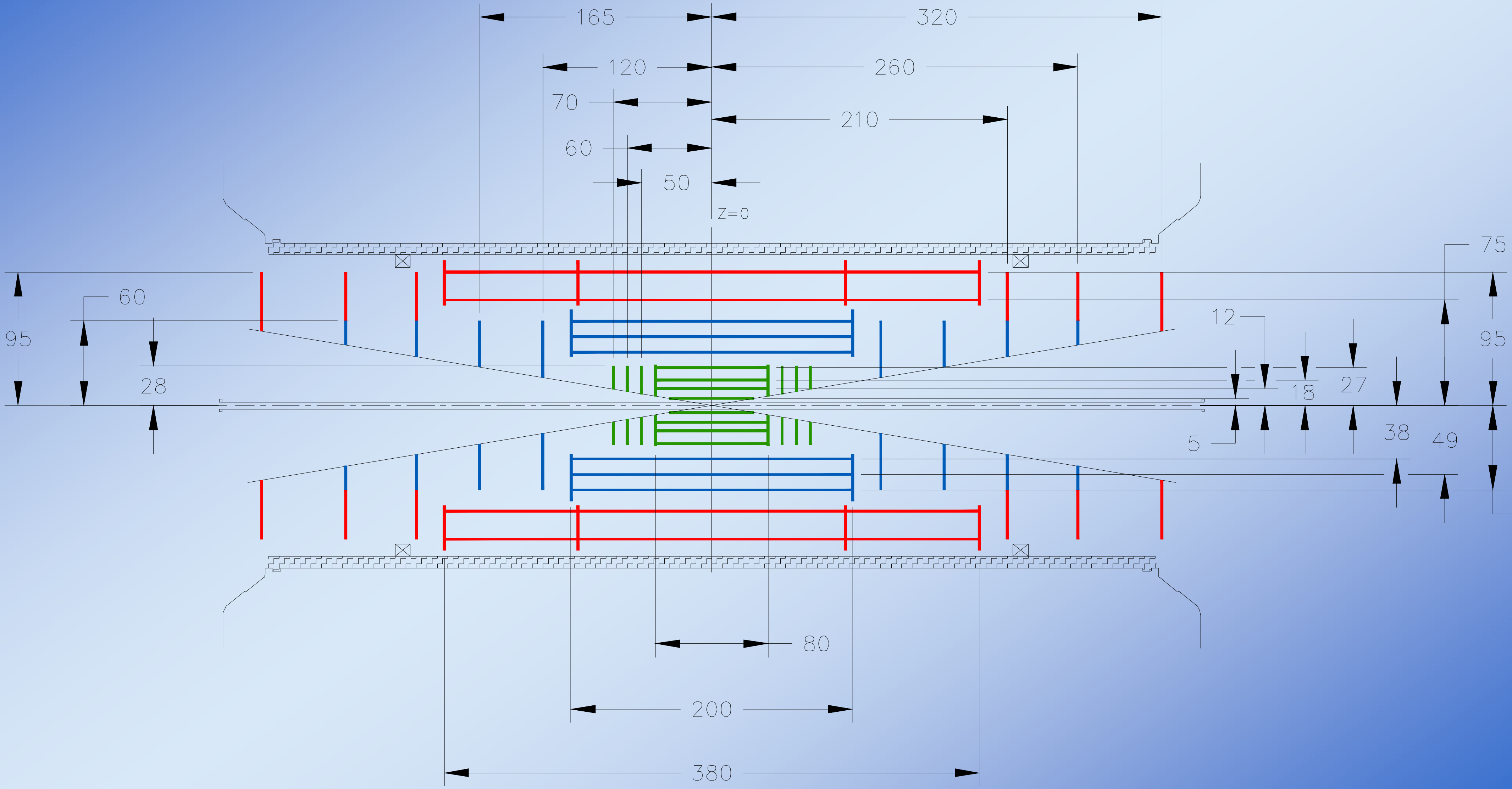
p-strips in n-type silicon, operated at -7°C

TRT 4mm diameter straw drift tubes: barrel + wheels 55cm < r < 105cm

- Additional pattern recognition by having many hits (~36)
- Standalone electron id. from transition radiation



Proposed Upgrade Layout

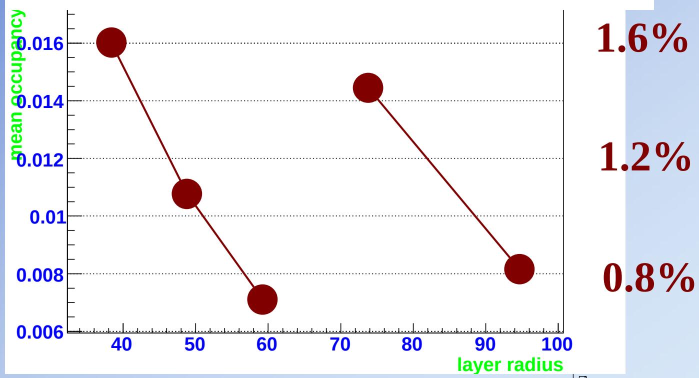


New SLHC Layout Implications

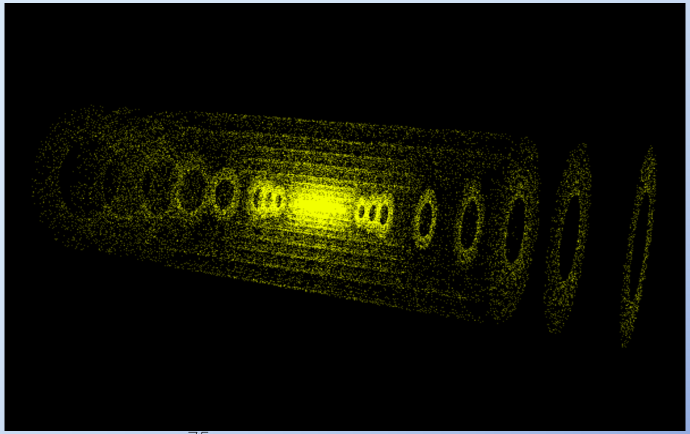
Strawman 4+3+2

Pixels:	r=5cm, 12cm, 18cm, 27cm	z=±40cm
Short (2.4 cm) μ-strips (stereo layers):	r=38cm, 49cm, 60cm	z=±100cm
Long (9.6 cm) μ-strips (stereo layers):	r=75cm, 95cm	z=±190cm

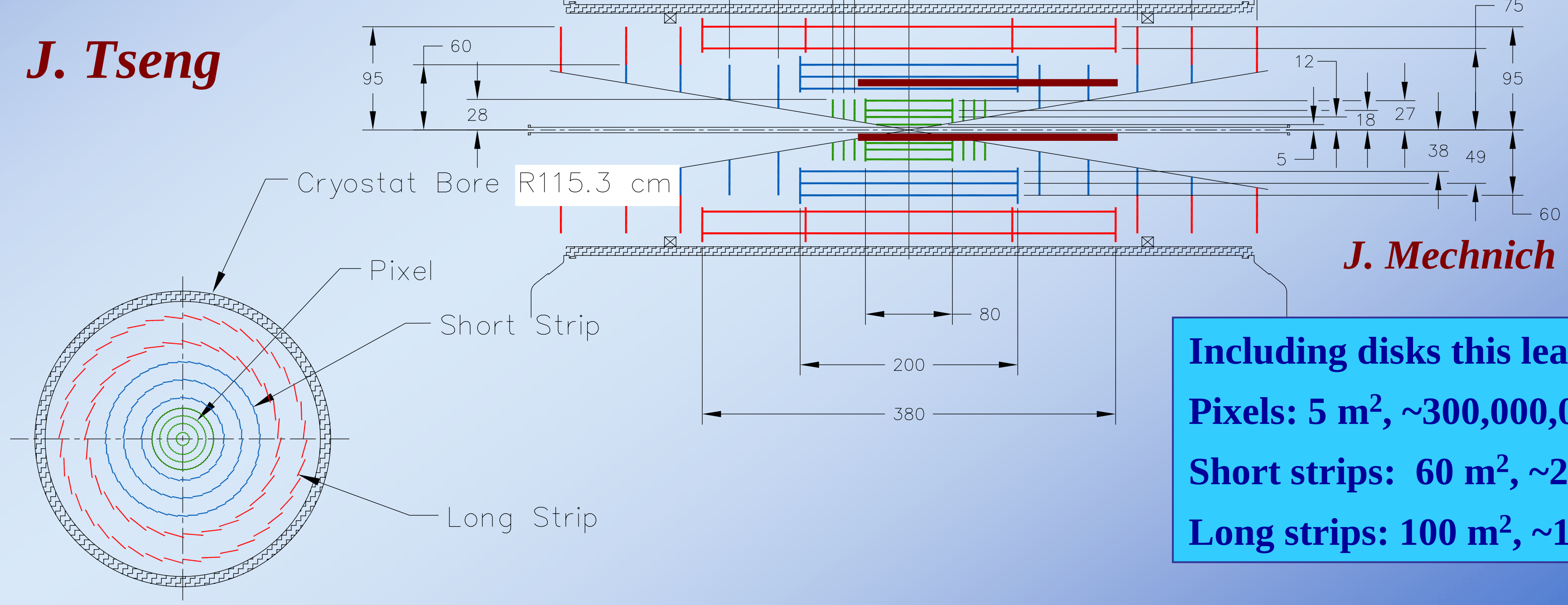
Short and Long Strip Occupancy

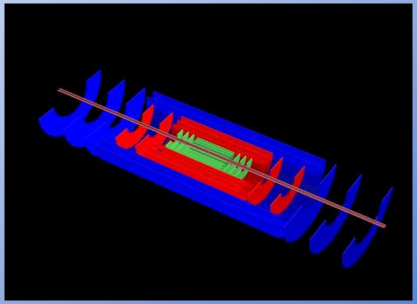


Only LO MC (Pythia) . May need to include ×2 safety factor?



J. Tseng





J. Mechnich

Including disks this leads to:

Pixels: 5 m^2, ~300,000,000 channels

Short strips: 60 m^2, ~28,000,000 channels

Long strips: 100 m^2, ~15,000,000 channels

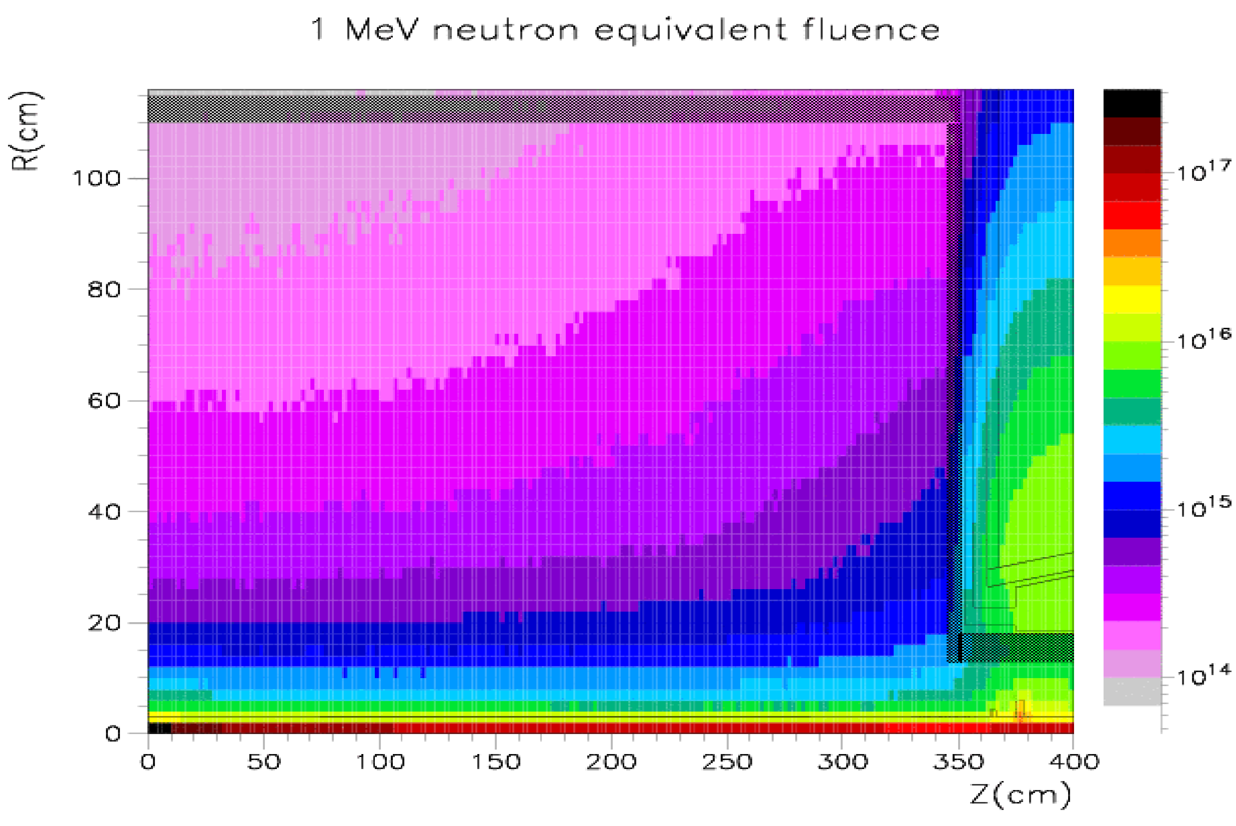
Radiation Levels

- **With safety factor of two, need pixel b-layer to survive up to $10^{16} n_{eq}/cm^2$**
- **Short microstrip layers to withstand $9 \times 10^{14} n_{eq}/cm^2$ (50% neutrons)**
- **Outer layers up to $4 \times 10^{14} n_{eq}/cm^2$ (and mostly neutrons)**

→ **Issues of thermal management and shot noise. Silicon looks to need to be at ~ -25°C (depending on details of module design).**

→ **High levels of activation will require careful consideration for access and maintenance.**

Issues of coolant temperature, module design, sensor geometry, radiation length, etc etc all heavily interdependent.



Quarter slice through ATLAS inner tracker Region, with 5cm moderator lining calorimeters. Fluences obtained using FLUKA2006, assuming an integrated luminosity of 3000fb^{-1}.

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B-layer: Replacement → Upgrade

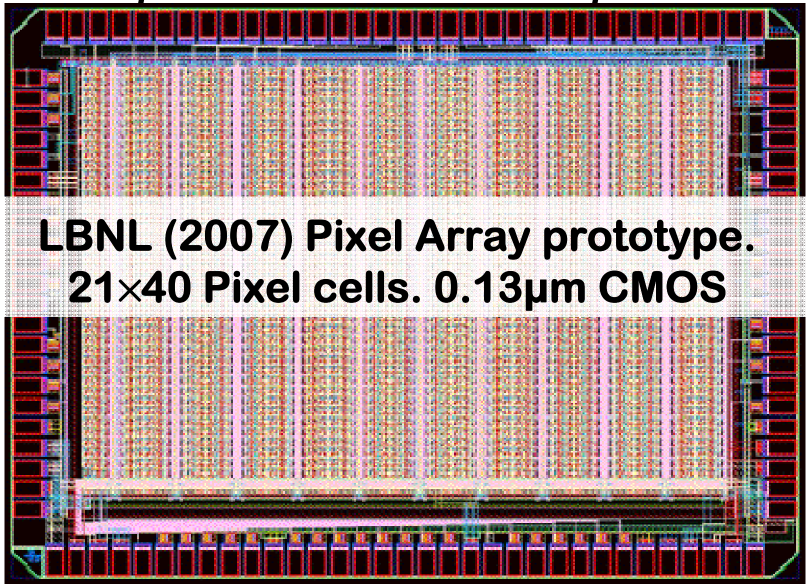
- *ATLAS considers to have a B-layer replacement after ~3 year of integrated full LHC luminosity **(2012)** and replace completely the Inner Tracker with a fully silicon version for SLHC (2016).*

- *The <u>B-layer replacement</u> can be seen as an intermediate step towards the full upgrade. Performance improvements for the detector (here some issues more related to FE chip):*
  - **Reduce radius** → Improve radiation hardness (→ 3D sensors, or possibly, thin planar detectors, diamond, gas, …?)
  - **Reduce pixel cell size and architecture related dead time** (→ deign FE for higher luminosity, use 0.13 µm 8 metal CMOS)
  - **Reduce material budget** of the b-layer (~3% X_0 → 2.0÷2.5% X_0)
  - **increase the module live fraction** (→ increase chip size, > 12×14 mm^2) possibly use “active edge” technology for sensor.
  - **Use faster R/O links**, move MCC at the end of stave

- *The <u>B-layer for the upgrade</u> will need radiation hardness ($10^{15} \rightarrow 10^{16}\ n_{eq}/cm^2$) and cope with detector occupancies up to (×15)*

New Pixel FE-ASIC Design

- *Design of a new Front-End chip (FE-I4) is going on as a Collaborative Work of 5 Laboratories: Bonn, CPPM, Genova, LBNL, Nikhef*
- *FE-I4 tentative schedule*
  - 9/2007: Architecture definition
  - 10/2007: Footprint frozen
  - 01/2008: Initial Design review
  - 12/2008: Final Design review
- *Some prototype silicon made of small blocks and analog part of the pixel cell in 0.13 µm.*

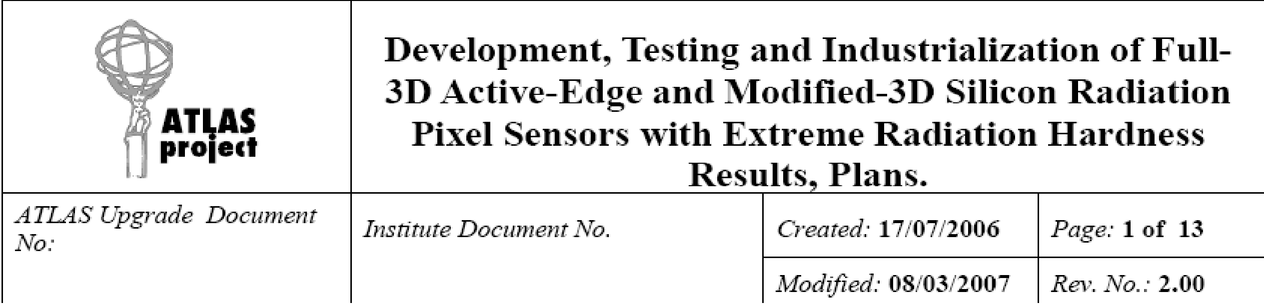


LBNL (2007) Pixel Array prototype. 21×40 Pixel cells. 0.13µm CMOS

Main Parameter	*Value*	*Unit*
Pixel size	50 x 250	μm^2
Input	DC-coupled negative polarity	
Normal pixel input capacitance range	300Ö500	fF
In-time threshold with 20ns gate	4000	e
Two-hit time resolution	400	ns
DC leakage current tolerance	100	nA
Single channel ENC sigma (400fF)	300	e
Tuned threshold dispersion	100	e
Analog supply current/pixel @400fF	10	µA
Radiation tolerance	200	MRad
Acquisition mode	Data driven with time stamp	
Time stamp precision	8	bits
Single chip data output rate	160	Mb/s

FE-I4 (B-layer Replacement) Specifications: main parameters

3D silicon sensors



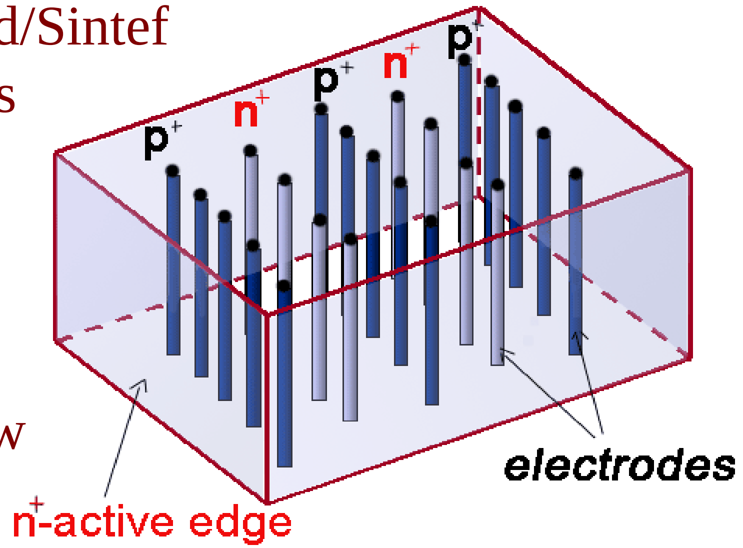
ATLAS project	Development, Testing and Industrialization of Full-3D Active-Edge and Modified-3D Silicon Radiation Pixel Sensors with Extreme Radiation Hardness Results, Plans.		
ATLAS Upgrade Document No:	*Institute Document No.*	*Created:* 17/07/2006	*Page:* 1 of 13
		Modified: 08/03/2007	*Rev. No.:* 2.00

Charge collection distance reduced → reduced charge trapping

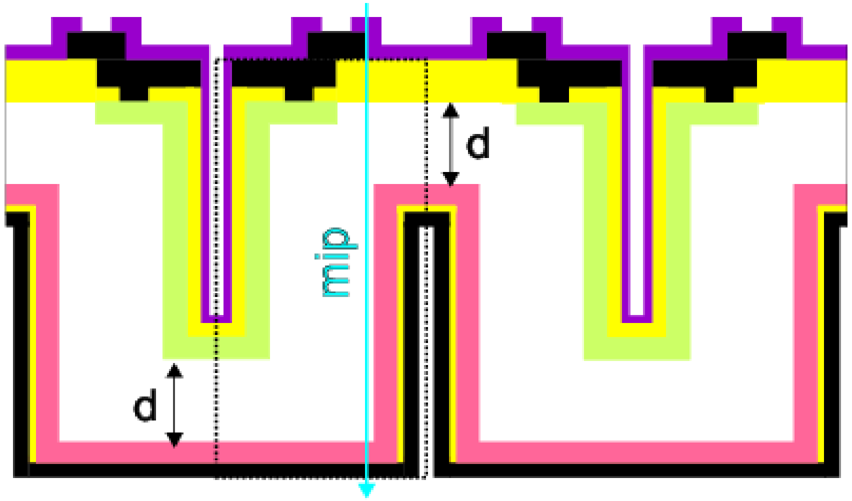
Stanford/Sintef

ICEMos

Glasgow

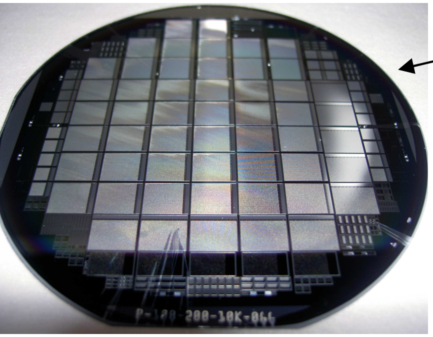


Alternative geometry with double sided electrodes

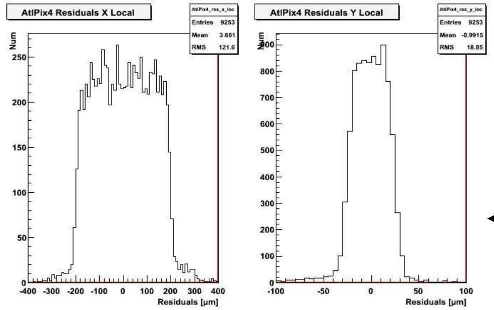


IRST

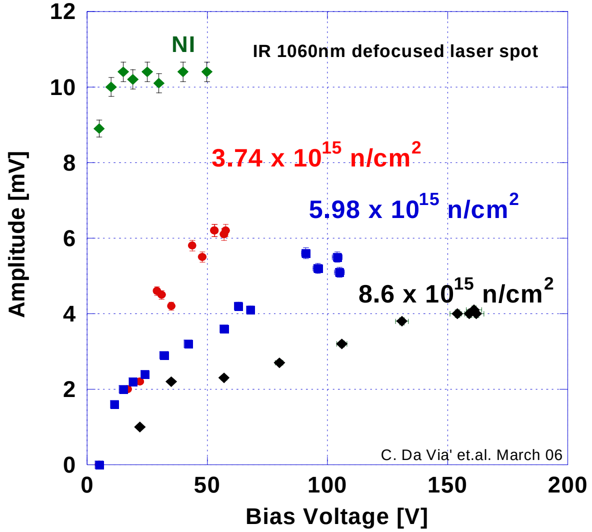
CNM



ATLAS pixel fabricated at Stanford

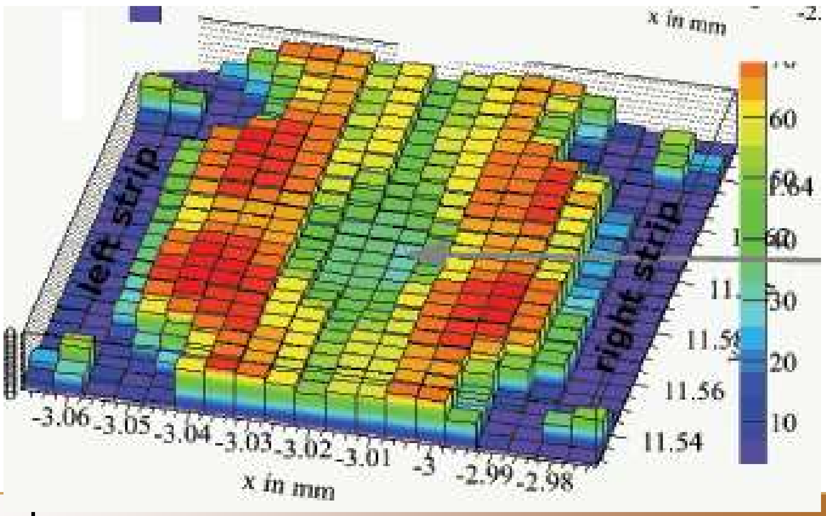


Radiation tests/Praha
CCE(V) with laser

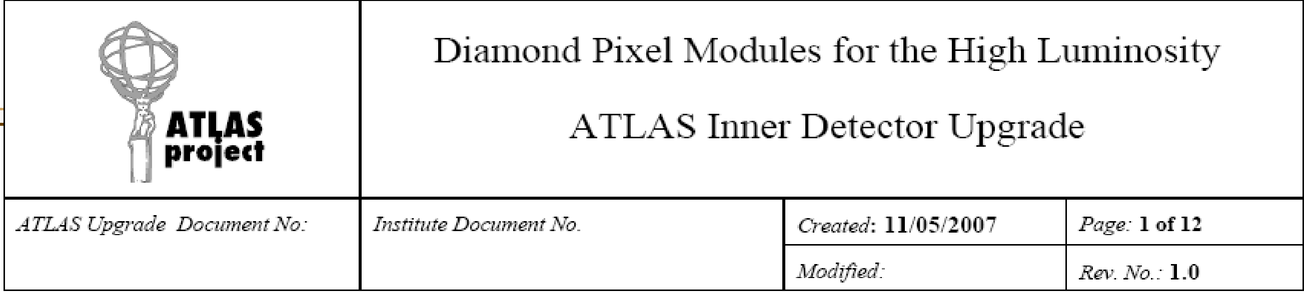


Test beam/data analysis from M. Mathes-Bonn

IR scan 3D- SCstrips/ Freiburg



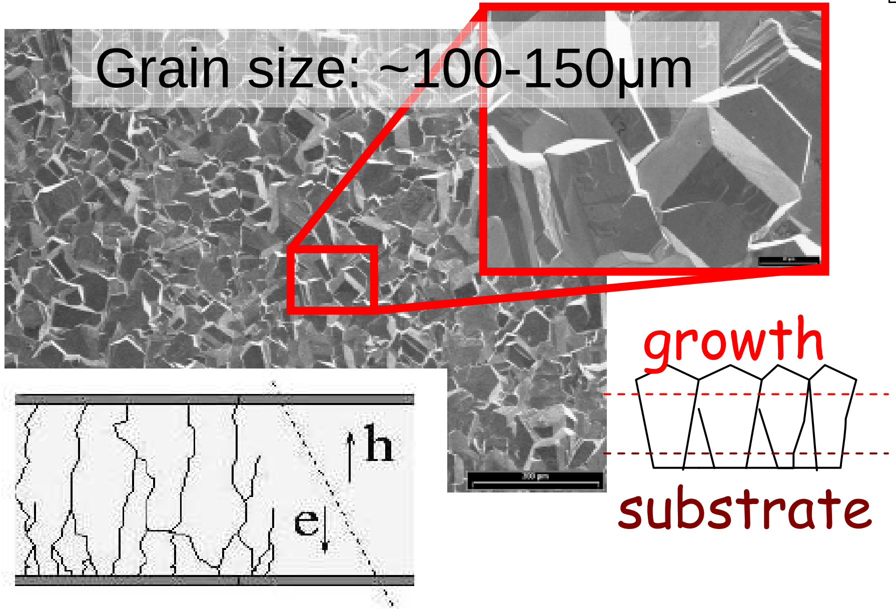
pCVD Diamond



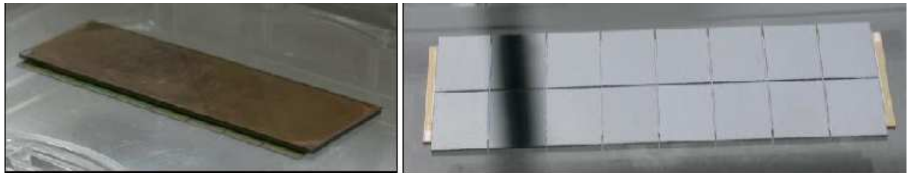
ATLAS project

Diamond Pixel Modules for the High Luminosity
ATLAS Inner Detector Upgrade

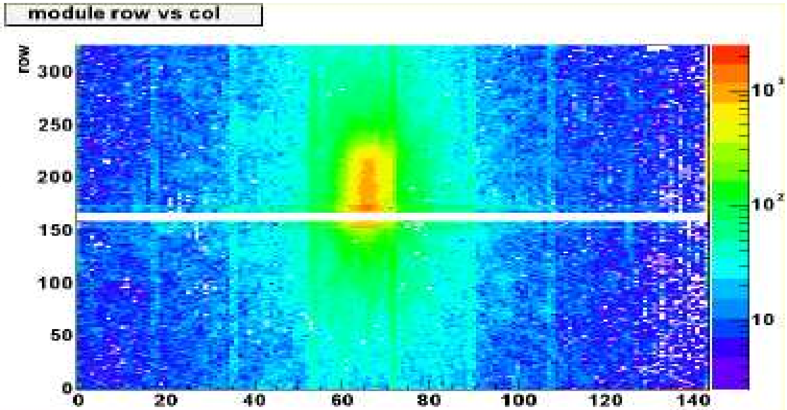
ATLAS Upgrade Document No:	*Institute Document No.*	*Created:* 11/05/2007	*Page:* 1 of 12
		Modified:	*Rev. No.:* 1.0



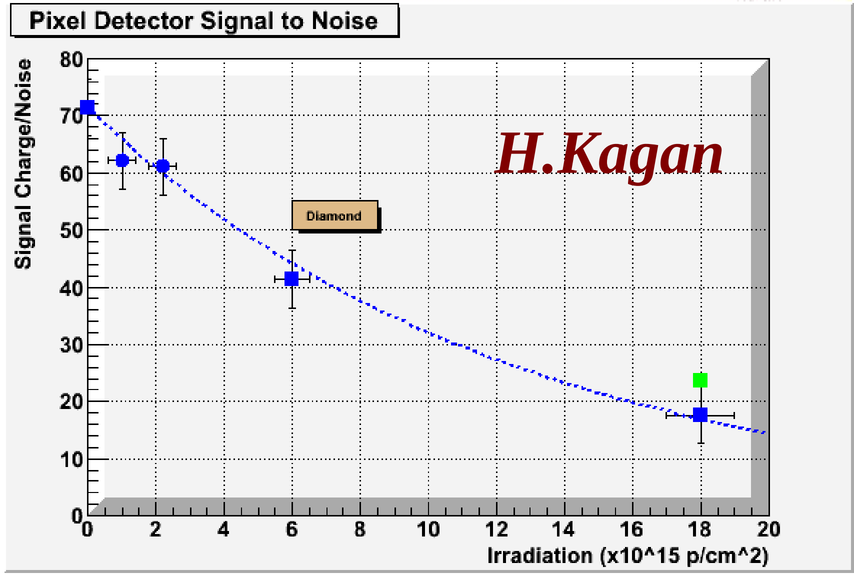
ATLAS pixel module



hitmap



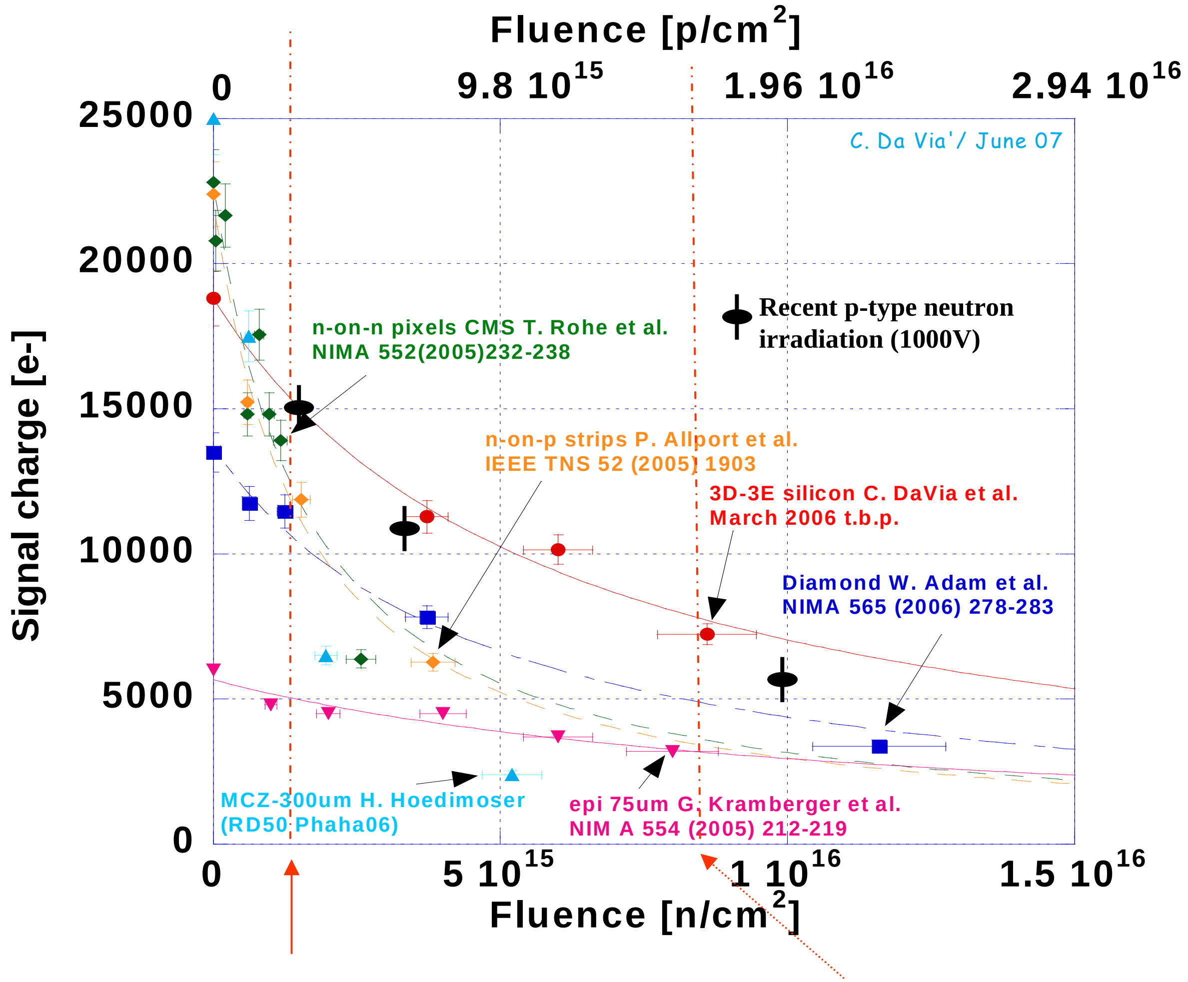
- *large band gap and strong atomic bonds promise fantastic radiation hardness*
- ***low leakage current and low capacitance both give low noise***
- *3 (1.5) times better mobility and 2x better saturation velocity give fast signal collection*
- ***Ionization energy is high: MIP≈2x less signal for same X_0 of SI***
  - Diamond: ~13.9ke^- in 361 μm (140 enc; bare threshold ~1500e)
  - SI: ~22.5 ke^- in 282 μm
- *Grain-boundaries, dislocations, and defects can influence carrier lifetime, mobility, charge collection distance and position resolution*
- *Available Size ~2 x 6 cm^2 (12cm diameter wafer; ~2mm thick)*



Some Compilation Plots

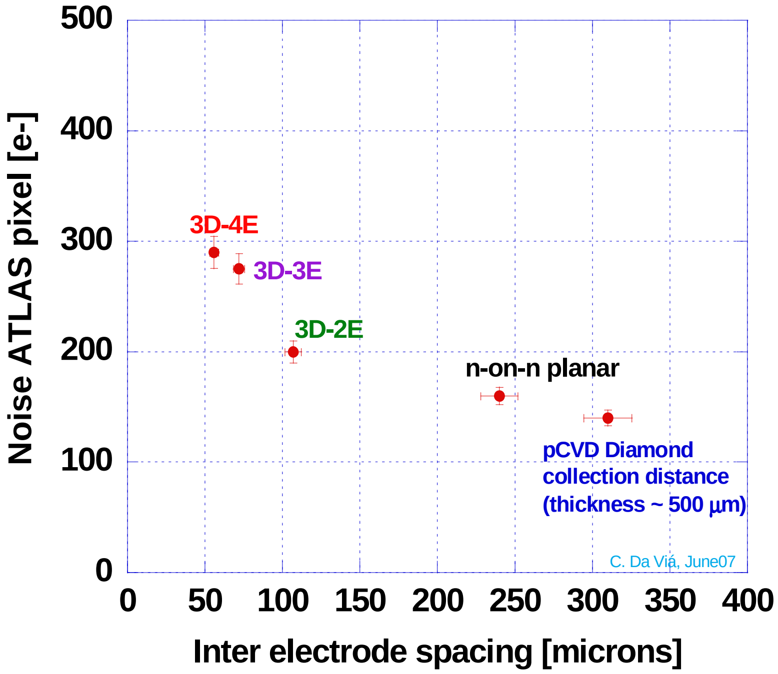
	My comments
Planar n-in-n or n-in-p:	**Conservative solution but high operating voltages: can thin help?**
3D- sensors:	**Highest signal (Efficiency in columns? Commercial fabrication?)**
Diamond:	**Lower currents, low noise (Cost? Uniformity?)**

Comparisons of minimum ionising particle (m.i.p.) CCE(V) and S/N after $10^{16} n_{eq}/cm^2$ needed



3 10¹⁵p/cm²

1.6 10¹⁶p/cm²



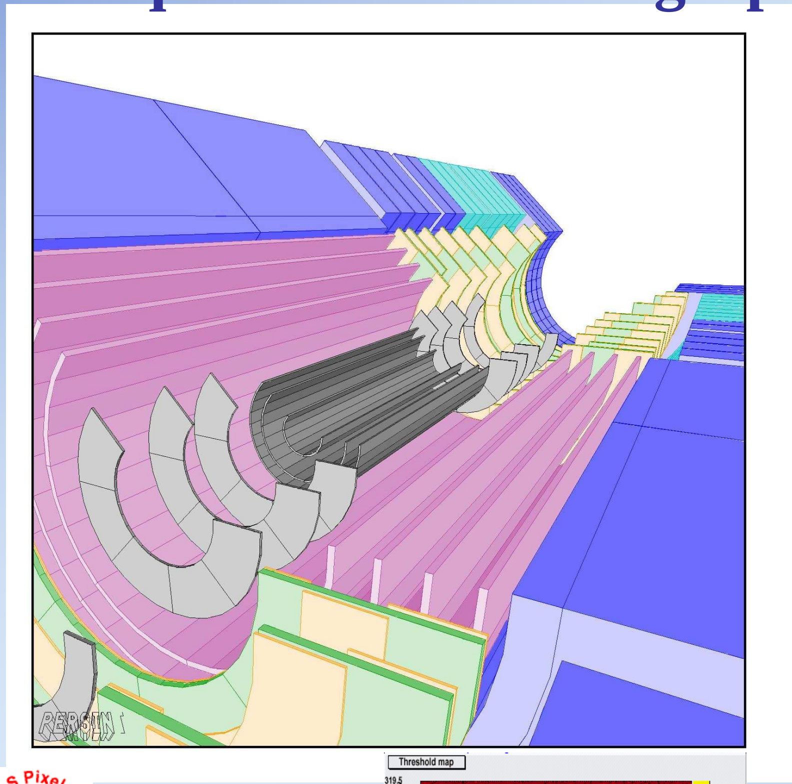
Atlas pixel assemblies

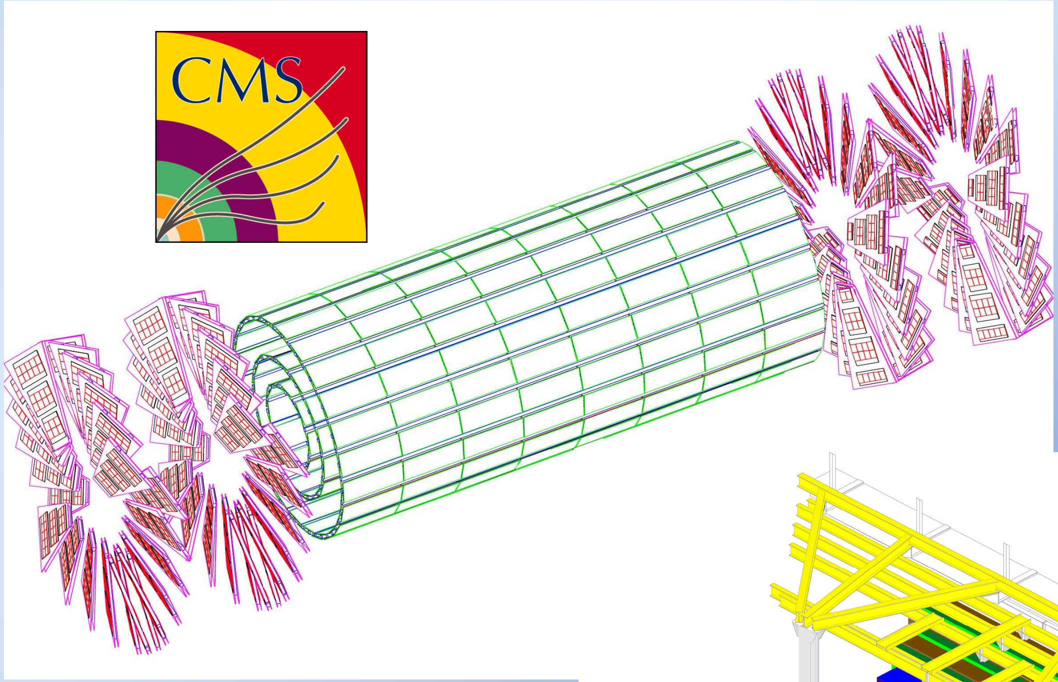
- Noise figure is very good for diamond
- 3D can still play with the substrate thickness
- Planar n-on-p can still play a role in case above technologies not ready

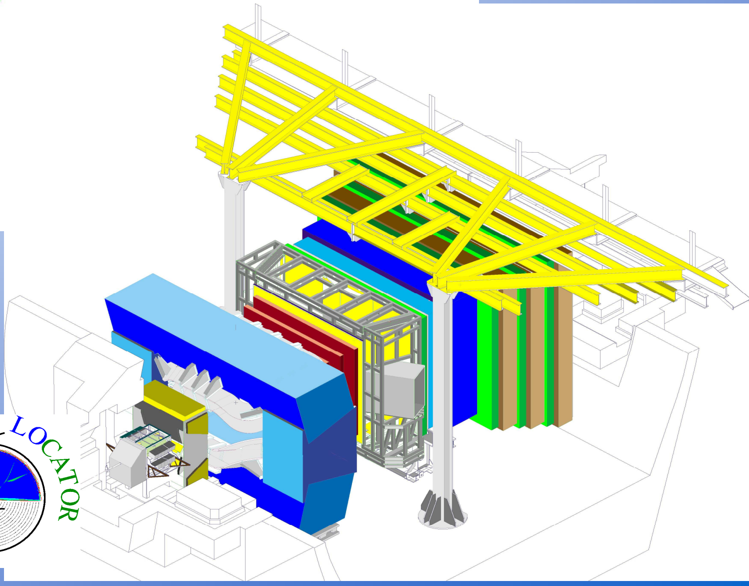
Innermost Detectors at Current LHC

LHC vertex detectors all use n^+ implants in n^- bulk:

- Because of advantages after heavy irradiation from collecting electrons on n^+ implants, the detectors at the LHC (ATLAS and CMS Pixels and LHCb Vertex Locator) have all adopted the n^+ in n^- configuration for doses of $5 - 10 \times 10^{14}\ n_{eq}cm^{-2}$
- Requires 2-sided lithography

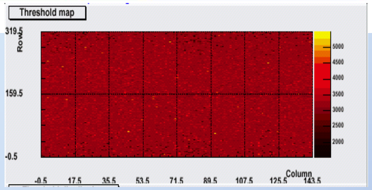






LHCb
Vertex Locator
Z(mm)=0-990

ATLAS 100 million Pixels



Motivations for P-type

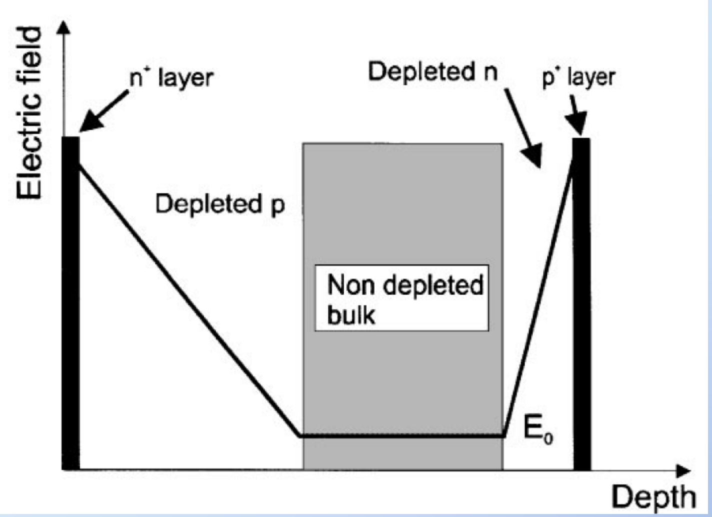
Starting with a p$^-$-type substrate offers the advantages of single-sided processing while keeping n$^+$-side read-out:

- **Processing Costs (~50% cheaper).**
- **Greater potential choice of suppliers.**
- **High fields always on the same side.**
- **Easy of handling during testing.**
- **No delicate back-side implanted structures to be considered in module design or mechanical assembly.**

So far, capacitively coupled, polysilicon biased devices fabricated to ATLAS mask designs with Micron Semiconductor (UK) Ltd (full size: 6cm×6cm), CNM Barcelona (miniature: 1cm×1cm), ITC Trento (miniature: 1cm×1cm) and Hamamatsu Photonics (1cm×1cm and orders placed for 10cm×10cm ATLAS prototypes)

N-side read-out for tracking in high radiation environments?

Schematic changes
of Electric field
after irradiation



Effect of trapping on
the Charge Collection
Efficiency (CCE)

$$Q_{tc} \cong Q_0 \exp(-t_c/\tau_{tr}),\ 1/\tau_{tr} = \beta\Phi.$$

Collecting electrons provide a sensitive advantage with respect to holes due to a much shorter t_c. P-type detectors are the most natural solution for *e* collection on the segmented side.

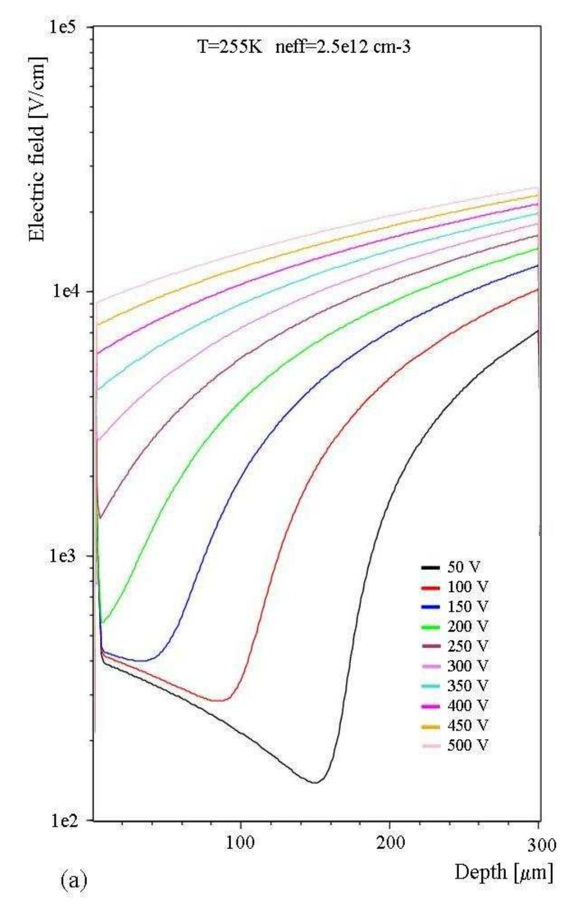
N-side read out to keep lower t_c

More realistic simulation (ISE-TCAD) of E of an irradiated detector.

P-type devices have always the high field region on the right side.

P-side

N-side



Effect of trapping on the Charge Collection Distance

$$Q_{tc} \cong Q_0 \exp(-t_c/\tau_{tr}),\ 1/\tau_{tr} = \beta\Phi.$$

$$v_{sat,e} \times \tau_{tr} = \lambda_{av}$$

$$\beta_e = 4.2\mathrm{E}{-16}\ \mathrm{cm}^{-2}/\mathrm{ns}$$

$$\beta_h = 6.1\mathrm{E}{-16}\ \mathrm{cm}^{-2}/\mathrm{ns}$$

From G. Kramberger et al., NIMA 476(2002), 645-651.

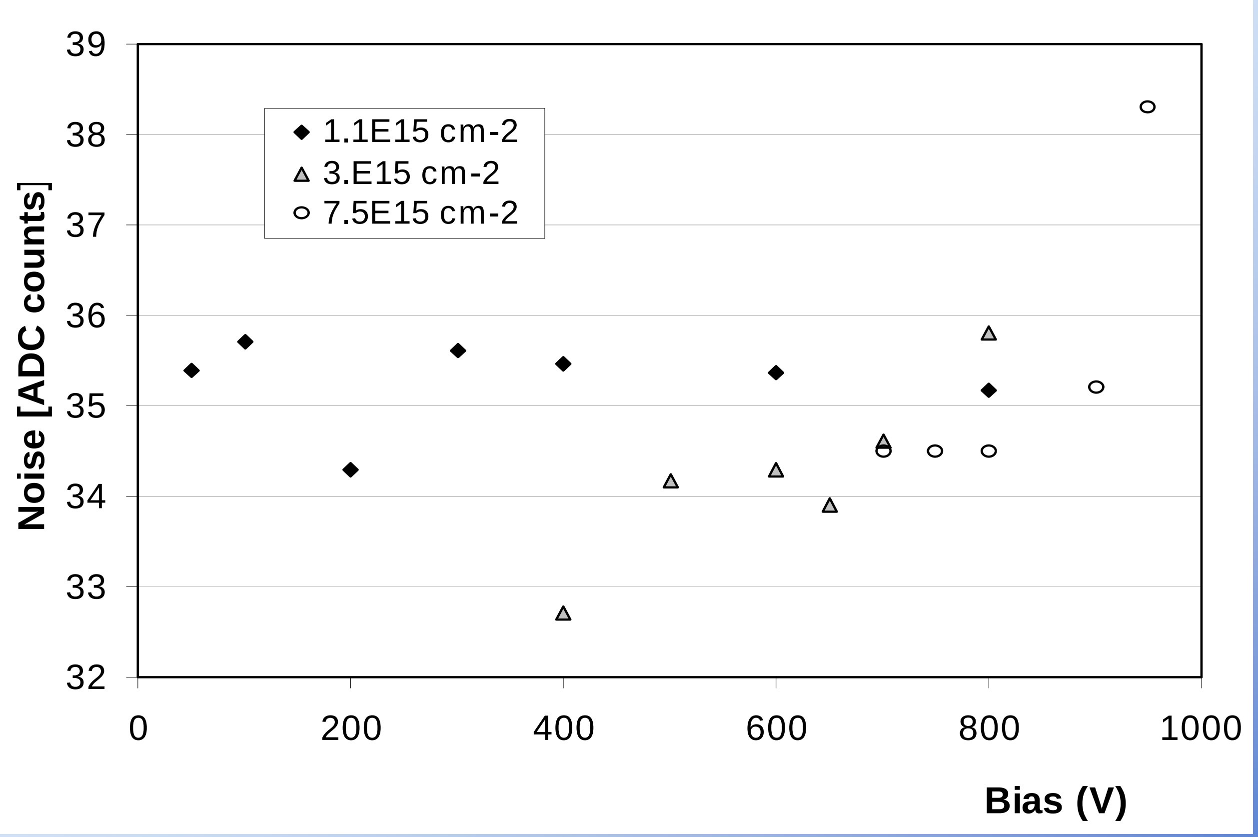
After heavy irradiation thin detectors should have a similar CCE as thicker ones.

$$\lambda_{av}\ (\Phi=1e14) \cong 2400\mu m$$

$$\lambda_{av}\ (\Phi=1e16) \cong 24\mu m$$

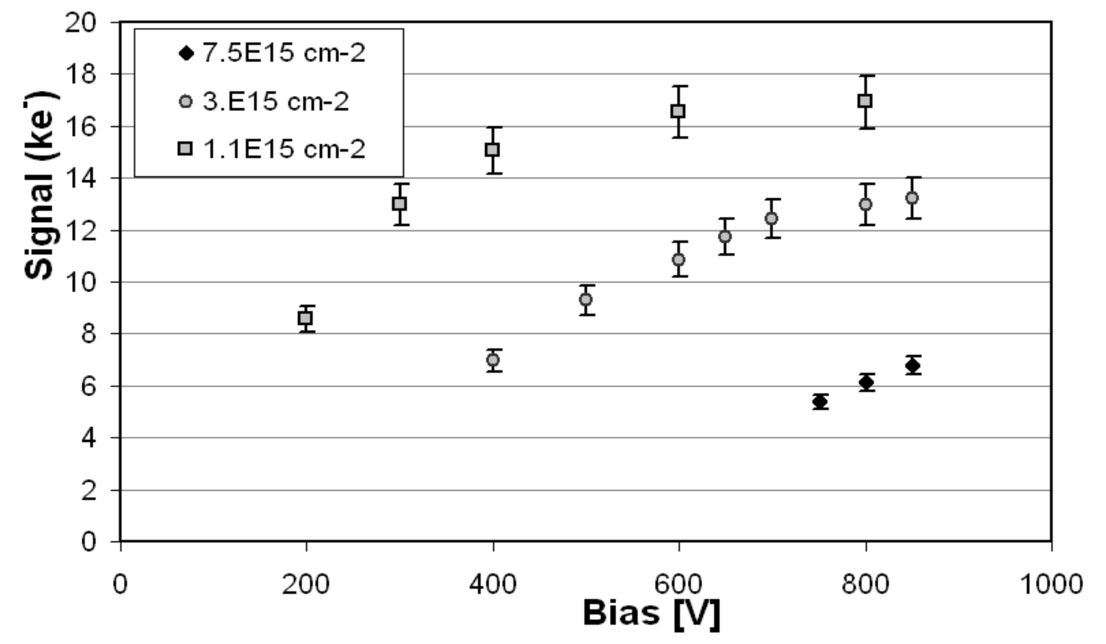
P-type miniature detectors from CNM

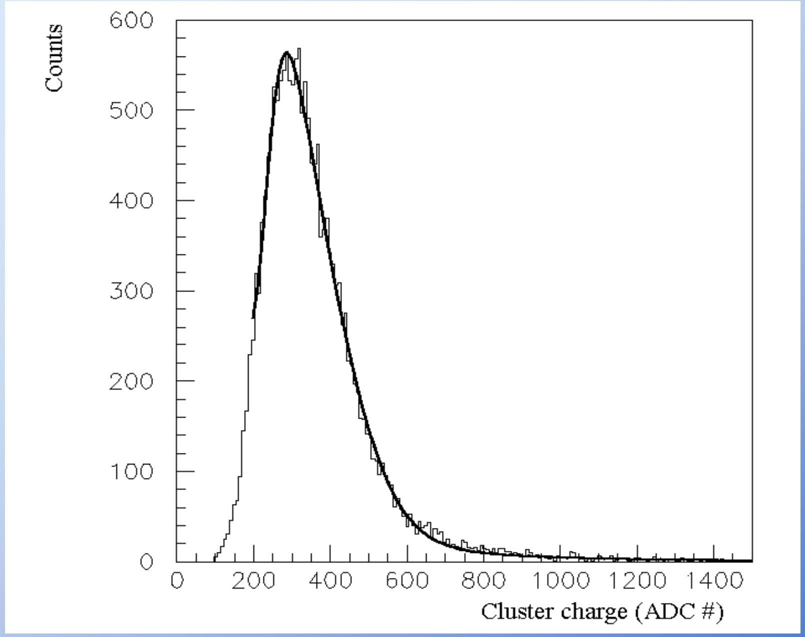
Despite the rather poor pre-irradiation characteristics, all the devices (~300µm thick) show a remarkable robustness, after irradiation, both in term of breakdown voltage and noise. A value of about 34 ADC counts was the typical one measured with similar geometry standard ATLAS non-irradiated miniature sensors.



P-type miniature detectors from CNM

Extremely good performances in term of charge collection after unprecedented doses (1., 3.5., and 7.5 10^{15} p cm^{-2}) are shown.

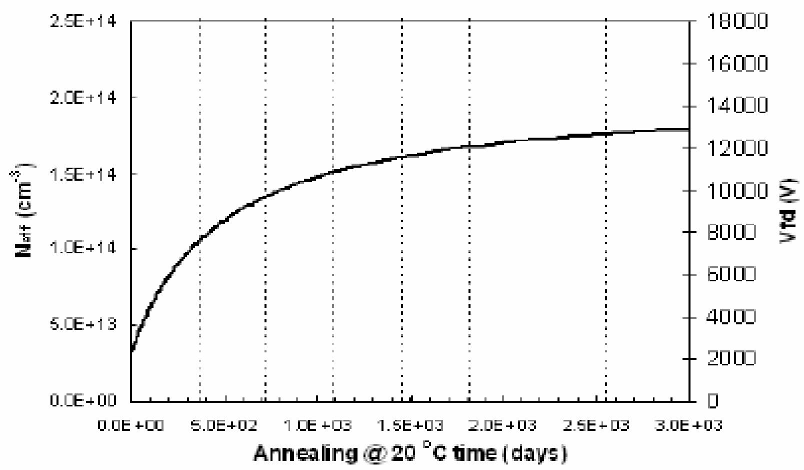




P-type miniature detectors from CNM

Another effect that has changed the way to regard at the reverse annealing has been measured on these devices. The reverse annealing has been always considered as a possible cause of early failure of Si detectors in the experiments if not controlled by mean of low temperature (not only during operations but also during maintenance/shut down periods). This was originated by accurate measurements of the annealing behaviour of the full depletion voltage in diodes measured with the CV method.

Initial V_{FD} ~ 2800V



Predictions from RD48 parameters for Oxygen enriched devices (best scenario: after 7 RT annealing years the V_{fd} goes from ~2800V to ~12000 V!

Expected changes of full depletion voltage with time after irradiation (as measured with the C-V method) for detector irradiated to 7.5 10^{15} p cm^{-2}.

Please notice that according to CV measurements the so called V_{FD} changes from <3kV to >12kV!

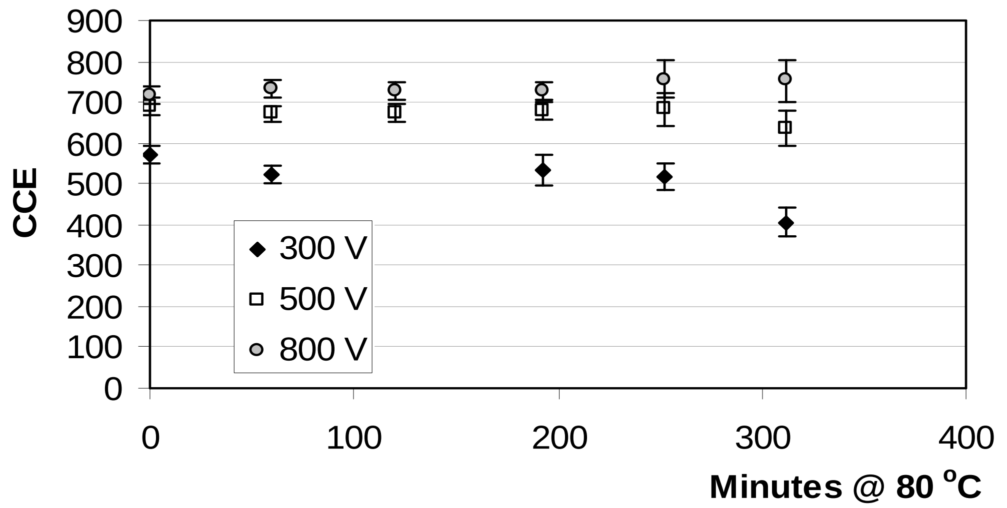
P-type miniature detectors from CNM

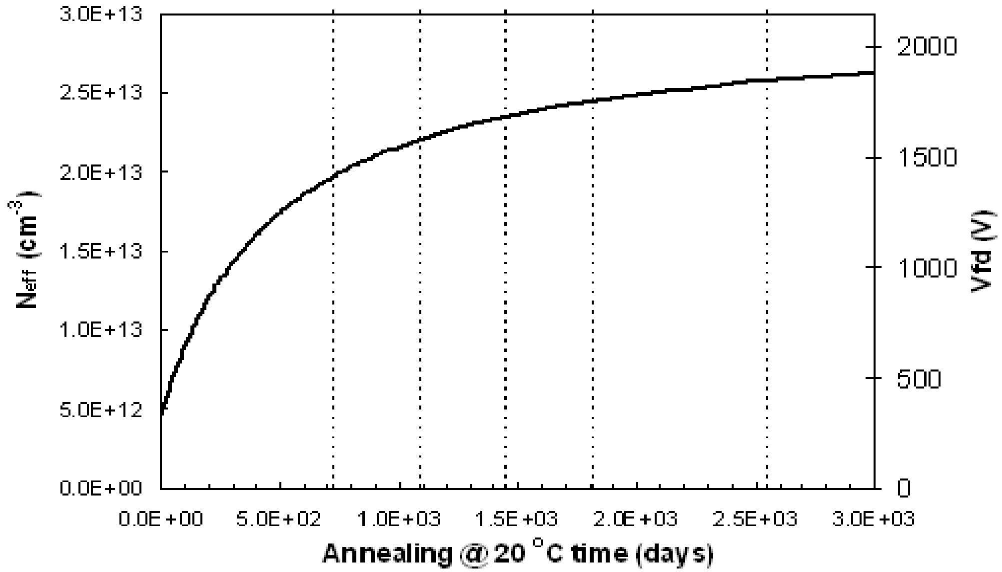
CCE annealing

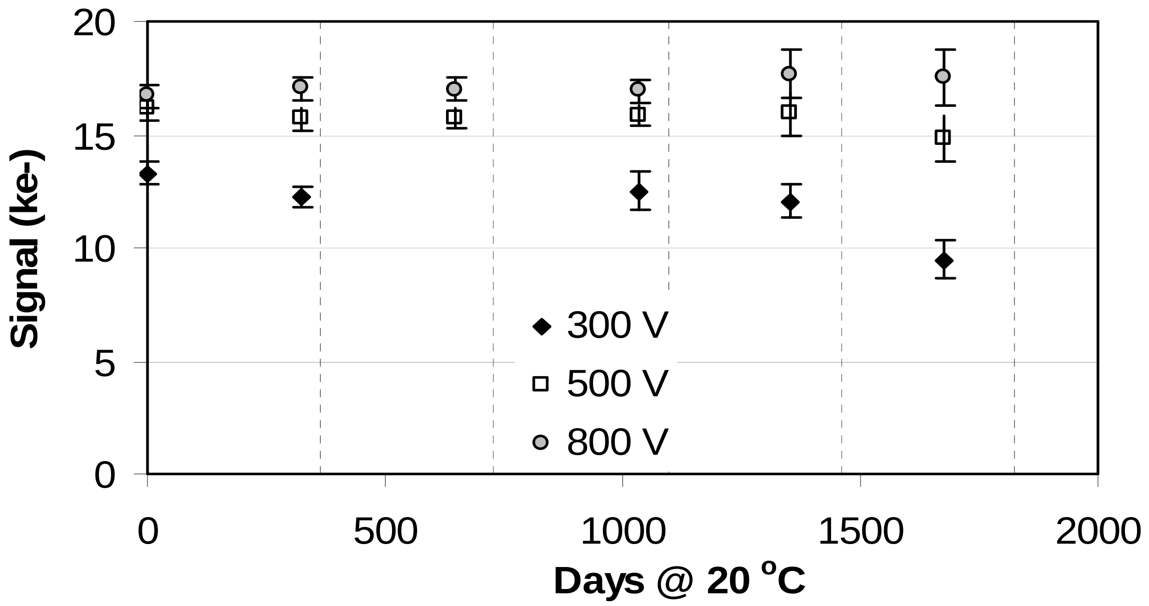
(1.1 10^{15} p cm^{-2})

Initial V_{FD} ~ 420V

Final V_{FD} ~ 1900V





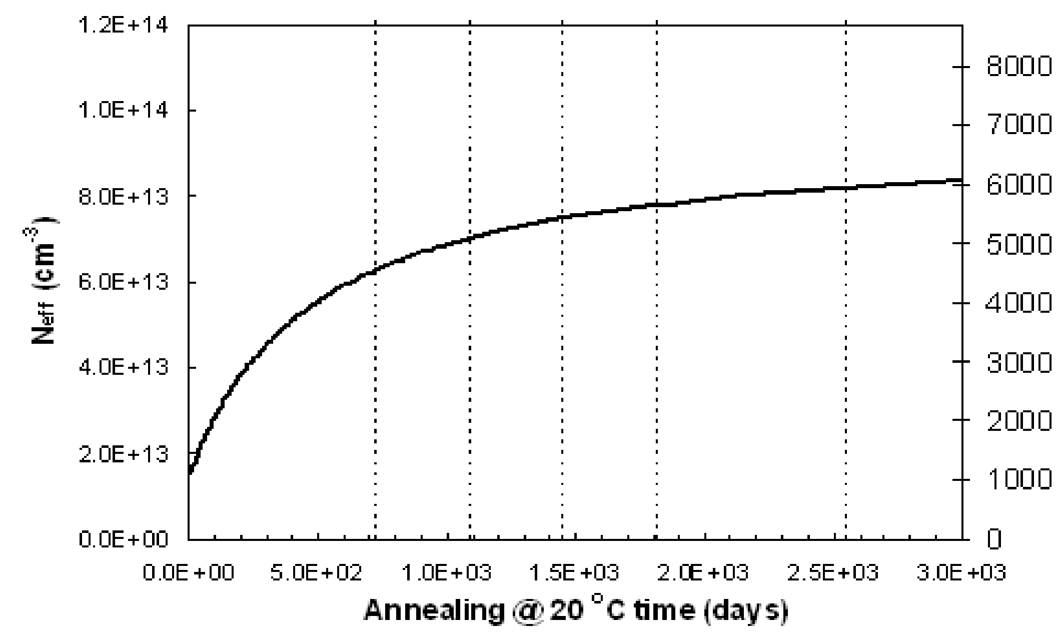


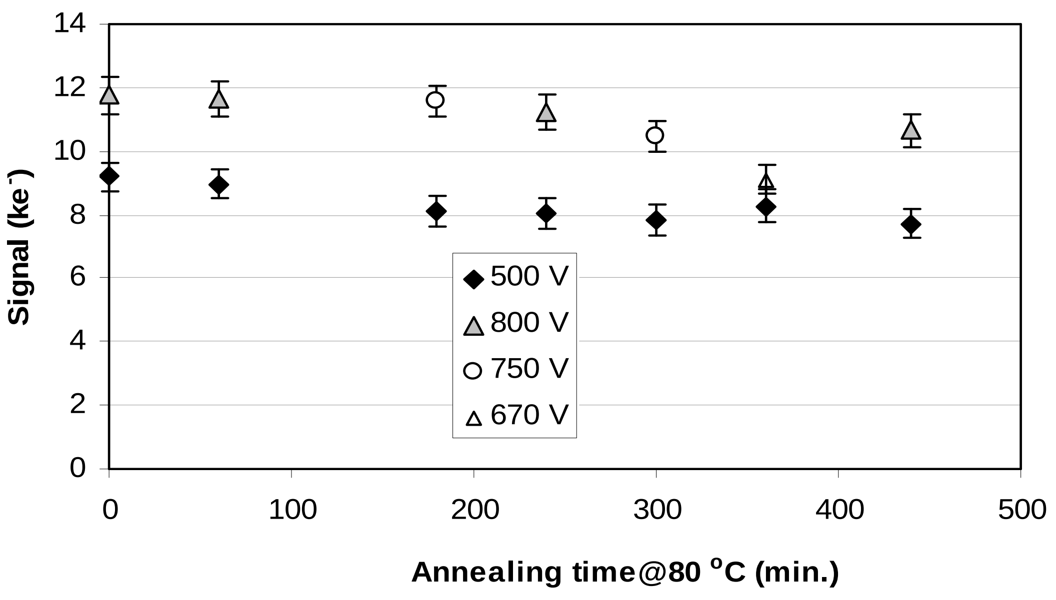
P-type miniature detectors from CNM

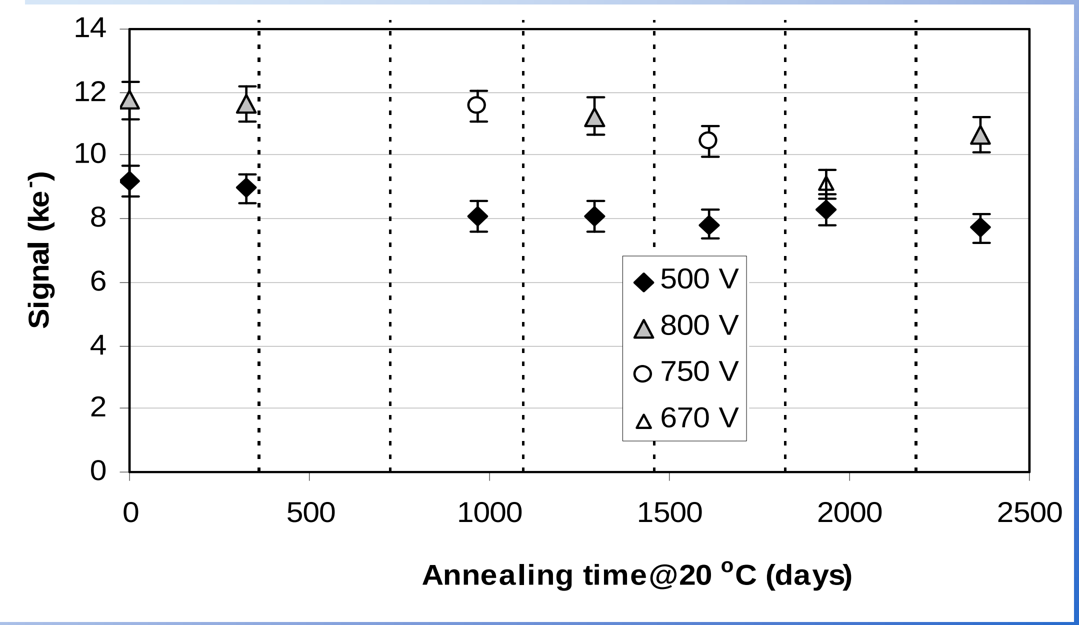
$3.5\ 10^{15}$ p cm^{-2}

Initial V_{FD} ~ 1300V

Final V_{FD} ~ 6000V





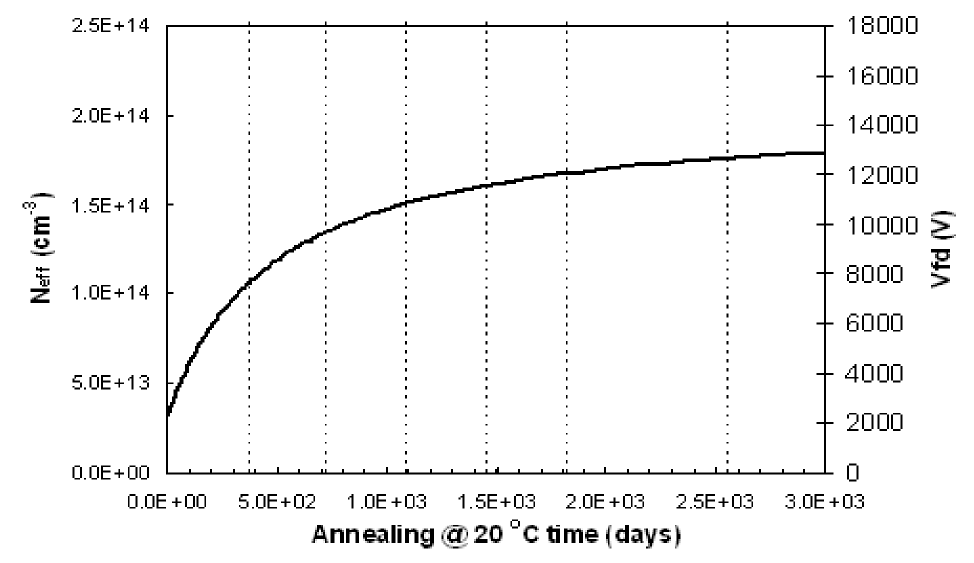


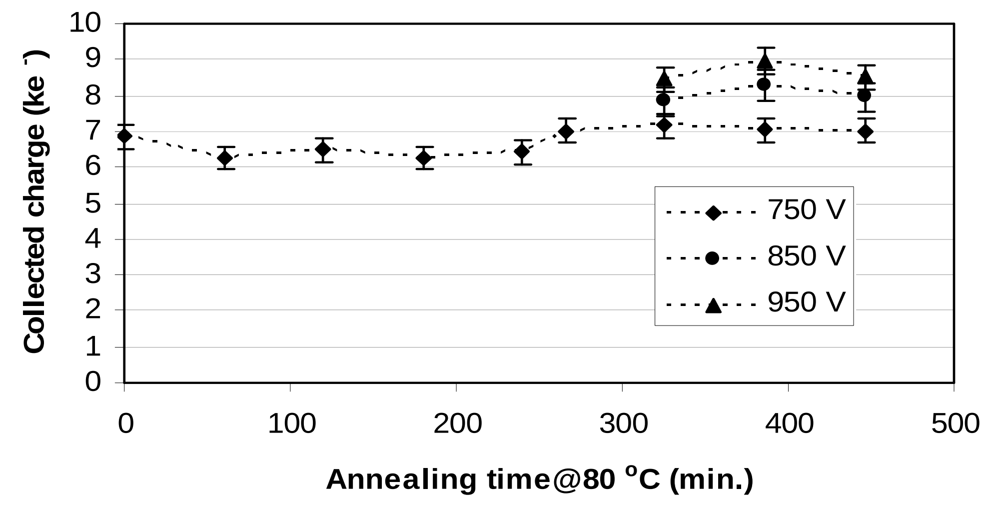
P-type miniature detectors from CNM

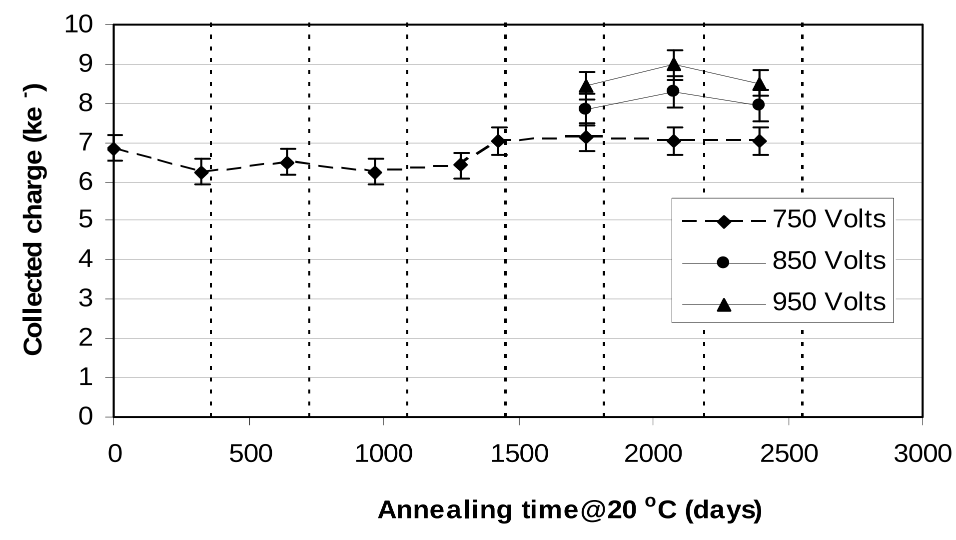
$7.5\ 10^{15}$ p cm^{-2}

Initial V_{FD} ~ 2800V

Final ~12000 V!

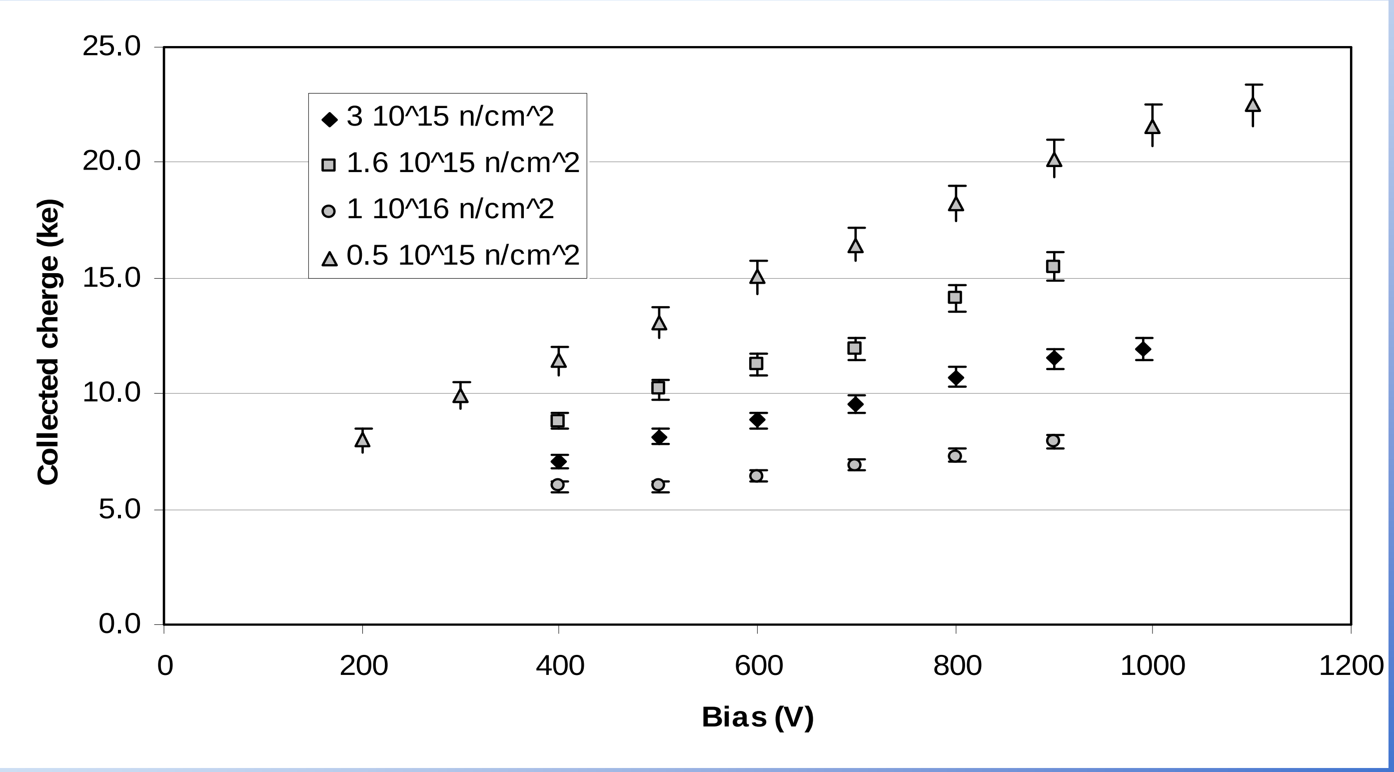




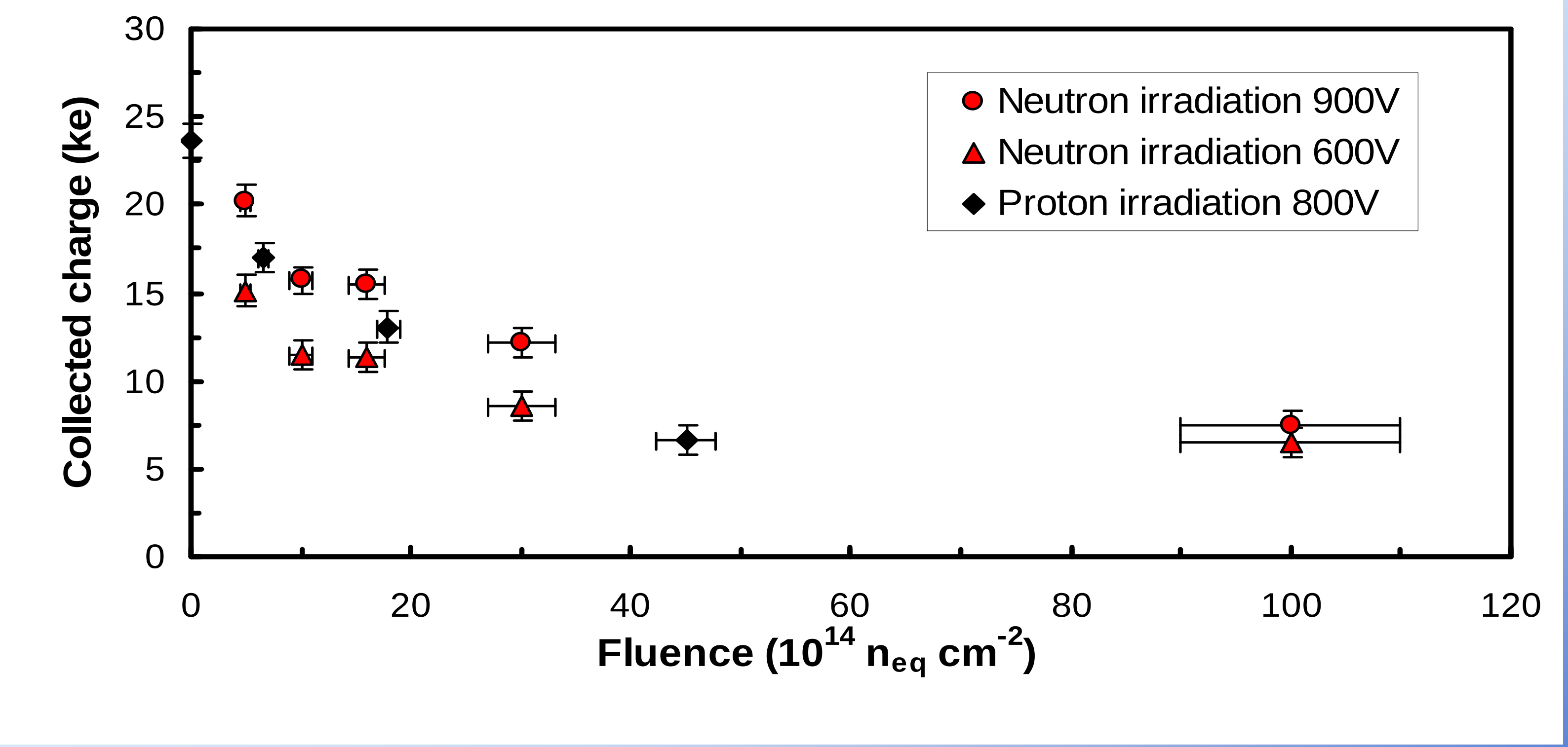


Results with neutron irradiated Micron detectors

Now μ-strip detector CCE measurements up to 1x10^{16} n cm^{-2}!!

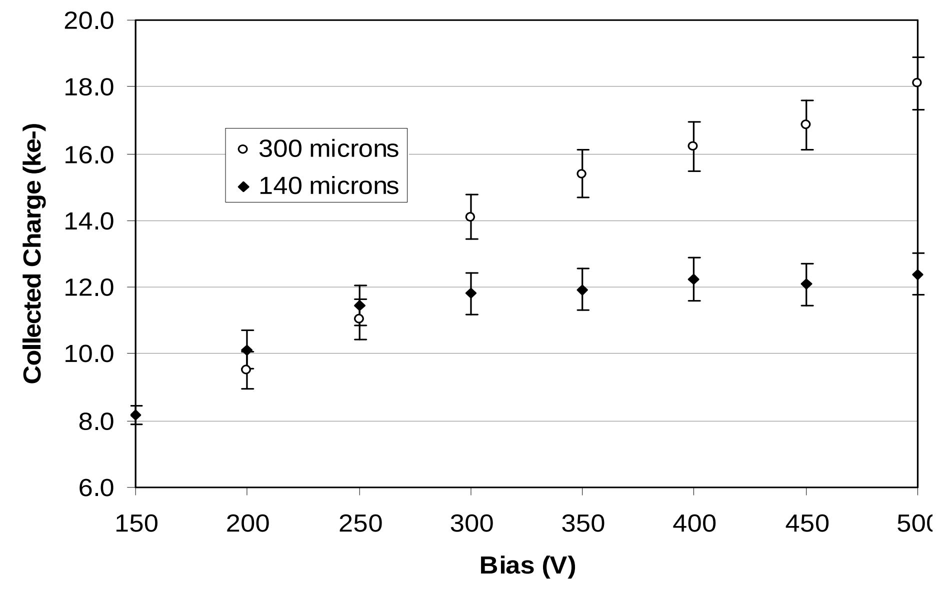


Charge collection efficiency vs fluence for micro-strip detectors irradiated with n and p read-out at LHC speed (40MHz, SCT128 chip).

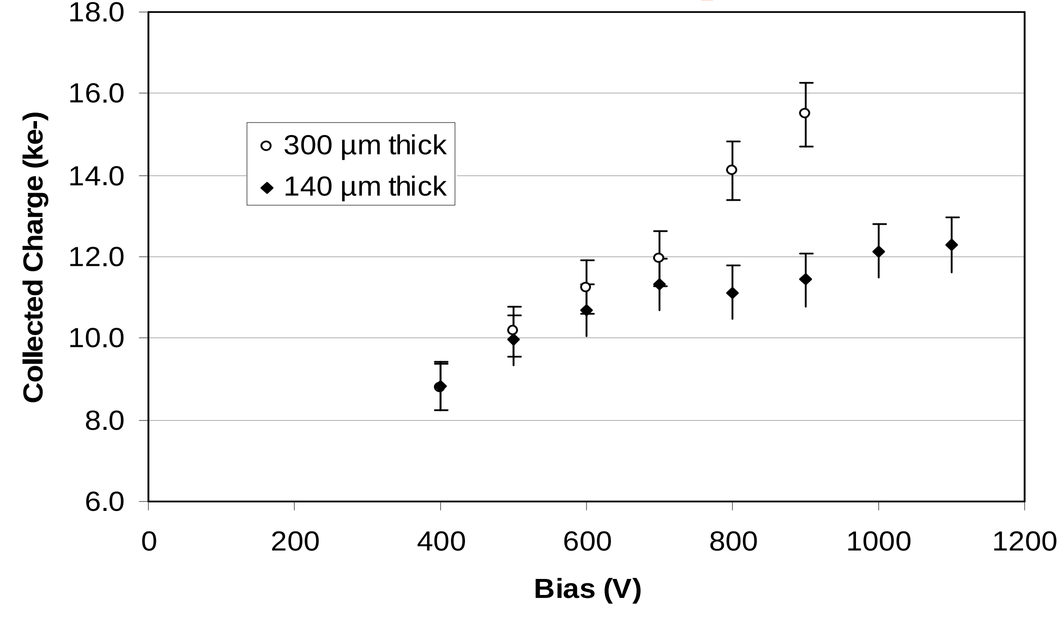


Comparison of CCE with 140µm and 300µm thick detectors from Micron irradiated to various n fluences, up to $1\text{x}10^{16}$ cm^{-2}!

$5\text{x}10^{14}$ (?) n_{eq} cm^{-2}



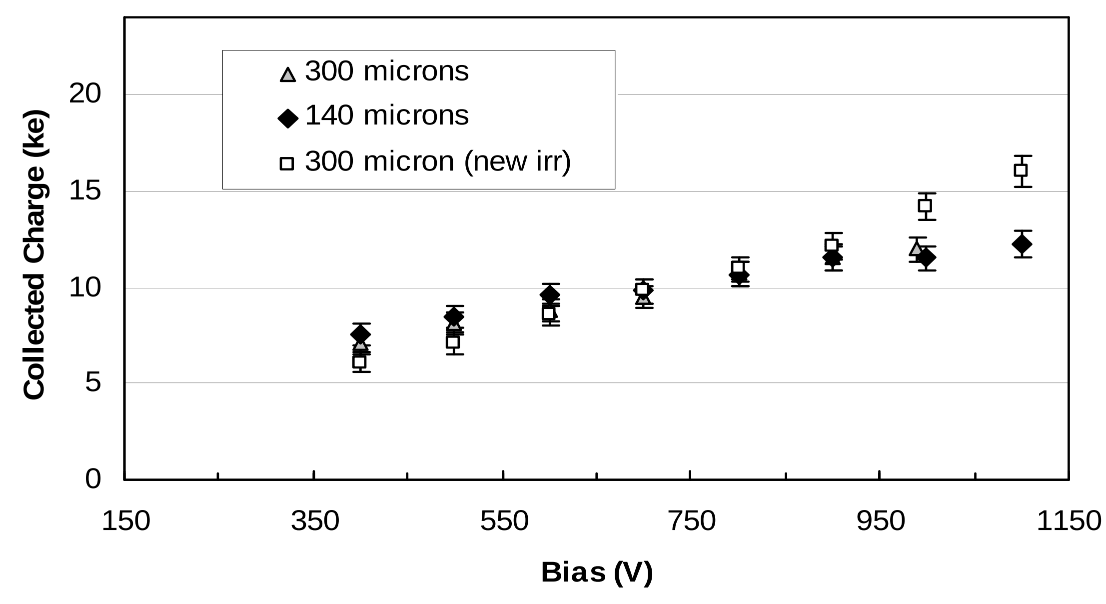
$1.6\text{x}10^{15}$ n_{eq} cm^{-2}

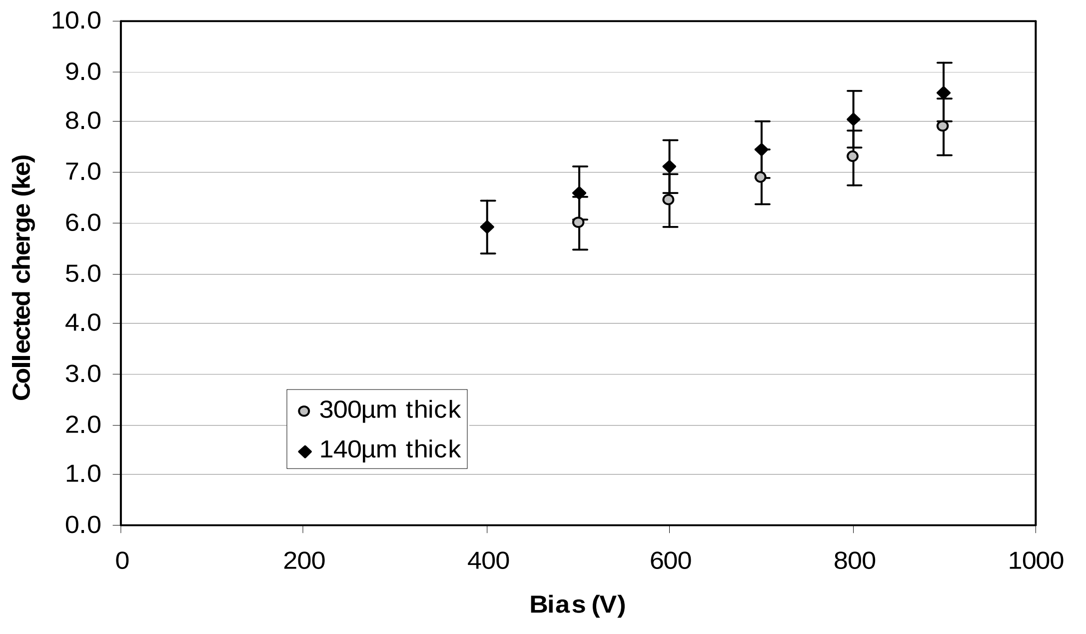


Comparison of CCE with 140µm and 300µm thick detectors from Micron irradiated to various n fluences, up to 1×10^{16} cm^{-2}!

$3\times10^{15}\ n_{eq}\ cm^{-2}$

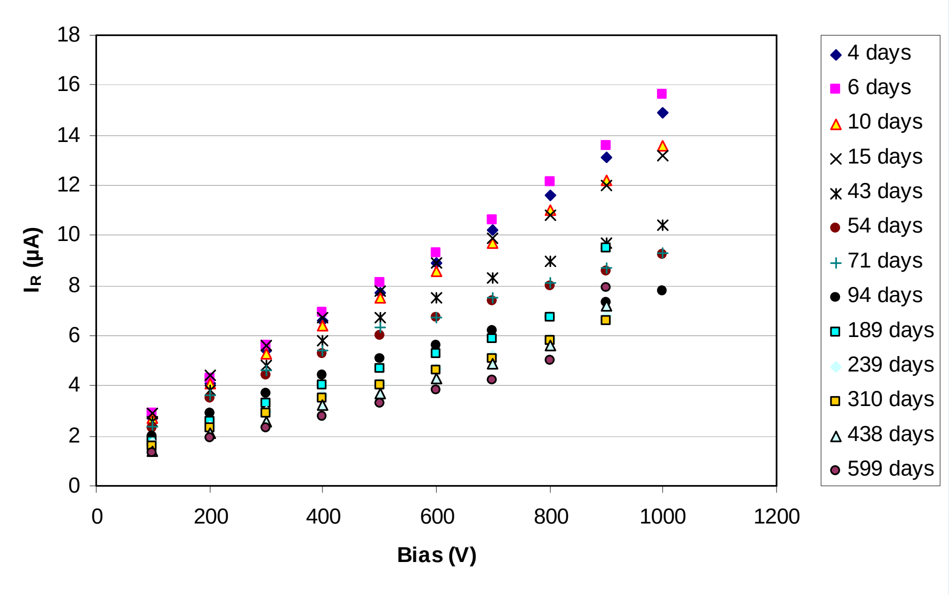
$1\times10^{16}\ n_{eq}\ cm^{-2}$

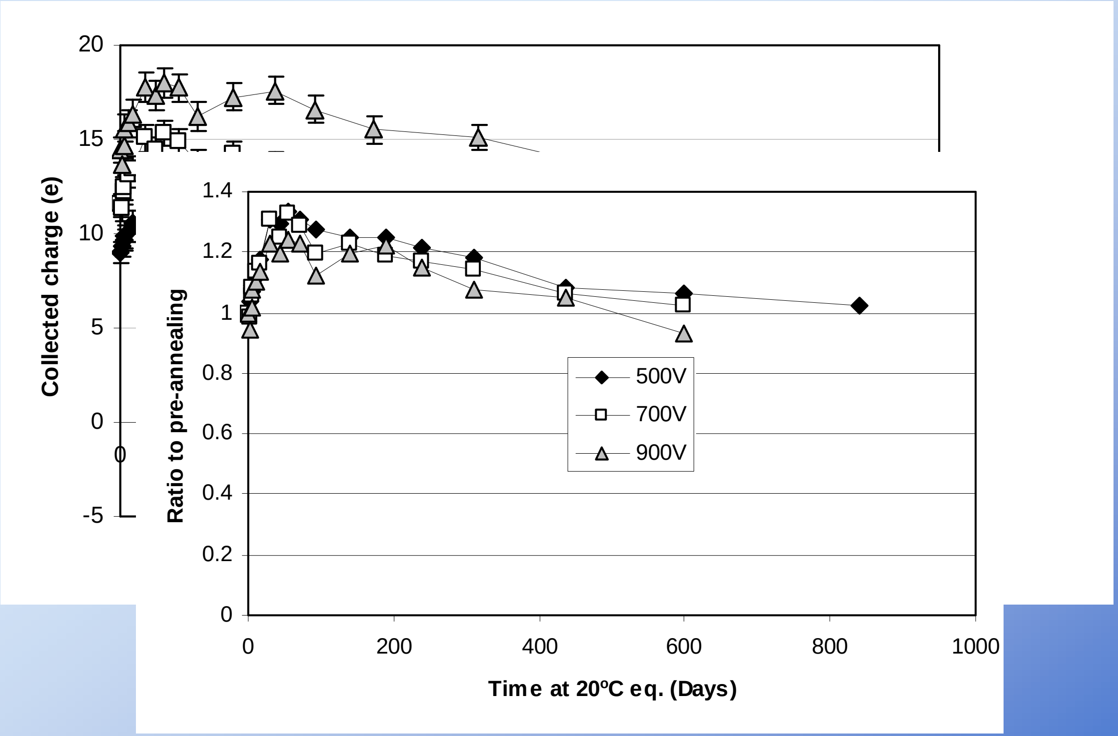




Operational parameters: temperature history

Essential to keep at -20/25°C during operation for reducing the runaway probability and shot noise increase. But in shut down period? The previous slides on annealing were taken with rough granularity. A detailed study of the annealing has been performed, and the results are quite impressive, in term of recovery of charge collection with neutron irradiated detectors.





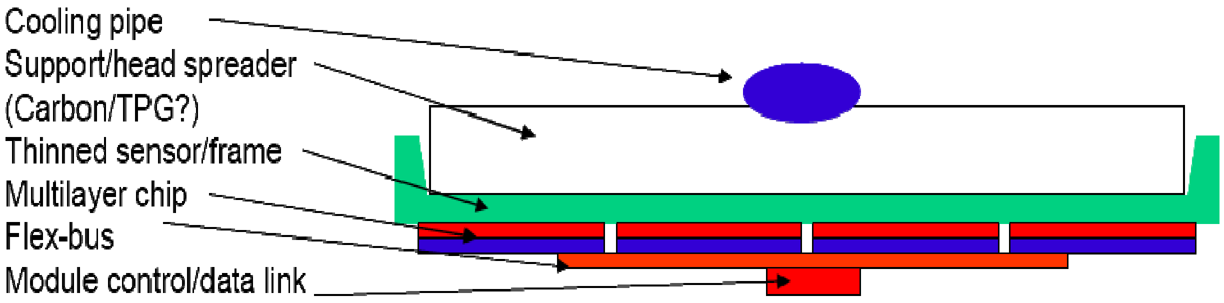
Microstrip Front-end ASIC (ABCn) Design Status

Front-End	Opt. short strip done Layout started	33mA/chip ✓ 750enc (2.5cm strips) Final S/N > 10 ✓
Back-End	Main change in DCL block to handle 160MHz	92mA/chip at 2.5V estimated
Powering	Integrated shunt regulators possible	Current limits to impose uniformity
Floor Plan	First Checks now	7.5mm by 6±1mm
P&R	Examples with pipeline and derandomizer OK	
Submission	Scheduled January 2008	Deliver by April

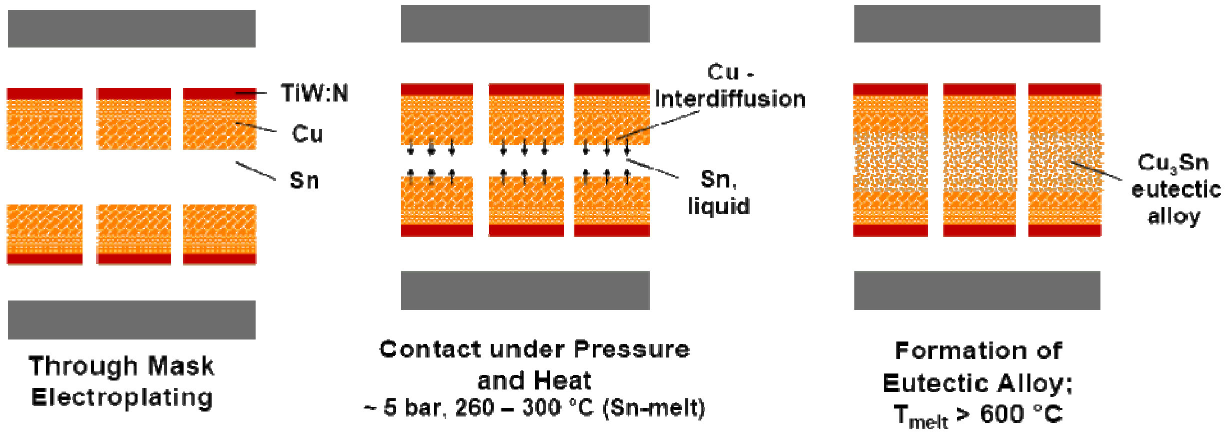
Thin Sensors and Vertical Integration

1) Low I_leak, low V_dep
2) Large live-fraction
3) SLID interconnection
4) 3D integration

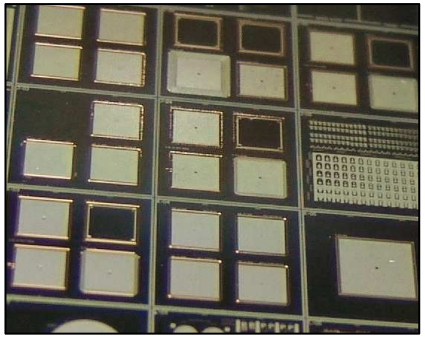
A sketch of the module concept

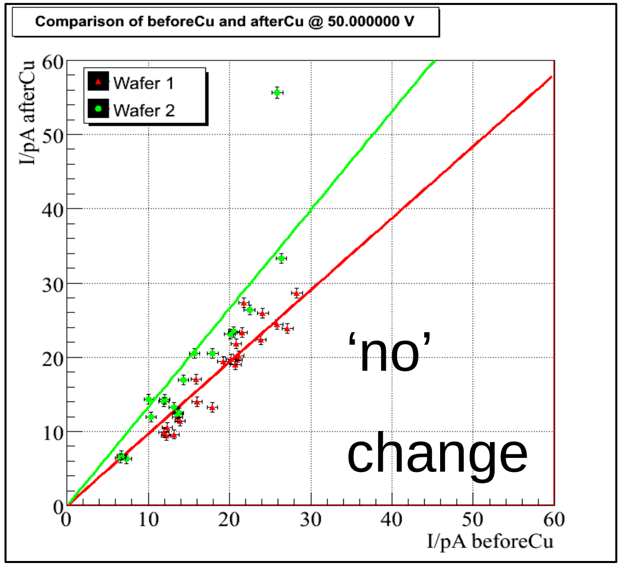


Solid Liquid Interdiffusion (SLID), IZM Munich



First diodes





'no' change

R. Nisius

Conducted by: Bonn, Dortmund, MPI, Oslo, Interon, IZM

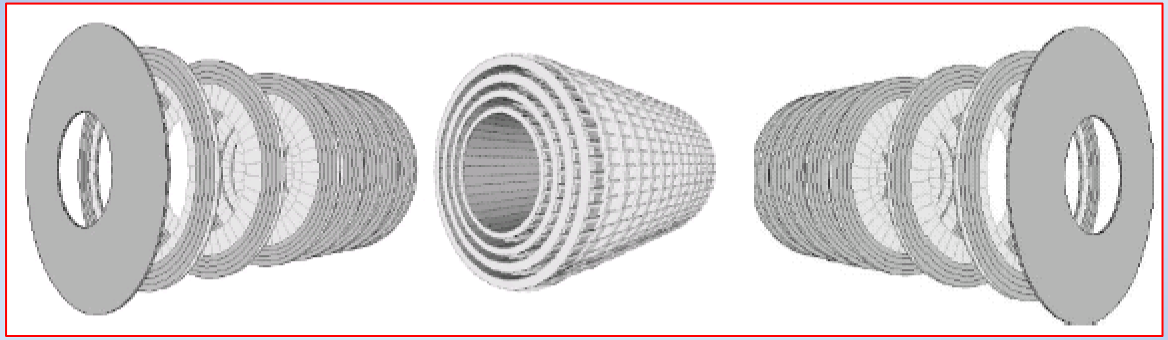
Detectors for sLHC

G. Casse
University of Liverpool Group
6th December 2007

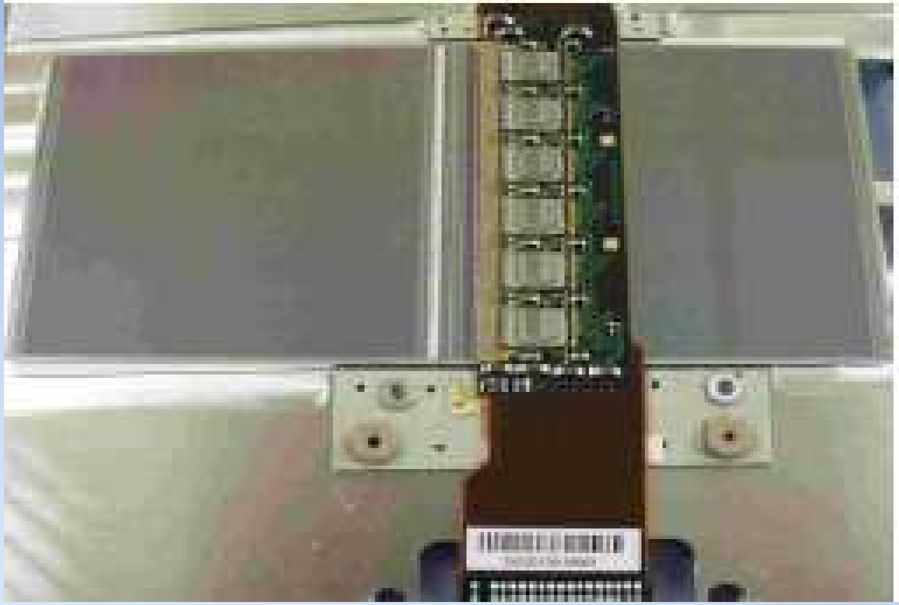
- **Proposed Tracker Layout and Simulations (Radiation and Occupancy)**
- **Sensor and FE Electronics R&D**
- **Microstrip Module and Engineering Concepts**
- **Power, DCS, Opto-electronics, Services, Cooling, …**
- **Conclusions**

Current SCT ATLAS Module Designs

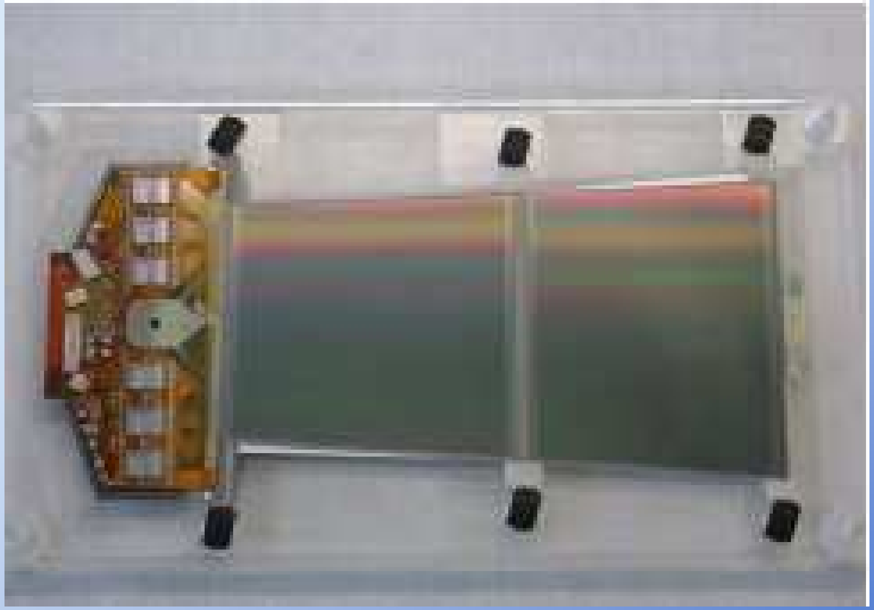
ATLAS Tracker Based on Barrel and Disc Supports



Effectively two styles of modules (with 2×6cm long strips)



Barrel Modules
(Hybrid bridge above sensors)



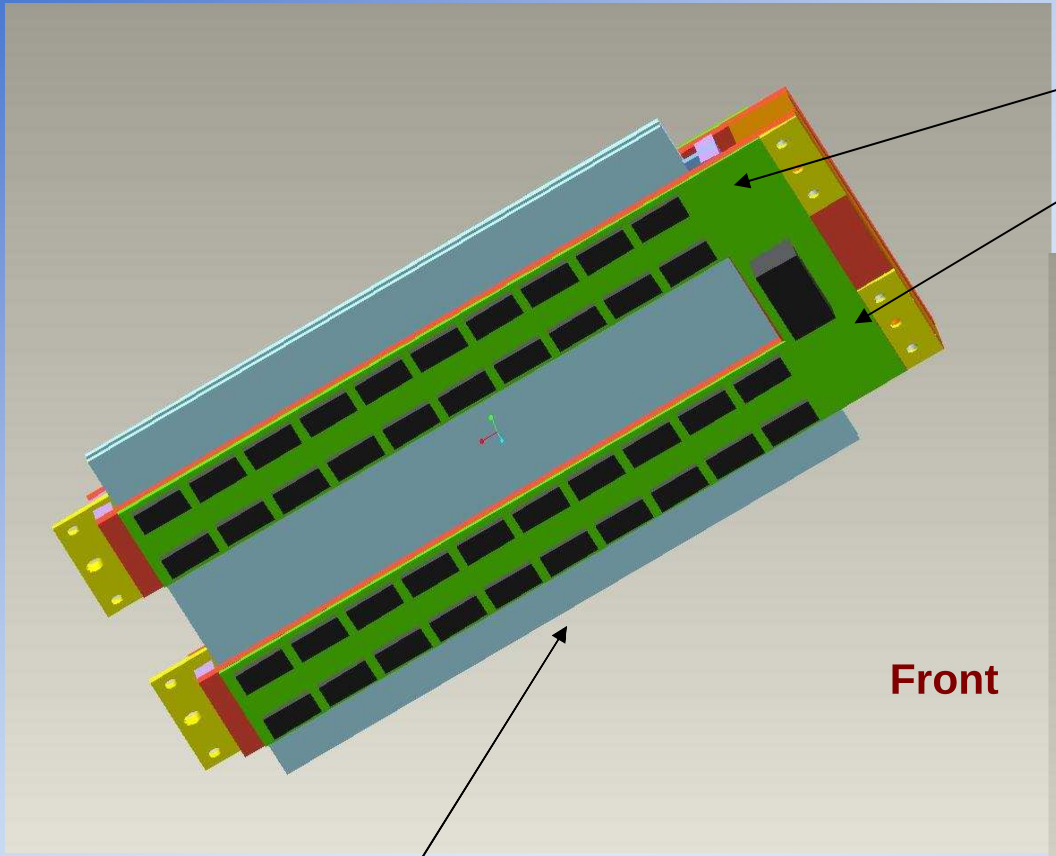
Forward Modules
(Hybrid at module end)

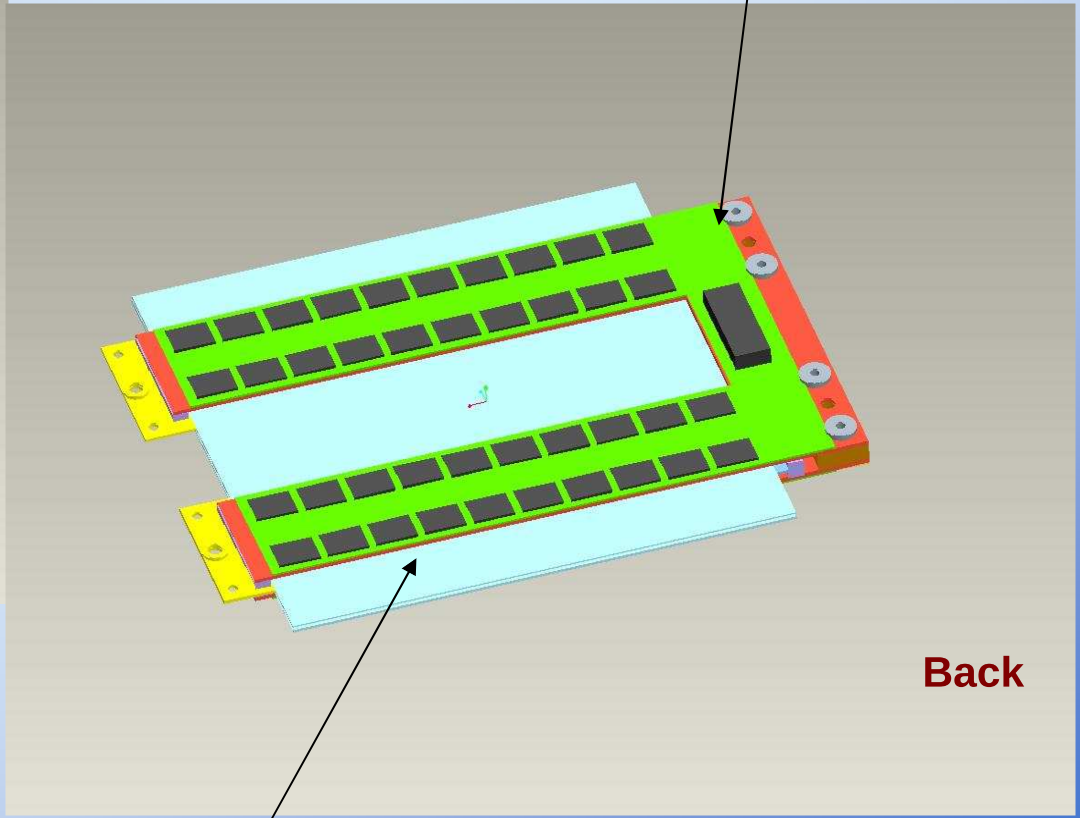
Super-LHC Double Sided Module

Sets of 10 FE Chips in 4 rows

Sets of 10 FE Chips in 4 rows

Module Controller Chip





2 single-sided 10cm square detectors mounted back-to-back around a high thermal conductivity base board

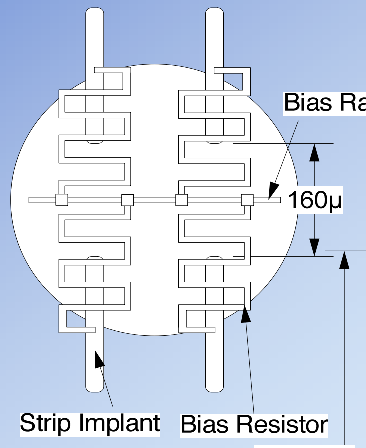
Each detector has 4 rows of 1280 2.4cm long striplets

The Multi-layer kapton circuit in green is the “hybrid” which busses signals to/from/between the microchips and provide the electrical services to the front end electronics

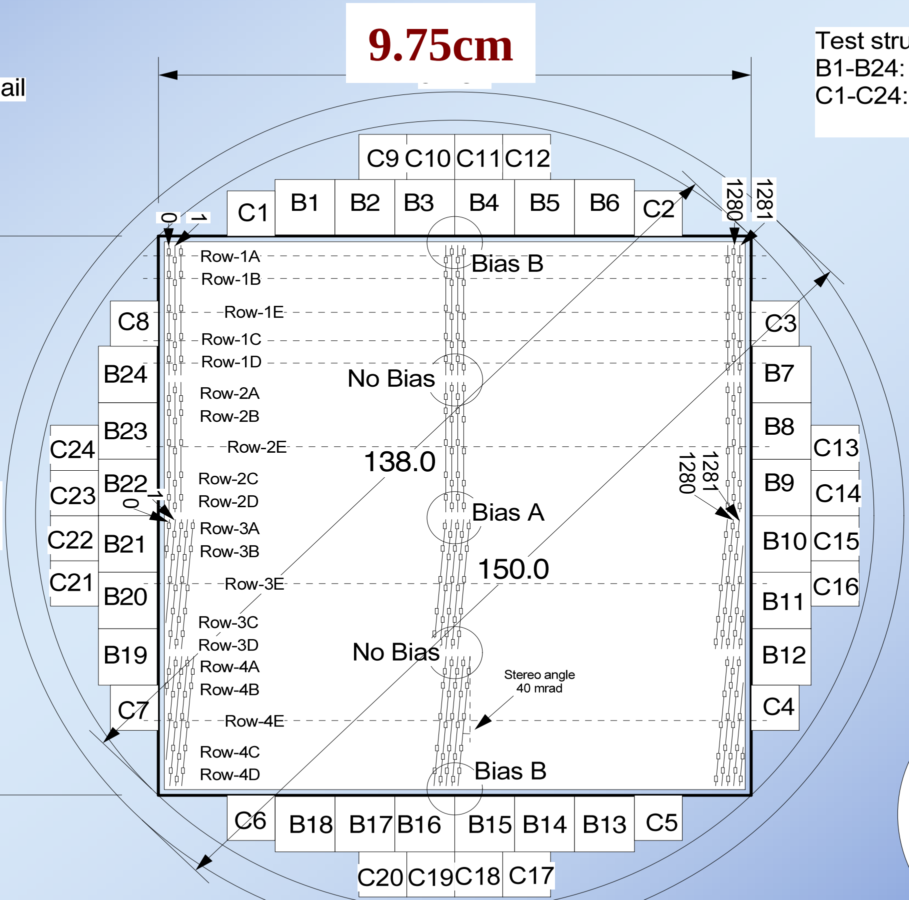
Wire bonds connect the electronics to the hybrid and provide the high density connections down from the front-end to the 4 pad rows on the detectors

New HPK Sensor ATLAS07 Order

- Strip segments
  - 4 rows of 2.38 cm strips (each row 1280 channels)
- **Dimension**
  - **Full square**
- **Wafer**
  - **150 mm p-type FZ(100)**
  - **138 mm dia. usable**
  - **320 µm thick**
- **Axial strips**
  - **74.5 µm pitch**
- **Stereo strips**
  - **40 mrad**
  - **71.5 µm pitch**
- **Bond pads location**
  - **accommodating 24-40 mm distances**
- **n-strip isolation**
  - **P-stop**
  - **Spray on miniatures**



Bias A

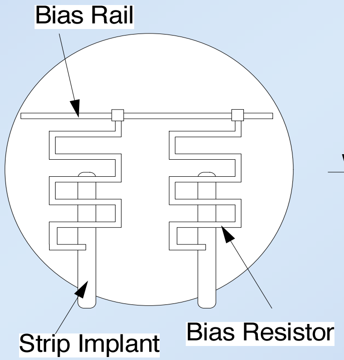


Axial-Stereo Sensor

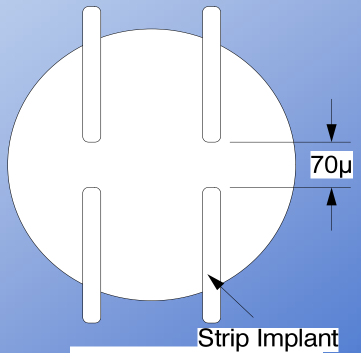
Test structures (TS):
B1-B24: 1cm x 1cm Miniature sensors
C1-C24: 8mm x 8mm Monitor Diodes and Vendor TS

Pad distances:
(X=A,B,C,D,E)
1X-2X=23890
1C-2D=27590
1E-2C=31300
1E-2D=35000
1B-2C=38710

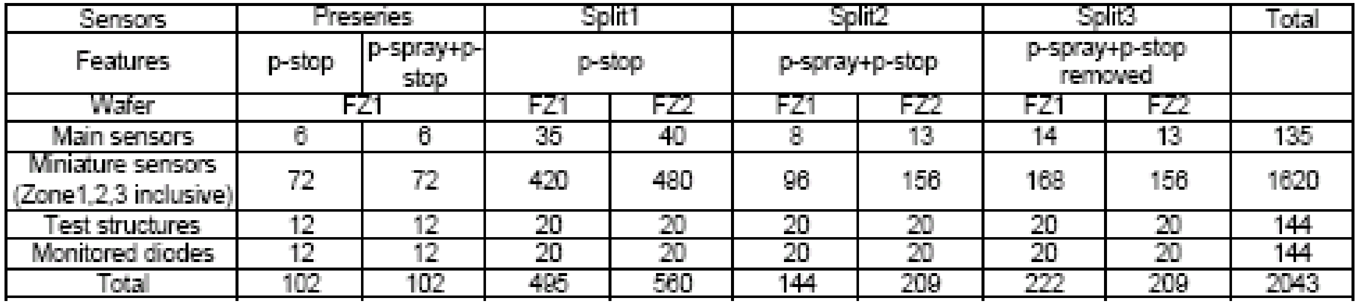
Y. Unno



Bias B



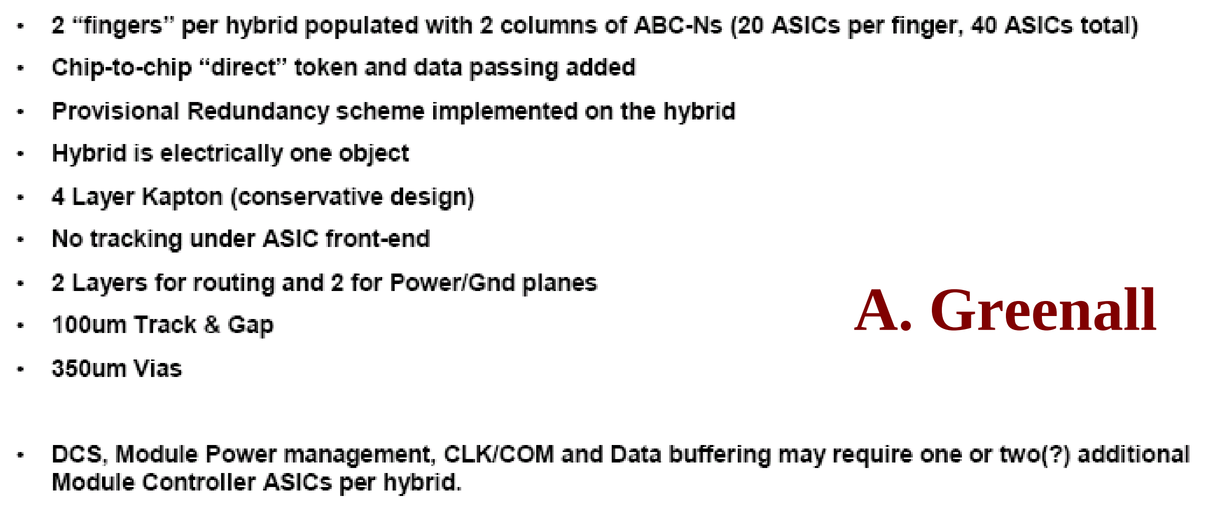
No Bias



Sensors	Preseries		Split1		Split2		Split3		Total
Features	p-stop	p-spray+p-stop	p-stop		p-spray+p-stop		p-spray+p-stop removed		
Wafer	FZ1		FZ1	FZ2	FZ1	FZ2	FZ1	FZ2	
Main sensors	6	6	35	40	8	13	14	13	135
Miniature sensors (Zone1,2,3 inclusive)	72	72	420	480	96	156	168	156	1620
Test structures	12	12	20	20	20	20	20	20	144
Monitored diodes	12	12	20	20	20	20	20	20	144
Total	102	102	495	560	144	209	222	209	2043

New Hybrid Designs

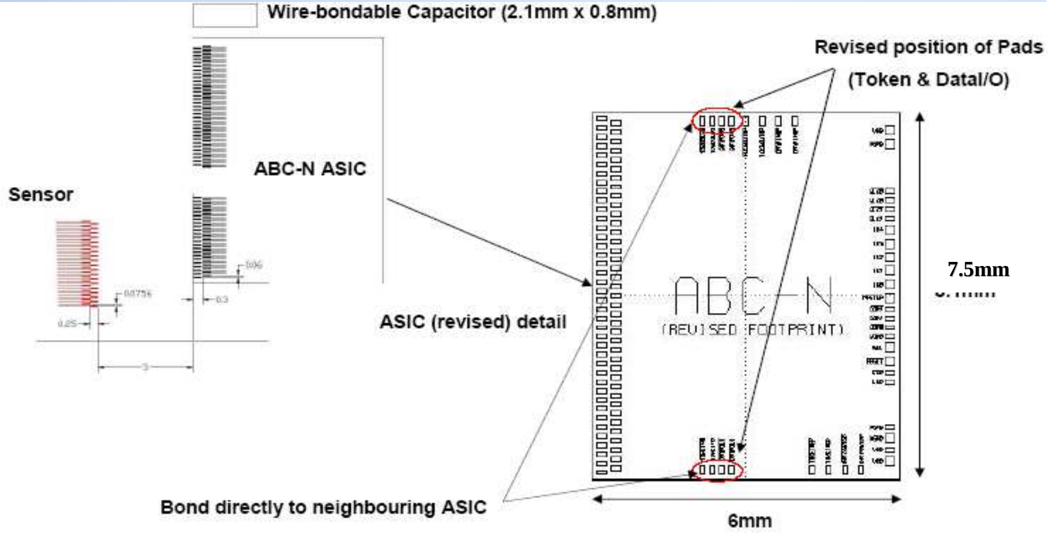
- Multi-layer kapton high density circuit on high thermal conductivity (carbon-carbon) baseboard
- FE ASIC microchip interconnect and high speed data transmission
- Redundancy scheme designed to allow single FE chip failure without loss of read-out from neighbouring ASICs



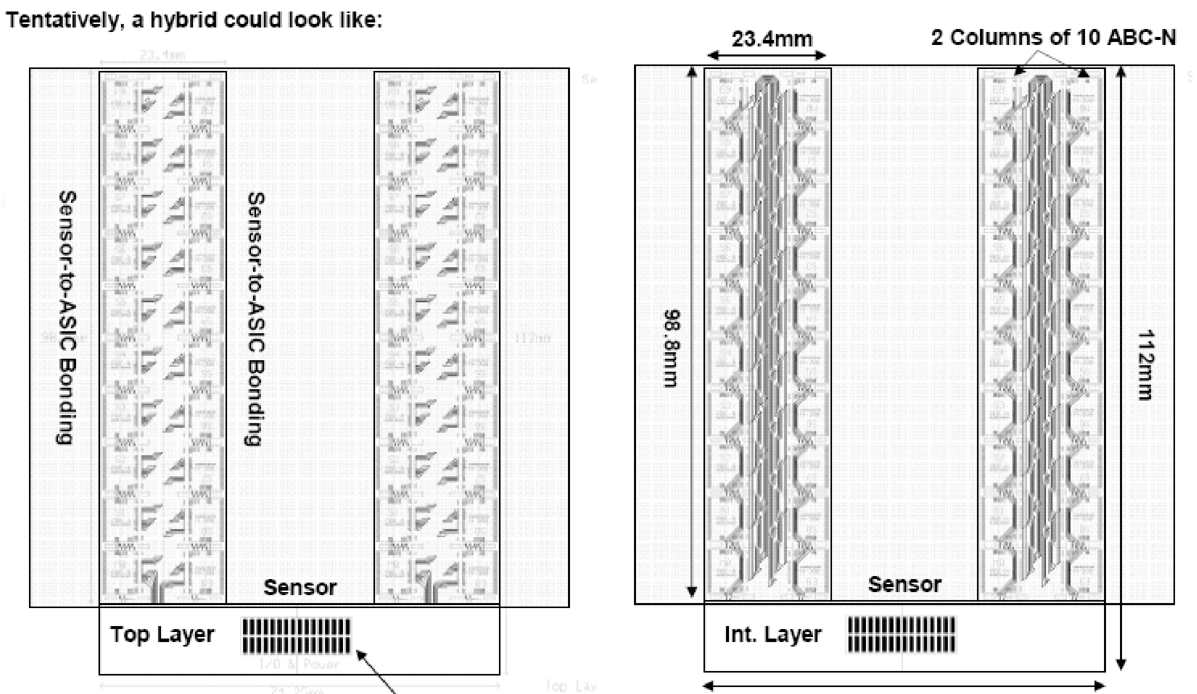
- 2 "fingers" per hybrid populated with 2 columns of ABC-Ns (20 ASICs per finger, 40 ASICs total)
- Chip-to-chip "direct" token and data passing added
- Provisional Redundancy scheme implemented on the hybrid
- Hybrid is electrically one object
- 4 Layer Kapton (conservative design)
- No tracking under ASIC front-end
- 2 Layers for routing and 2 for Power/Gnd planes
- 100um Track & Gap
- 350um Vias

- DCS, Module Power management, CLK/COM and Data buffering may require one or two(?) additional Module Controller ASICs per hybrid.

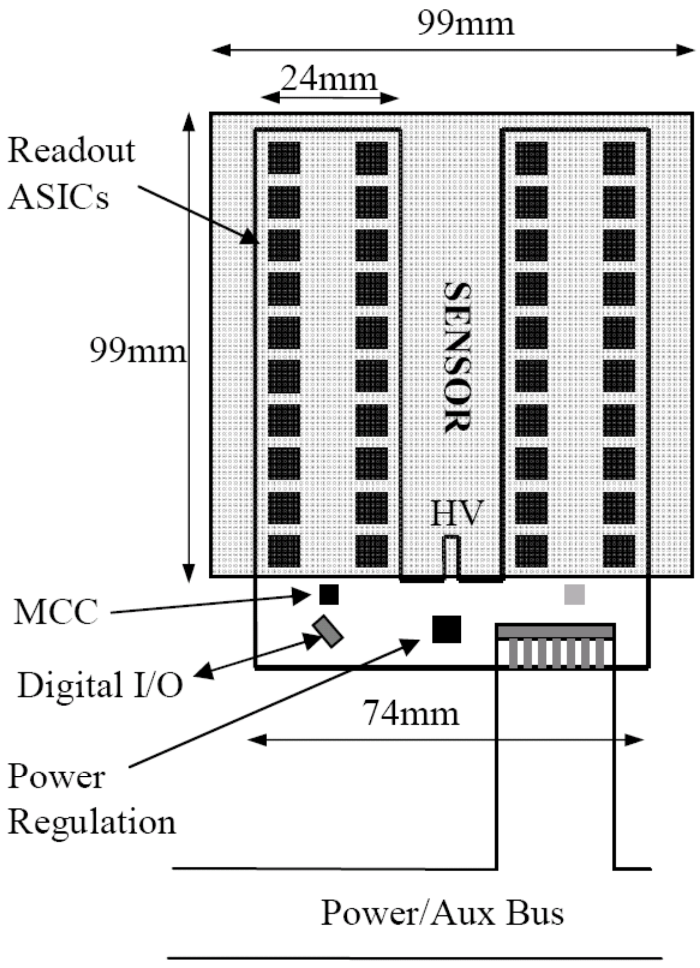
A. Greenall



Tentatively, a hybrid could look like:



Review of Hybrid concept



Detail

- Designed to match to a single sensor of 99mm x 99mm
- 2 ‘fingers’ per hybrid populated with 2 columns of 10 ABCNs (40 total)
- 4 Cu Layers with Kapton dielectrics
- Standard build (to maximise yield)
  - 100µm track and gap
- Wire bonding directly from ABCN to sensor
  - Eliminates the need for pitch adaptors
  - ABCN die size is fixed to 7.5mm width to allow this
  - Length is still unknown (currently 8.2mm)

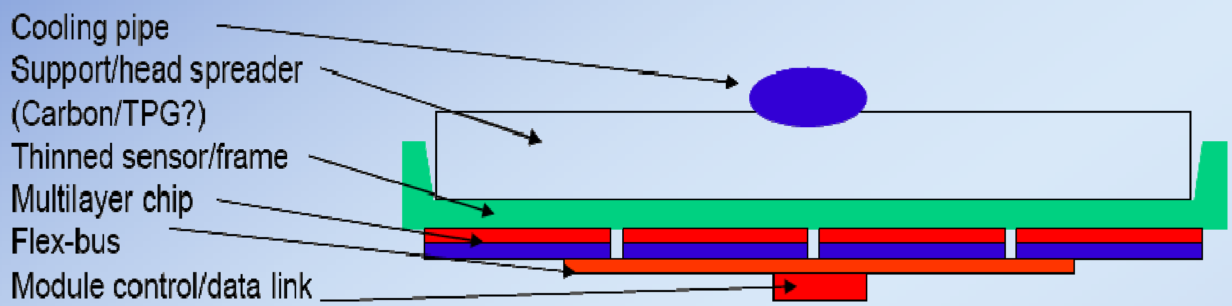
A. Greenall

MCC: Module Controller Chip

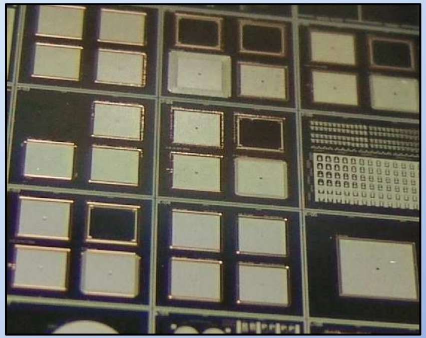
HEP R&D on Vertical (3D) Integration

- **Work already underway in Germany and US**
- **UK has purchased RD50 wafers for trials adding polyimide layers to Micron sensors**
- **Survey of companies for MCMD in progress**

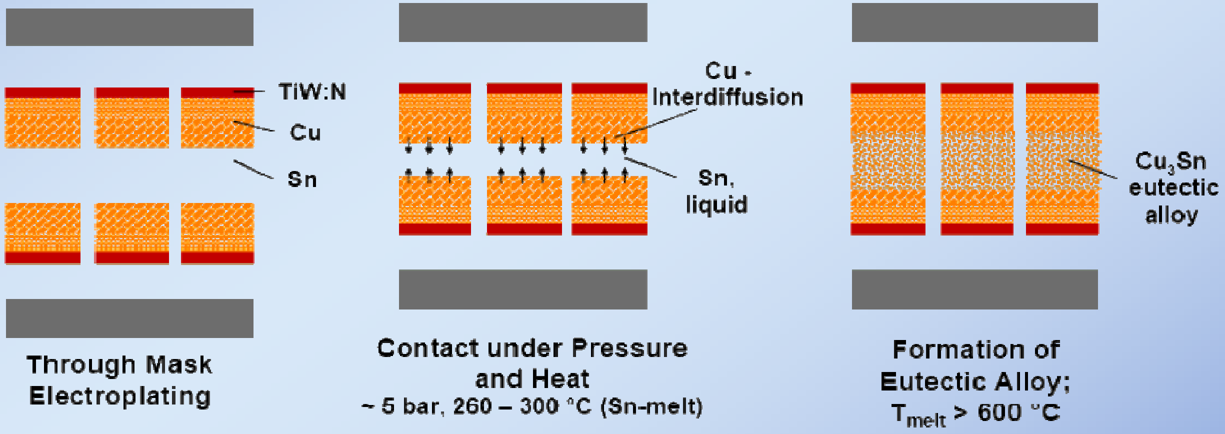
1) Low I_leak, low V_dep
2) Large live-fraction
3) SLID interconnection
4) 3D integration



First diodes



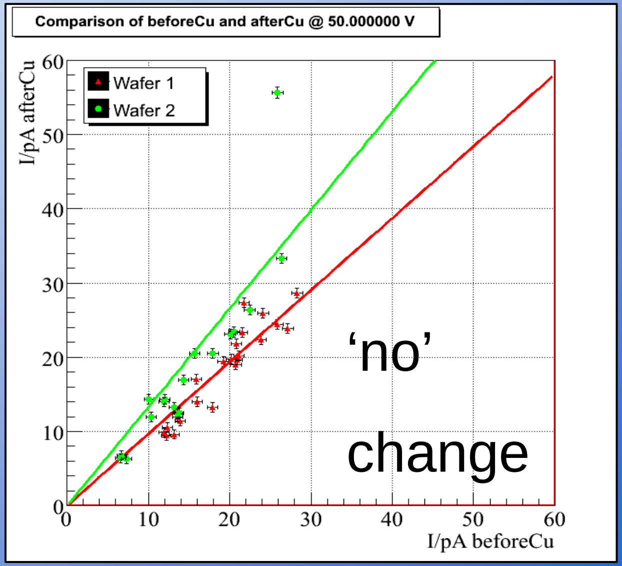
Solid Liquid Interdiffusion (SLID), IZM Munich



Through Mask Electroplating

Contact under Pressure and Heat ~ 5 bar, 260 – 300 °C (Sn-melt)

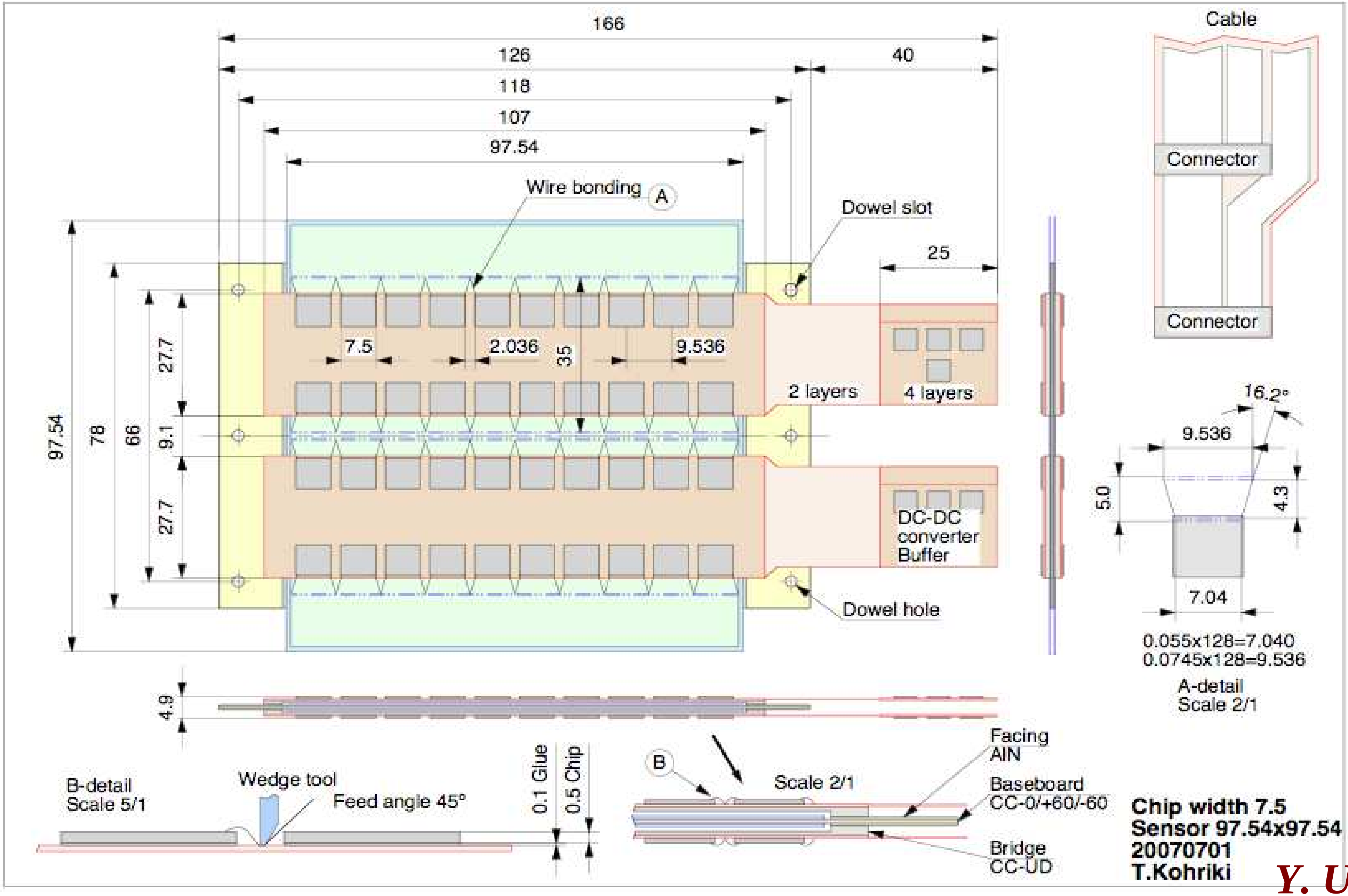
Formation of Eutectic Alloy; T_{melt} > 600 °C



Conducted by: Bonn, Dortmund, MPI, Oslo, Interon, IZM

Double-sided Hybrid Designs - KEK

Four hybrids/module, four connectors/module square sensors (9.754 cm x 9.754 cm)



Chip width 7.5
Sensor 97.54x97.54
20070701
T.Kohriki

Y. Unno

SLHC module - Optimization

FEA thermal analyses using ANSYS

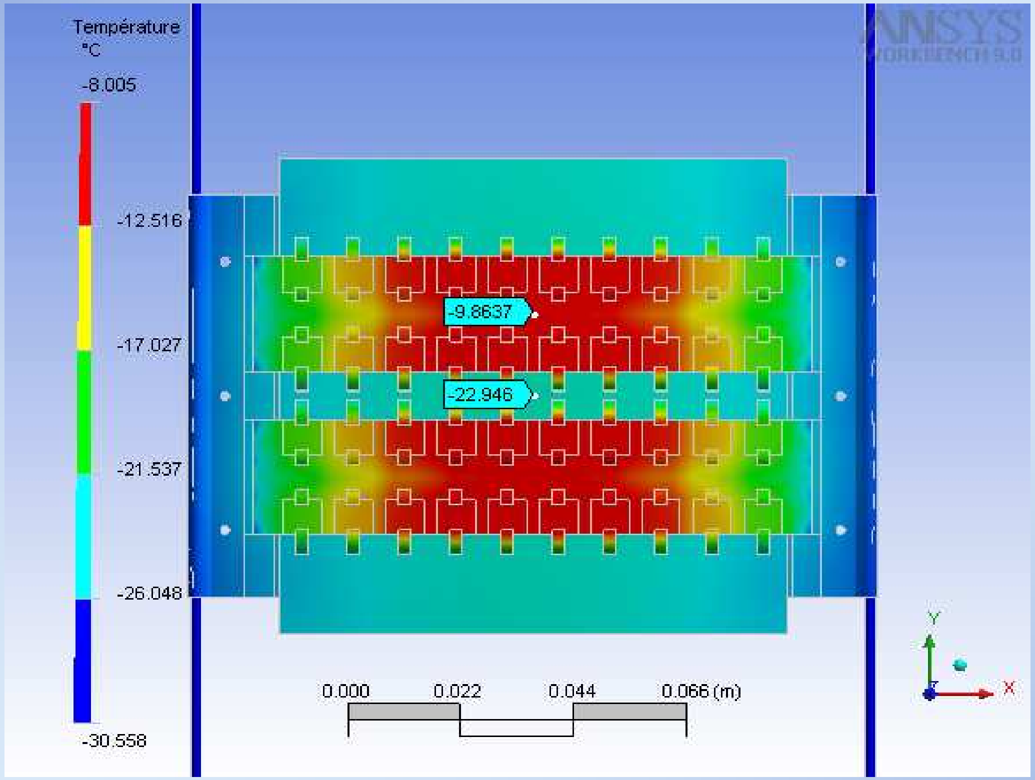
Need cooling from both ends (current ATLAS single-ended cooling)

(2-dimensional calculation)

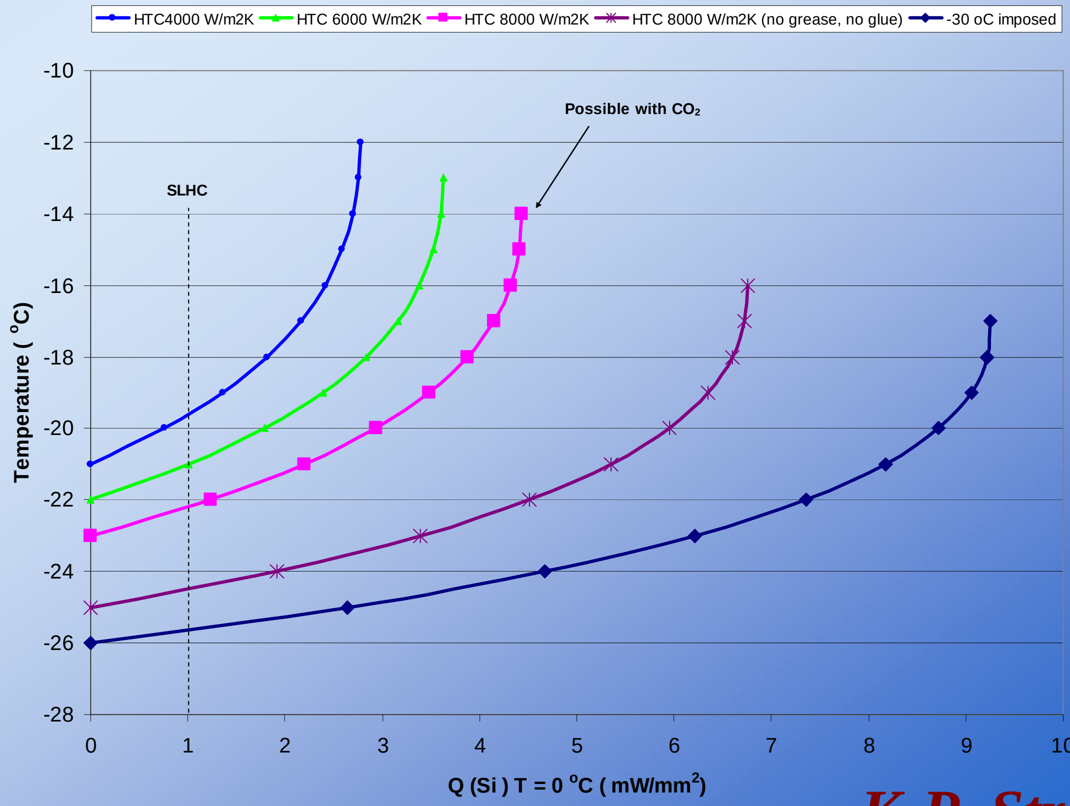
- 0.1mm thick thermal grease around cooling pipe (2W/m/K)
- Dead air between sensor and hybrid (0.024W/m/K)

Thermal distribution

2mW/ch, HTC 8000 W/m²K, -30 ºC, <u>Q (Si) = 0</u>



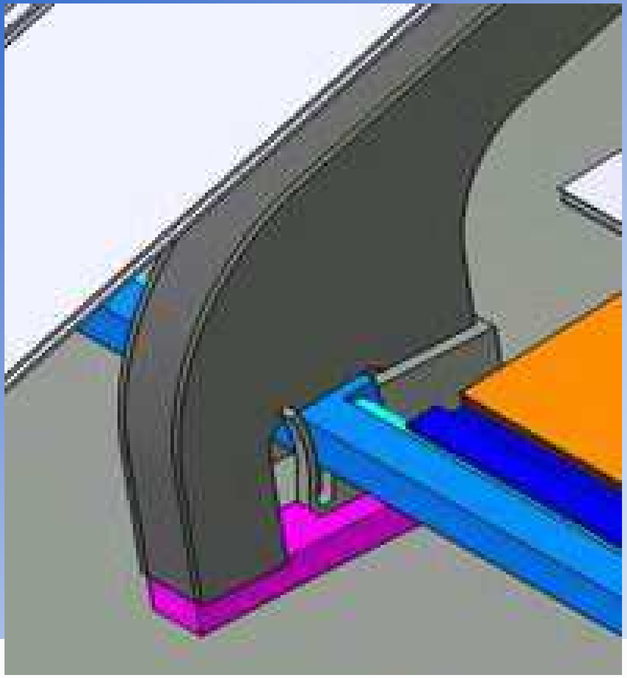
Runaway simulations for different cooling systems (cooling -30 ºC , 2mW/ch)



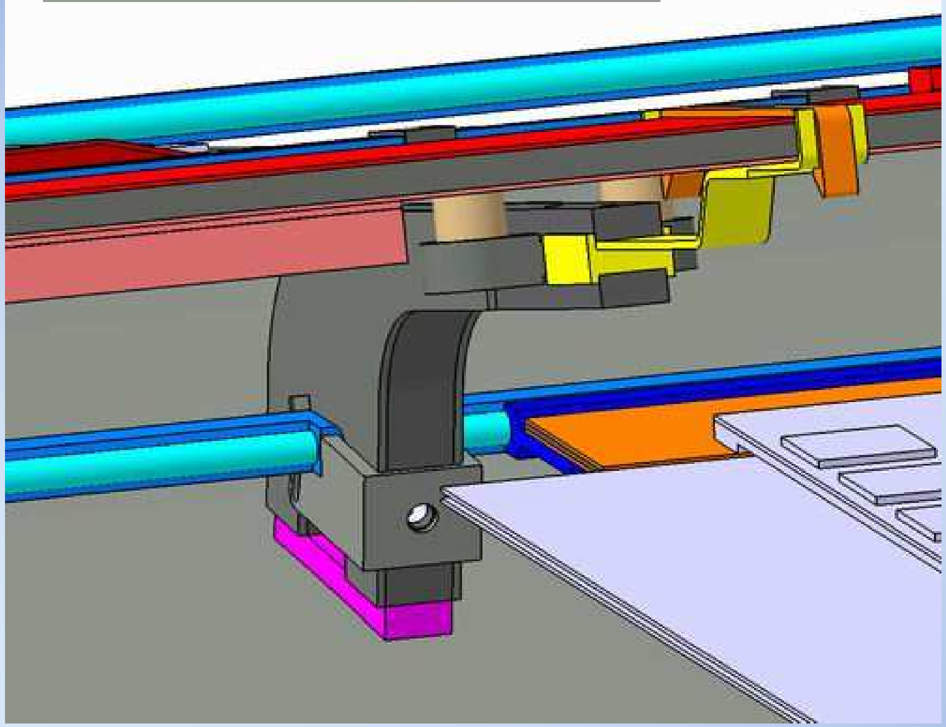
K-P. Streit

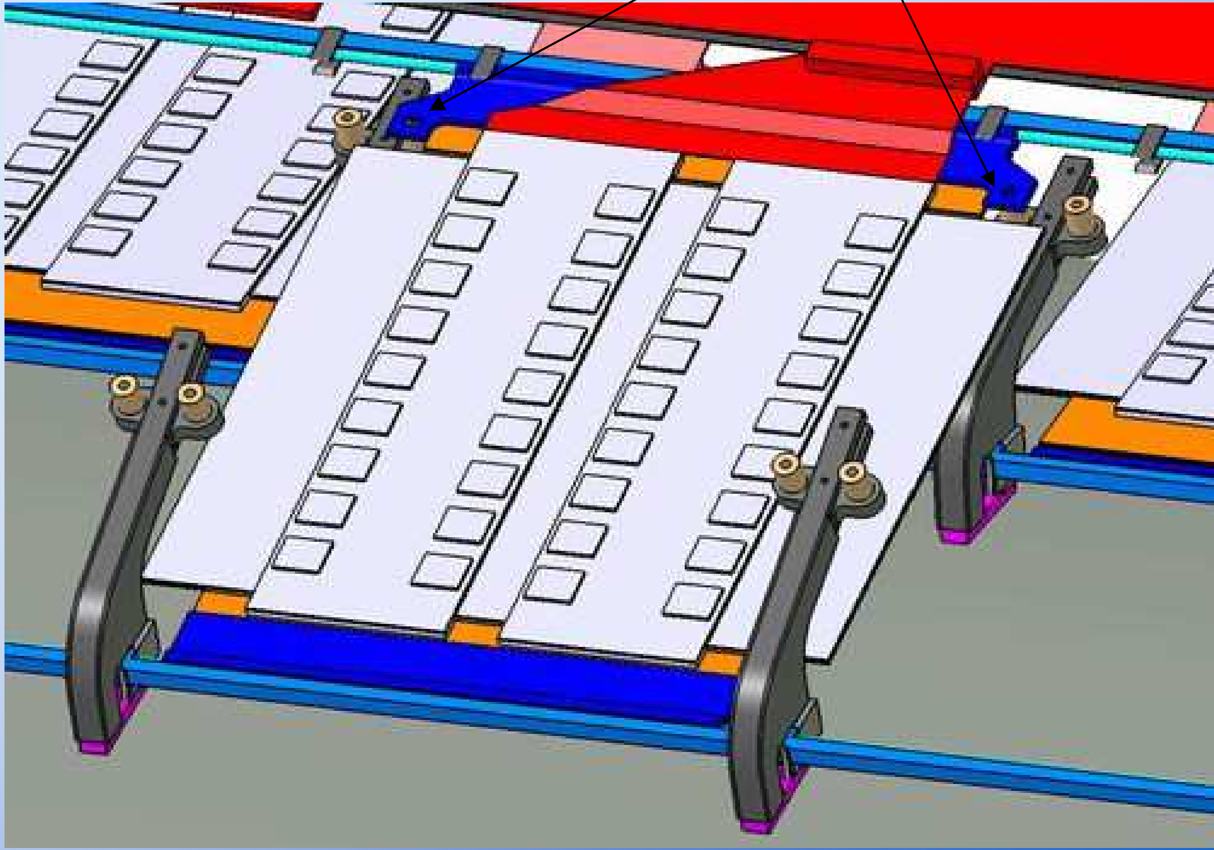
Individual Module - Direct Mounting

- 3rd “point” is defined by the pipe
- Cooling block is set with 2 fixation points on the pig-tail side
- 1 bracket is holding 2 neighboring modules
- The bottom left pipe is embedded in the brackets and must be assembled before the module.



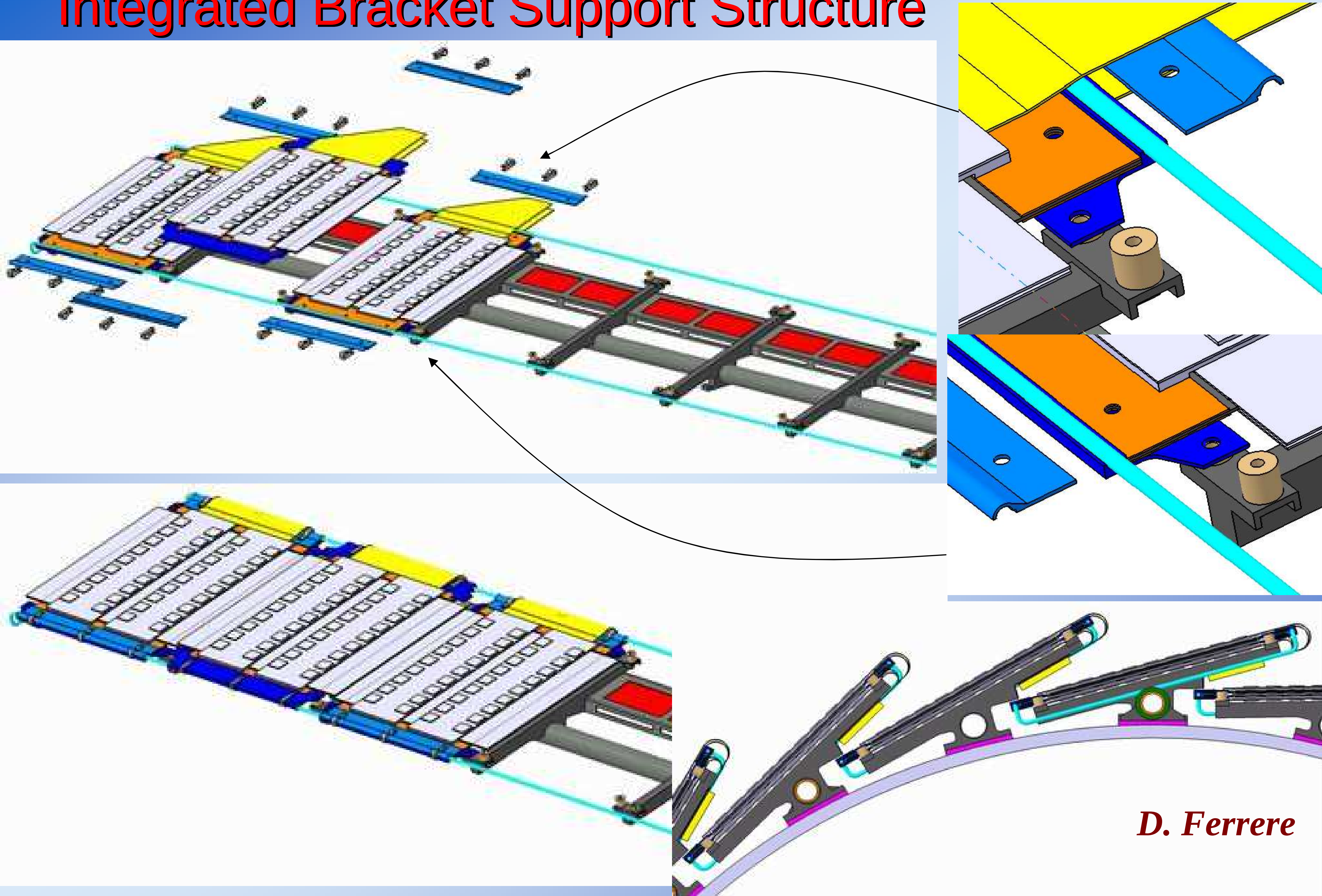
Y. Unno





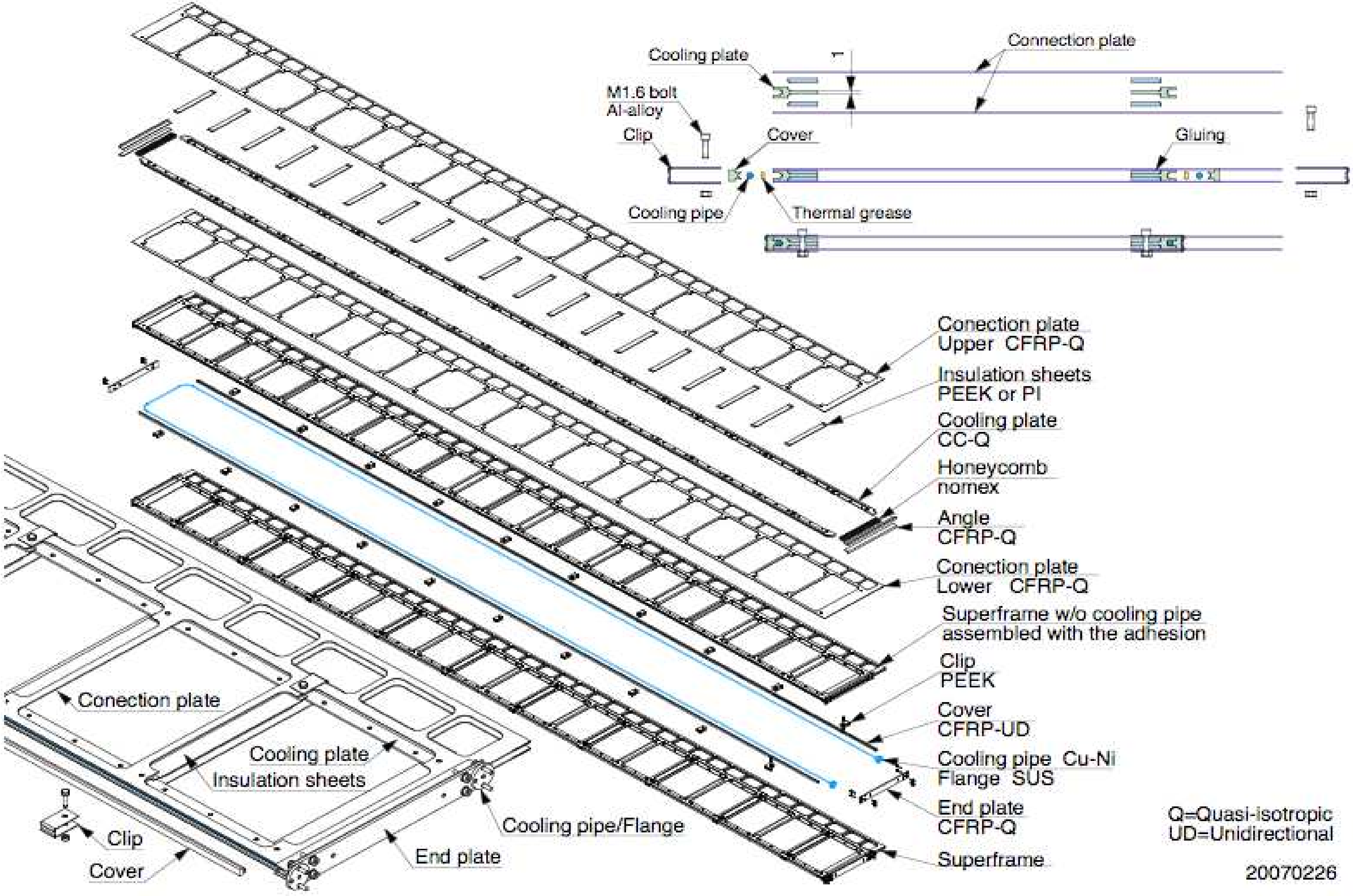
2 fixed mounting points

Integrated Bracket Support Structure



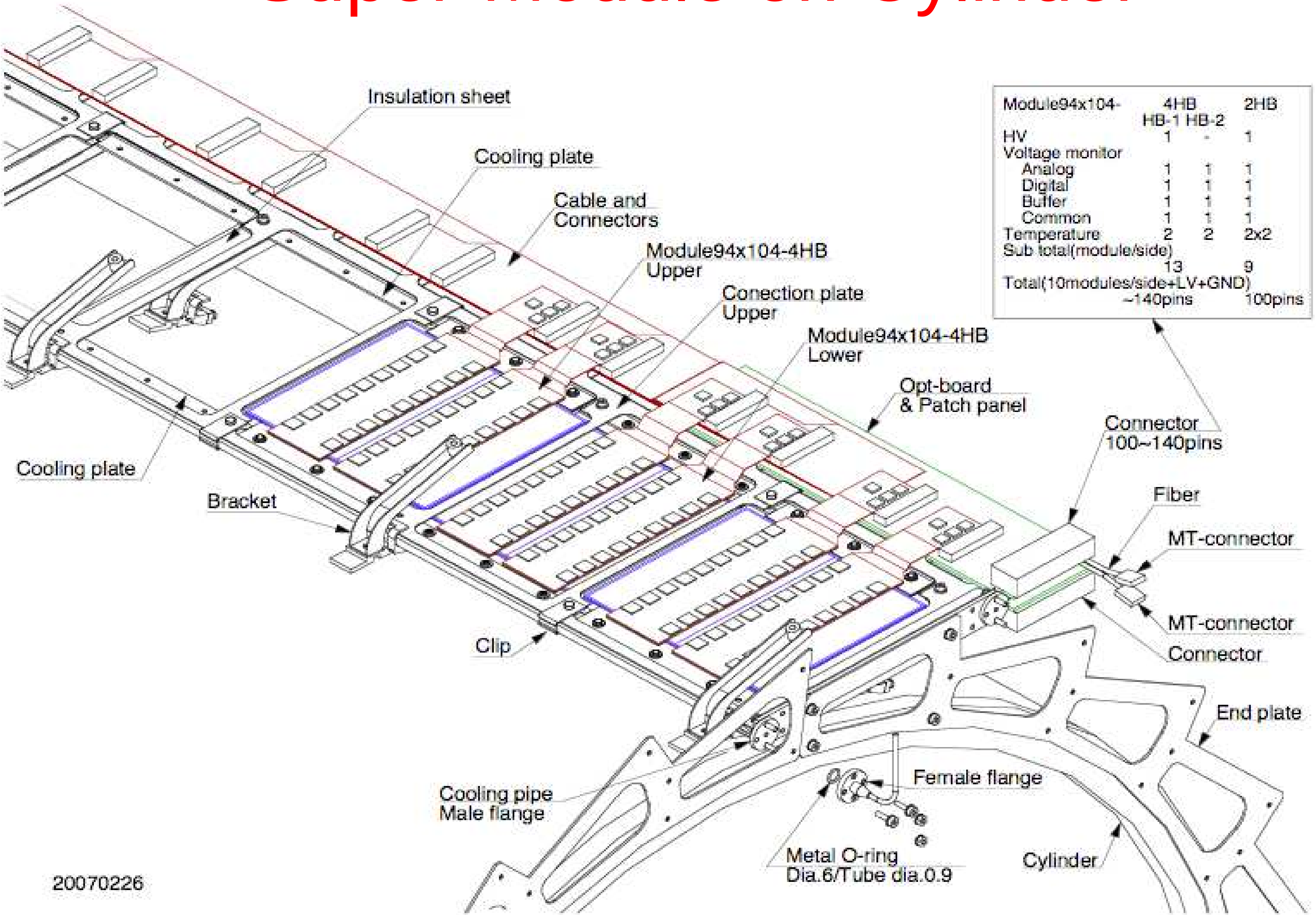
D. Ferrere

Super-Module Concepts: Super-Frame



Y. Unno

Super-Module on Cylinder



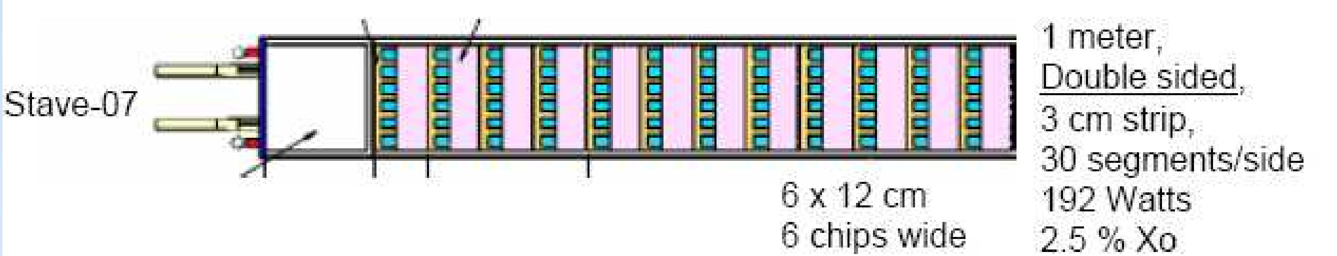
Module94x104-	4HB		2HB
	HB-1	HB-2	
HV	1	-	1
Voltage monitor			
Analog	1	1	1
Digital	1	1	1
Buffer	1	1	1
Common	1	1	1
Temperature	2	2	2x2
Sub total(module/side)	13		9
Total(10modules/side+LV+GND)	~140pins		100pins

Y. Unno

Stave Module Concept

- The “stave” concept has hybrids glued to sensors glued to cold support
- A first prototype version based on the CDF run-IIb concept but using ATLAS ASICs already exists

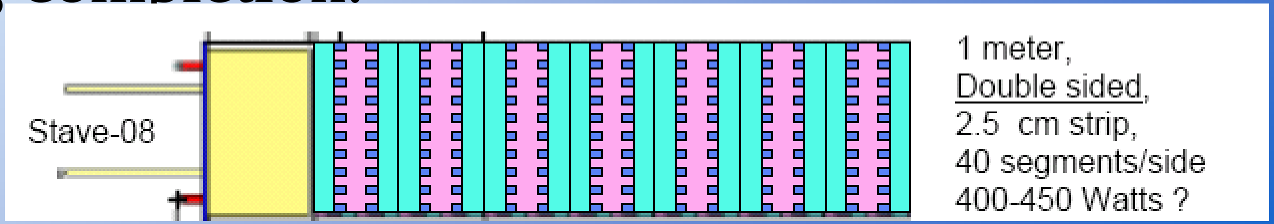
- A 6-chip wide version (Stave 2007) will use short p-in-n sensors and incorporate many of the final proposed, mechanical, thermal, electrical, serial powering and read-out features.



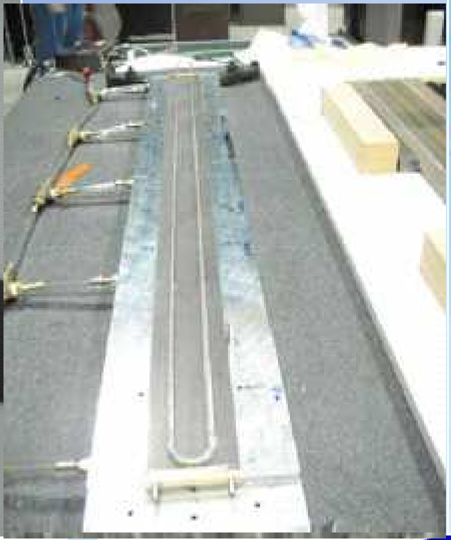
- The first prototype staves are expected by Autumn this year
- Stave core fabrication, BeO hybrid design, cooling concepts and automated assembly nearing completion.

C. Haber

- 10 chip wide version under development



Stave R&D



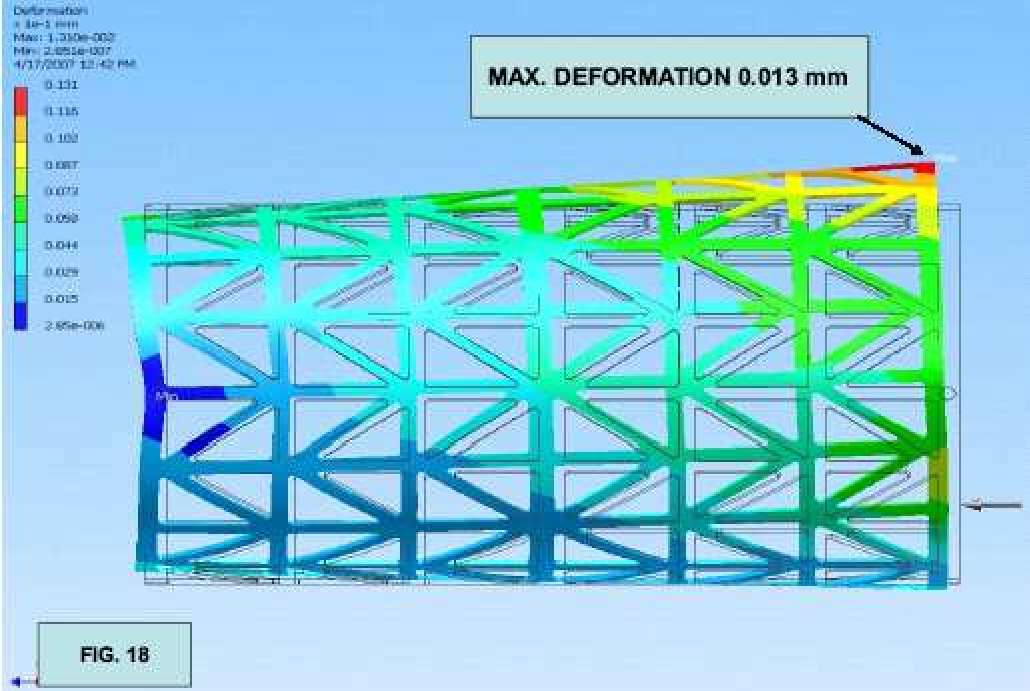
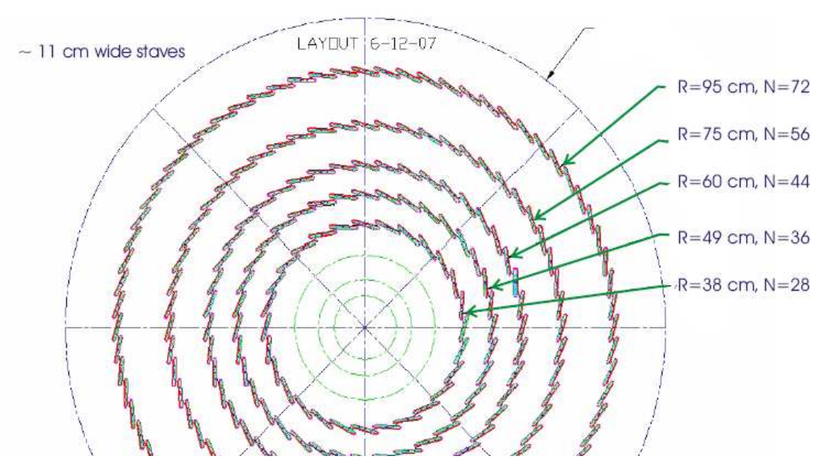
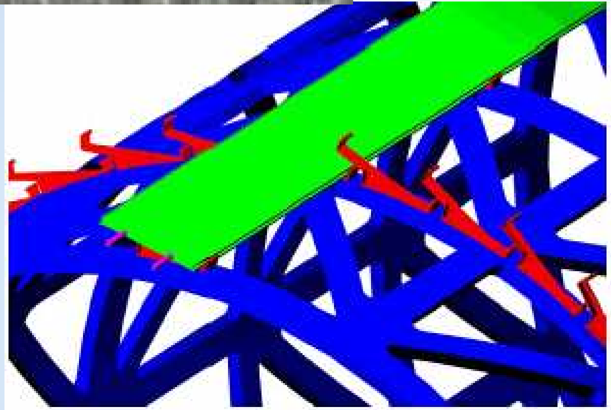
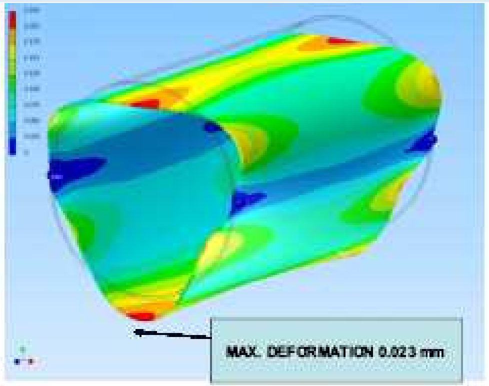
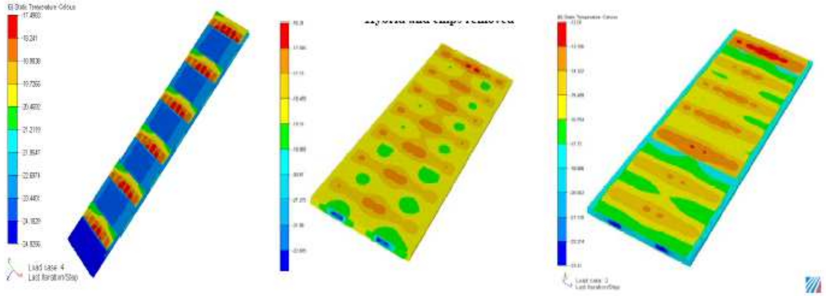


FIG. 18







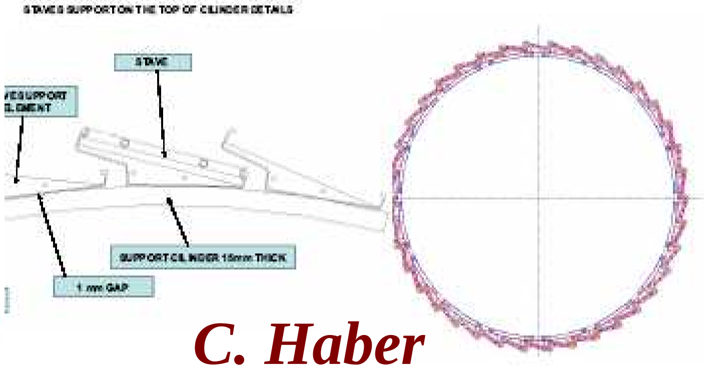


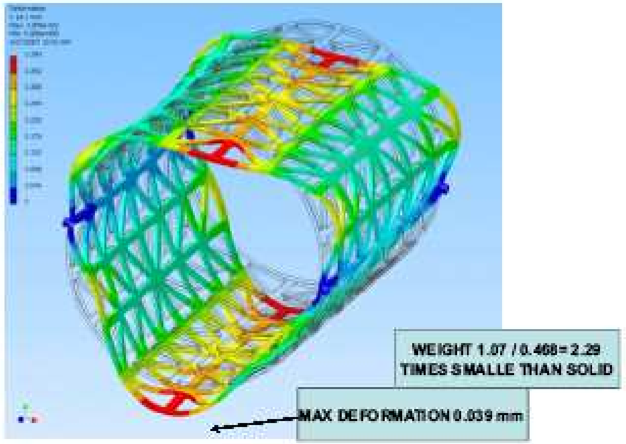
Single sided / DS low cable TC / DS high cable TC

-17.5 C Chip/Silicon -23.5 C

-12.6 C Chip/Silicon -13.6 C

-16.7 C Chip/Silicon -17.4 C



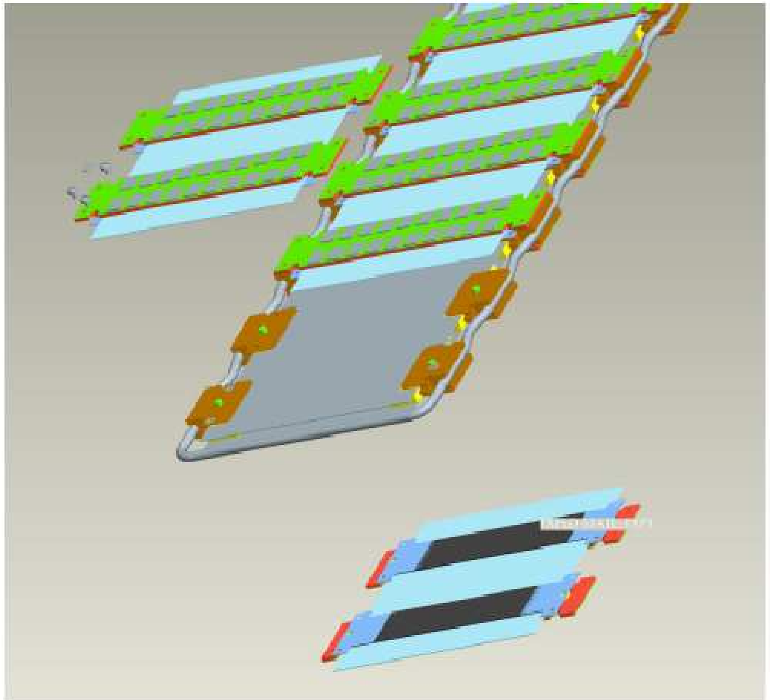


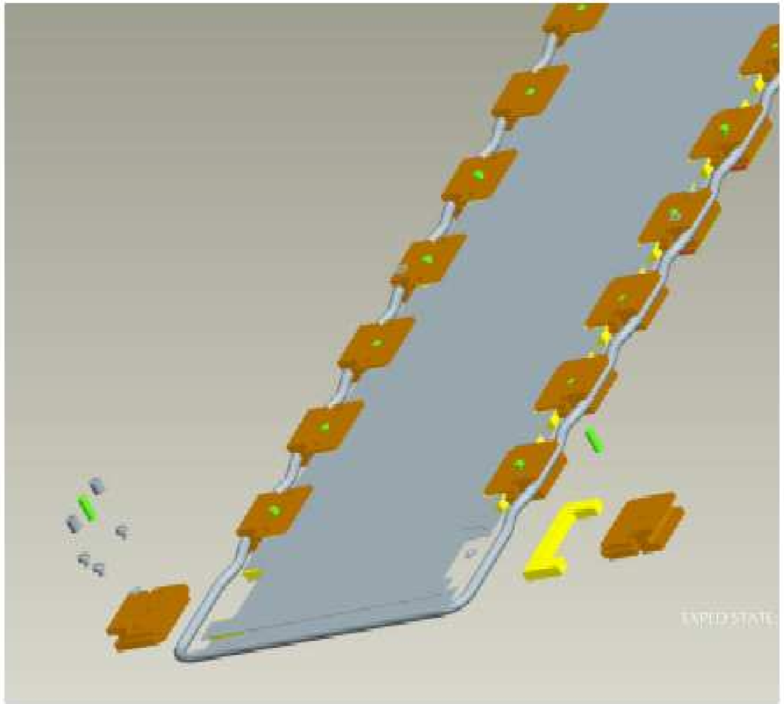
C. Haber

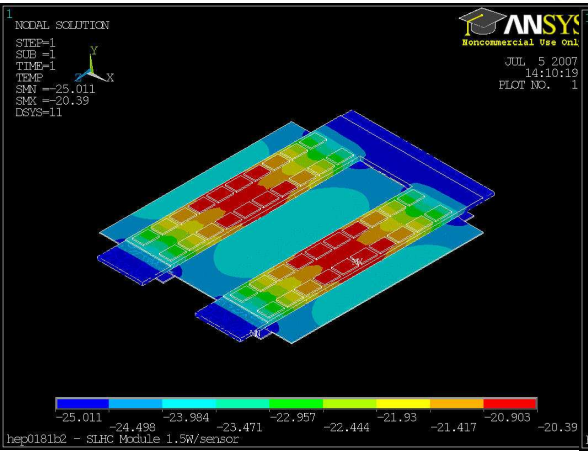
Single-sided Concept

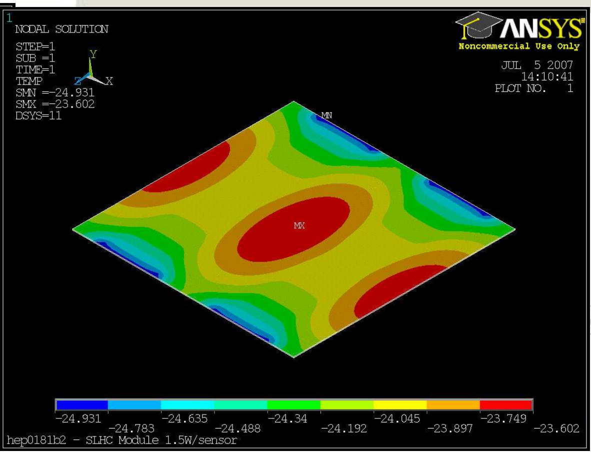
Bridged hybrid assemblies on cooled support

1.5W/Sensor
Max Chip temp: -20.4C
Max Silicon Temp: -23.6C
Temp Gradient over Si: 1.33C

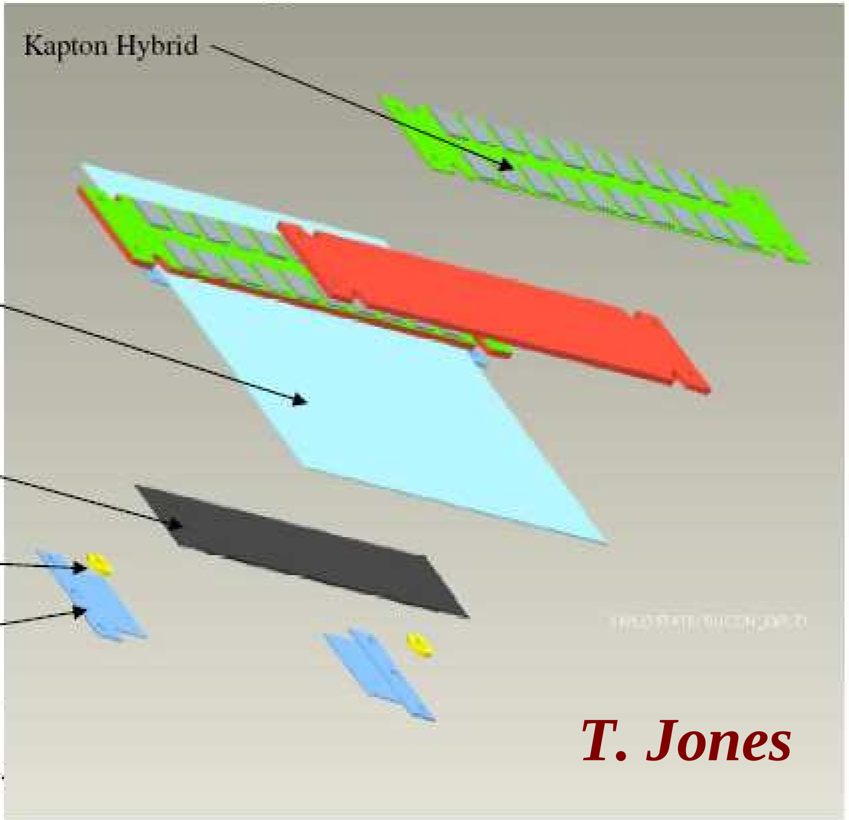








Possible Demountable Module/Stave Concept (single-sided assembly step)



Kapton Hybrid

Silicon Sensor

TPG Heat Spreader

Precision Location Washer

Alumina location tab

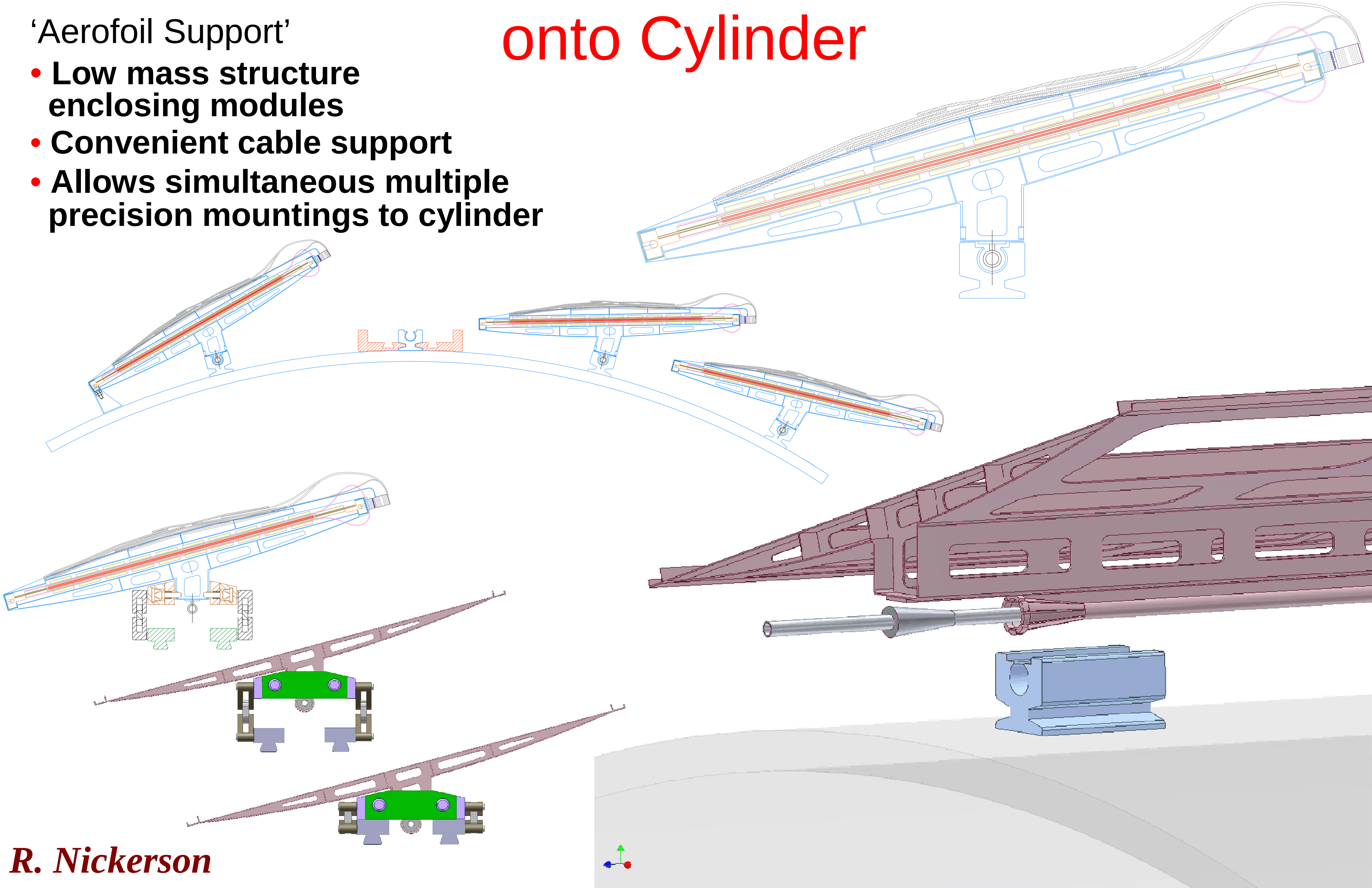
- Single sided silicon module.
- Alumina and TPG heat spreader, spliced as in ATLAS module.
- Integral precision location washers (holes and slots)
- Carbon Carbon hybrid base, with added non conductive spacers.

T. Jones

Alternative Mounting Scheme for Super-Module onto Cylinder

‘Aerofoil Support’

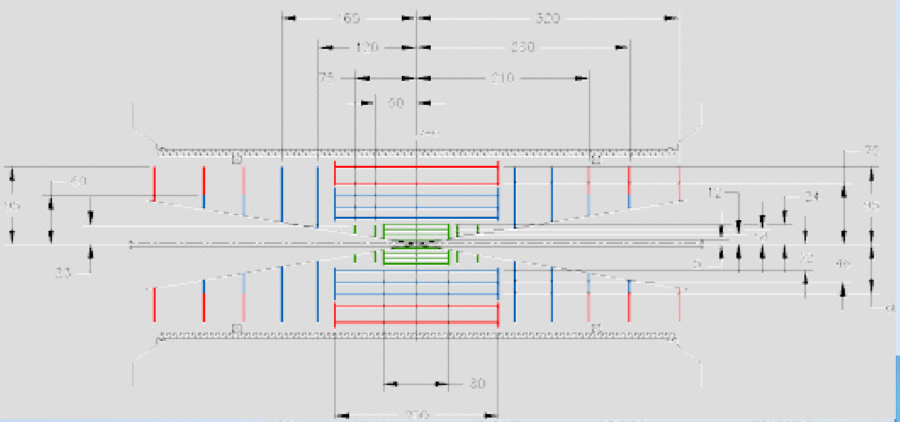
- **Low mass structure enclosing modules**
- **Convenient cable support**
- **Allows simultaneous multiple precision mountings to cylinder**



R. Nickerson

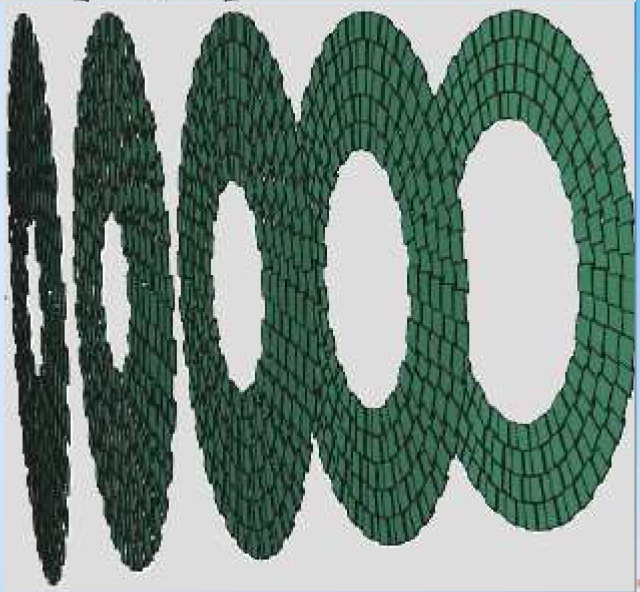
Forward Module Concepts

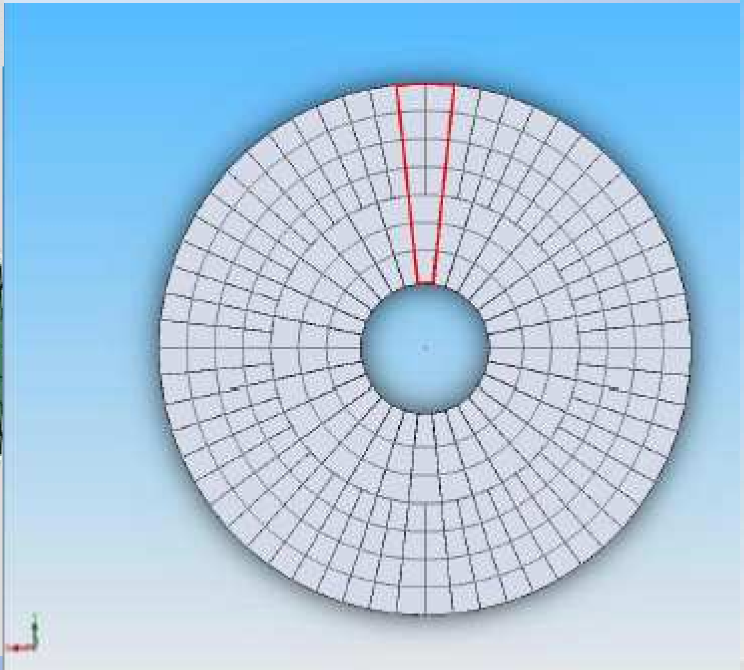
- As for current ATLAS SCT, Forward Modules likely to require several different wedge shaped sensors
- 5 discs on each side with outer radius 95cm and inner radii from 30cm

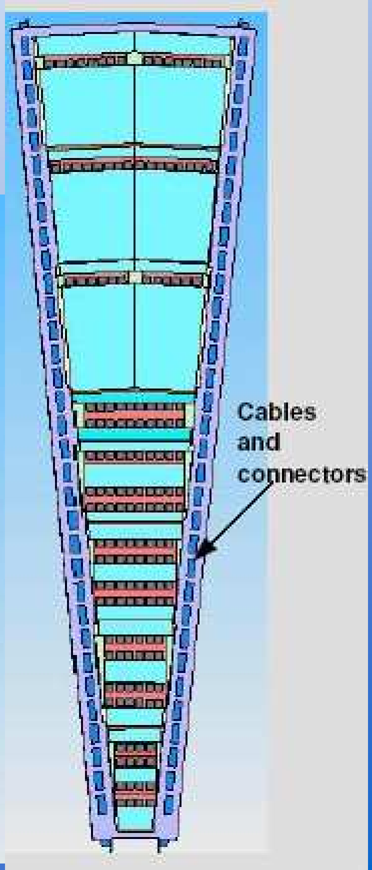


Can consider super-modules/staves or individual modules as now

Mean pitch about 80μm as at present







C. Lacasta

Detectors for sLHC

G. Casse
University of Liverpool Group
6th December 2007

- Proposed Tracker Layout and Simulations (Radiation and Occupancy)
- Sensor and FE Electronics R&D
- Microstrip Module and Engineering Concepts
- **Power, DCS, Opto-electronics, Services, Cooling, …**
- Conclusions

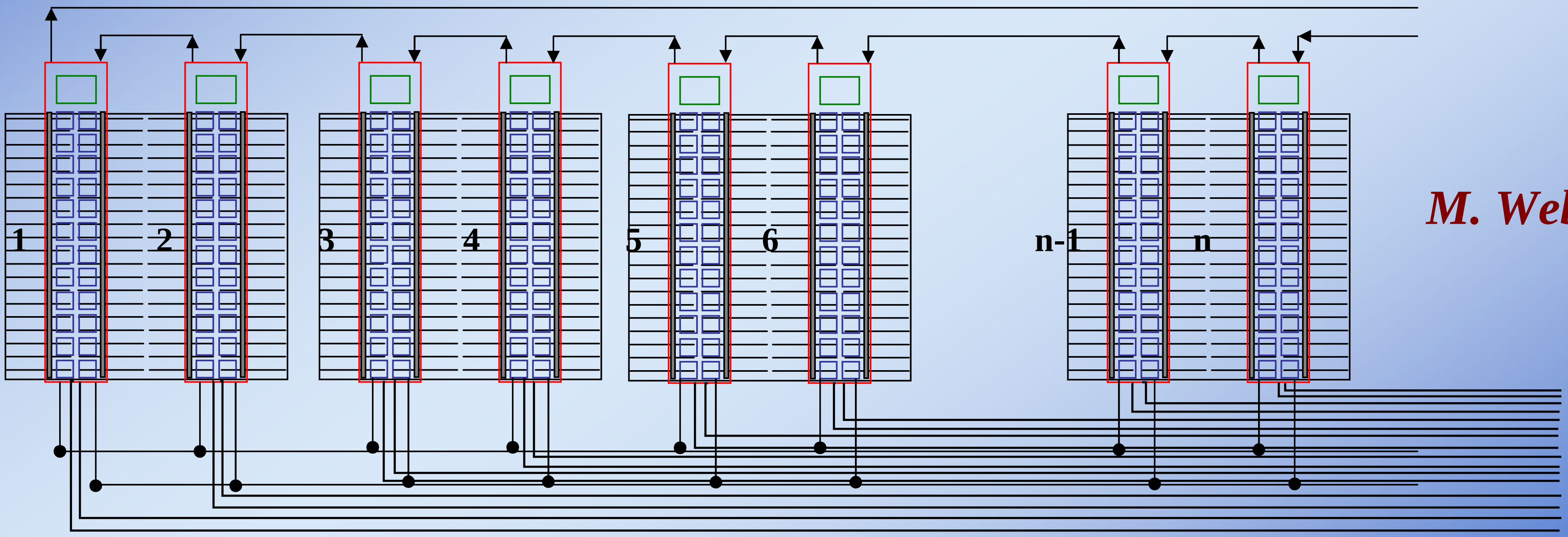
Powering Issues

V_{ABC-N} = 2.5 V; I_{Hybrid} = 2.4 A; 20 hybrids. **Low V + High I ➔ I^2R losses in cables**
(Want power transmission at High V + Low I)

Serial Powering: n=20; $I_H = I_{PS} = 2.4$ A; $V_{PS} = nV_{ABC-N} = 50$ V

Also saves factor ~8 in power cables/length over SCT

- Need detailed studies of failure modes and recovery



M. Weber

DC-DC Conversion : n=20; g =20; I_{PS}= n/g I_H = 2.4A; V_{PS}= gV_{ABC-N}= 50V

Parallel powering also saves factor ~8 in power cables as for Serial Powering

- Issues with switched capacitors (noise?) and need for custom design to get large g

(Independent powering with DC-DC costs too many cables)

Total Microstrip Power

	BIS	BOS	ECA	ECB	Total
Power [kW]	71.8	45.7	18.3	18.3	154.2
	47%	30%	12%	12%	

- Going to $P_{chan} = 2mW \rightarrow P_{total} = 120kW$,
- Several contributions missing (SMC, Opto-converter, DCS, etc…)
- Best guess (strips) $P_{total} = 150kW$ within ±40kW (2-3×SCT).
- Dominated by barrel (even if BOS shortened).
- Investigating cooling using C_3F_8 (again), C_2F_6 or CO_2
- Reuse of existing services could represent a major challenge

G. Viehhauser

DCS: SLHC- Services

of rows (draft) - SLHC Strawman Layers for barrel:

Layer	# of rows	Radius (mm)
SS layer 1	28	380
SS layer 2	36	490
SS layer 3	44	600
LS layer 1	56	750
LS layer 2	72	950

Numbers not yet available for the ECs

Estimation of 2 interlock temperature sensors per cooling loop → 944 NTCs in total

SCT barrel DCS: 48 type 2-DCS cables of (28 pins Milli-Grid) → 672 twisted pairs!
SCT ECs DCS: 80 type 2-DCS cables of (28 pins Milli-Grid) → 1120 twisted pairs!

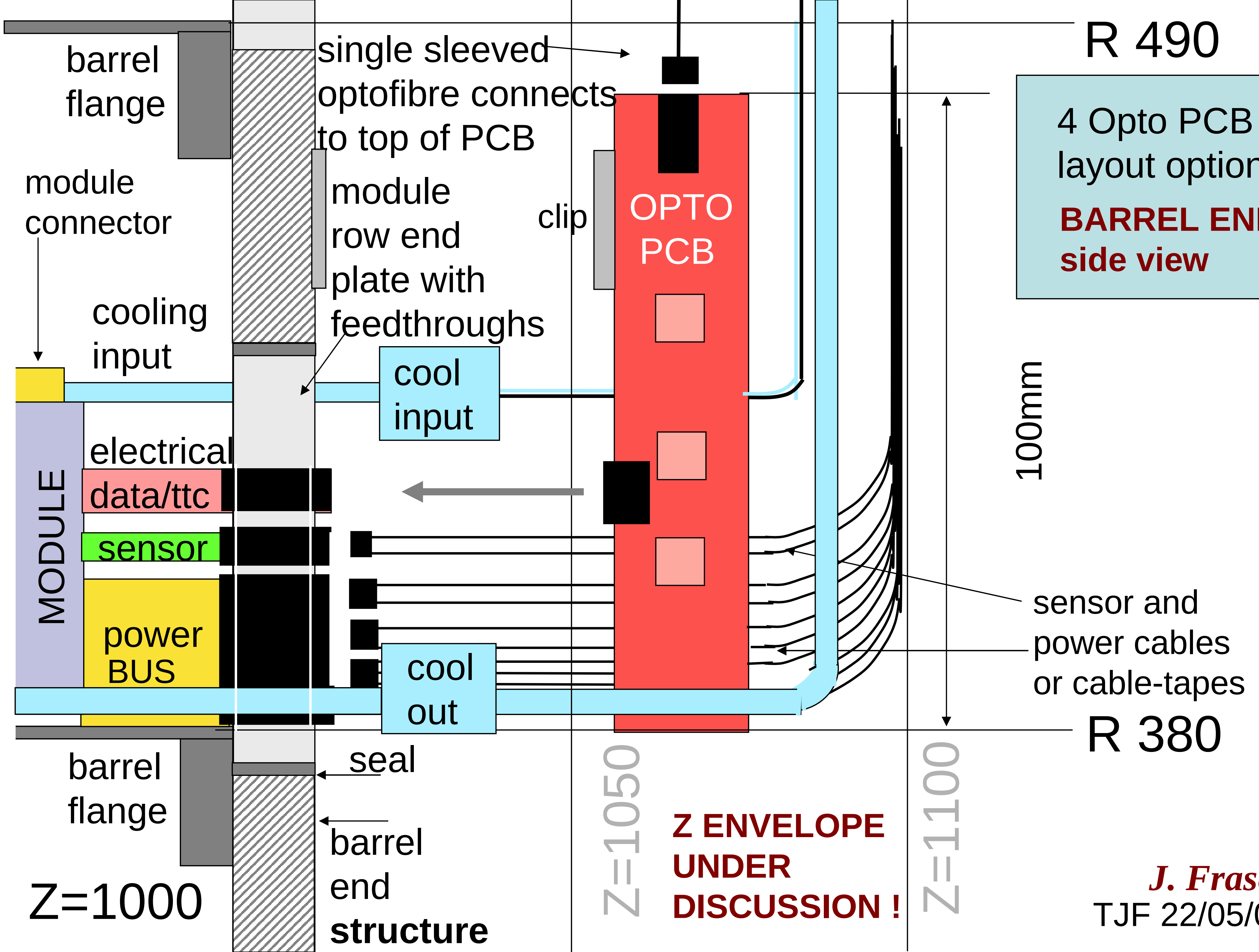
Barrel SS layers could use the current barrel DCS type 2 for the interlock & LS could use part of the current EC DCS type 2.
→ Most probably NOT enough left for the SLHC ECs

Can existing cables be used?
What type of connectors required and where?

D. Ferrere

4 Opto PCB
layout option

BARREL END
side view



R 490

barrel
flange

single sleeved
optofibre connects
to top of PCB

module
connector

module
row end
plate with
feedthroughs

clip

OPTO
PCB

cooling
input

cool
input

100mm

MODULE

electrical
data/ttc

sensor

power
BUS

cool
out

sensor and
power cables
or cable-tapes

R 380

barrel
flange

seal

barrel
end
structure

Z=1000

Z=1050

Z ENVELOPE
UNDER
DISCUSSION !

Z=1100

J. Fraser
TJF 22/05/07

Conclusions

- **Activities in many areas still just starting with emphasis on completion and commissioning of current ATLAS Detector**
- **Management structure includes Upgrade Steering Group, Upgrade Project Office and 8 working groups in the area of the tracker replacement alone**
- **Major recent tracker workshops include: Genoa (18/7/05 - 20/8/05), Liverpool (6/12/07- 8/12/07) and Valencia (10/12/07- 12/12/07)**
- **Some impressive progress, but still plenty to do and not so much time to do it …**

  ATLAS Inner Detector Technical Design Report now 10 years old
  http://atlas.web.cern.ch/Atlas/GROUPS/INNER_DETECTOR/TDR/tdr.html
- **For more material of past internal meetings see ATLAS *indico* pages** ***http://indico.cern.ch/categoryDisplay.py?categId=350***