N-in-p silicon detectors for the SLHC

University of Bonn Seminar

15 December 2005

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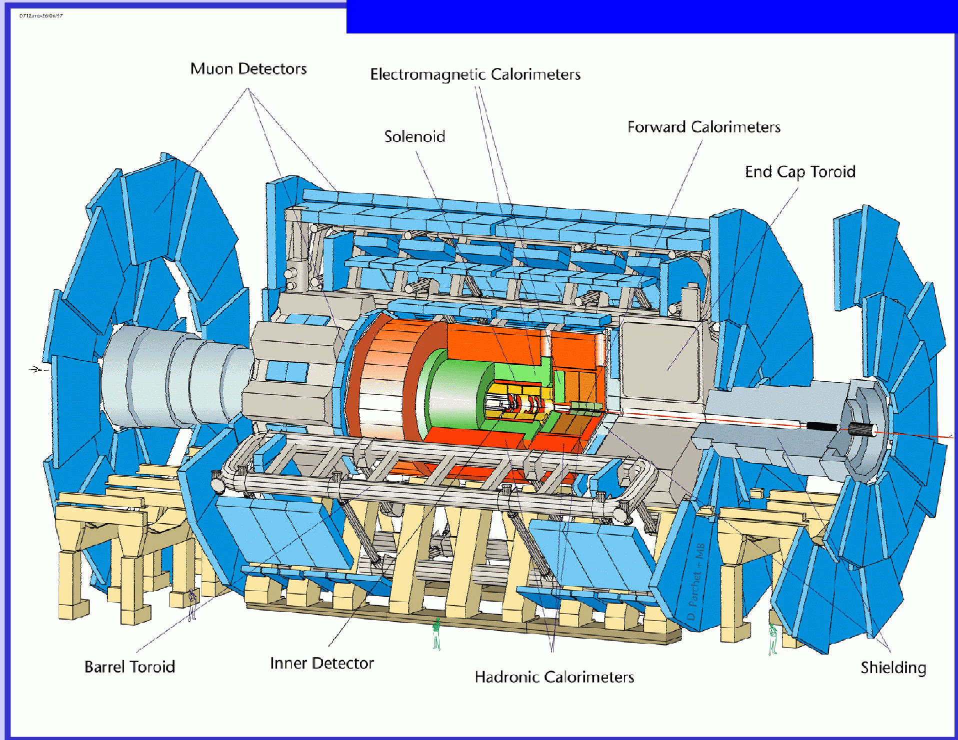
THE UNIVERSITY of LIVERPOOL

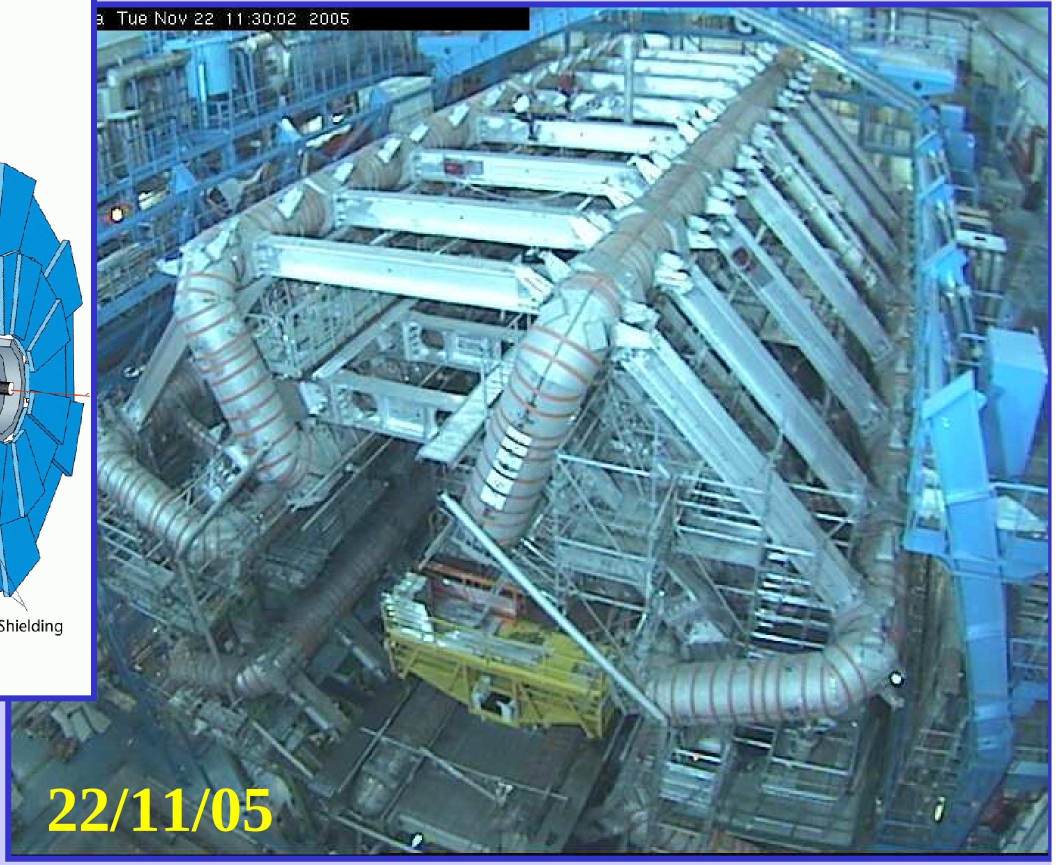
Outline

This talk takes the ATLAS Tracker upgrade as an example of application of p-type detectors. The results about detector technology are though transferable to every other high radiation environment. Concerning the details of ATLAS or other upgrades at sLHC, they are obviously very preliminar!

- Current ATLAS tracker *(just to fix the ideas about the challenge waiting for us)* .
- SLHC proposal
- ATLAS tracker upgrade
  - Layout, occupancy and dose rate
  - **Sensor technologies: already a viable solution?**
  - Thermal issues
  - Other issues (cooling, electronics, ..)
- Summary

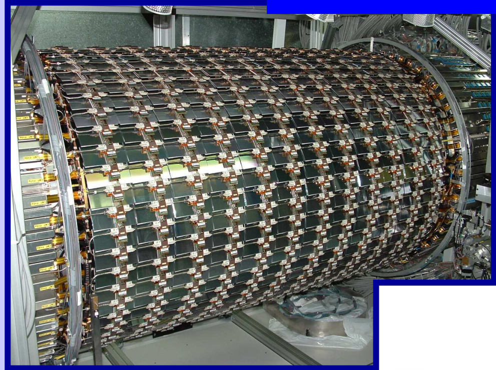
ATLAS Status

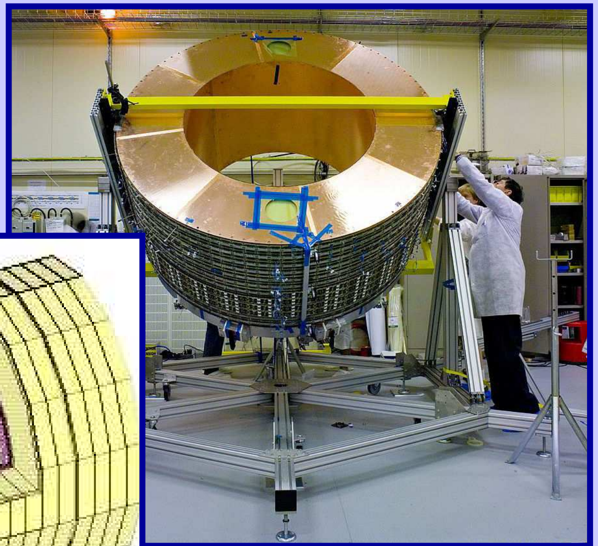


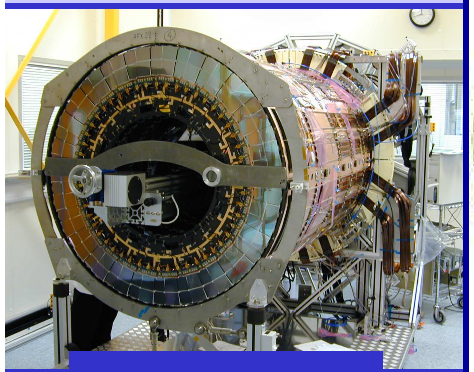


- most sub-detector assembly work coming to an end
- Integration and installation in the pit: now + next year
- Commissioning, cosmic tests: now until 2007
- summer 2007: single beams and .. Collisions!

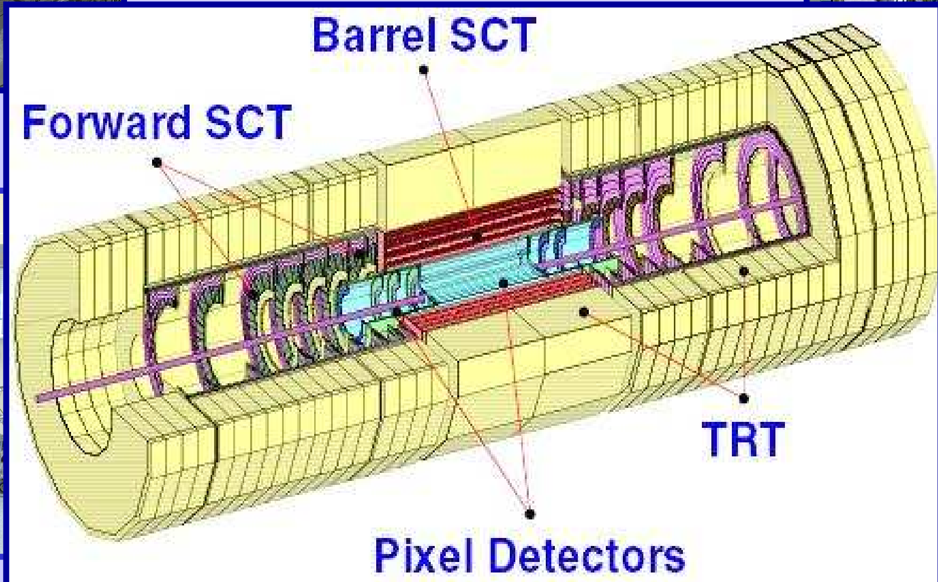
ATLAS Inner Tracker



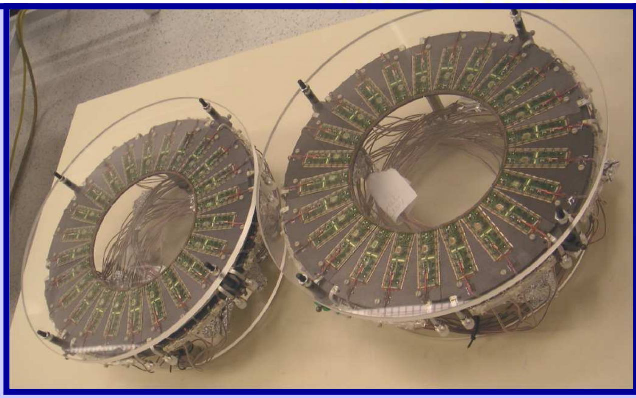


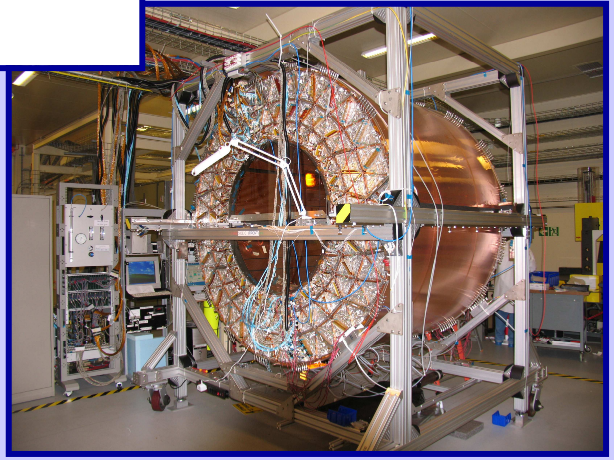


Last week



diameter: 2.3m
length: 7 m
B-field: 2T





Constraints on current inner tracker

Tracking requirements:

- Efficient tracking/pattern recognition ($|\eta| < 2.5$)
- High momentum resolution ($\Delta p/p < 30\%$ for p = 500 GeV/c)
- Efficient b-tagging
- Fast trigger (level 2)

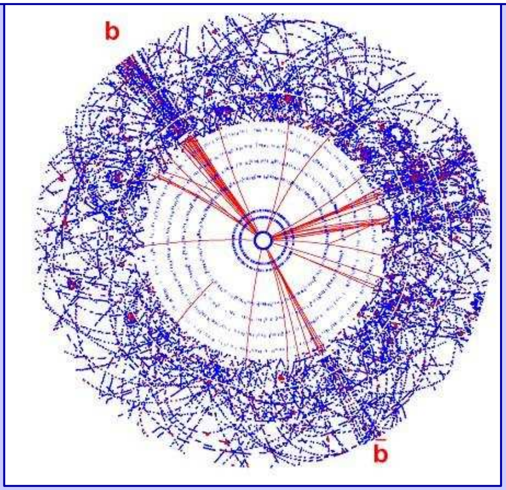
Environment:

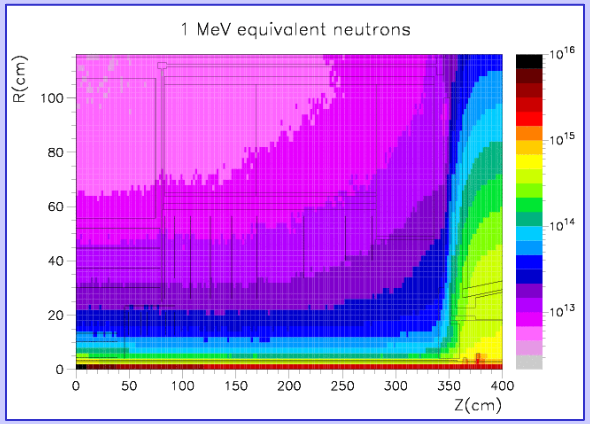
- High multiplicity environment.
  LHC: 3 years $L=10^{33}cm^{-2}s^{-1}$, then $L= 10^{34}cm^{-2}s^{-1}$
- High radiation levels.
- 25 ns bunch-crossing
- 10 years operation

Detector requirements

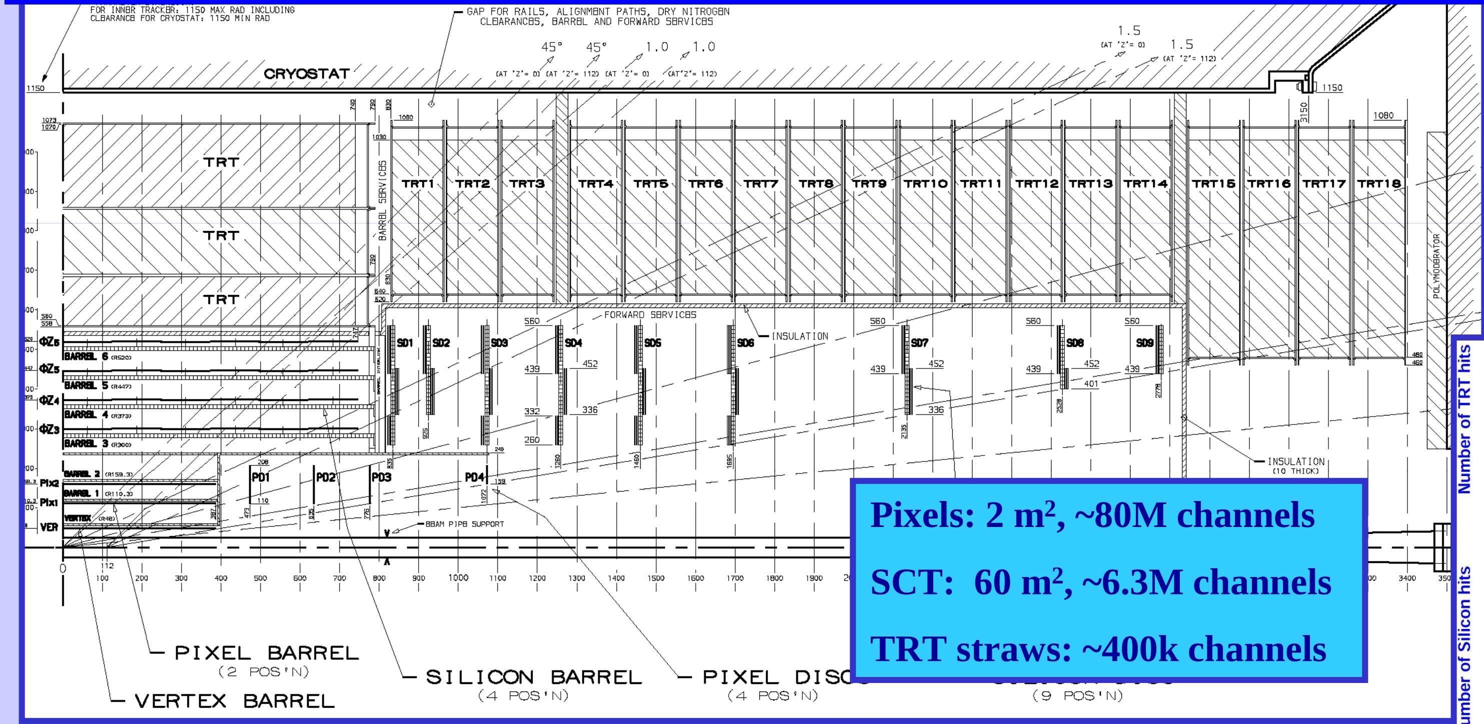
- Several space points with adequate precision in rφ and z to limit ambiguities.
- Very precise rφ space points over significant range of radii
- Limited material
- Precise space point near IP

~23 collisions and ~2000 tracks per bunch crossing





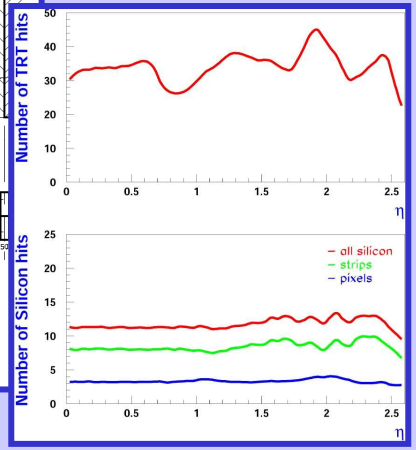
Current Atlas inner tracker

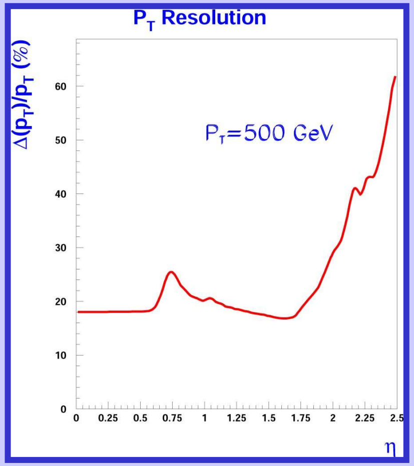


Pixels: 2 m^2, ~80M channels

SCT: 60 m^2, ~6.3M channels

TRT straws: ~400k channels





Pixels (50 μm × 400 μm): 3 barrels, 2×3 disks, r=4.7cm .. 20cm

- **Pattern recognition in high occupancy region**
- **Impact parameter resolution (in 3d)**

Radiation hard technology: n$^+$-in-n Silicon technology, operated at -6°C

Strips (80 μm × 12 cm) (small stereo angle): 4 barrels, 2×9 disks, r=30cm .. 51cm

- **pattern recognition**
- **contribution to momentum resolution**

p-in-n Silicon, operated at -6°C

TRT 4mm diameter straw drift tubes: barrel + wheels, r=55cm .. 105cm

- **Strong pattern recognition by having many hits (~36)**

Standalone electron id. from transition radiation

LHC Machine Upgrade

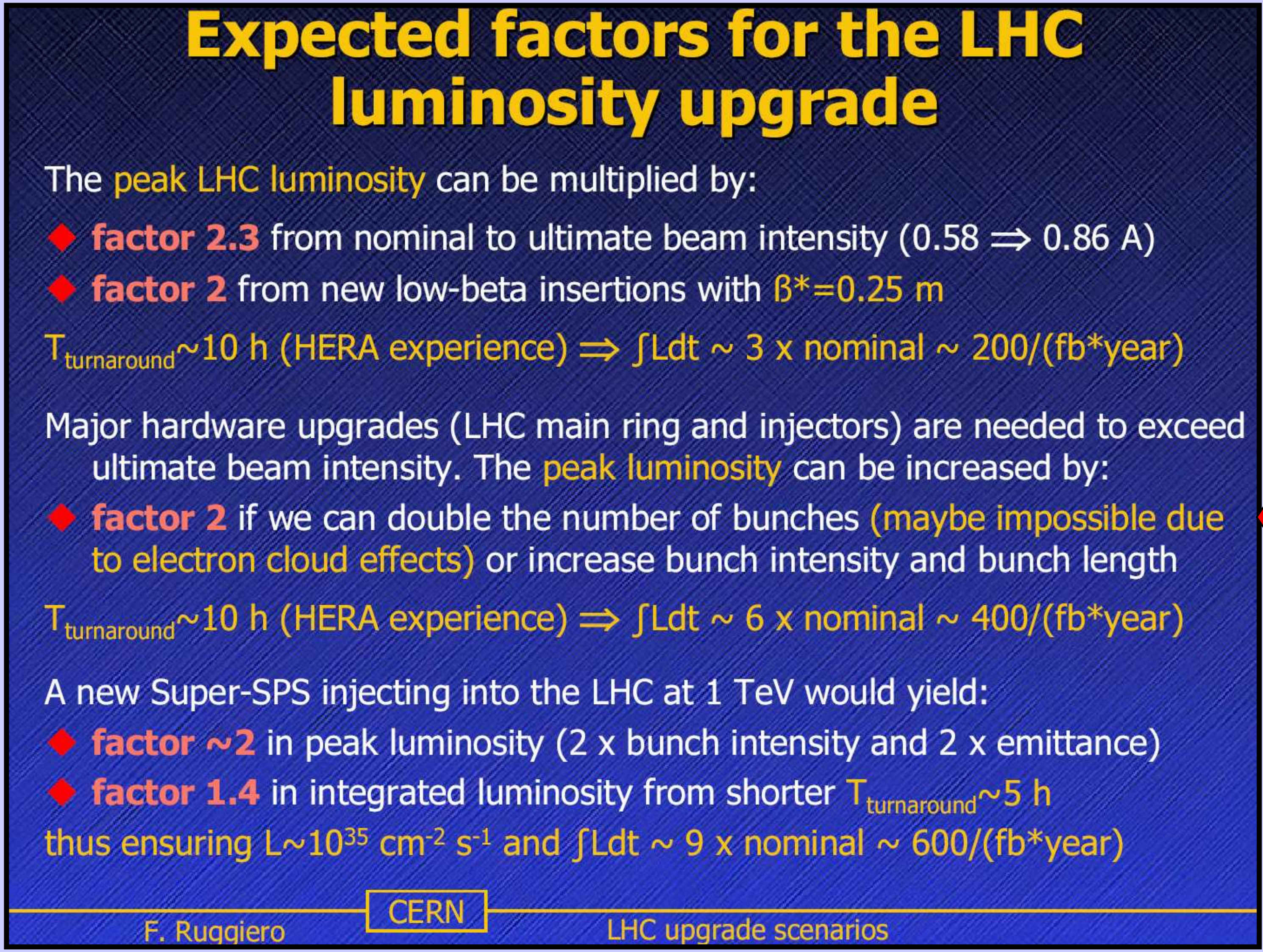
LHC status around 2015:

- Takes many years to significantly improve statistical precision
- End of life expectancy IR quadrupoles

An energy upgrade would be favoured from a physics point of view, but would essentially mean building a new machine.

Most likely option is a luminosity upgrade to 10^{35} $cm^{-1}s^{-1}$ (Super-LHC) .

SLHC Luminosity Upgrade
F. Ruggiero, Genoa workshop



Most likely bunch-crossing time of 10 or 15 ns!

Physics Gain Luminosity Upgrade

(Real physics case can only be made after LHC start-up.)

See Eur. Phys. J. C39(2005)293

Precision physics in rare Electro weak processes (often sensitive to new physics)

- Higgs couplings ($g_{W,Z}$, g_t)*
- Higgs self couplings
- Triple (and quartic) gauge couplings
- Vector-Boson-Scattering (if there is no Higgs)
- Rare top decays through FCNC

Extended mass reach for new physics (by ~30%):

- Heavy Higgs bosons
- SuSy particles (if they exist and turn out to be heavy)

If we find new physics:

- Parameters of new physics

Because of high luminosity and high mass reach SLHC is to a large degree complementary with ILC in case of overlap.

ATLAS Tracker Replacement

To keep ATLAS running more than 10 years the inner tracker will need to be replaced. (Current tracker designed to survive up to 700 fb^{-1})

In case of a luminosity (SLHC) upgrade the new tracker needs to cope with:

- higher occupancy
- higher dose rates

while keeping a similar tracking performance.

Main impact on design of the tracker:

- Radiation hard technology
- Fine granularity
  - pattern recognition
  - Resolution

Schedule
M. Tyndel, Genoa workshop

When can the Upgrade start?

- Finalise sLHC machine specification ~ 1/2 years 2006/2007
- Freeze the physics requirements
  - ideally after the first year of operation end 2007
- Complete 'proof of principle' RD ~ 2 year end 2007
- Prepare TDR ~0.5 year
- Obtain funding
  - ➲ <u>Start Upgrade construction mid 2008</u>

		2008	2009	2010	2011	2012	2013	2014	2015
TDR									
Parts (sensors, ASICs, Opto…)									
Modules									
Sub-assemblies									
Integration									
Commissioning									
Installation									

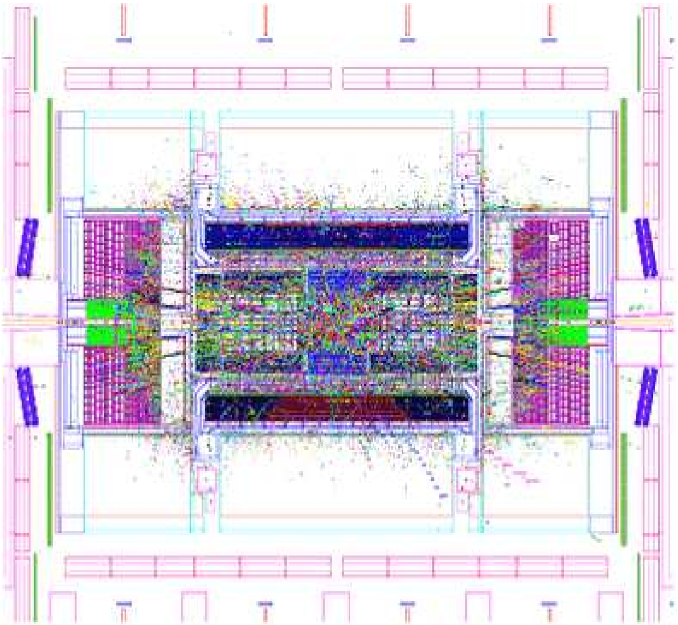
➲ <u>Will not meet target end-date without radical steps</u>

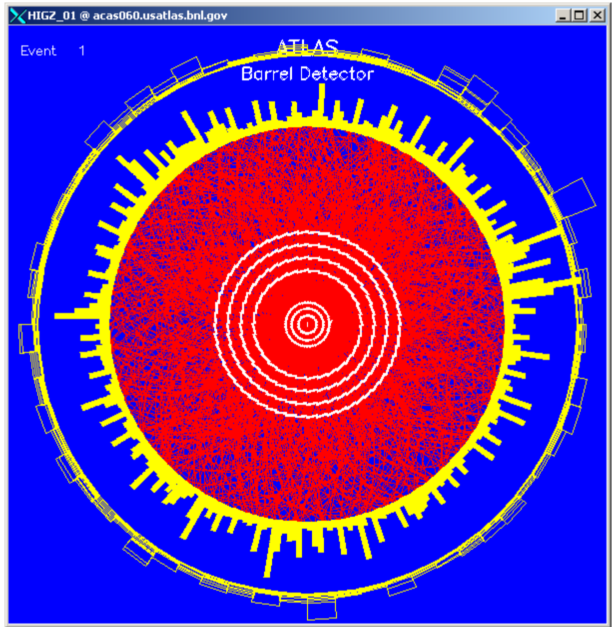
1. Restrict RD to a minimum – try and advance pre-series
2. Create large assembly facilities with many sets of tooling

**Working back from 2015 we need a TDR by end 2008.
R&D and design work needs to start now!**

Pile-up and Occupancy
P. Nevski, Genoa workshop

Expected Pile-up at Super LHC





$N_{ch}(|y|\leq 0.5)$

- 230 min.bias collisions in bunch
- ~ 10000 particles in $|\eta| \leq 3.2$
- mostly low p_T tracks

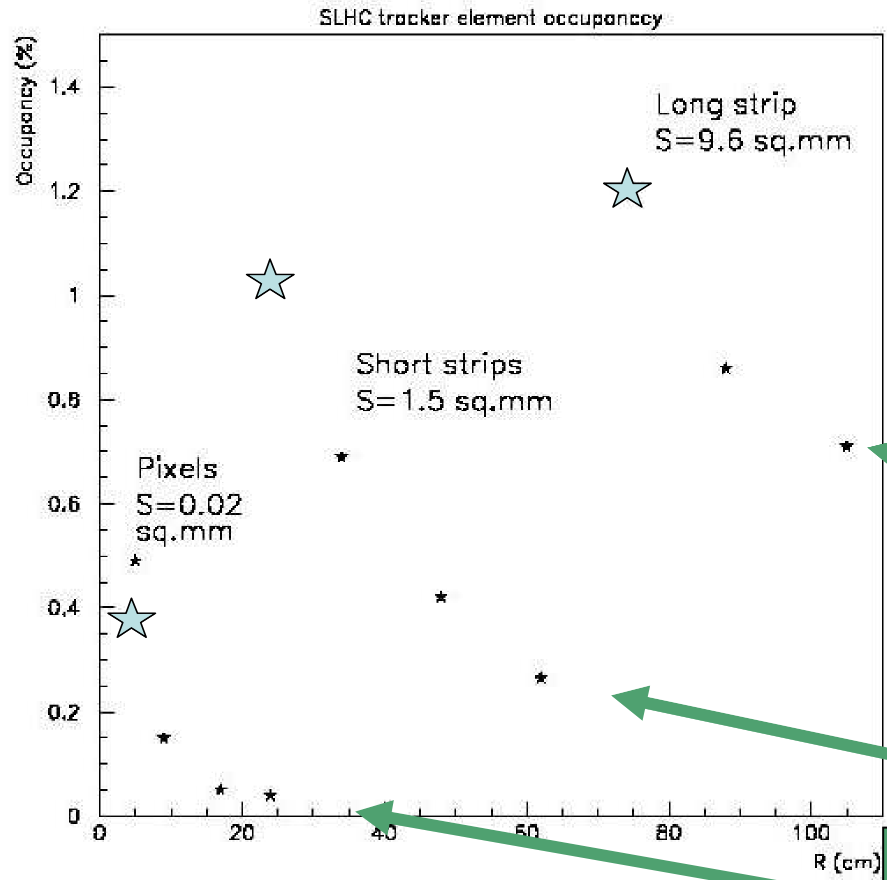
Note: numbers based on factor 10 increase in luminosity but still 25 ns bunch crossing. May need to use similar numbers for 10-15 ns, as we could see pile-up from previous bunch crossing?

Occupancy
P. Nevski (Genoa Meeting)

SLHC predicted occupancy

Few comments:

- At 4-6 cm pixel layer should be 300µ
- At 24 cm even short strips are too big
- At 75 cm long strips are too big



Long strips: 12cm×80µm

Short strips: 3cm×50µm

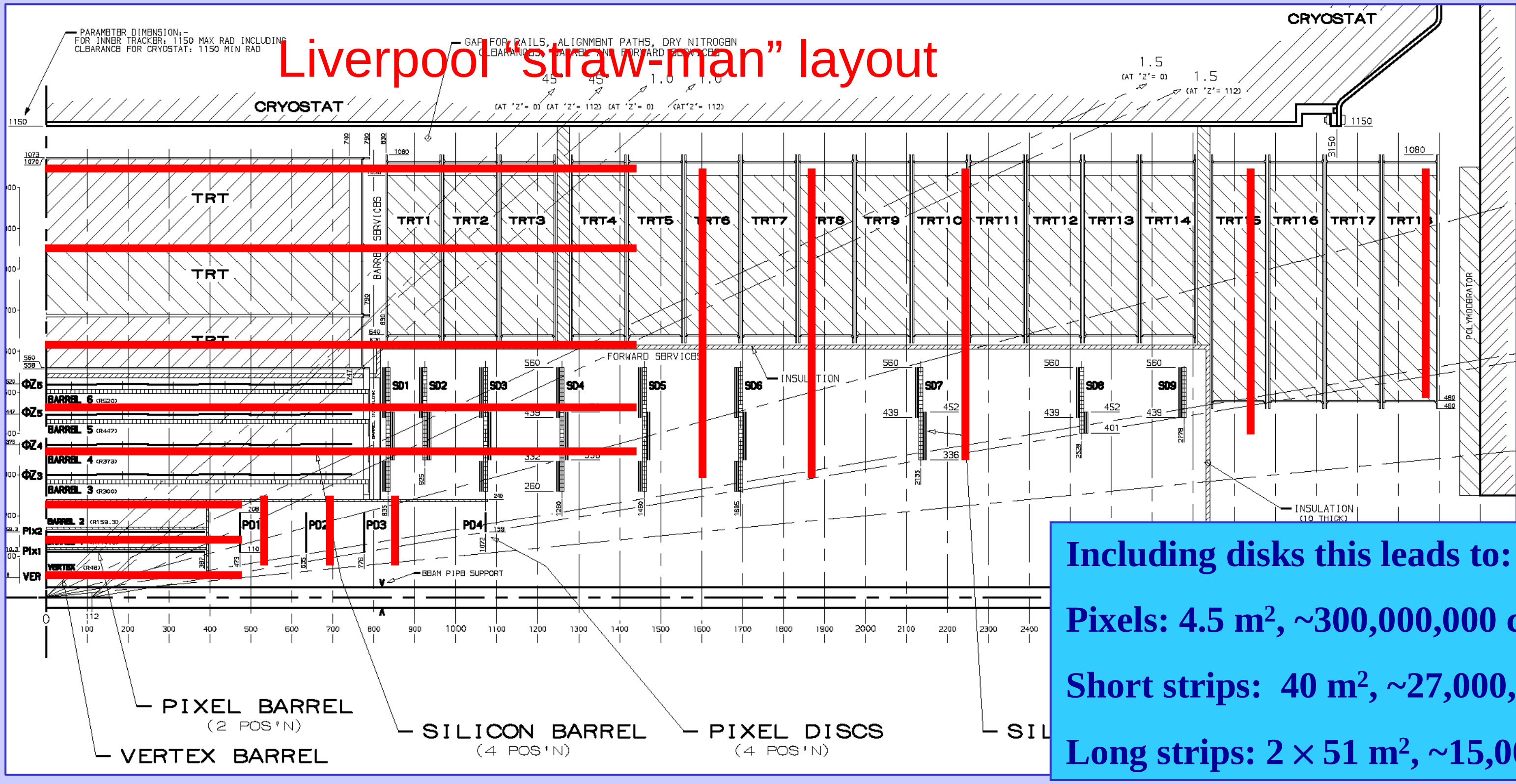
Pixels: 400 µ m×50µm

Example Tracker Layout

Some layout proposals have been made.

<u>All Silicon tracker</u>

Pixels:	**r=6cm, 15cm, 24cm**	**z=±50cm**
Short (3cm) μ-strips (single layer?):	**r=35cm, 48cm, 62cm**	**z=±144cm**
Long (12 cm) μ-strips (stereo layers):	**r=84cm, 105cm**	**z=±144cm**



Including disks this leads to:

Pixels: 4.5 m², ~300,000,000 channels

Short strips: 40 m², ~27,000,000 channels

Long strips: 2 × 51 m², ~15,000,000 channels

SLHC dose estimates (in 1 MeV neutron equivalent fluence)

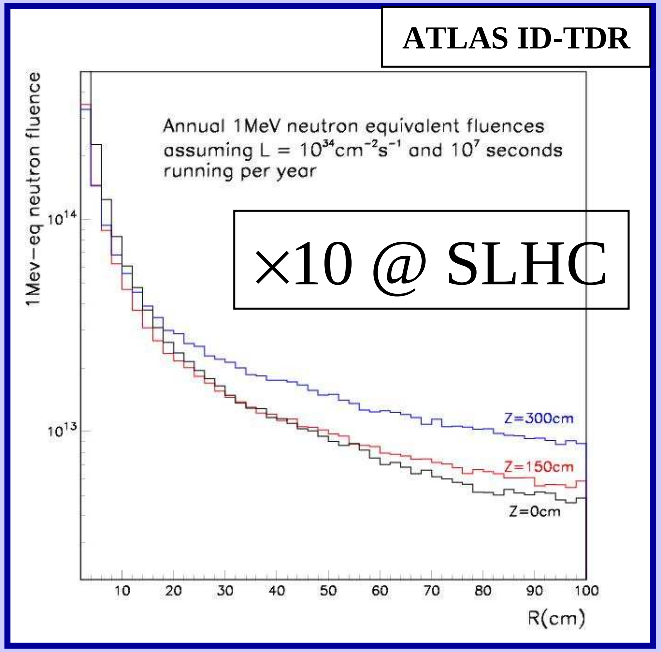
Flux scales with luminosity.

(Thermal neutron flux depends on added moderator material to compensate for loss of neutron moderating effects of TRT.)

Assume overall factor 10 increase.

Assuming 10 years of SLHC running (~6000fb^{-1}).

Pixels	Max. annual dose	10 years (~6000 fb^{-1})
Disks, r=9-25 cm, z=50-85 cm	~8×10^{14} n_{eq}/cm^2	~8×10^{15} n_{eq}/cm^2
barrel, r=6 cm	~2×10^{15} n_{eq}/cm^2	~2×10^{16} n_{eq}/cm^2
barrel, r= 15 cm	~4×10^{14} n_{eq}/cm^2	~4×10^{15} n_{eq}/cm^2
barrel, r= 24 cm	~2.5×10^{14} n_{eq}/cm^2	~2.5×10^{15} n_{eq}/cm^2



Short strips	Max. annual dose	10 years (~6000 fb^{-1})
disks, r=35-80 cm, z=150-300 cm	~1.3×10^{14} n_{eq}/cm^2	~1.3×10^{15} n_{eq}/cm^2
barrel, r= 35 cm	~1.4×10^{14} n_{eq}/cm^2	~1.4×10^{15} n_{eq}/cm^2
barrel, r= 48 cm	~1×10^{14} n_{eq}/cm^2	~1×10^{15} n_{eq}/cm^2
barrel, r= 62 cm	~8×10^{13} n_{eq}/cm^2	~8×10^{14} n_{eq}/cm^2

Long strips	Max. annual dose	10 years (~6000 fb^{-1})
disks, r= 80-100 cm, z= 150-300 cm	~1×10^{14} n_{eq}/cm^2	~$1.\times10^{15}$ n_{eq}/cm^2
barrel, r= 84 cm	~6×10^{13} n_{eq}/cm^2	~6×10^{14} n_{eq}/cm^2
barrel, r= 105 cm	~5×10^{13} n_{eq}/cm^2	~5×10^{14} n_{eq}/cm^2

Assumptions made on SLHC running can vary between “5 years SLHC” and “10 years SLHC + 50% safety margin”

Predicting Limit of Operation of Silicon at SLHC doses

For LHC dose rates:

• Main failure mode is when full depletion (V_{FD}) voltage goes beyond the maximum voltage allowed by the system. Prediction carried out on the basis of V_{FD}.

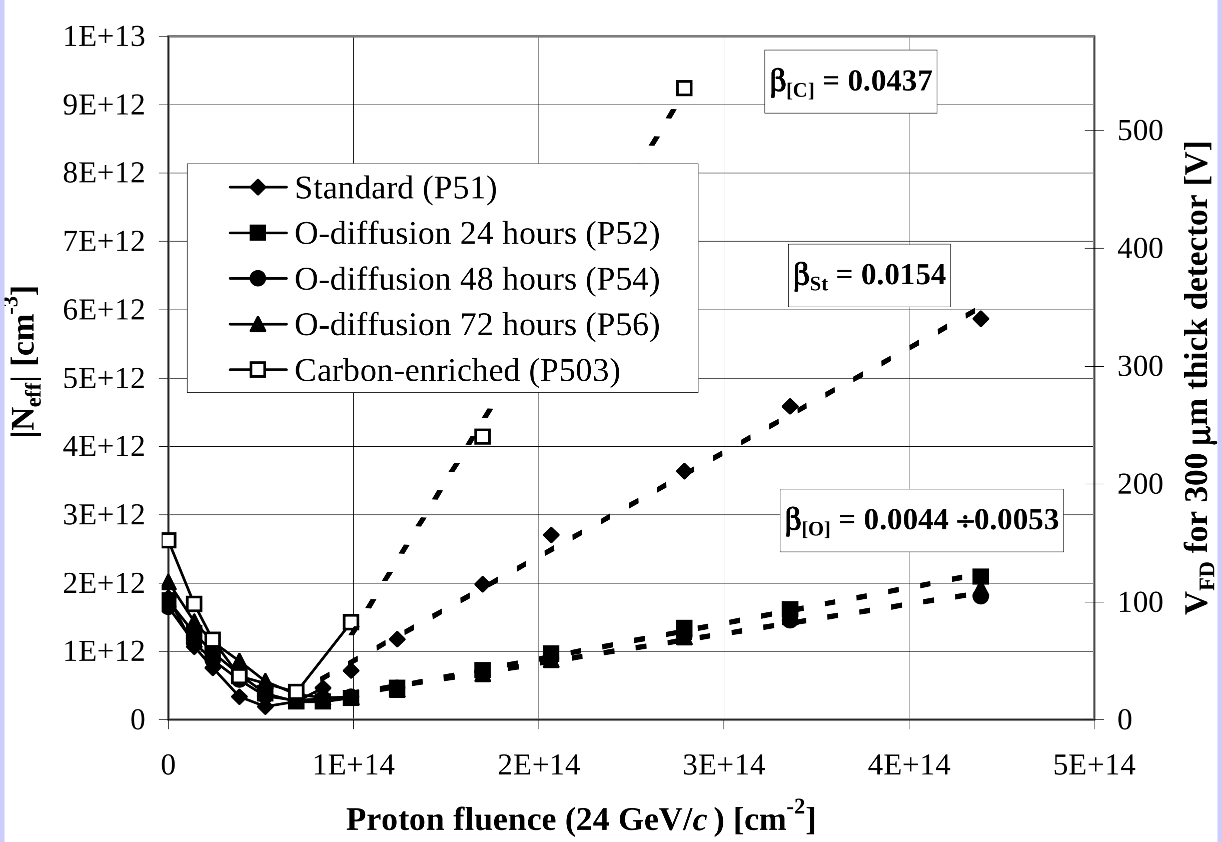
For the SLHC dose rates

•Trapping will be the most important radiation effect.

•What is the suitable prediction criterion?

Changes of V_{FD} with fluence

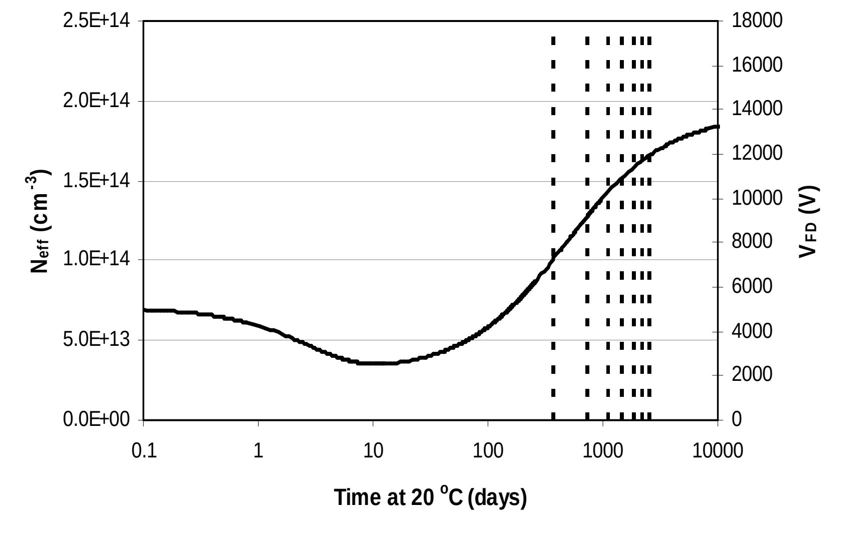
Space charge density N_{eff} and full depletion voltage V_{FD} versus proton fluence for standard, carbon-enriched and three types of oxygen diffused samples: 24, 48 and 72 hour diffusion at 1150°C

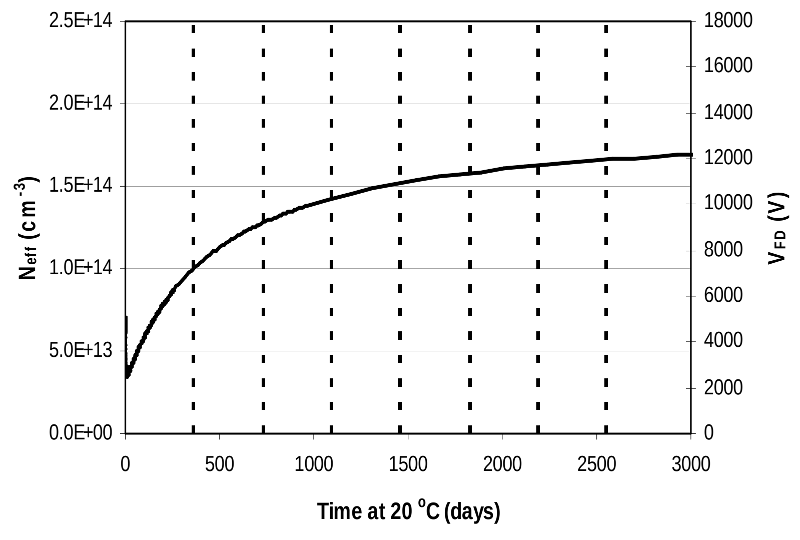


$$N_{eff} = N_{eff}(0)e^{-c\phi} - \beta\phi$$

Changes of V_{FD} with time

N_{eff} and V_{FD} versus time after irradiation to $7.5x10^{15}$ p cm^{-2} of a silicon detector stored at 20°C.





The annealing behaviour are unusual: after some recovery (expected annealing behaviour) a strong '*reverse*' annealing takes place.

$$\Delta N_{eff}(t,\Phi) = \Phi \times \sum_i g_{a,i} \exp\left(-\frac{t}{\tau_{a,i}}\right) + N_c(\Phi) +$$

$$N_{y,\infty} \times \left(1 - \frac{1}{1 + t/\tau_y}\right)$$

Temperature dependence of the annealing

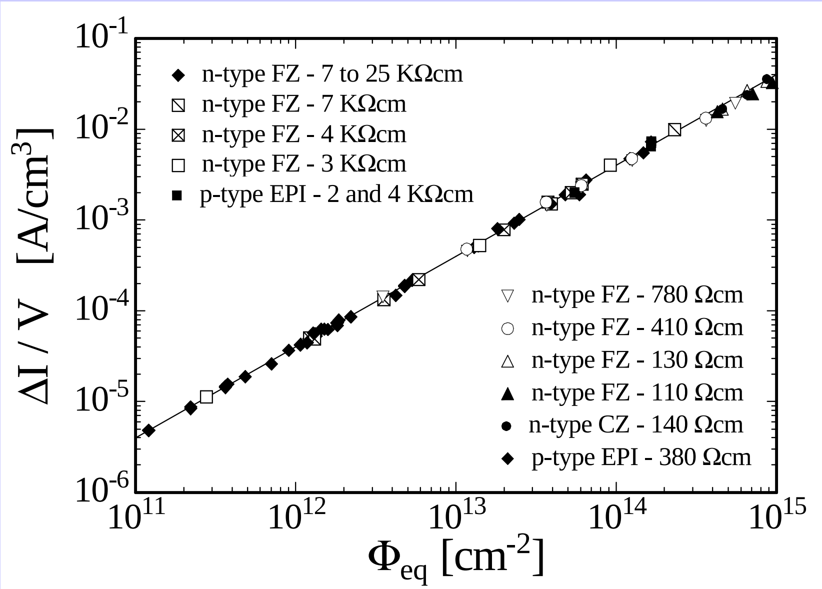
$$\frac{1}{\tau_Y} = k_Y = k_{0Y} \exp\left(-\frac{E_Y}{k_B T_a}\right)$$

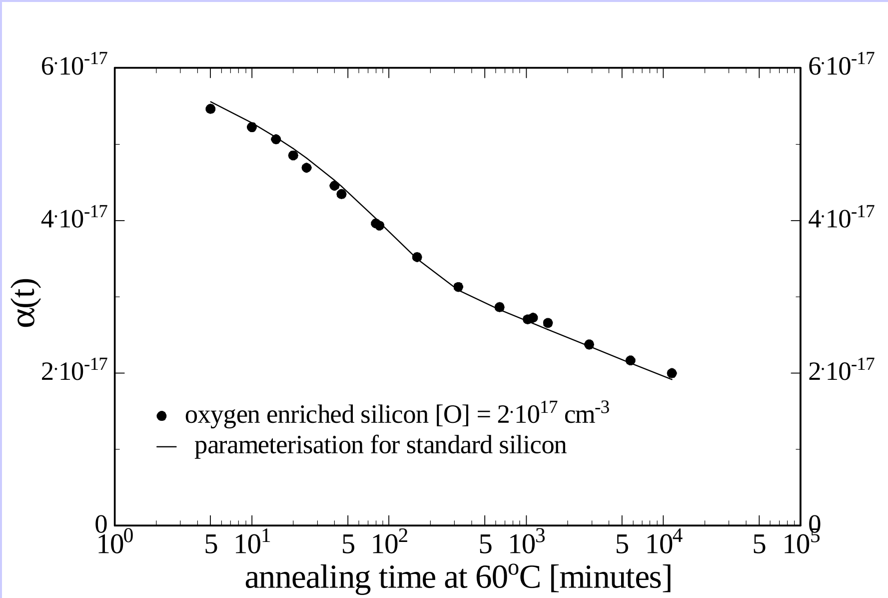
Can use the temperature to accelerate the reverse annealing relative to RT (e.g. @80^{o}C acceleration factor ~7300), or to store avoiding reverse annealing (e.g. @0^{o}C~1/50)

Changes of I_V with fluence and time

$$I = \alpha \, \Phi_{eq} \, V$$

$$\Delta I_r(t) = \Delta I_r(t=0) \times \sum_i d_i \exp\left(-\frac{t}{\tau_i}\right)$$





Fluence dependence of leakage current for detectors produced by various process technologies from different silicon materials. The current was measured after a heat treatment for 80 min at 60°C .

Current related damage rate α as function of cumulated annealing time at 60°C.

Temperature dependence of the reverse current

The reverse current is independent on the silicon bulk material. It can though be controlled by temperature:

$$I_r(T) \propto T^2 \exp\left(-\frac{E_g}{2k_B T}\right)$$

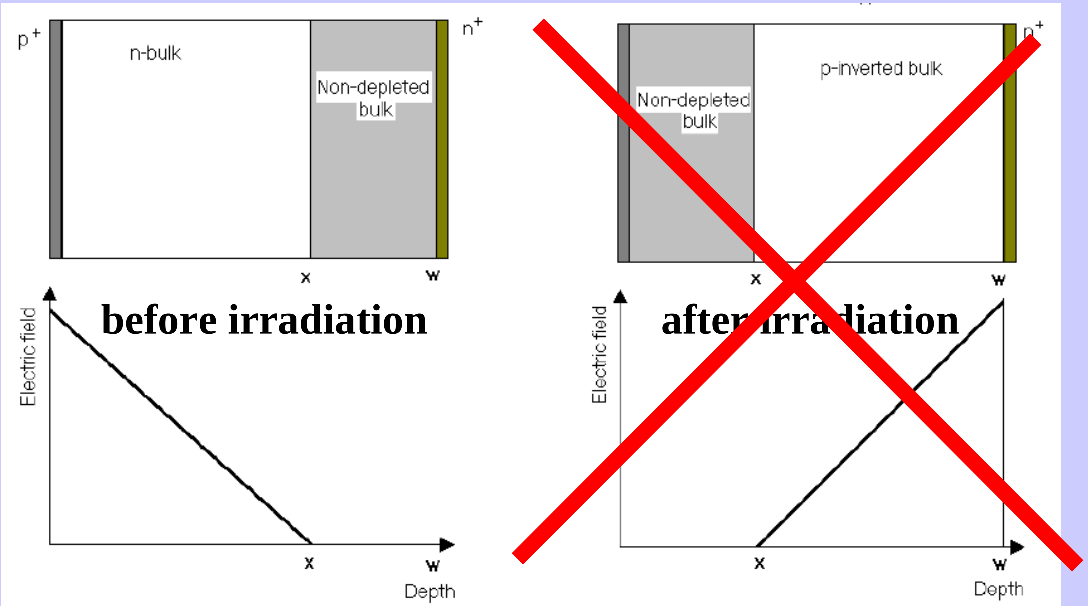
It reduces by a factor of two every 7-8 degrees.

Changes in the electric field after irradiation

<u>p-in-n</u> sensors after irradiation:

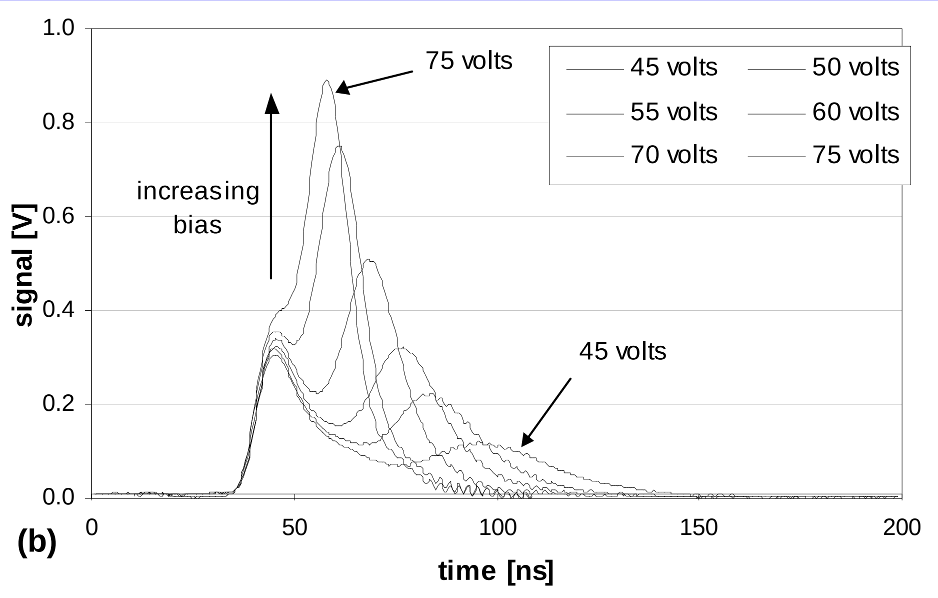
Standard n-bulk inverted to p-type, naïve description:

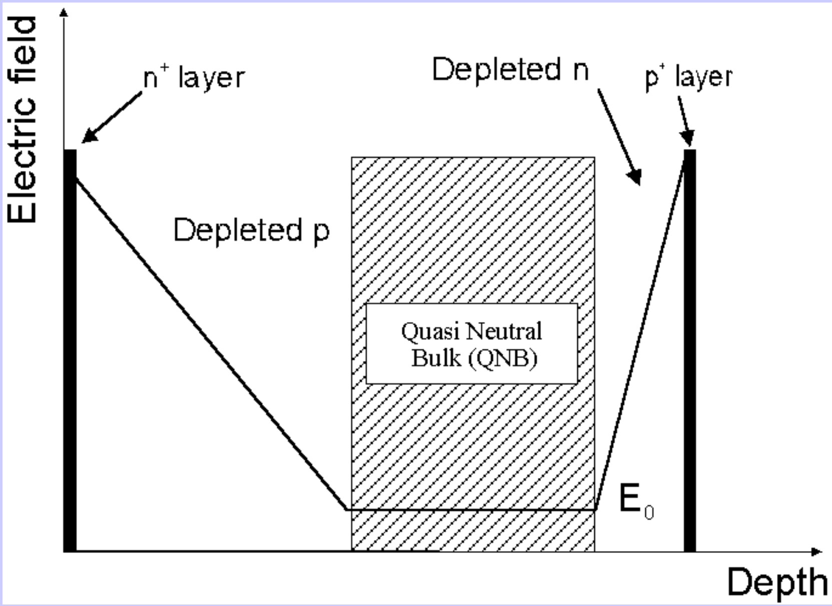
mirror image with respect to pre-inversion.



There is evidence that a more structured E develops after irradiation

Changes in the electric field after irradiation

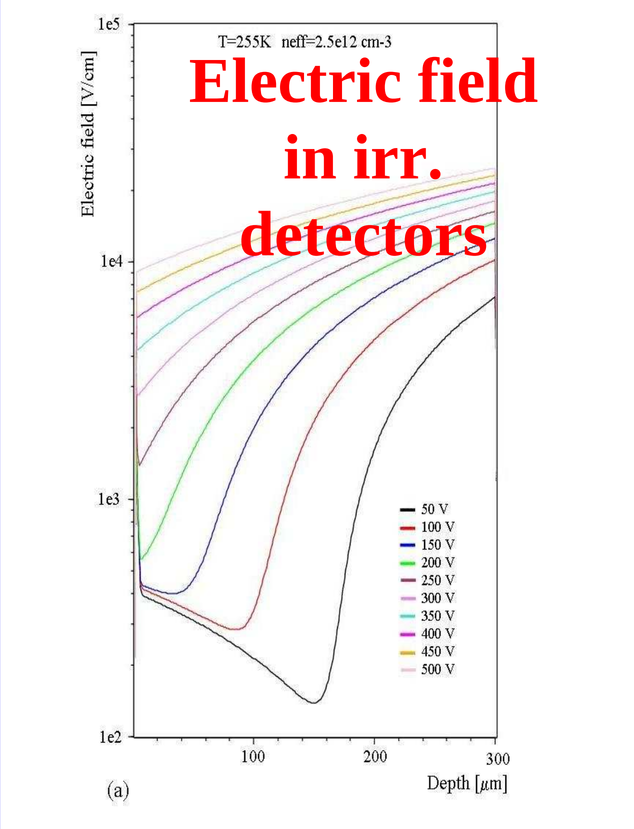


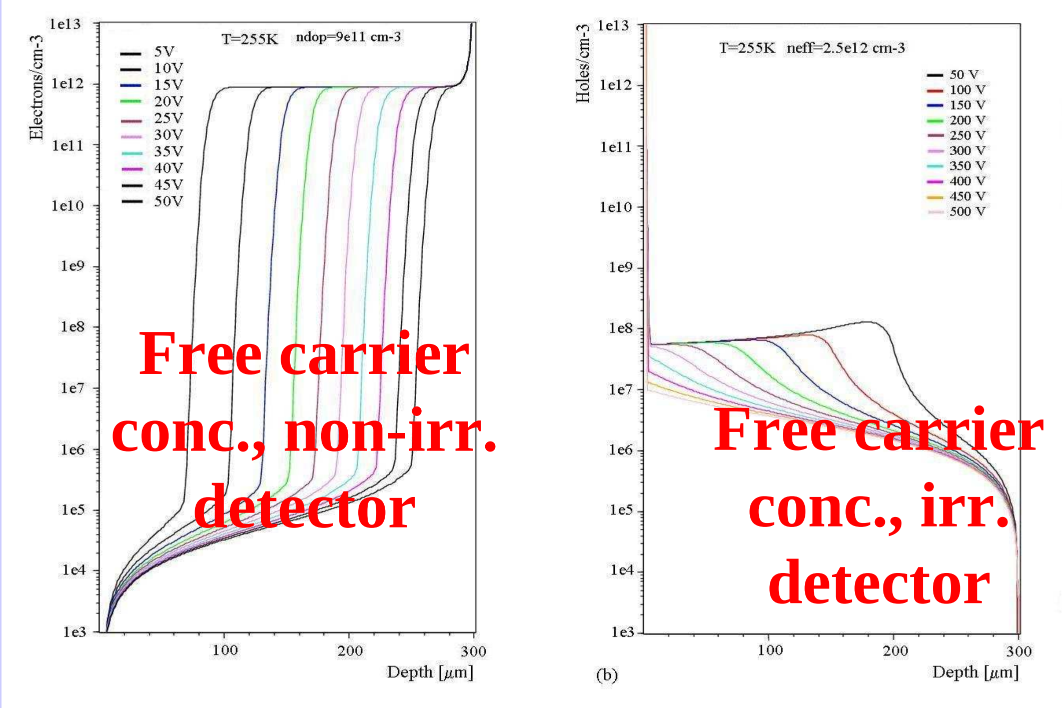


A *double peak* is observed with front (p-side) illumination with low range particles of an inverted Si detector.

Shape of the electric field implied by the double peak signal, but the depth of the high-peak layer is small and doesn’t affect much the signal of mip’s in hep detectors. The dominant signal develops in the *main* region. For practical reasons the naïve description still holds.

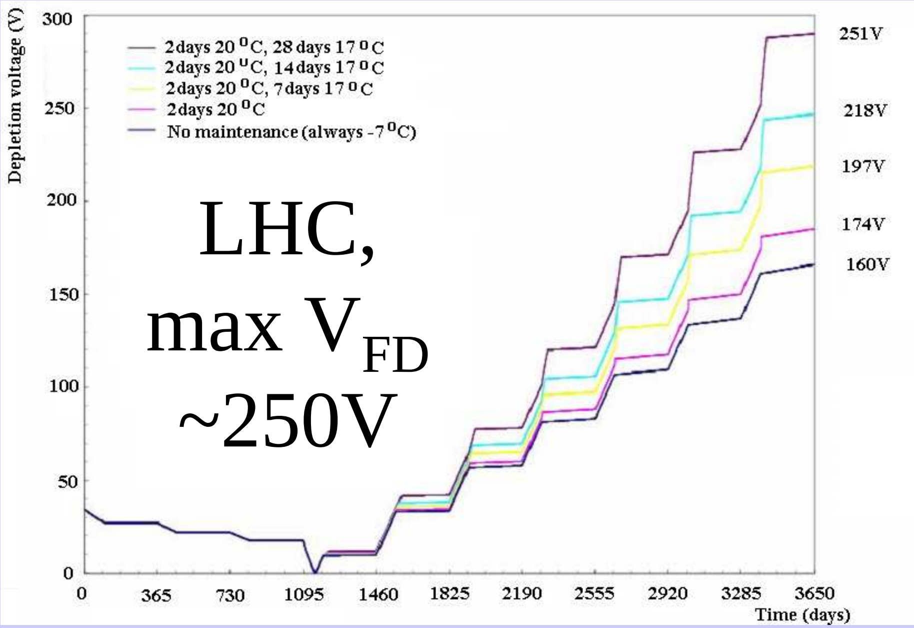
Changes in the electric field after irradiation

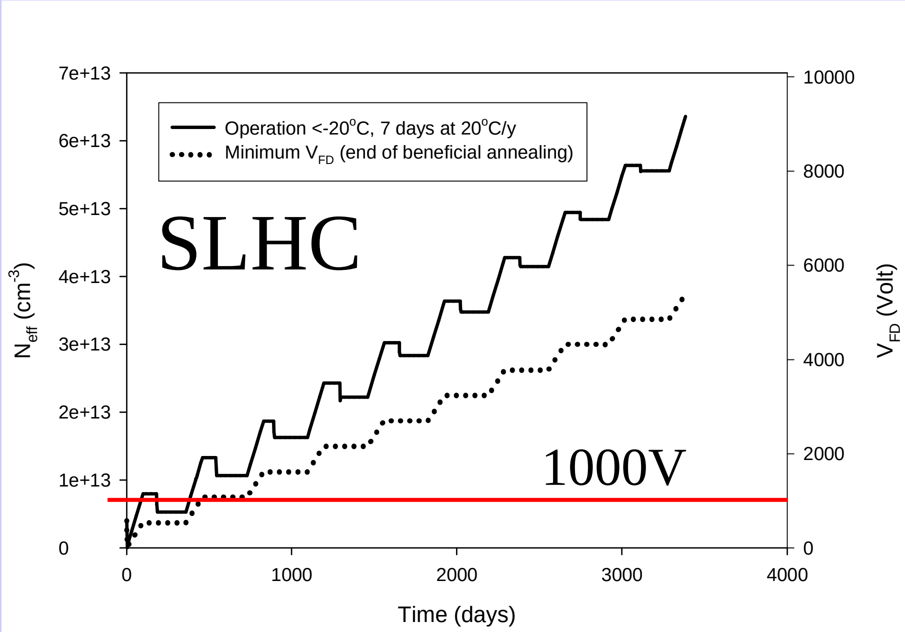




A more *realistic* profile of the electric field needs simultaneous solution of the Poisson equation and e and h continuity equations. The knowledge of radiation induced defects is necessary. In this simulation, 3 known defects and 2 *effective* ones are used. This simulation confirms a ‘double junction’ shape and a low concentration of free carriers in irradiated detectors at any voltage (the idea of full depletion seems incorrect).

Evolution of V_{FD} with operation time in LHC tracker and middle sLHC pixel layer

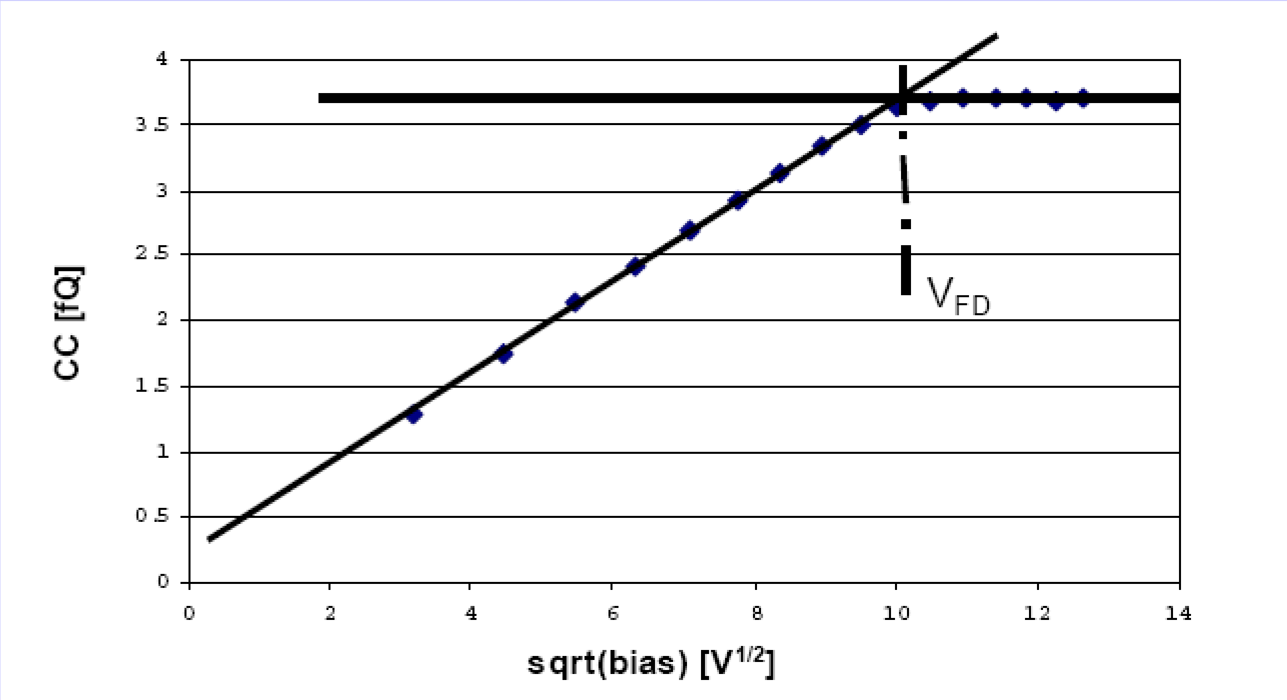




According to this scenario the V_{FD} in the SLHC middle pixel layer (right) exceeds 1000V already in the first year. This voltage can be considered the very maximum achievable for a large silicon detector system. The prediction based on V_{FD} would lead to the conclusion that a Si-tracker in the upgraded machine is unfeasible.

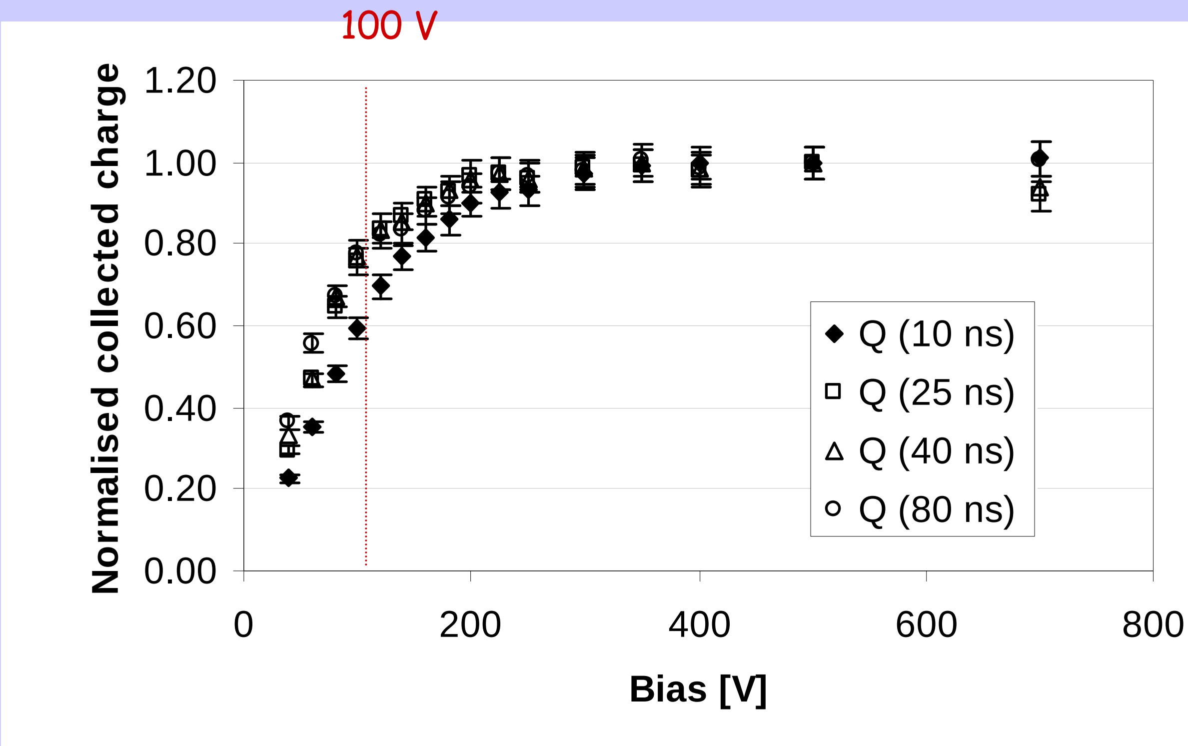
Comparison V_{FD} – CCE(V)

Charge collection as a function of bias for a non-irradiated silicon diode. The collected charge clearly saturates at V_{FD}.



Evaluation of Trapping Effects

Corresponding Charge Collection Efficiency vs Voltage for diodes irradiated to ~2.10^{14} p cm^{-2}. At V_{FD} ~ 80% of the plateau charge is collected. The CCE above V_{FD} is due to the reduction of trapping because of shorter collection time (t_c).



Evaluation of Trapping Effects

- The effects of trapping can be parameterized in terms of effective trapping time (*Kramberger et al*) or, equivalently, velocity dependent attenuation length (*Marti i Garcia et al*)
- In both cases, it accounts for highest trapping where $\bar{E}$ field is lowest
- These parameterizations assume timescales such that the total un-trapped charge is collected, integrating over transient effects.

$\rightarrow$ No influence of ballistic deficit is taken into account, but the measurements show that this is not influent for integration times of 25ns.

- Nevertheless, both analyses give values of the trapping parameter β (averaged over *e* and *h*) that agree. $\beta_{e,h} \times \Phi_{eq} = 1/\tau_{\mathrm{eff}\ e,h}$ (trapping ∝ fluence)

$$q(V) = \frac{Q_0}{w_0} \int_0^{w(V)} \exp\left(-\int_x^{w_0} \frac{dx'}{\lambda(x')} \right) dx$$

$$1/\tau_{eff} = \beta\Phi$$

$$\lambda(x) = \lambda_0 + \lambda_1 \frac{v(x)}{v_s}$$

$$v(x) = \mu(x)\varepsilon(x)$$

$$\mu(x) = \frac{\mu_0}{1 + \mu_0 \varepsilon(x)/v_s}$$

$$\varepsilon(x) = \frac{2V_{\mathrm{fd}}}{w_0^2}(w(V) - x).$$

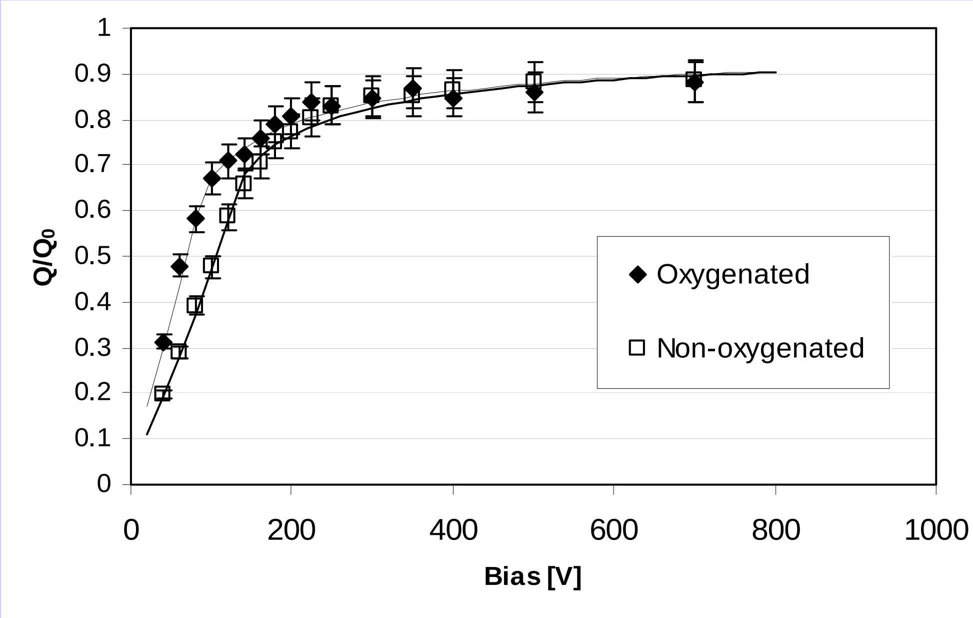
Fits to the Charge Collection Efficiency

V_{FD} oxy. 50V

V_{FD} std. 100V

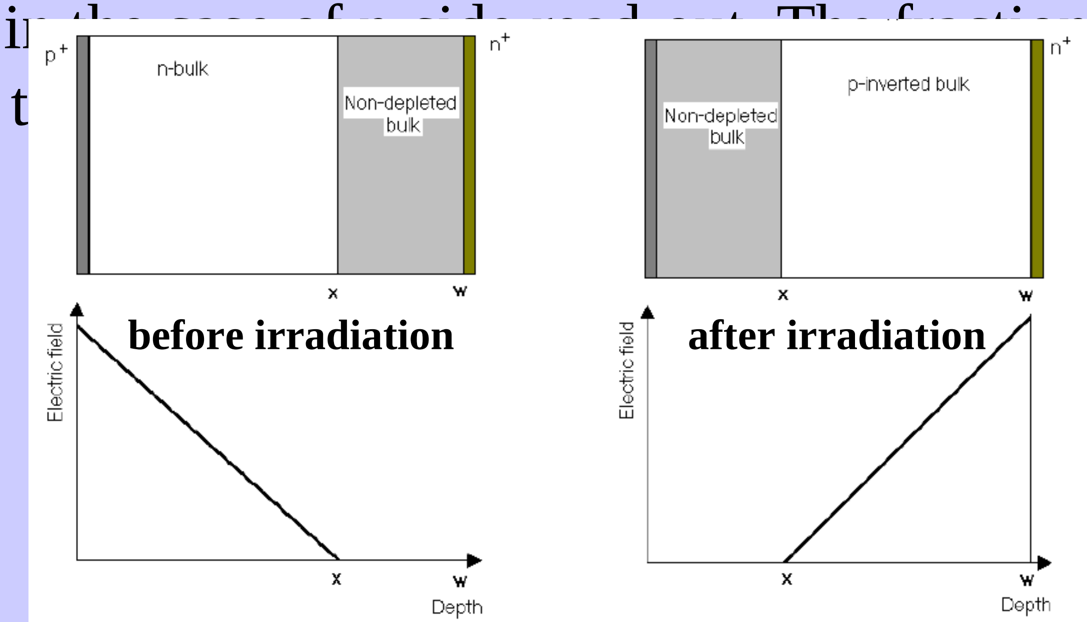
Whit trapping, the collected charge doesn't saturate at the so-called V_{FD}. Strong over-depletion is needed to reach the plateau charge. Even the plateau charge is lower than the ionised charge Q_0 due to the trapping. The charge deficit is proportional to Φ. Free parameters:

attenuation length λ,
depletion voltage V_{FD}
total generated charge Q_0



1.9×10^{14} p/cm^2

The signal formation in the case of diodes is due to both charge carriers (e-h). In the case of finely segmented devices the signal is mainly due to one type of charge carrier, namely h in the case of p-side and e i[illegible] of charge loss due to t[illegible]vo cases.

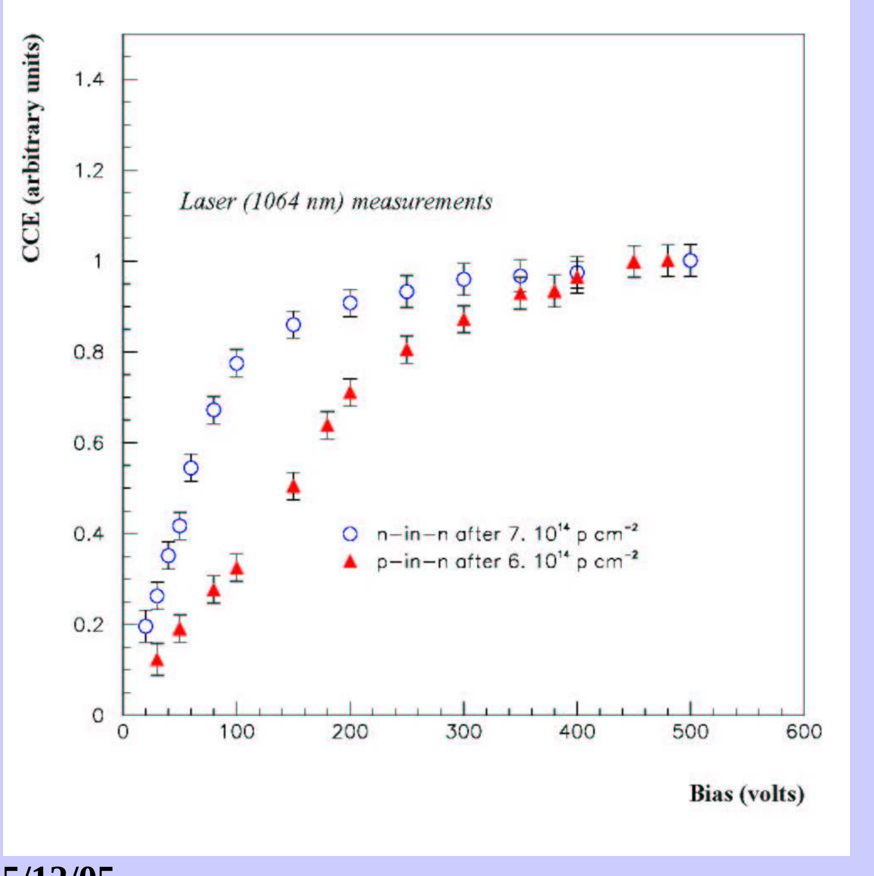


The above description of the CCE(V) properties suggest that trapping is inversely proportional to the collection time, therefore in the case of segmented detectors reading-out from the high-field n-side (after type inversion) leads to better CCE(V) behaviour

Charge Collection Efficiency: n-side vs p-side read-out

Direct comparisons of n-side and p-side detectors with the same masks fabricated on the same material confirm the superiority of n-side read-out after irradiation.

Laser (1060 nm) CCE(V) in the highest irradiated areas for a n-in-n (7. 10^{14} p cm^{-2}) and p-in-n (6. 10^{14} p cm^{-2}) 200 μm thick microstrip detectors

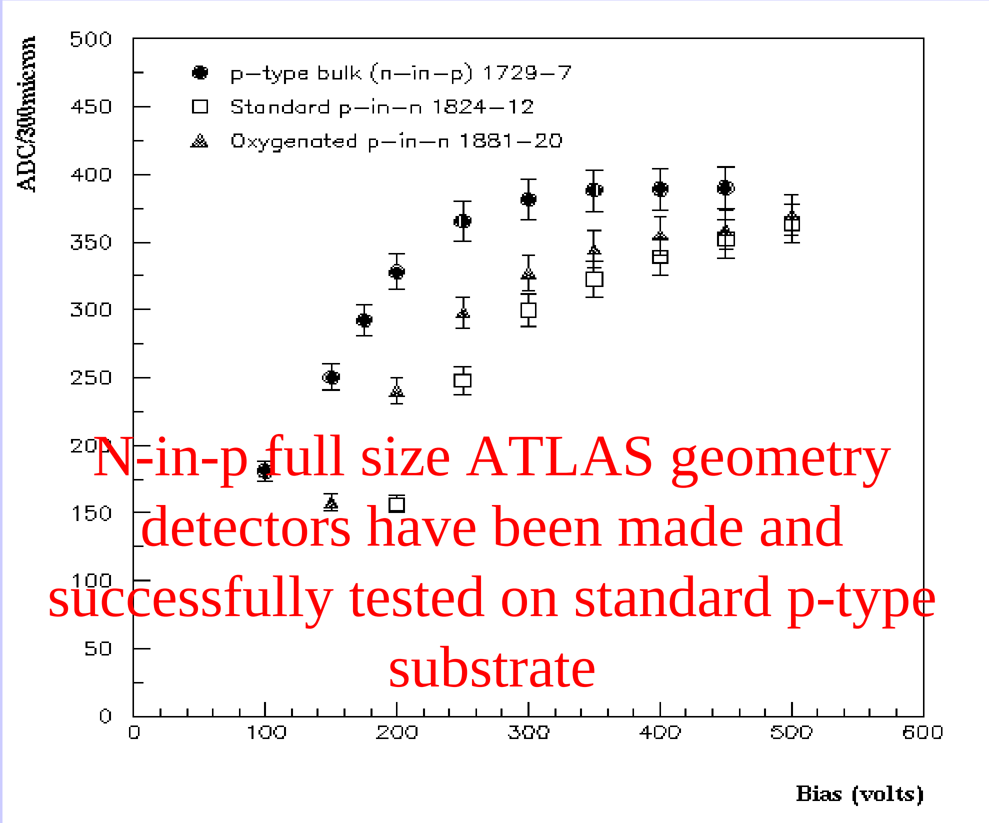


Implementing n-side read-out on p-type silicon

The n-side read-out can be equally well implemented on a p-type substrate and keep the same advantages for CCE after irradiation and exhibiting two additional advantages compared to the n-type bulk.

• The p-type bulk doesn’t invert, so the junction side will always be on the same side before and after irradiation

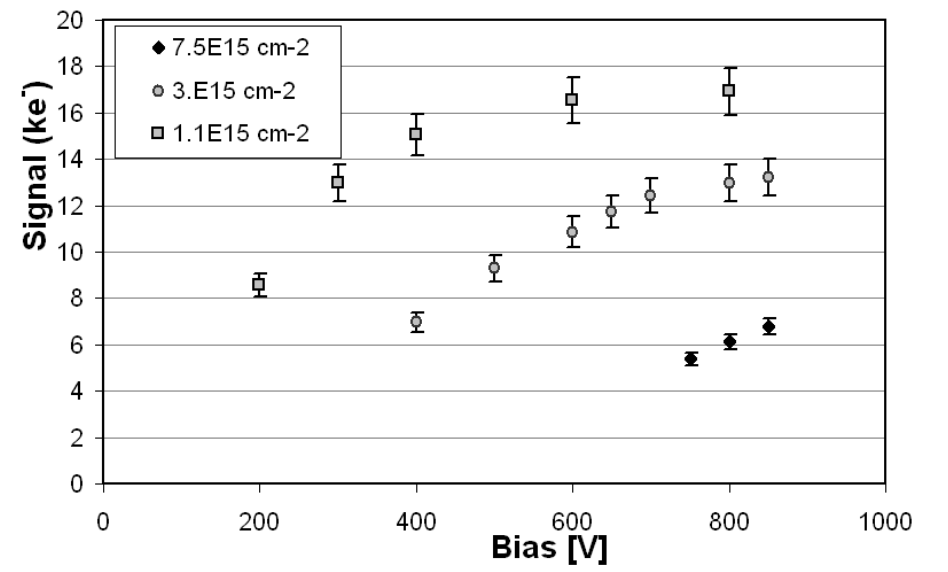
•The p-type substrate devices don’t required backplane processing, which turns out being cheaper (40-50%) than the n-type. This argument can be of capital importance for large area coverage (sLHC trackers).

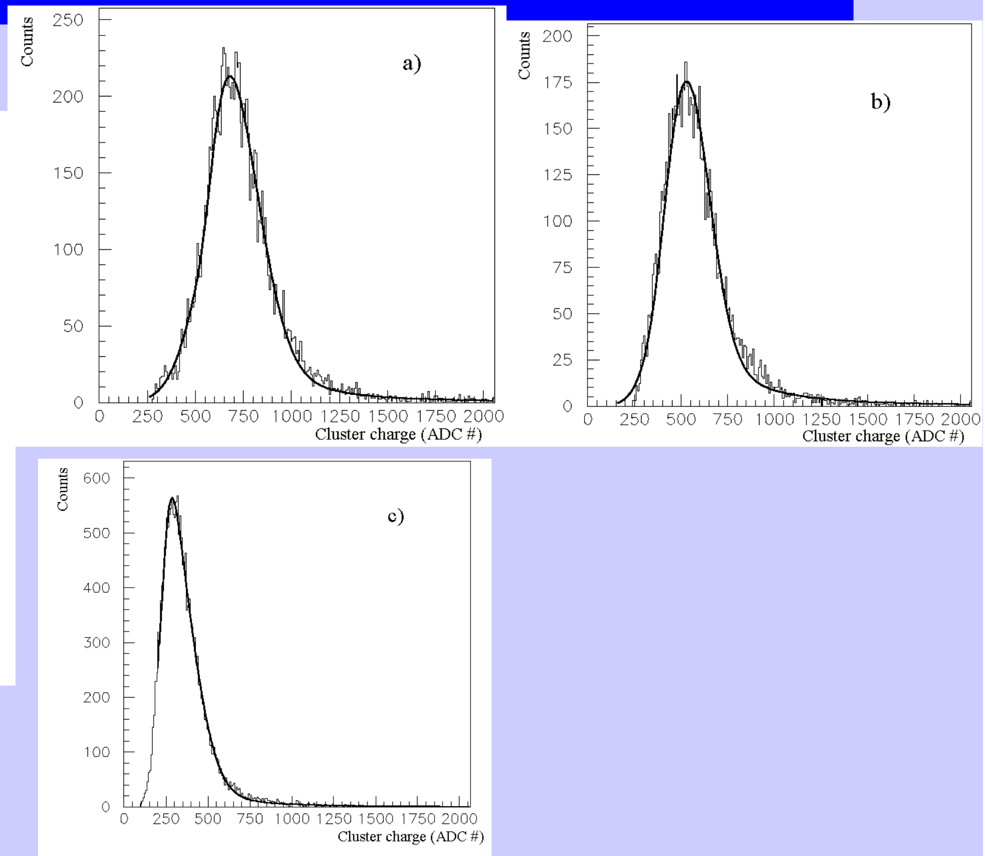


N-in-p full size ATLAS geometry detectors have been made and successfully tested on standard p-type substrate

Improvements of CCE(V) confirmed

CCE of n-in-p detectors after SLHC radiation levels

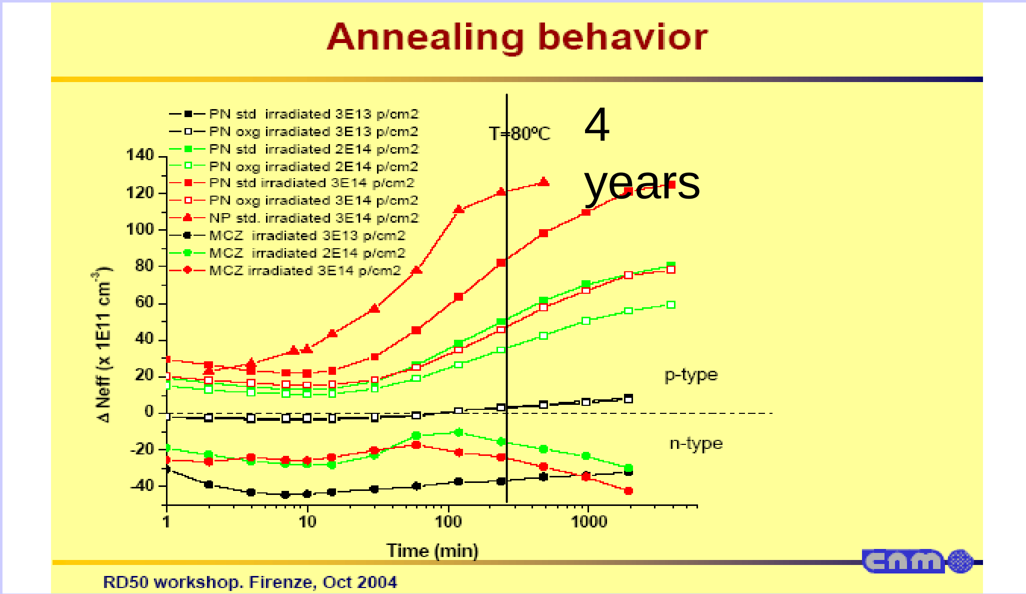




Collected charge as a function of the bias voltage of miniature (1x1 cm^2) microstrip detectors after SLHC level irradiation: 1.1, 3.5 and 7.5×10^{15} p cm^{-2}. NOTICE: > 6000e after higher dose!

Reverse annealing of irradiated p-type detectors

Remember changes of V_{FD}. They are verified also for p-type devices.

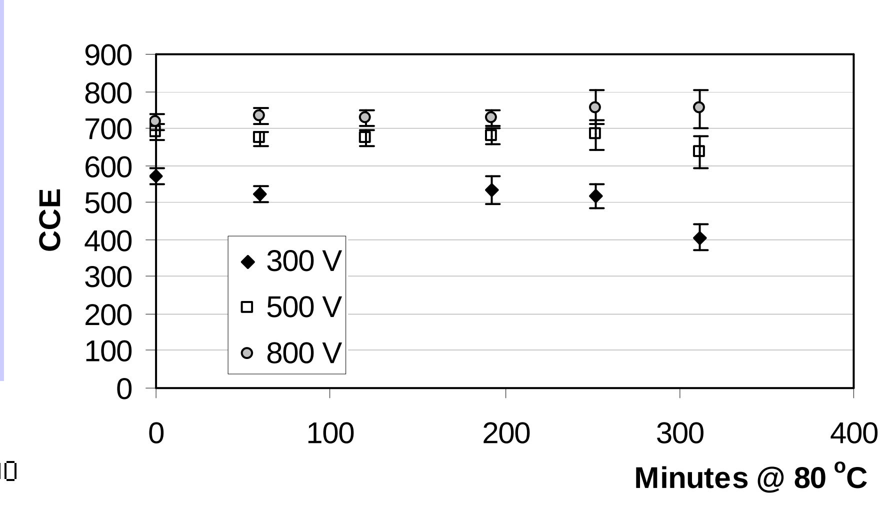


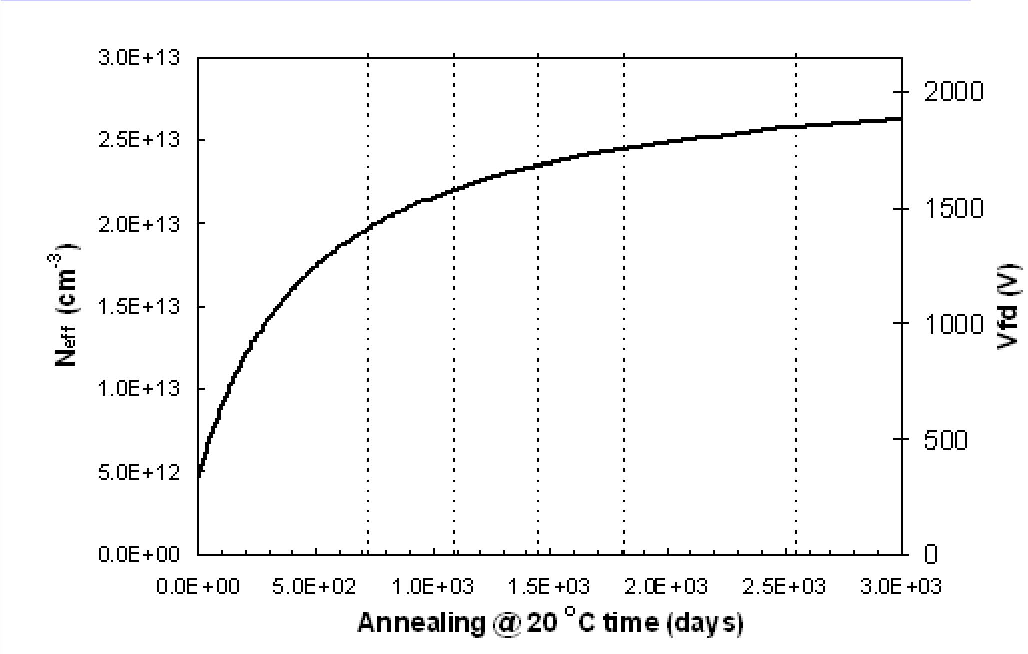
Reverse annealing of irradiated p-type detectors

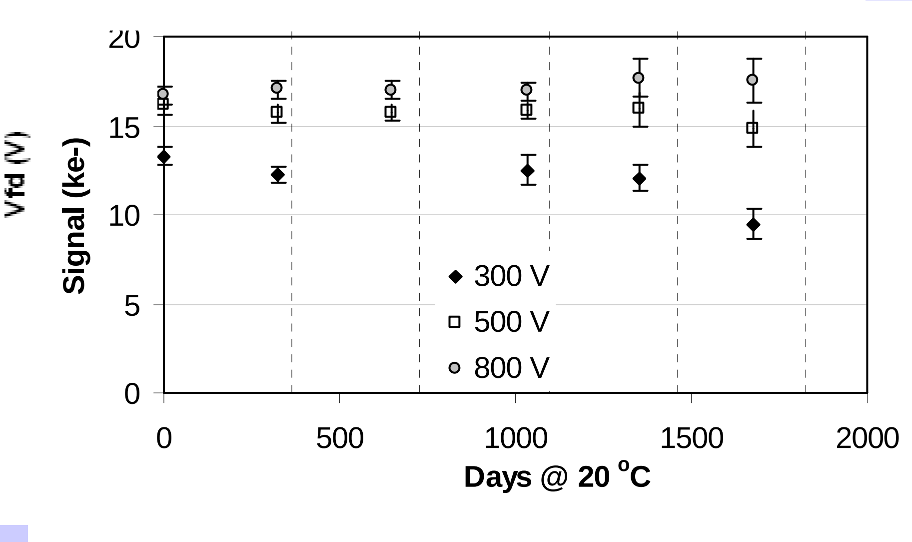
1.1 10^{15} p cm^{-2}

Initial V_{FD} ~ 420V

Final V_{FD} ~ 1900V





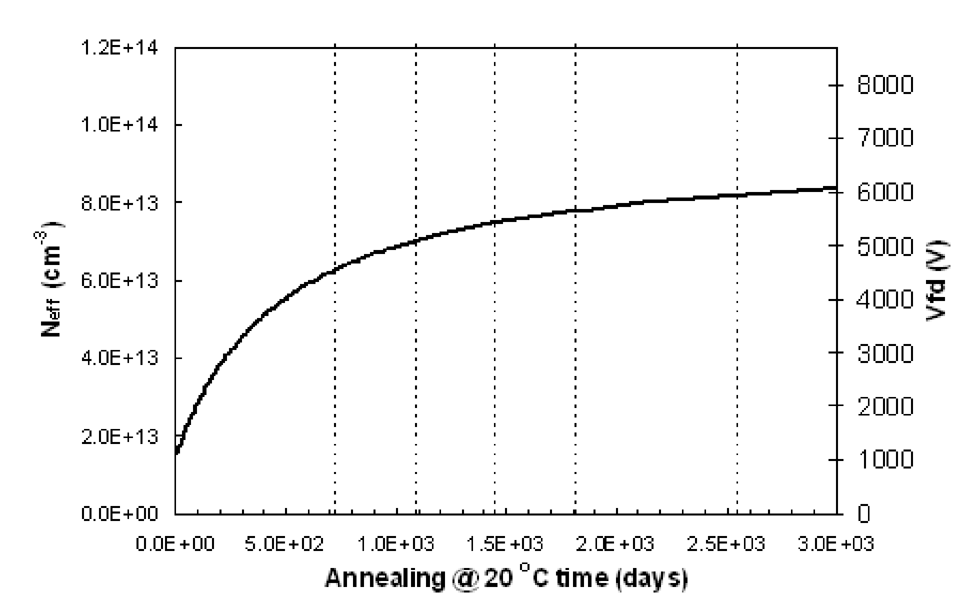


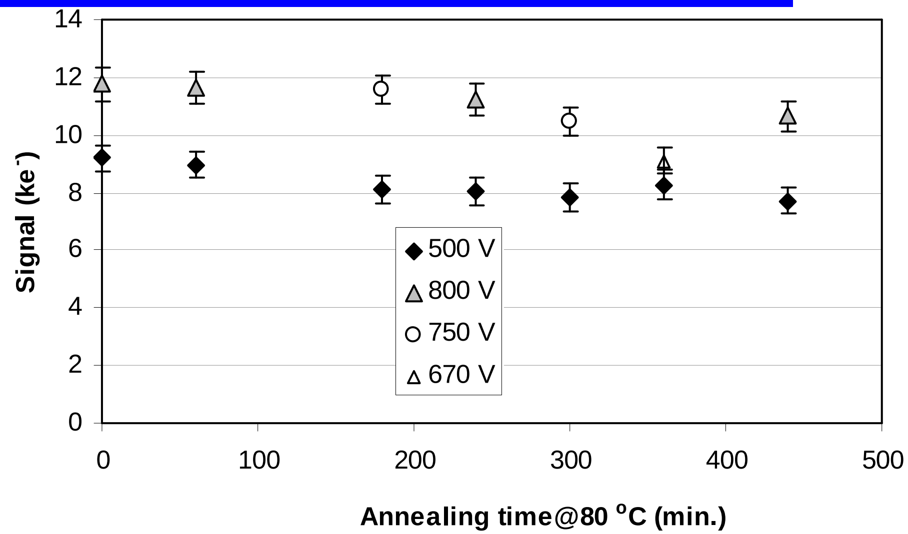
Reverse annealing of irradiated p-type detectors

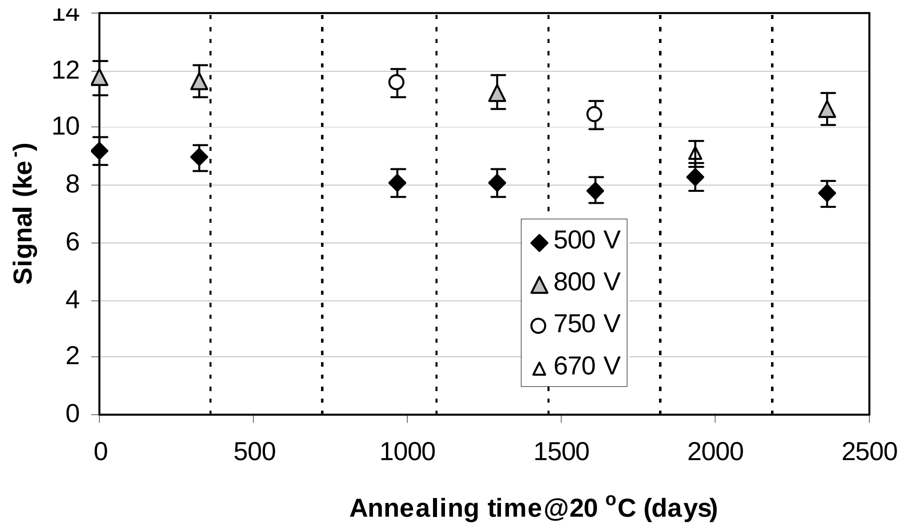
3.5 10^{15} p cm^{-2}

Initial V_{FD} ~ 1300V

Final V_{FD} ~ 6000V



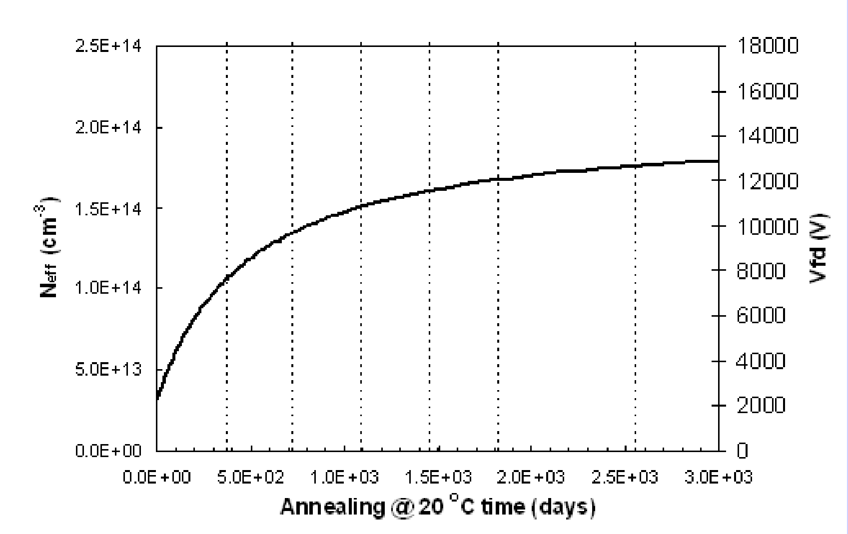


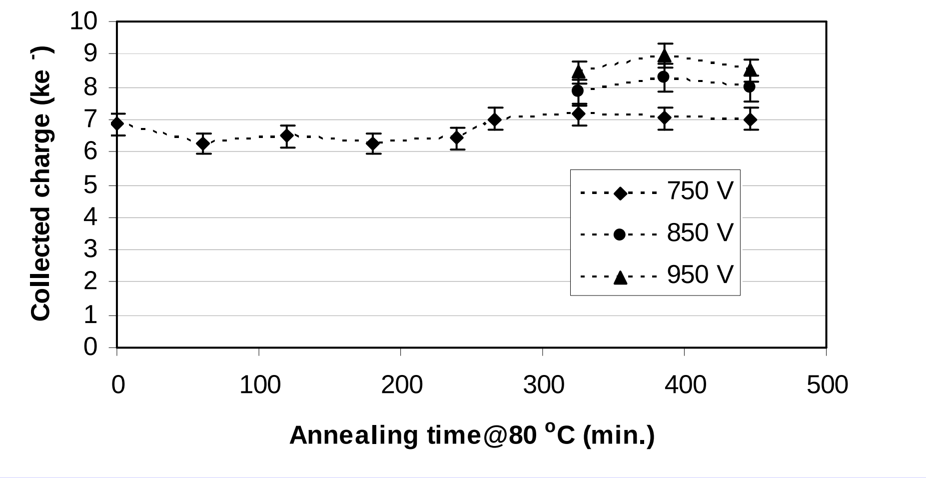


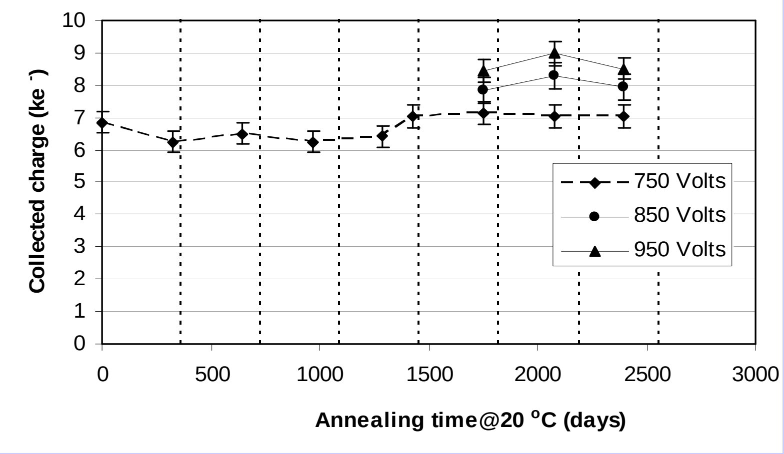
Reverse annealing of irradiated p-type detectors

$7.5\ 10^{15}$ p cm^{-2}

Initial V_{FD} ~ 2800V







Predictions from RD48 parameters for Oxygen enriched devices (best scenario: after 7 RT annealing years the V_{fd} goes from ~2800V to ~12000 V!

Noise in Si detectors

Can identify three parameters:

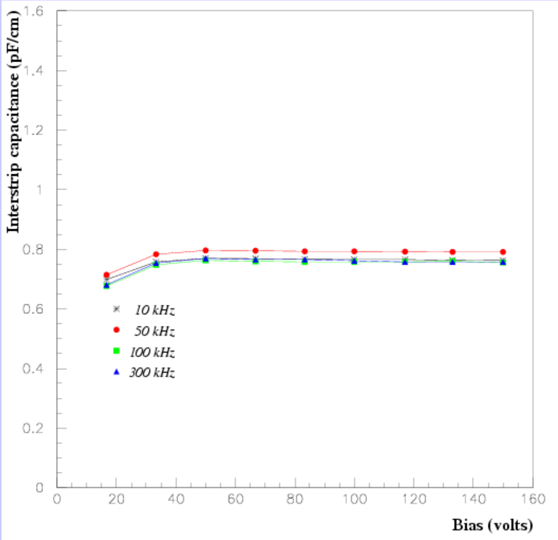
- Changes in the input capacitance
- Changes in the reverse current per channel
- Generation of micro-discharge noise

C related noise: ENC ~ 600+50*C_{in}(pF)

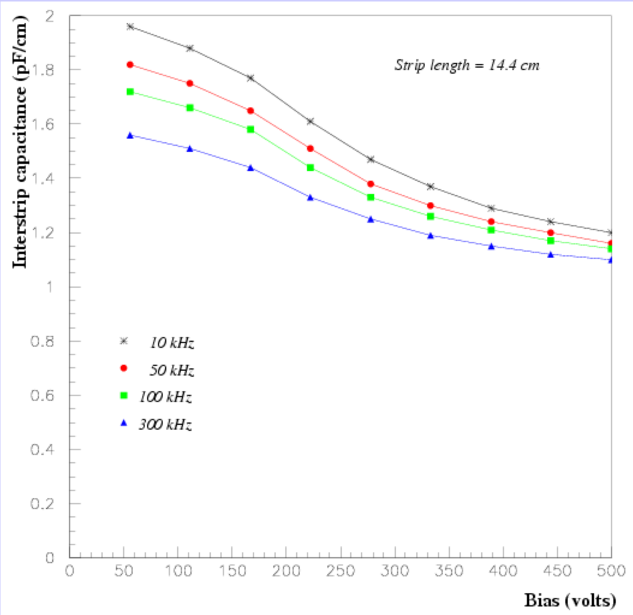
$$\text{shot noise (ENC)} \approx \sqrt{12\, I_{detector}\,(\text{nA})\; t_{shaping}\,(\text{ns})}$$

Changes of interstrip capacitance with Φ

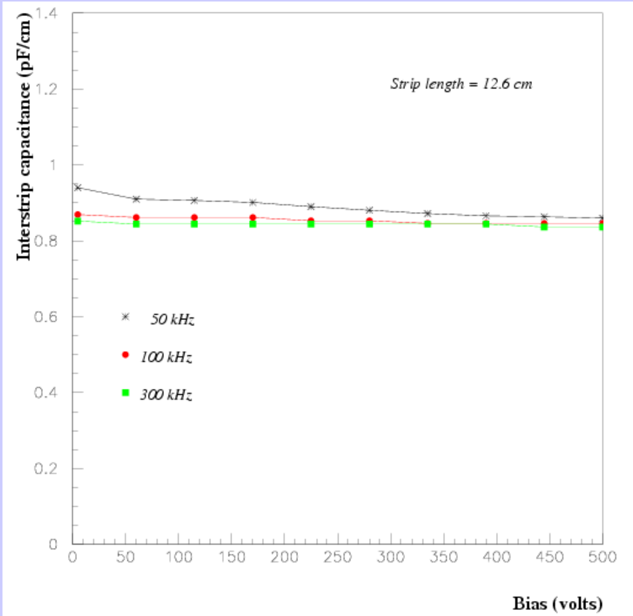
Pre-irradiation



<111> Si after $4x10^{14}$ p cm^{-2}

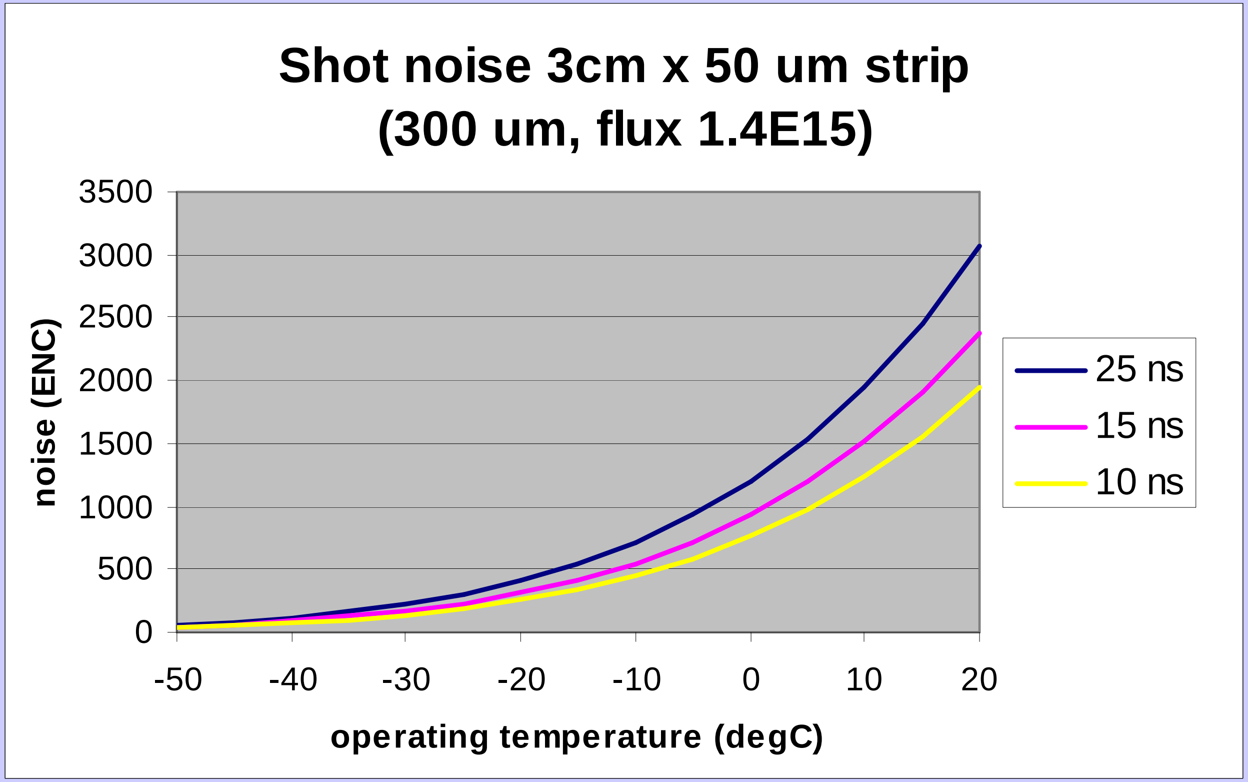


<100> Si after $4x10^{14}$ p cm^{-2}



Shot Noise

High leakage current also adds to the noise.

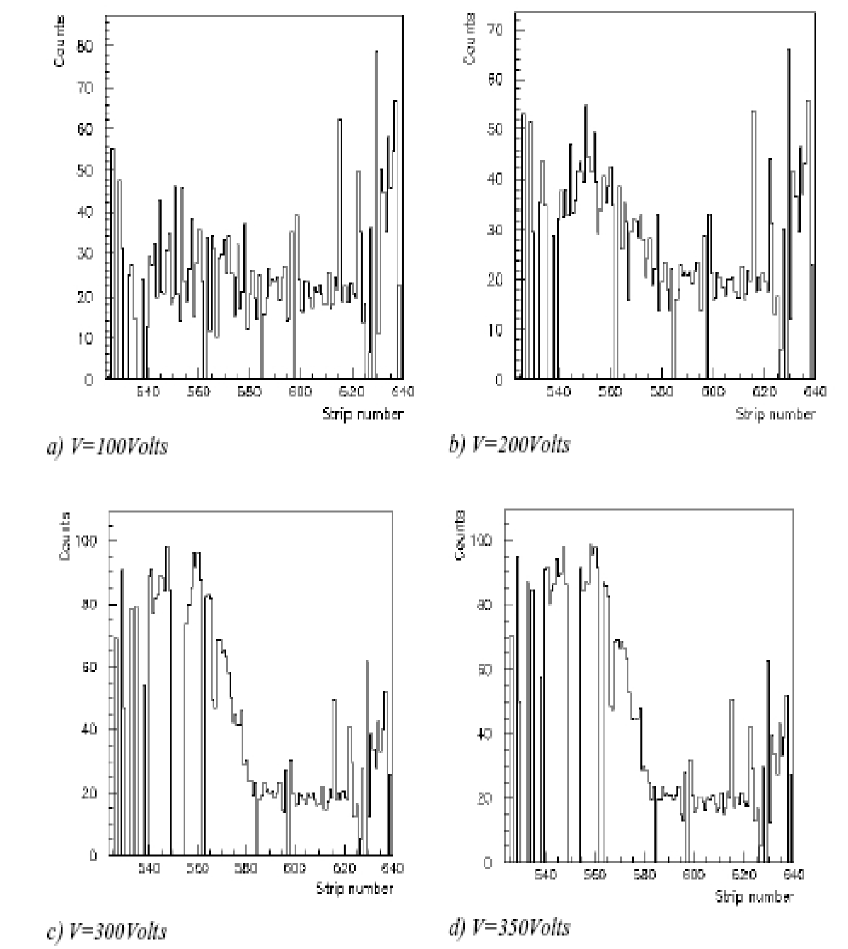


This gets added in quadrature to other noise contributions.

In short strip region probably need to keep total noise below ~1000ENC (for 25 ns shaping time).

To keep shot noise contribution below ~400enc, need to keep the operating temperature below -10 to -20°C.
(Shot noise reduced by 20% for 200µm sensor.)

Micro-discharge noise



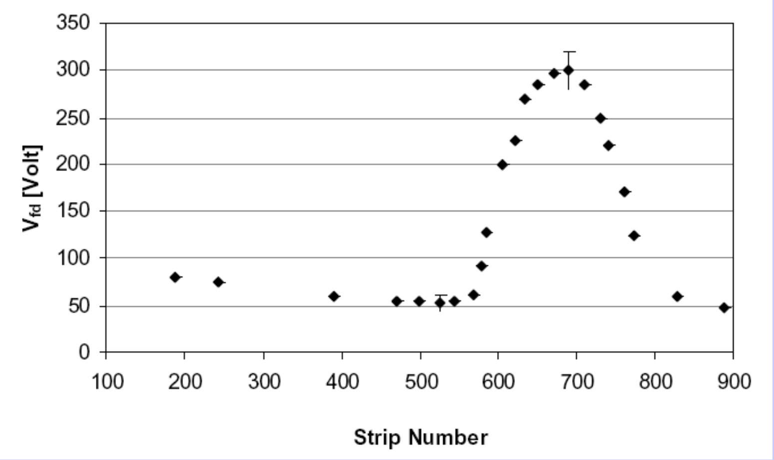
a) V=100Volts

b) V=200Volts

c) V=300Volts

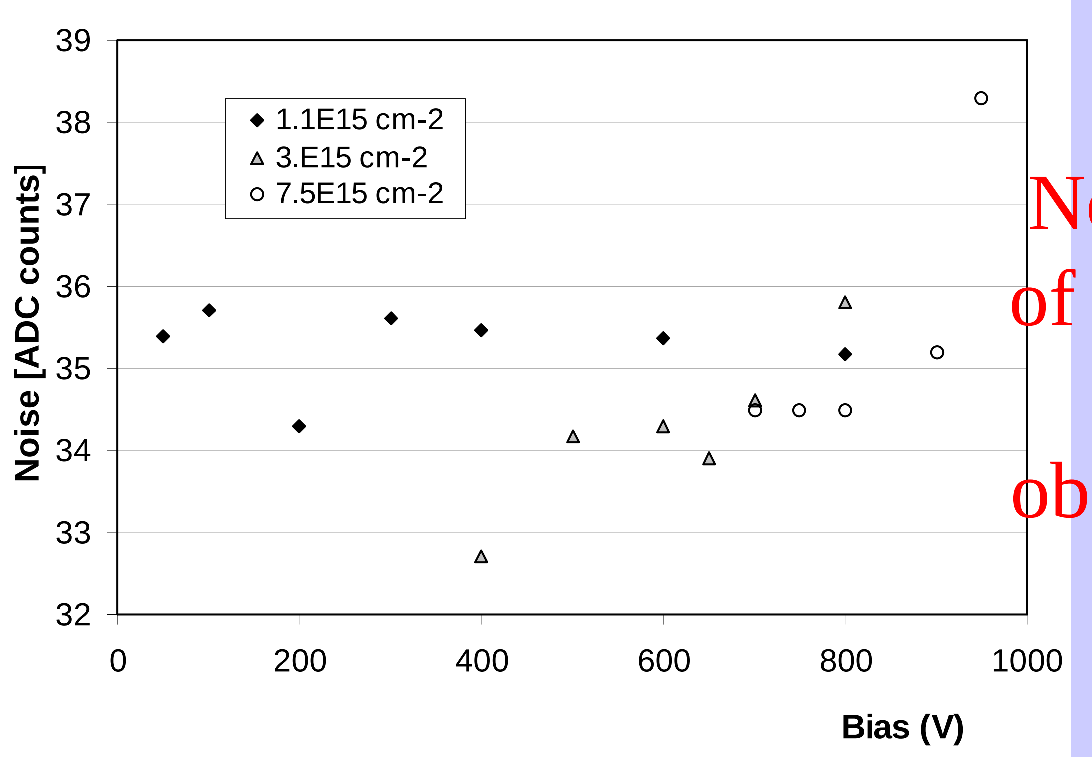
d) V=350Volts

Micro-discharges can represent the earliest mechanism of failure for micro-strip detectors when operated at high voltage, when high peak electric field are found. Here it is shown the development of micro-discharge noise in a partially irradiated p-in-n detector: the non-irradiated area has a higher electric field for the same applied voltage and the noise is clearly anti-correlated to the irradiation profile.



Noise in p-type miniature detectors

The irradiated devices (~280µm thick) show a remarkable robustness after irradiation, both in term of breakdown voltage and noise. The temperature should be kept low (in this case at -22^{o}C) to control the reverse current and avoid thermal run-away after heavy doses.



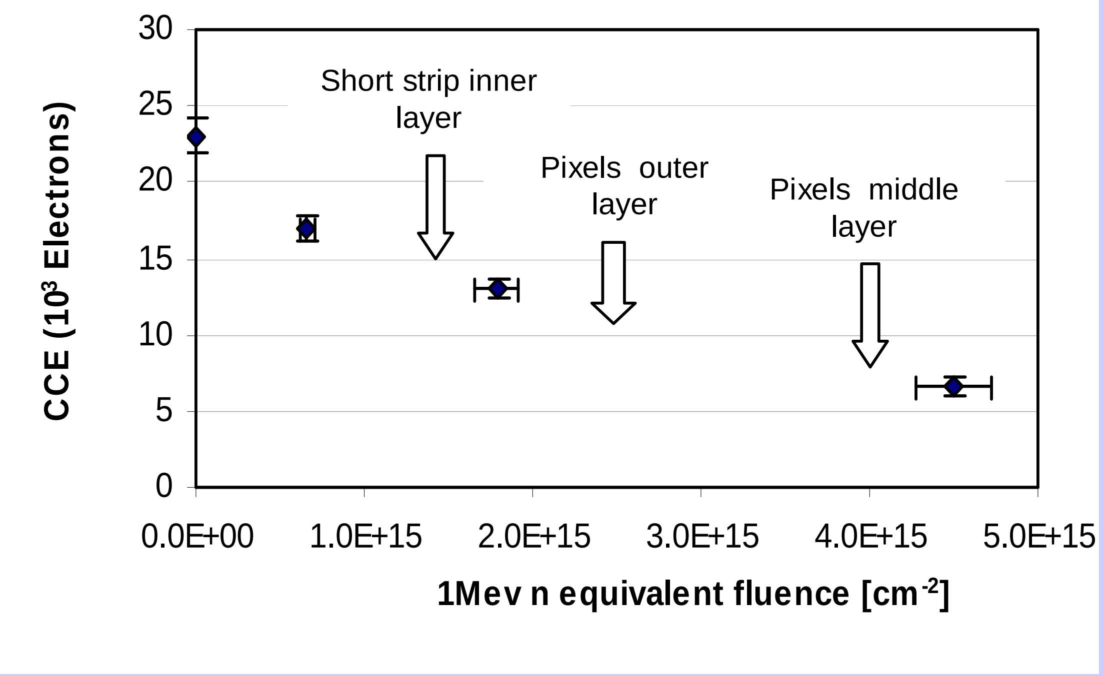
No sensitive dependence of noise on bias and dose!
No micro-discharges observed up to 950 Volts!

SLHC predictions

Signal over noise (S/N) can be taken as the criterion to fix the operation limit of silicon detectors in high radiation environments.

A tentative number of 10 can be assumed as a safe S/N to guarantee efficiency and purity of the reconstructed tracks.

SLHC predictions with p-type devices



Signal degradation measured with p-type detectors as a function of the 1MeV n Φ_{eq} for p-type micro-strip detectors

SLHC predictions with p-type devices

Assumptions on noise:
Unchanged by radiation
300e for pixels
1000e for inner short strips
1000e for inner short strips

Assumptions on speed: 25 ns shaping time

S/N figures at end of SLHC operations:
Innermost pixel layer: 3 (9 after 5 years).
Middle pixel layer: >20
Innermost short strips: 14
Innermost long strips: 10

Not enough!

Summary

Likely date for SLHC luminosity upgrade is around 2015.

Preparations for required inner tracker replacement have started.

The changes of V_{FD} shouldn't be use as a base for prediction.
For most layers n-side readout Silicon pixel/strip technology would provide at least 10 years of operation, as demonstrated by CCE(V) measurements.
b-layer may need new technology.

Probably need to operate sensors colder than at the LHC (around -20°C?)

Engineering may be the biggest challenge:

- Limited time to build the tracker
- Very limited space for services.
- Many channels, high power dissipation.
- Cooling to low temperature
- Many modules to be produced in a short time.

Thermal issues for SLHC

- Expected leakage currents and power dissipation
- Thermal runaway
- Shot noise

Concentrate on at short strip region.

Increase in leakage current

Flux dependence leakage current:

$$I = \alpha \, \Phi_{eq} V$$

- **Independent of bulk type**
- **Temperature dependent. Common to use $\alpha_{20°C}$ and calculate temperature dependence using:**

$$I(T) = I_{20^\circ C}\left(\frac{T}{293}\right)^2 \exp\left[-\frac{E_{gap}}{2k_B}\left(\frac{293-T}{293T}\right)\right]$$

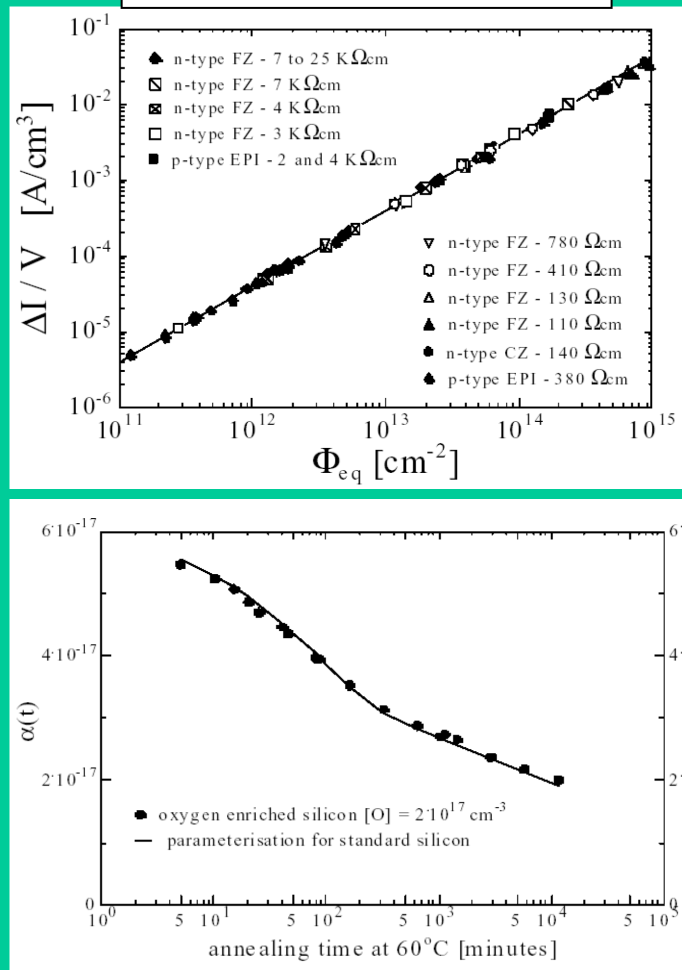
- **Annealing time dependent. $\alpha_{20°C}$ is:**

4E-17A/cm ⇒ ~400 days

5E-17A/cm ⇒ ~100 days ⇐ used here

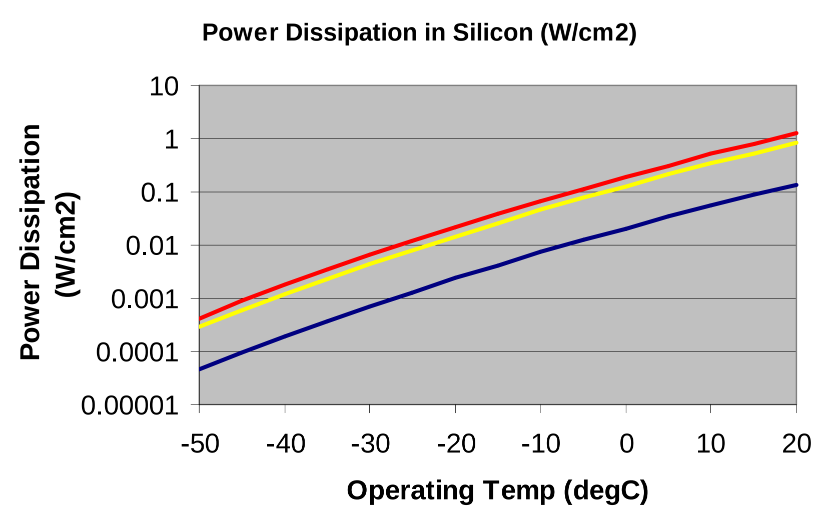
5.5E-17A/cm ⇒ ~25 days

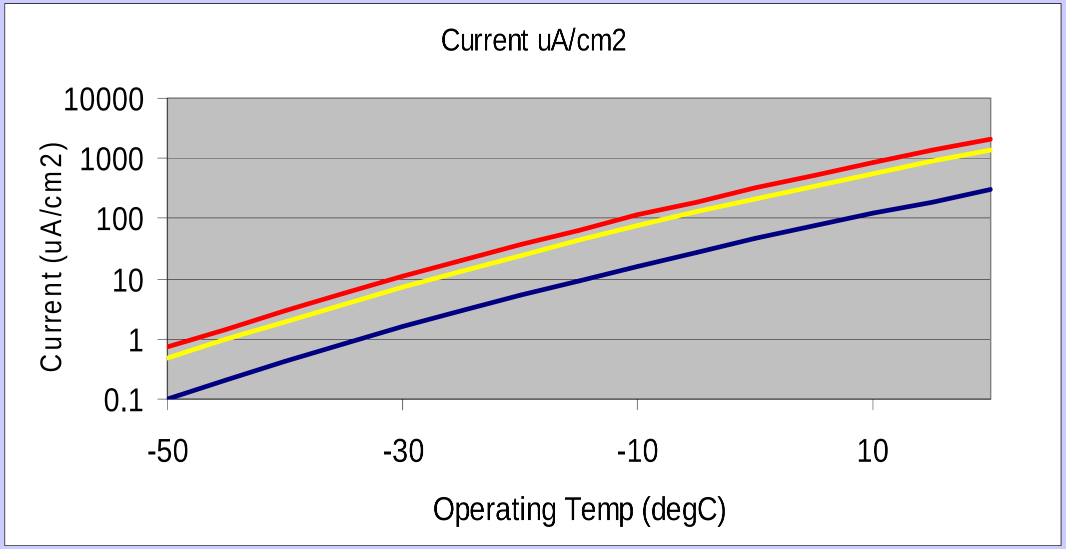
RD48 3rd Status Report



Current & power dissipation

Innermost short strip radius:





LHC: flux = 2×10^{14} n_{eq}/cm^2, bias = 450V, 300µm

SLHC: flux = 1.4×10^{15} n_{eq}/cm^2, bias = 600V, 300µm

SLHC: flux = 1.4×10^{15} n_{eq}/cm^2, bias = 600V, 200µm

Temperature	-40°C	-30°C	-20°C	-10°C	0°C	10°C	20°C
LHC (mW/cm^2)	0.19	0.70	2.4	7.2	21	54	135
SLHC (mW/cm^2)	1.8	6.5	22	67	192	508	1260

Currents: $\times$ 7
Power: $\times$ 10

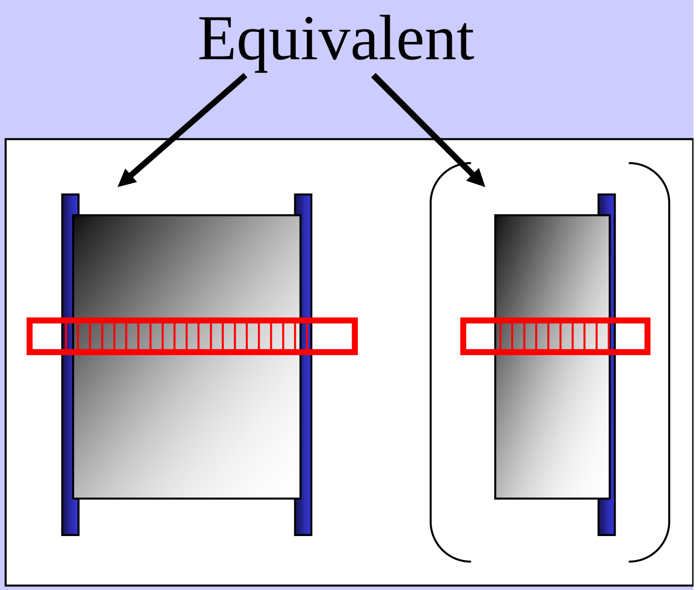
SLHC: to keep power dissipation same as LHC would need to run ~20°C colder.

Note: no longer needed to keep sensors cold outside operation! (At SLHC we will not operate sensors fully depleted, therefore reverse annealing is not a major issue.)

Thermal runaway

Strong temperature dependence power dissipation can lead to thermal runaway.

simple model:



Input:

Silicon sensor cooled at either end (no substrate or spine)

2 Cases: 4.5cm & 9cm wide (results independent thickness)

Assumptions:

Heat exchange in 1 dimension only

Perfect connection to cooling

Thermal conductivity Silicon: 130 W/mK

Model to determine the thermal runaway points:

- Take "strip" across the sensor and divide into small cells.
- Calculate power dissipation and heat exchange every 1 ms in each cell.
- Continue until it stabilises or diverges.

Alternative model (cross-check):

- Use equilibrium condition: dissipated power + heat conduction = 0

Thermal runaway results

Temperature gradient across sensor for different coolant temperatures.

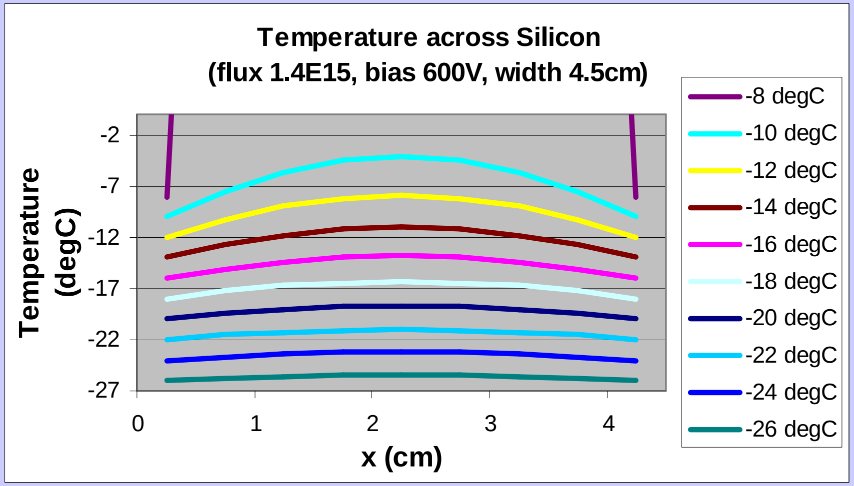
Thermal run-away points:

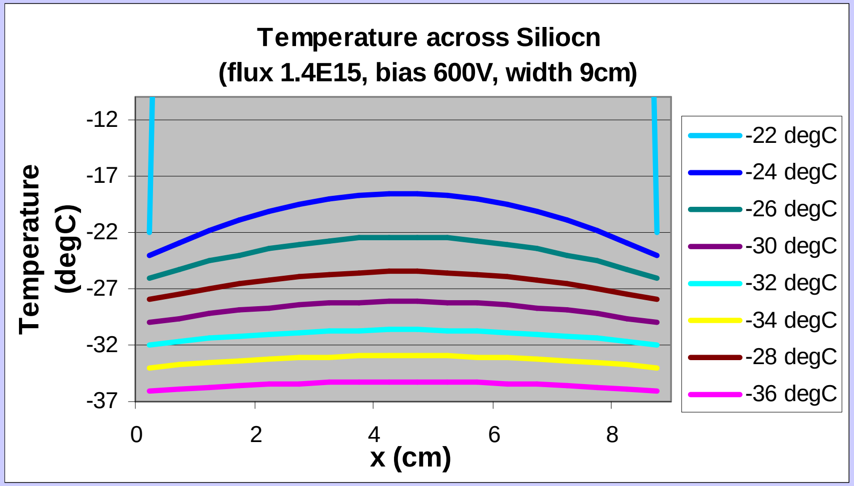
4.5cm wide sensor:~ -9°C

(+17 °C for LHC)

9cm wide sensor: ~ -23°C

(-1 °C for LHC)





Thermal runaway temperatures down by 22 to 28°C (LHC⇒SLHC).

- **need a spine or substrate underneath sensor for heat extraction**
- **need to run Silicon colder than at LHC**

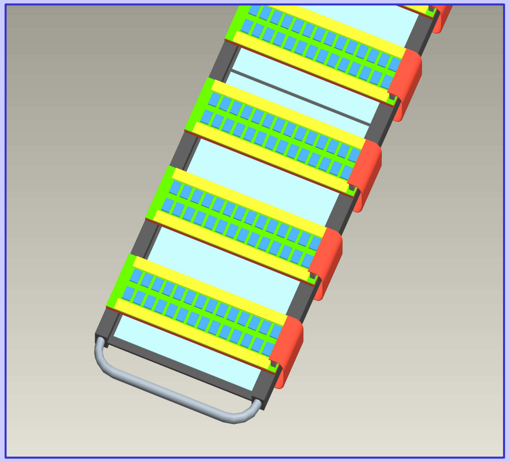
NOTE: heat from ASICs or environment not included!)

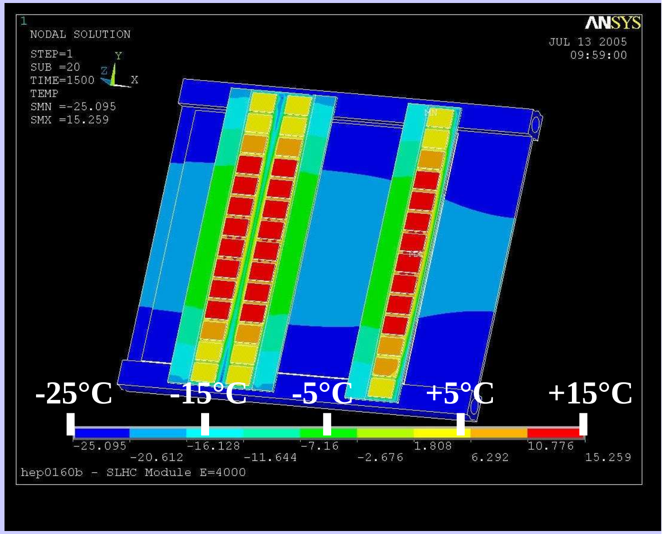
- **Probably need good thermal isolation Silicon to ASICs**

Full Thermal simulation

Full simulation including proper treatment of heat input from environment and ASICs can be done in finite element simulation (e.g. ANSYS).

But needs a detailed module design.





FIRST ATTEMPT

Stave

single sensor layer

carbon-carbon

1mm carbon-carbon under sensor

Sensor

8 cm wide, 300µm, 3 cm strips

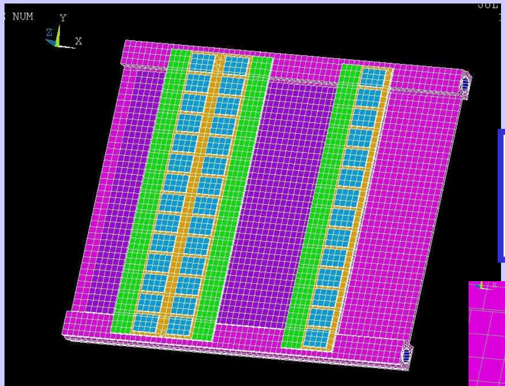
Φ= 2.2×10^{15} n$_{eq}$/cm^{2,} V$_b$= 800 V

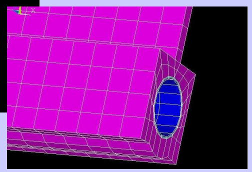
Hybrid:

CC base with thin kapton layer

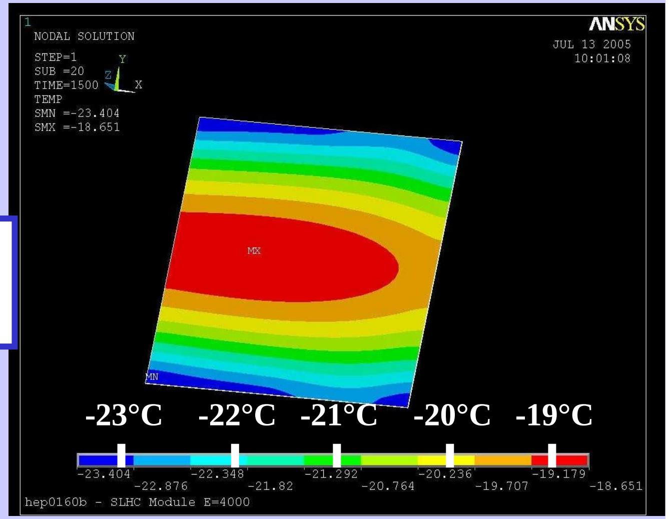
14 chips per sensors (0.5 W)

distance to hybrid 2.7 mm (air)





Efficient cooling using -25 °C coolant.
But simulation still incomplete.



Conclusions Operating temperature

Thermal runaway point is down by 22 to 28°C!

- Need efficient coupling to cooling (spine or substrate) and thermal decoupling from ASICs.
- Need to operate colder.

Shot-noise considerations suggest to operate below -15 to -25°C. (depends on expected signal from sensor)

Obvious challenge designing a cooling solution a to operate this cold.

Cooling challenge

Good experience with C_3F_8 evaporative cooling system for the current SCT.

- constant temperature throughout cooling lines
- high cooling capacity (limited flow)

Also in current SCT (endcap modules) successful thermal separation hybrid and sensors

<u>For the SLHC:</u>

- more modules
- more power dissipation
- operation of sensors at lower temperature

Use two-phase cooling again.

Limited number of coolants available. Likely candidates:

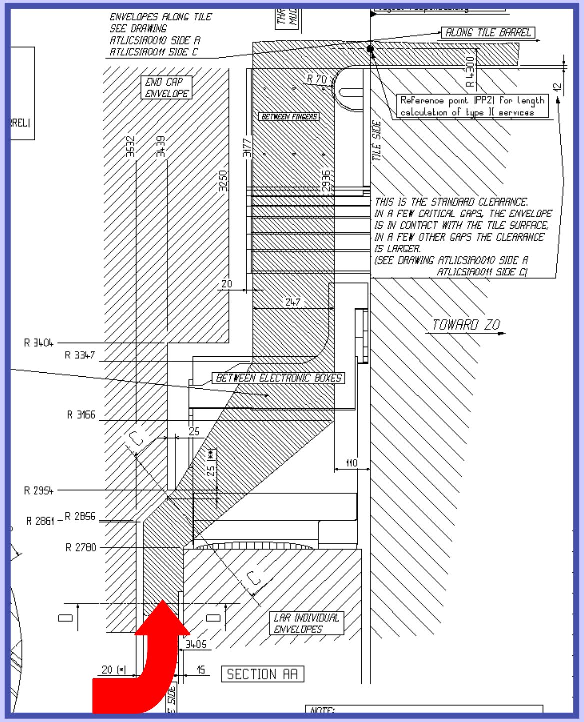
- C_3F_8
- CO_2 (operated at high pressures, but high cooling capacity, i.e. thin tubes)

Still need efficient thermal decoupling sensors and ASICs

Other challenges
(mainly for middle and outer radii)

Replacement inner tracker will need to fit in the same space as the current one.

The same goes for the services! (Almost factor 10 more channels in SCT/TRT region!)



Limited time for building system with many modules!

Should make something that's easy to build.

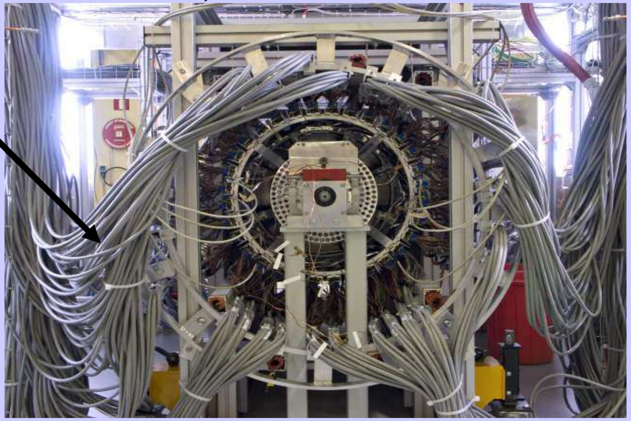
Where possible use experience of the current build.

- Build something similar or completely different?

Electronics and power distribution

Front-end electronics will almost certainly be deep-submicron.

- Reduced power dissipation per chip but more chips. Overall about a factor 2 power increase.
- Low driving voltages (large voltage drop, or thick cables)
- Cannot afford to have thousands of these



Shared power to modules.

DC-DC conversion near the modules.

Readout

Similar problem, more channels limited space.

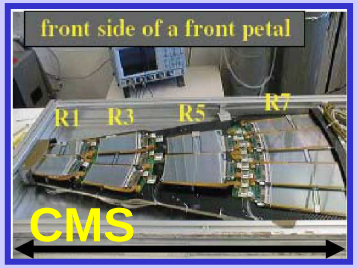
Use shared high speed optical links.

Some engineering issues

Main considerations are dead material budget, reliability of services, ease of construction.
Detectors needs to be mass produced in a relatively short time!

Staves on a space frame: easy to build and handle, fewer connectors(?)
Modules on barrels: less dead material(?) mechanically more stiff, i.e. better knowledge module positions.

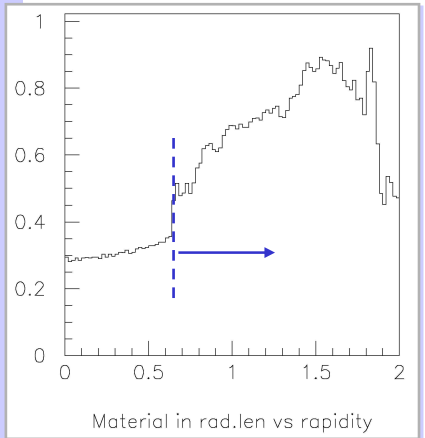
Full disks or "petals": full disks would have ~2m diameter!



Layout:

- Long barrel + few disks (compared to short barrel and more disks): material services shifted away to higher rapidity. Easier for pattern recognition. Higher inclination detectors to tracks.

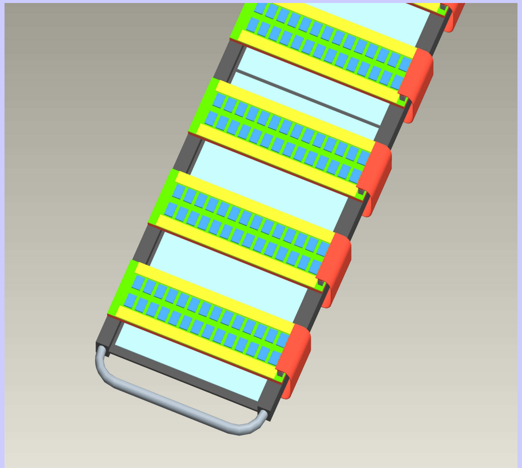
Material current inner tracker

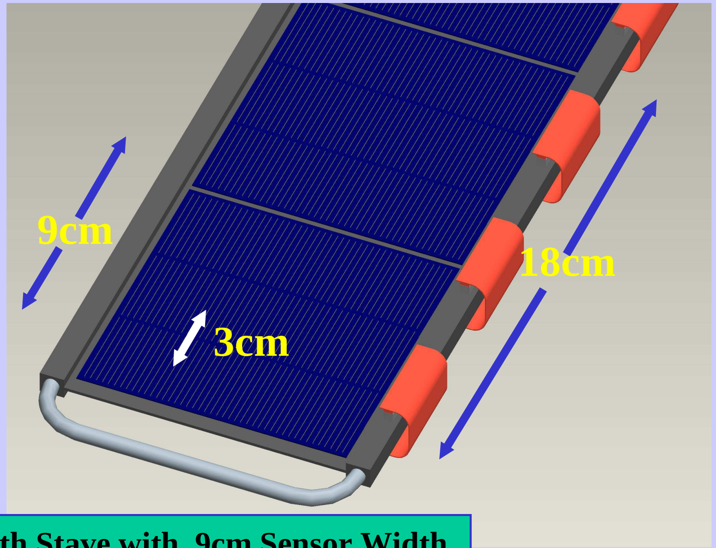


Overall engineering:

- Insertion tubes: independent subassembly different layers
- Integrated detector (excl. b-layer on beam-pipe): less material, better control over position layers.

Stave Concept for Short Strip Layers





Z=0 End of 144cm Length Stave with 9cm Sensor Width

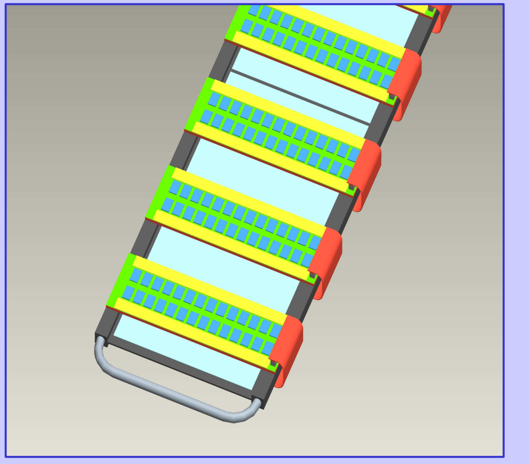
- Mechanically stable
- Efficiently cooled (high thermal conductivity substrate/spine)
- Optimal use 6'' wafer

  ⇒ 9×9cm sensor (3 sets of 3cm long and 50 μm pitch strips)

Single sensor layer on stave

Double (28 chip) hybrids

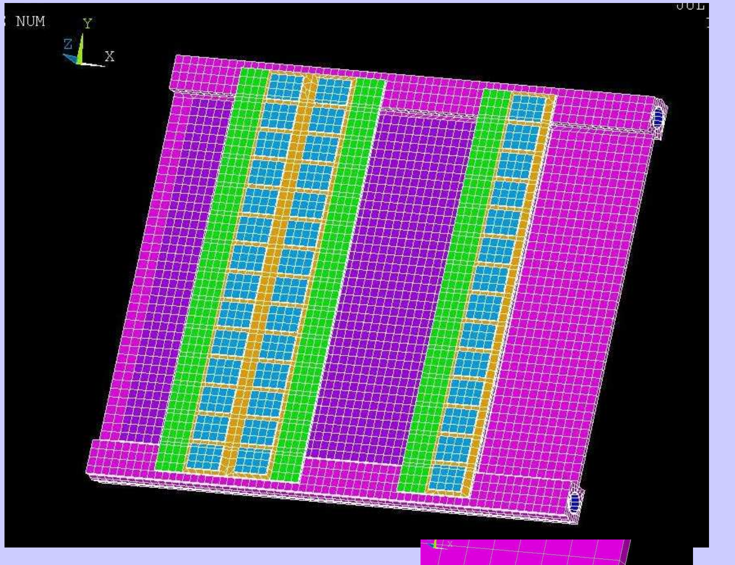
Thermal simulation

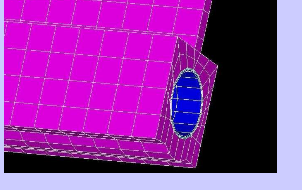


Work done using ANSYS package (finite element thermal simulation)

<u>Added to this package: simulation heat dissipation in Silicon (including the temperature dependence).</u>

Work based on ladder design with single sensor layer.





<u>In ANSYS:</u>
- **carbon-carbon ladder**
- **diameter cooling pipe 5mm**
- **CC substrate under sensor 1mm (too thick!)**

<u>Sensor</u>:
- **8 cm wide, 300μm, 3 cm length strips**
- **power based on: $\Phi = 2.2\times10^{15}$ $n_{eq}/cm^{2,}$ $V_b = 800$ V**

<u>Hybrid</u>:
- **CC base with thin kapton layer**
- **14 chips per sensors (0.5 W)**
- **distance to hybrid 2.7 mm (air)**

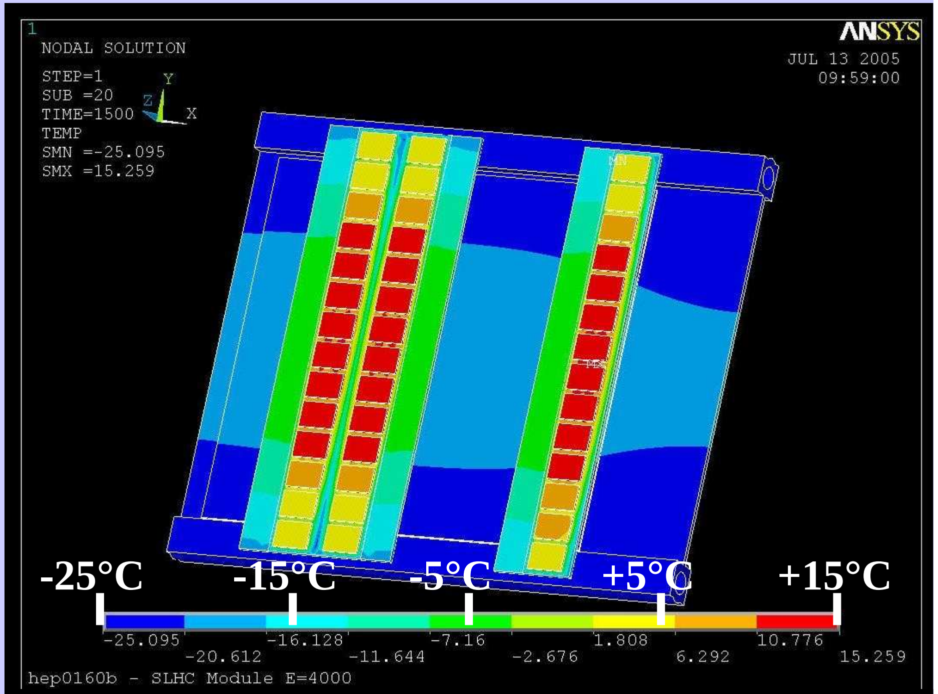
Thermal runaway model: Results

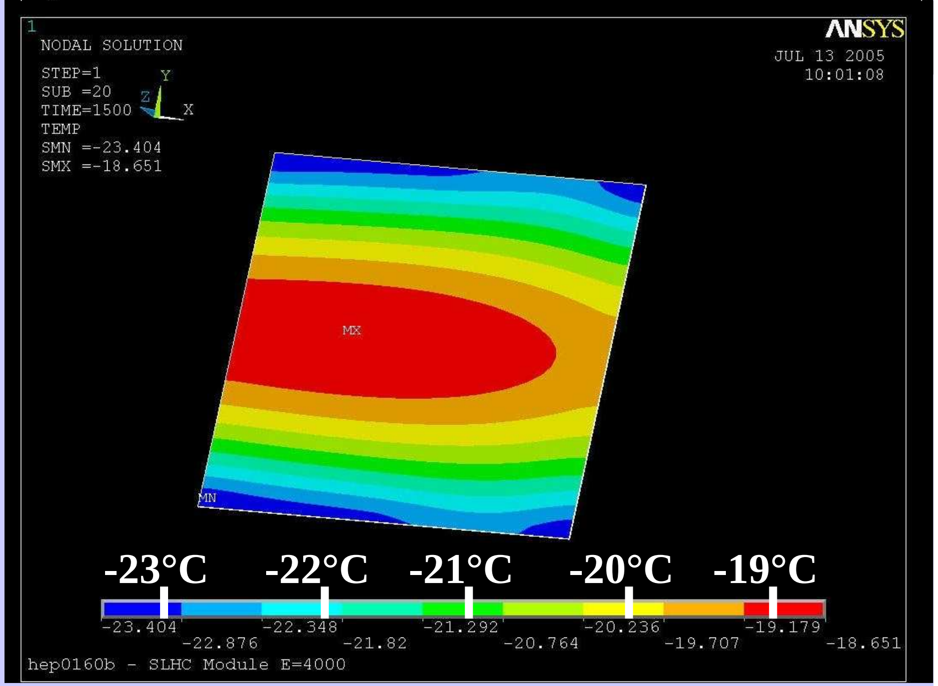
Coolant temperature: –25 °C

Sensor: hottest point ~ –19°C
Hybrid: hottest chip ~ +14°C

No sign of thermal runaway with –25 °C coolant temperature.

Some caveats:
- substrate is unreasonably thick
- simulation still incomplete, e.g. heat input from electronics and environment in to silicon needs more detailed treatment.





Trigger at the SLHC
G.Polesello, genoa workshop

Triggering at $10^{35}\text{cm}^{-2}\text{s}^{-1}$

Strategy:

- High-threshold inclusive triggers addressing high-p_T (discovery?) physics
- Pre-scaled semi-inclusive triggers selecting calibration samples (e.g $Z \to \ell\ell$)
- Exclusive menus to select specific final states already observed at the LHC (e.g. specific Higgs or SUSY decay channels)

Channel	Threshold (GeV)	Rate (kHz)
Inclusive isolated e/γ	55	~ 20
Di-electrons/di-photons	30	~ 5
Inclusive isolated muon	30	~ 25
Di-muons	20	< 5
Inclusive jets	350	~ 1
Jets + $\not{E}_T$	150,80	$\sim$ 1-2
Total		50 kHz

Possible example of first level inclusive menus

Tracking requirements

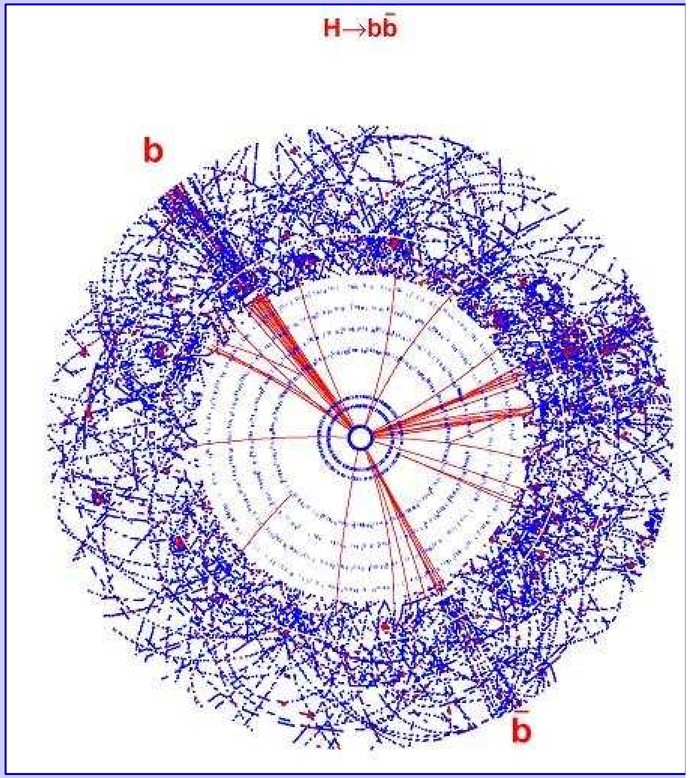
<u>Tracking requirements:</u>

- Efficient tracking/pattern recognition ($|\eta| < 2.5$)
- High momentum resolution ($\Delta p/p < 30\%$ for $p = 500$ GeV/c)
- Efficient b-tagging
- Fast trigger (level 2)

High multiplicity environment.

LHC: 3 years $L=10^{33}cm^{-2}s^{-1}$, then $L= 10^{34}cm^{-2}s^{-1}$

~23 collisions and ~2000 tracks per bunch crossing



<u>Detector requirements</u>

- Several space points with adequate precision in both rφ and z to limit ambiguities
- Very precise rφ space points over significant range of radii
- Limited material
- Precise space point near IP

Further constraints

In addition to high track multiplicity:

<u>High radiation levels</u>

- Radiation damage
  - degradation signal/noise
  - Silicon
    - thermal management
    - high voltage operation

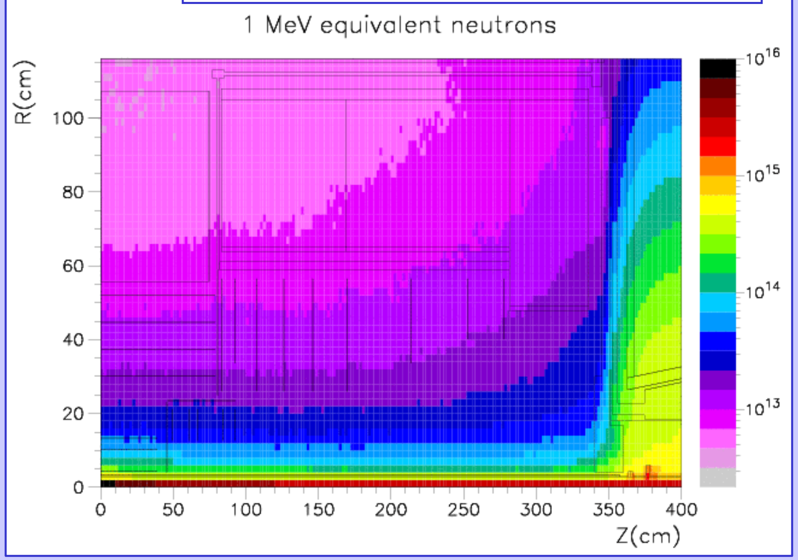
<u>25 ns bunch-crossing time</u>

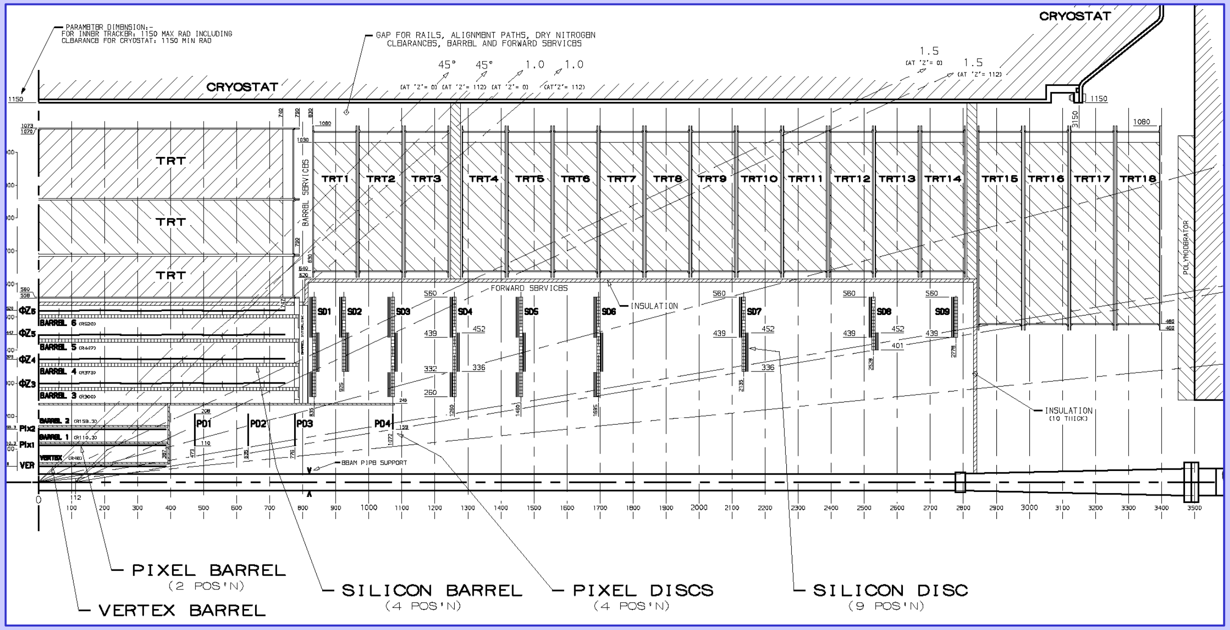
- Fast readout detectors

<u>Aim for detectors to work for 10 years.</u>

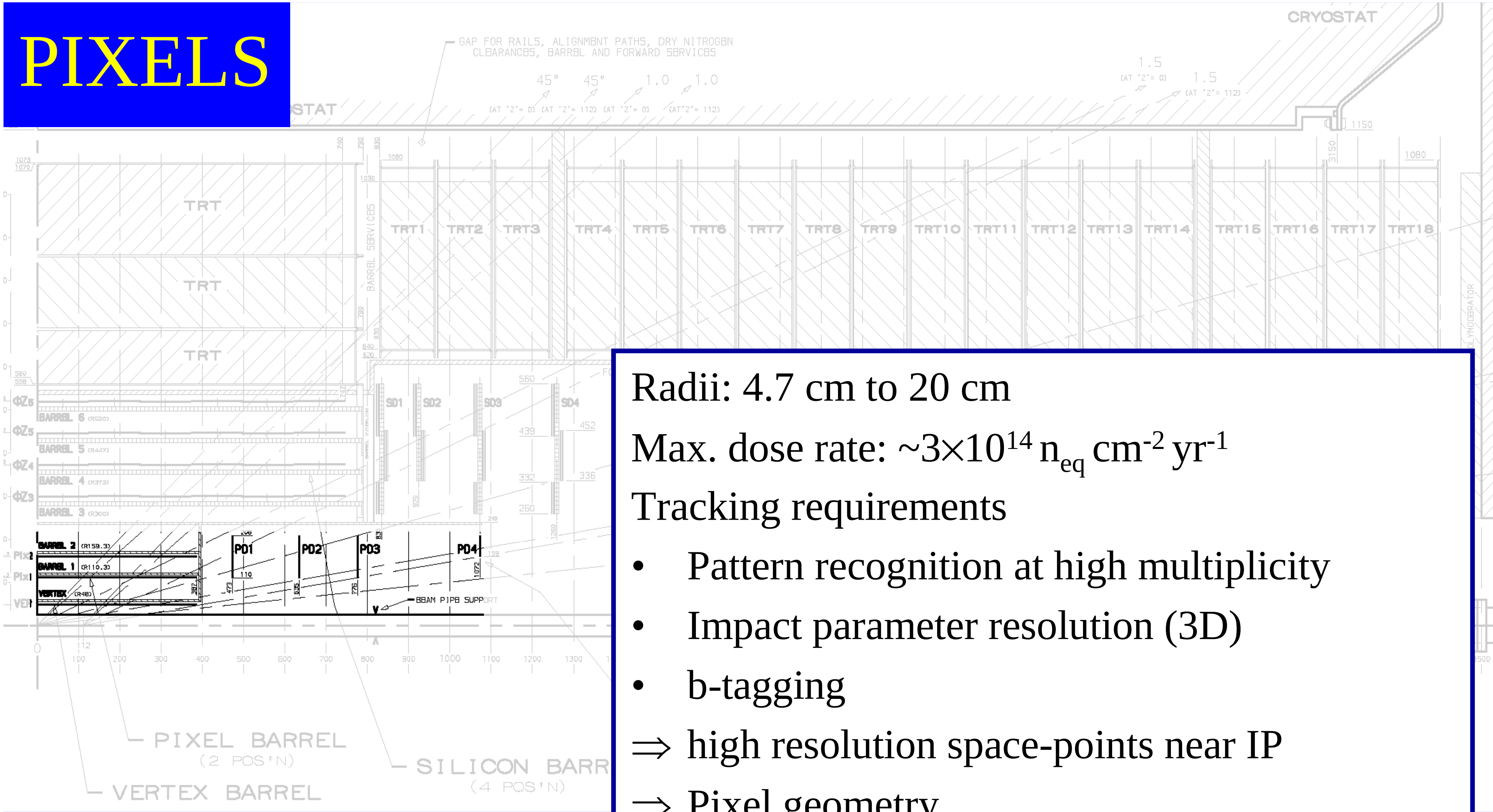
<u>Natural to separate regions of different radii</u>

Ian Dawson, Genova workshop





PIXELS



Radii: 4.7 cm to 20 cm

Max. dose rate: ~3×10^{14} n_{eq} cm^{-2} yr^{-1}

Tracking requirements

- Pattern recognition at high multiplicity
- Impact parameter resolution (3D)
- b-tagging

⇒ high resolution space-points near IP

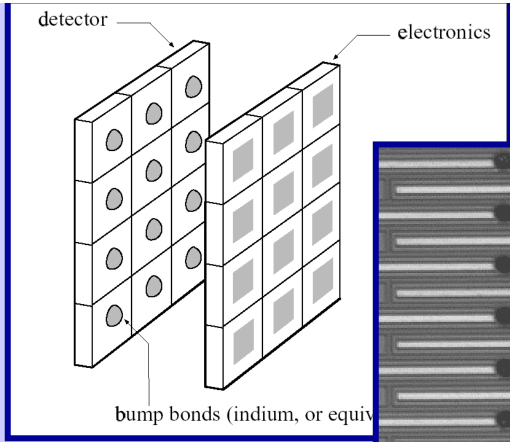
⇒ Pixel geometry

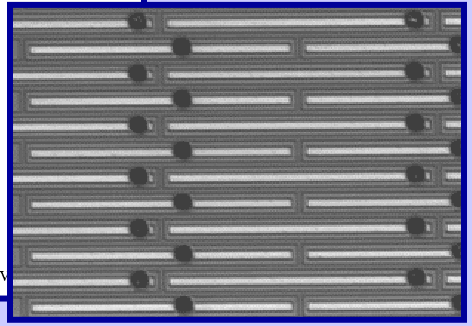
Big challenge is radiation-hardness

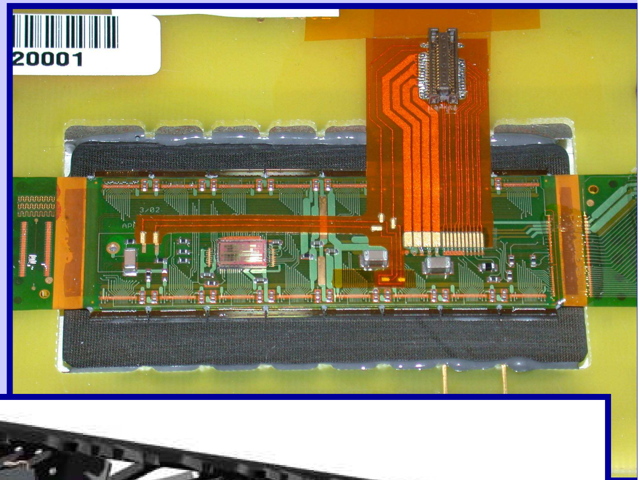
PIXEL Detector:

Sensors:

- HAPS (hybrid active pixel sensor)
  (pixel sensor bump-bonded to readout chip)
  $50 \times 400\ \mu m$ pixels $\Rightarrow \sigma_{r\varphi}=12\mu m$, $\sigma_z=66\mu m$
- Radiation hard sensor (n+-in-n oxygenated silicon) operated at -6°C

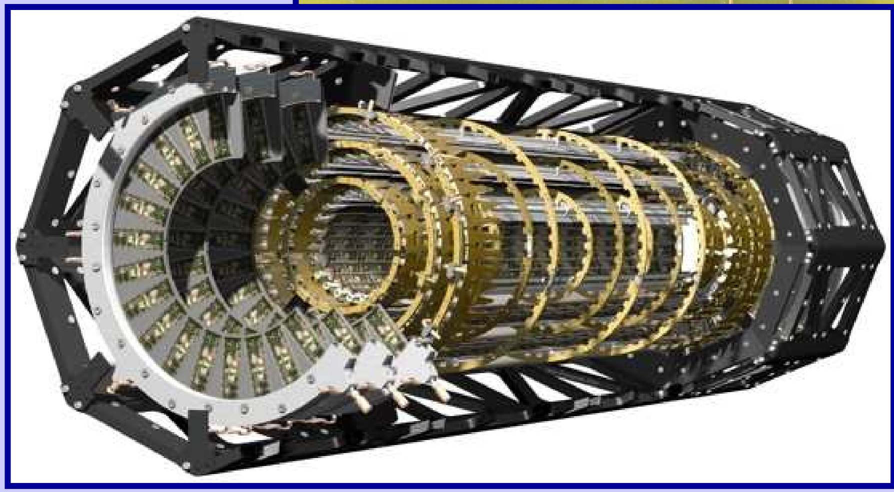




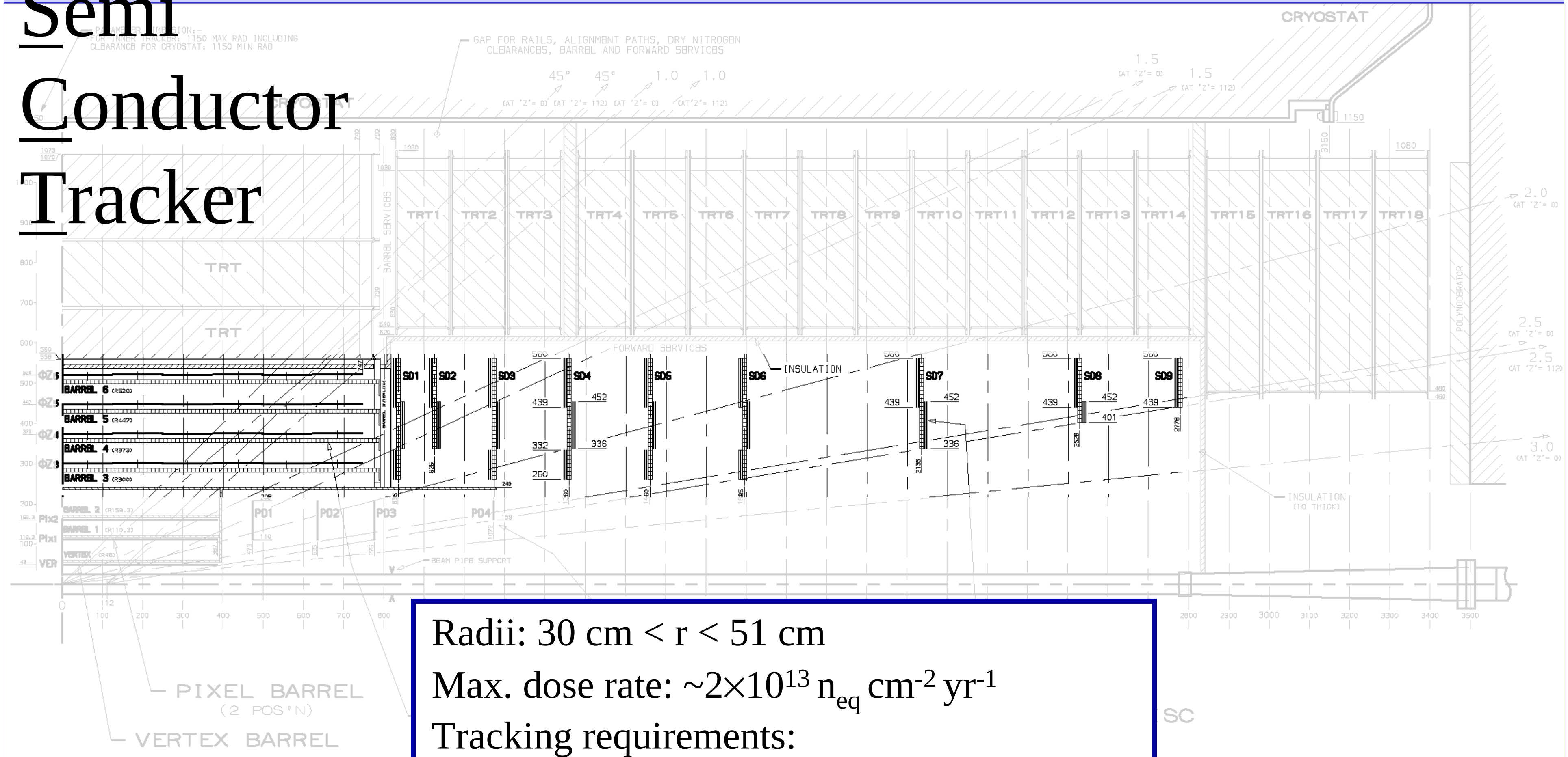


Detector:

- 3 barrels
  - "disposable(?)" b-layer @ 4.7 cm
    $\Rightarrow$3 years at $L=10^{33}cm^{-2}s^{-1}$ +
    1 year at $L=10^{34}cm^{-2}s^{-1}$
  - 2 layers at 10.5 cm and 13.7 cm
- 2×3 disks
- 3 high resolution space points per track
- ~80M channels



Semi Conductor Tracker



Radii: 30 cm < r < 51 cm

Max. dose rate: ~2×10^{13} n_{eq} cm^{-2} yr^{-1}

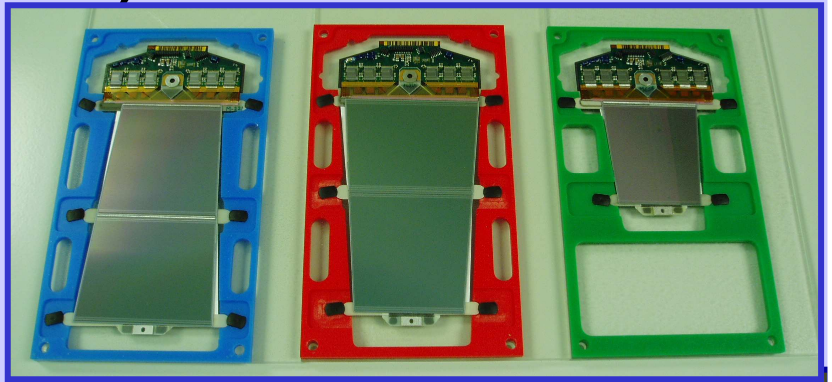
Tracking requirements:

- Contribution to pattern recognition
- Strengthen momentum resolution

⇒ high resolution in rφ

⇒ Slightly less high granularity in z

Semi Conductor Tracker (SCT)



Sensors/modules

- Silicon strip detector: 80 μm × 12 cm strips (shorter at high η)

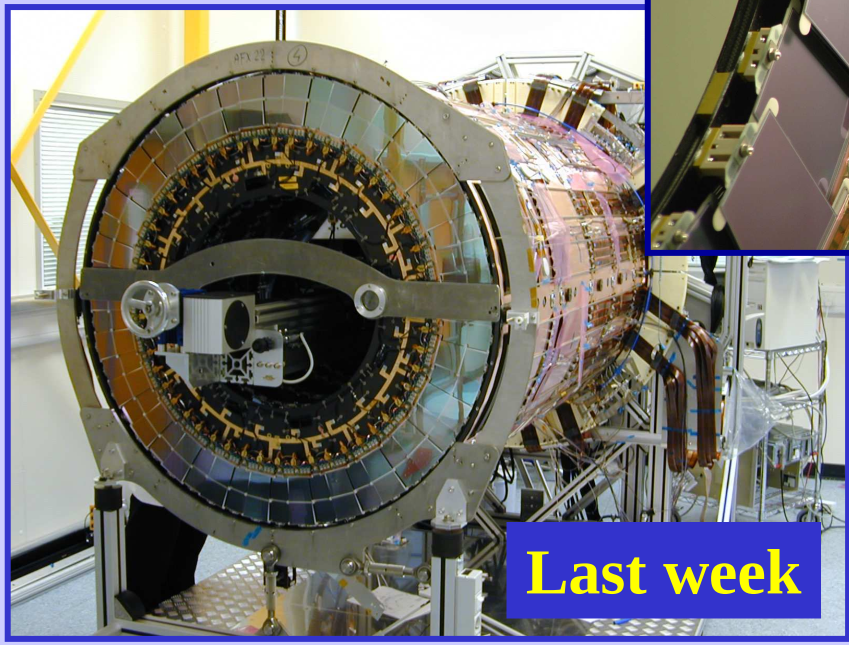
  (note: pitch constrained by occupancy not by momentum resolution!)
- p-in-n Silicon, operated at -7°C.
- Two sensor layers per module (small stereo angle)
- Space points with $\sigma_{r\varphi}$=16μm, σ_z=580μm

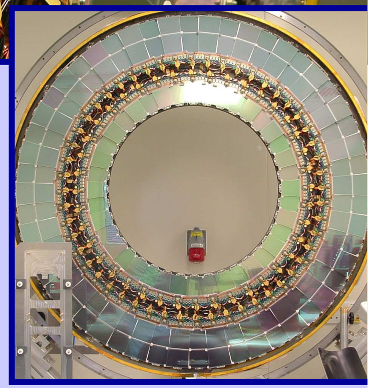
Detector

- 4 barrels,
- 2×9 wheels

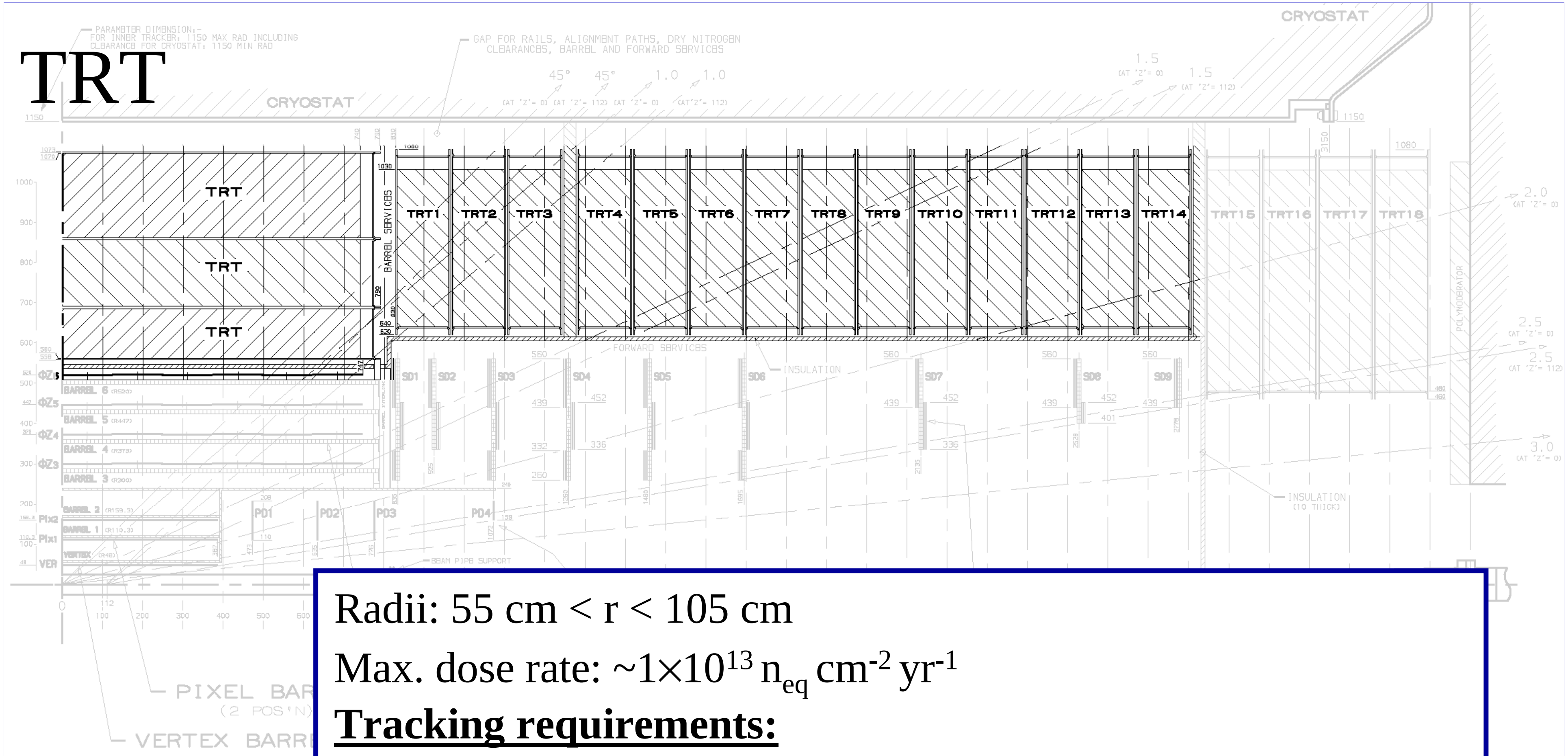
⇒ 4 space-points per track.

⇒ 6.3M channels





TRT



Radii: 55 cm < r < 105 cm

Max. dose rate: ~$1\times10^{13}\ n_{eq}\ cm^{-2}\ yr^{-1}$

Tracking requirements:

- Strong contribution to pattern recognition
- contribution to momentum resolution
- Fast track trigger (level 2)
- Standalone electron ID

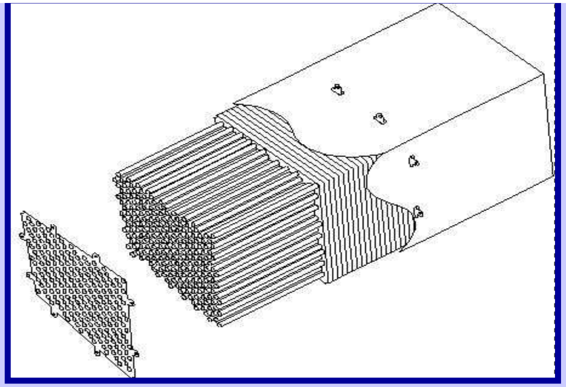
⇒ Many space-points combined with relatively high granularity.

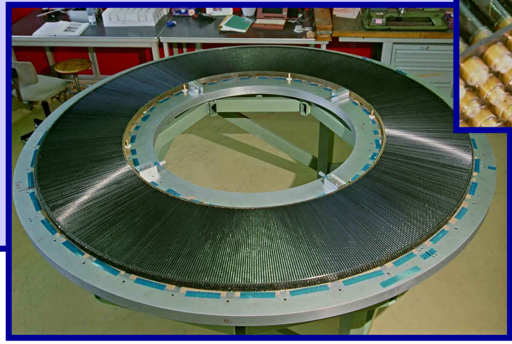
TRT

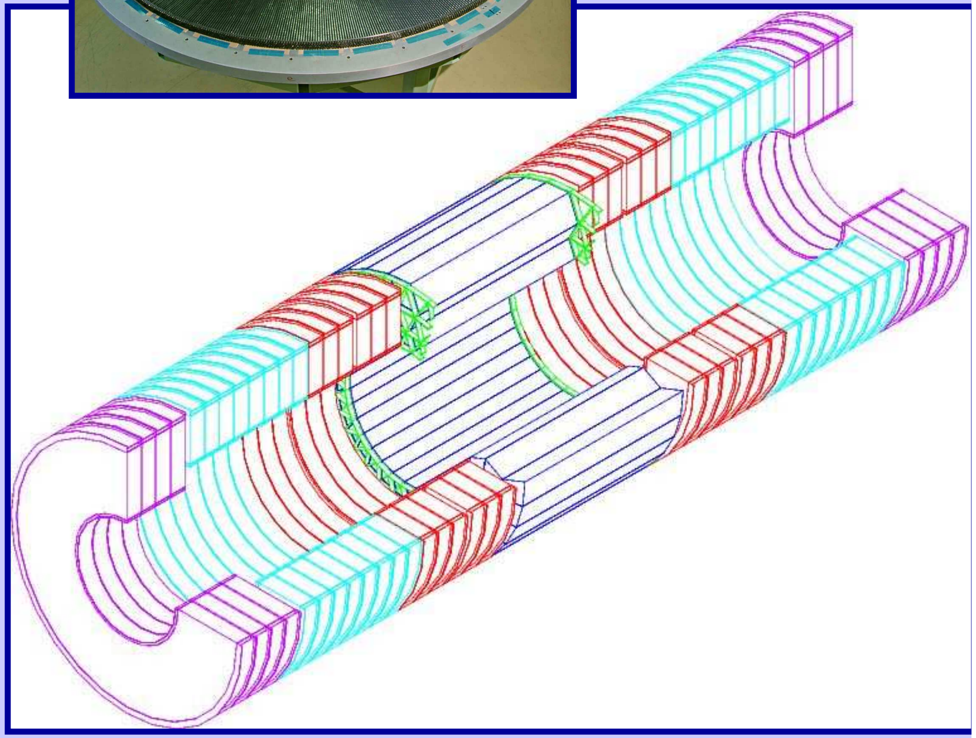
Technology:

Thin-straw drift tube tracker.

- d_{tube} = 4 mm, d_{wire} = 30 μm
- many space points (~36 per track)
- per straw $\sigma_{r\varphi}$=170μm
- polypropylene foils/fibres added in between straws to induce transition radiation for electron identification (independent of the EM calorimeter)







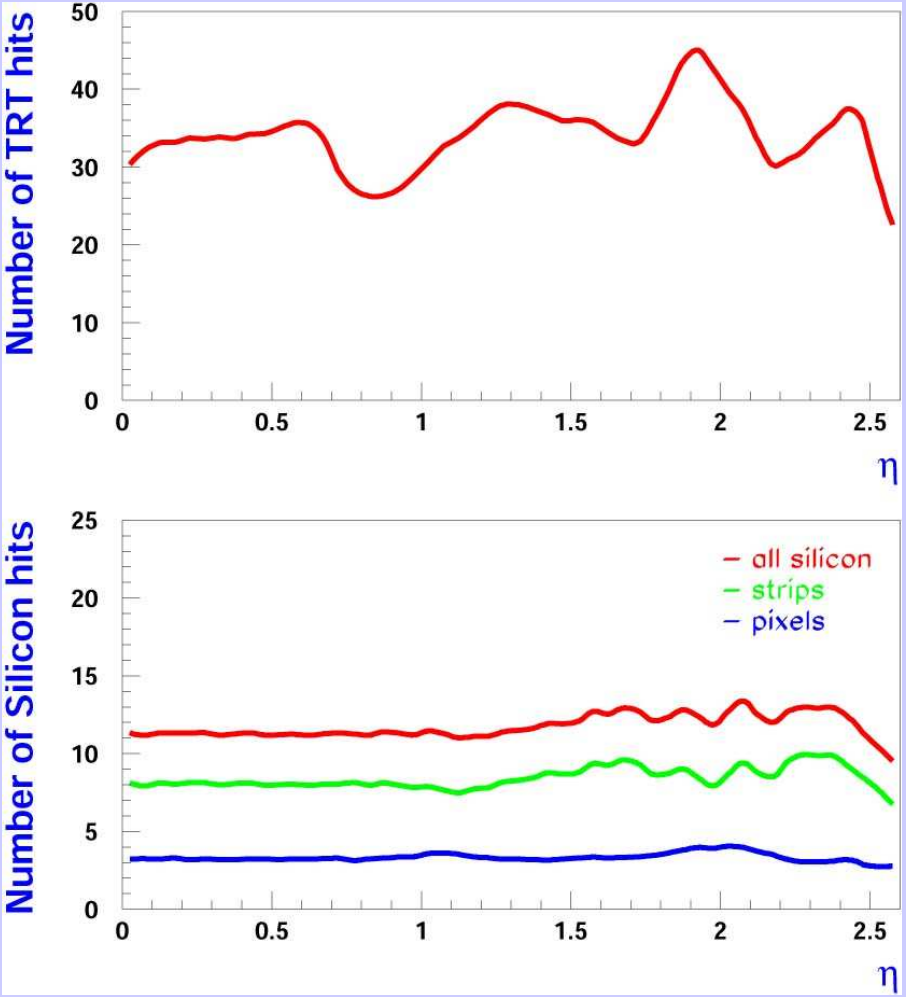
Detector:

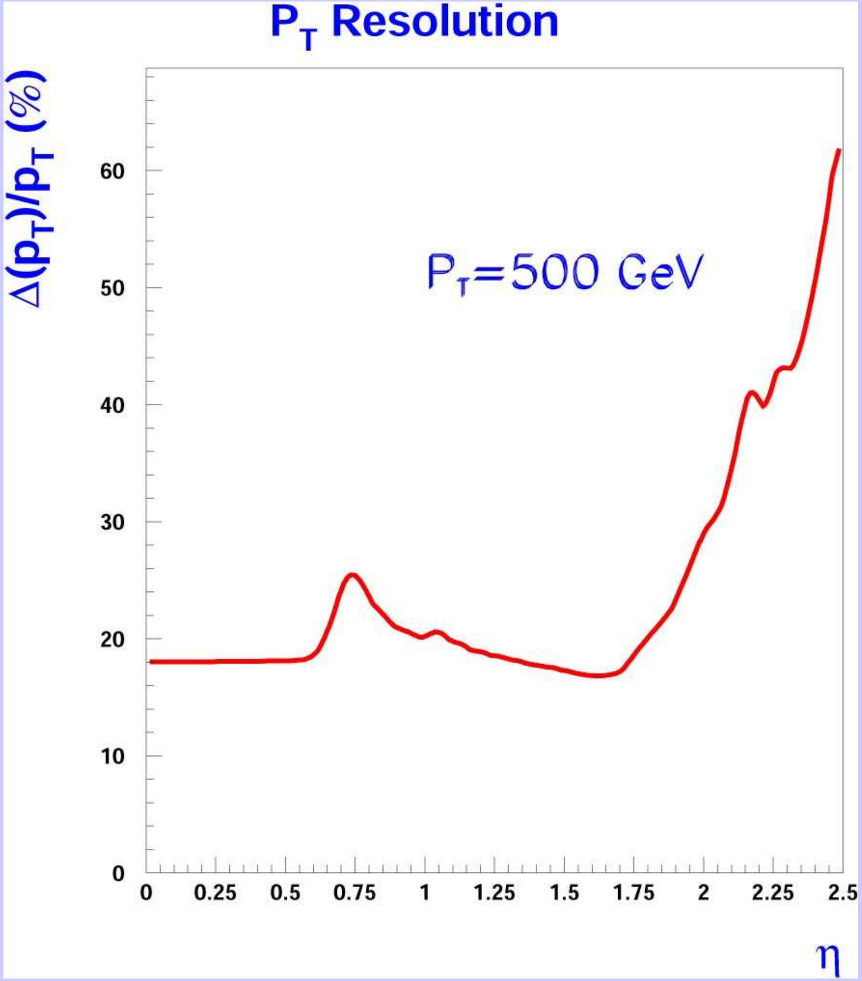
- Barrels:

  longitudinal straws + radiator fibres.
- Disks:

  radial straws + radiator foils.
- ~400k channels.

Overall Inner tracker performance (TDR)



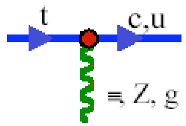


Other implications SLHC

- Replacement electronics for calorimeter and muon systems
- New beampipe
- …

Flavour-Changing-Neutral-Current top decays
G. Polesello, Genoa workshop

FCNC top decays at the SLHC



Most measurement in top sector (e.g. $\sigma(m_{top}) \sim 1$ GeV) limited by systematic

$\Rightarrow$ no improvement at SLHC

Exception: FCNC decays

some theories beyond SM (e.g. some SUSY models, 2HDM) predict

BR$\sim 10^{-5} - 10^{-6}$, at the limit of LHC sensitivity

Expected 99% CL confidence limits in units of 10^{-5}

Channel	LHC (600 fb^{-1})	SLHC (6000 fb^{-1})
$t \rightarrow q\gamma$	0.9	0.25
$t \rightarrow qg$	61	19
$t \rightarrow qZ$	1.1	0.1

These channels require b-tagging performance at SLHC similar to the one at LHC

Again: physics gains only achieved if detector performance is comparable!