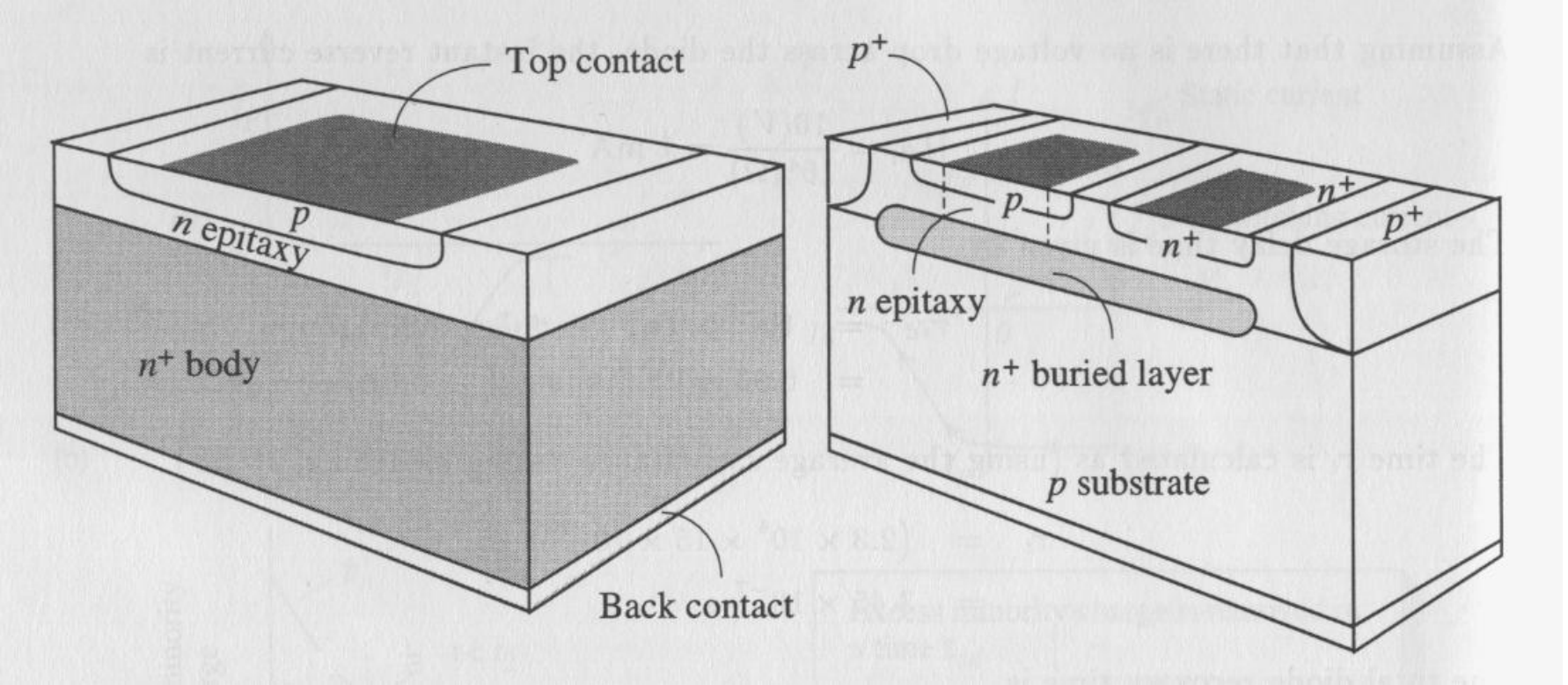
Lecture 7: Devices

- Crystal growth
  - Czochralski
  - High Pressure Bridgeman
  - Epitaxial
- Lithography
- Etching
- Doping

Model of a P-N diode

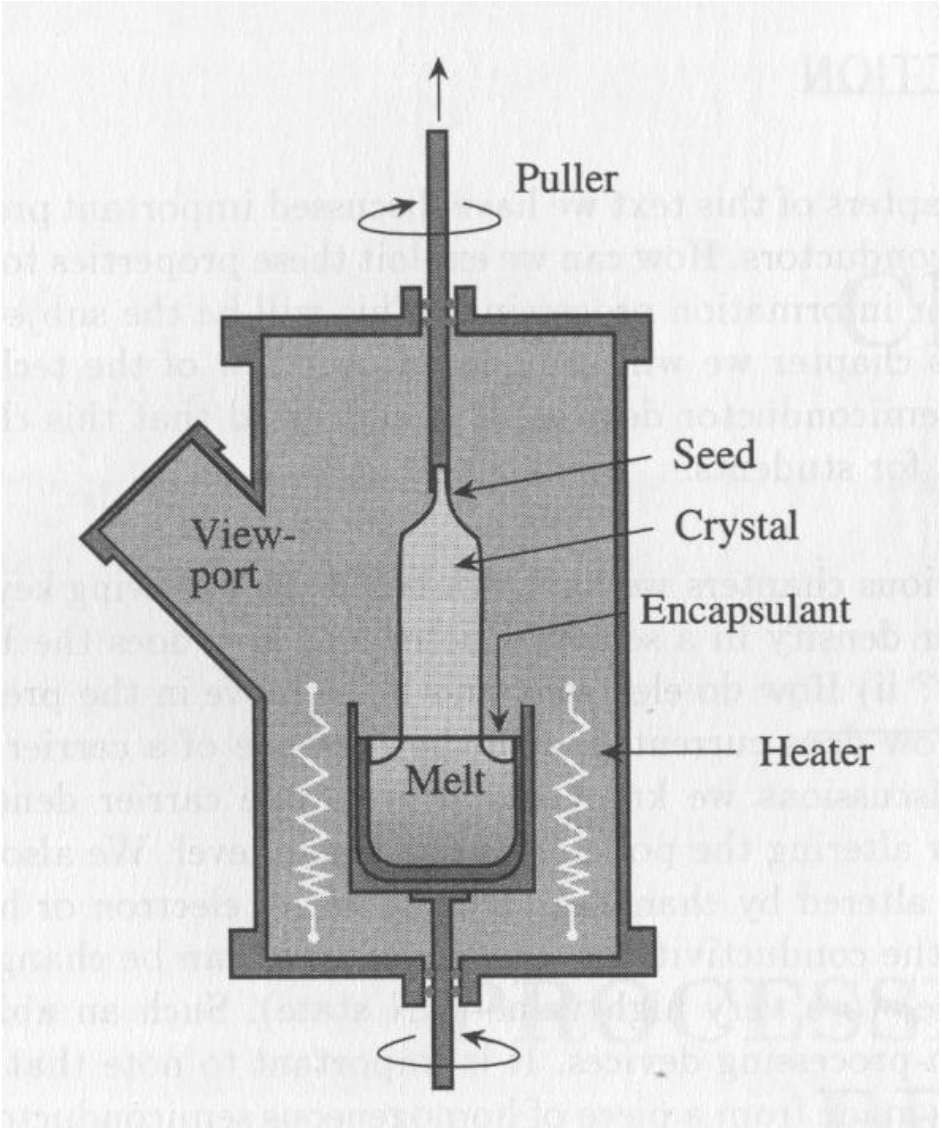


- Cross section of a discrete p-n diode and a p-n diode in IC technology.

Crystal growth

- Bulk crystal growth techniques are used to produce substrates on which devices are fabricated.
- For semiconductors such as Si, Ge and CdTe bulk crystal growth techniques are highly matured.
- The aim of the bulk crystal techniques is to produce single-crystals with as large a diameter as possible and very few defects.
- Some important bulk growth techniques:
  - Czochralski
  - High Pressure Bridgeman (HPB)
  - Travelling heater method (THM)

The Czochralski technique

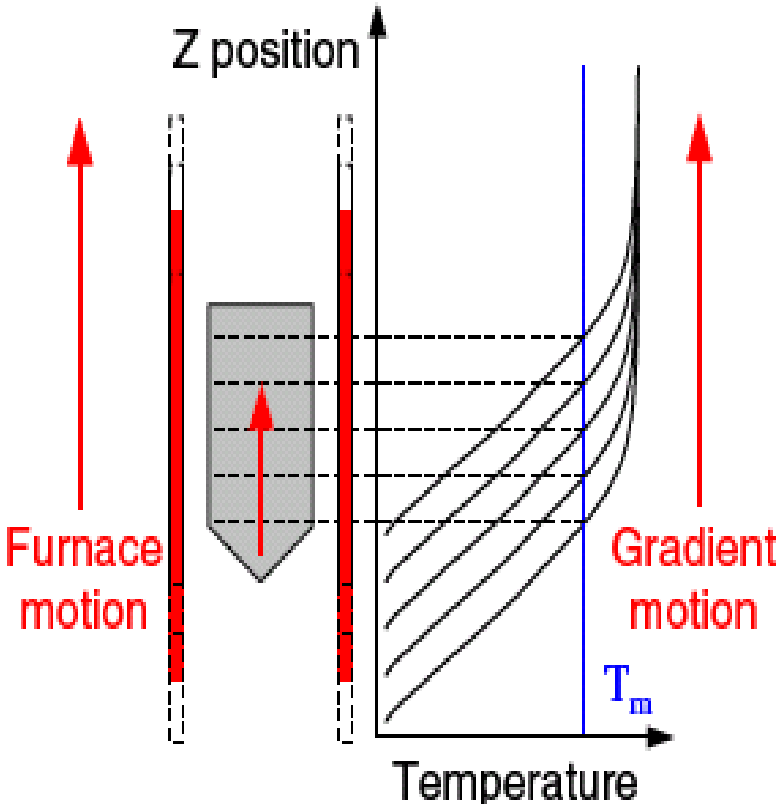


Silicon crystals have reached 30cm diameter and lengths approaching 100cm. Large size substrates ensure low-cost device production.

The Czochralski technique

- The crystal melt is held in a vertical crucible.
- The top surface of the melt is just above the melting temperature.
- A seed crystal is lowered into the melt and slowly redrawn.
- The heat from the melt flows up the seed, the melt surface cools and the crystal grows.
- The seed is rotated about its axis to produce a roughly circular cross-section crystal.
- The rotation inhibits the natural tendency of the crystal to grow along certain orientations to produce a faceted crystal.
- This technique can produce long ingots of semiconductor materials.

High Pressure Bridgman



- Compound semiconductor growth
- Crystals grow from a melt of nearly equal quantities of cadmium and tellurium, with small cadmium excess.
- The cadmium excess generates high vapour pressure that requires growth furnace of special design.
- The crystal grows at high temperature, above 11000 C, at a high growth rate of few millimeters per hour.

Epitaxial Crystal Growth

- The substrates that result once the bulk semiconductor ingot is sliced are seldom used directly for devices.
- An additional epitaxial layer is grown that may be a few microns in thickness.
- The word epitaxy is Greek meaning “epi” upon and “taxis” order or the ordered continuation of a crystal.
- Epitaxial growth techniques have an extremely slow growth rate.
- Using techniques like molecular beam epitaxy (MBE) and metal organic chemical vapour deposition (MOCVD) monolayer (0.3nm) control in the growth direction is achievable.

Molecular Beam Expitaxy

- Is one of the most important epitaxial growth techniques. Almost every semiconductor has been grown with this technique.
- A high vacuum technique (~10^{-11}torr).
- Elements contained in crucible which makes up the components of the crystal to be grown, as well as any dopants.
- Upon heating of the crucible atoms or molecules of the component are evaporated travelling in straight lines to impinge on a heated substrate.
- The growth rate is ~1.0 monolayer per second

MOCVD

- **Metal Organic Chemical Vapour Deposition** is capable of producing monolayer abrupt interfaces between semiconductors.
- Utilizes gases that are complex molecules that contain elements like Ga and As to form the crystal, unlike MBE where single element gases are used.
- Growth depends on chemical reactions occurring at the heated substrate surface.
- The grown of GaAs uses triethyl gallium and arsine and the crystal growth depends on the following reaction:

$$Ga(CH_3)_3 + AsH_3 \rightarrow GaAs + 3CH_4$$

Lithography

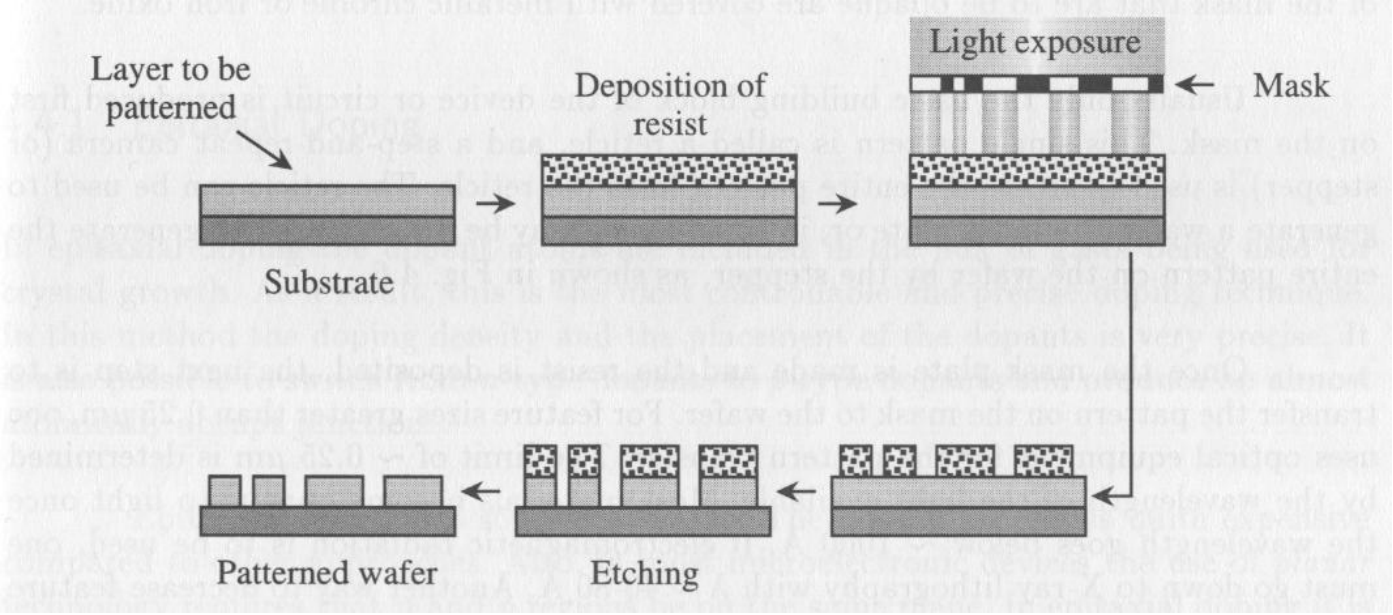
- The success of solid state electronics is due to device fabrication techniques that can produce extremely complex devices with high yield.
- Crystal growth processes do not produce any controlled lateral variations in the material properties. Lithographic techniques are required.
- The lithographic process takes a certain design created in a computer and transfers it to a wafer.
- New advances in lithographic techniques are introducing continual changes.
- Important concepts to remember are **Photoresist coating** and **Mask generation** and **Image transfer**.

Lithography: Photoresist coating

- In order to transfer an image to a wafer, the surface has to be made sensitive to light.
- A photoresist is spread on the wafer by a process called spin coating. It must:
  - Have good bonding to the substrate.
  - Have uniform thickness.
  - Should be reliably controlled over different wafer runs.
- Spin coating involves a puddle of resist being applied to the centre of a wafer.
- The wafer is then spun at 2000-8000rpm for 10 to 60 seconds. Finally soft baking at ~100C improves adhesion to the oxide.
- The thickness of the resist is usually 0.7 to 1.0μm.

Lithography: Photoresist coating

- The resist is exposed to an optical image through a mask for a certain exposure time.
- A resist becomes more soluble then exposed to illumination called positive, it's image is identical to the opaque image on the mask plate.
- Washing through a solvent develops the image by washing away the regions of higher solubility.



Mask generation and Image transfer

- Allows the transfer of a circuit pattern onto the sensitive resist.
- A CAD program allows a mask plate to be generated optically or by electron beam writing (allows the production of finer features).
- The mask plate is used to repeatedly transfer patterns to different wafers, it must therefore have good mechanical and thermal properties.
- Usually only the basic building block of the circuit is produced first. This single pattern called a **reticle** is used to create an entire pattern on a wafer-size plate by use of a stepper.
- Now transfer the pattern from the mask to the wafer.

Mask generation and Image transfer

- For feature sizes greater than 0.25μm, optical equipment is used for pattern transfer.
- The limit of 0.25μm is determined by the wavelength of the light available.
- Most materials become opaque to light once the wavelength goes below ~100nm.
- The use of X-ray lithography available as well as electron beam lithography.
- Once the image is transferred the resist is developed and **etching** is carried out.
  - Specially designed etchants allow material to be removed from a wafer with resist patterning in a selective manner.
  - The etchants must be able to remove a layer of material from the region where there is no resist and not attack the resist.
  - It should attack on layer SiO_2 not Si.

Etching: Wet chemical etching

- Wet chemical etching is the simplest and most common etching technique.
  - The wafer is soaked in a liquid chemical that dissolves the semiconductor.
  - Following chemical reaction with the semiconductor the reaction products are rinsed away.
- Etchants are usually either acids or alkaline solutions that are diluted in water.
- In many devices an import film to be etched is SiO_2. It is etched with hydrofluoric acid solutions and the ease and control of the process is an important reason for the success of silicon technology.
- Hydrofluoric acid is usually buffered with NH_4F to produced buffered oxide etch (BOE).

Etching: Plasma etching

- Plasma is produced by passing an rf electrical discharge through through a gas at low pressure.
- The rf discharge creates ions and electrons, the ions are then used to interact with elements in the substrate and cause etching.
- Control of the electric field used to accelerate the ions allows the ions energy to be appropriately selected.
- At low energy the ions can cause chemical reactions at the surface and cause the removal of atoms selectively.

Doping of semiconductors

- Once a dopant is selected we need to:
  - Get the dopant onto the crystal.
  - Activate the dopant – getting the dopant to a proper crystal site and removing any damage resulting from the doping process.
- **Epitaxial** doping required dopant atoms to be included in the flux of gas being used for crystal growth.
- Advantages:
  - The doping density and placement of dopants is extremely precise. It is possible to switch from n-type to p-type dopants and produce an almost atomically abrupt junction.
- Disadvantages:
  - Expitaxial doping is expensive compared to other approaches.
  - Planar electronic devices require n and p regions in the same plane.

Doping by Diffusion

- A wafer is place in a furnace in which inert gases carry the dopant which is deposited on the wafer – this process is known as **predeposition**.
- The wafer is then heated for a period of time to allow the deposited dopants to diffuse into the wafer – refered to as **drive-in**.
- The dopants move from the surface (an area of high concentration) to the bulk (an area of low concentration). This results in a less abrupt doping profile than that possible with epitaxial doping.

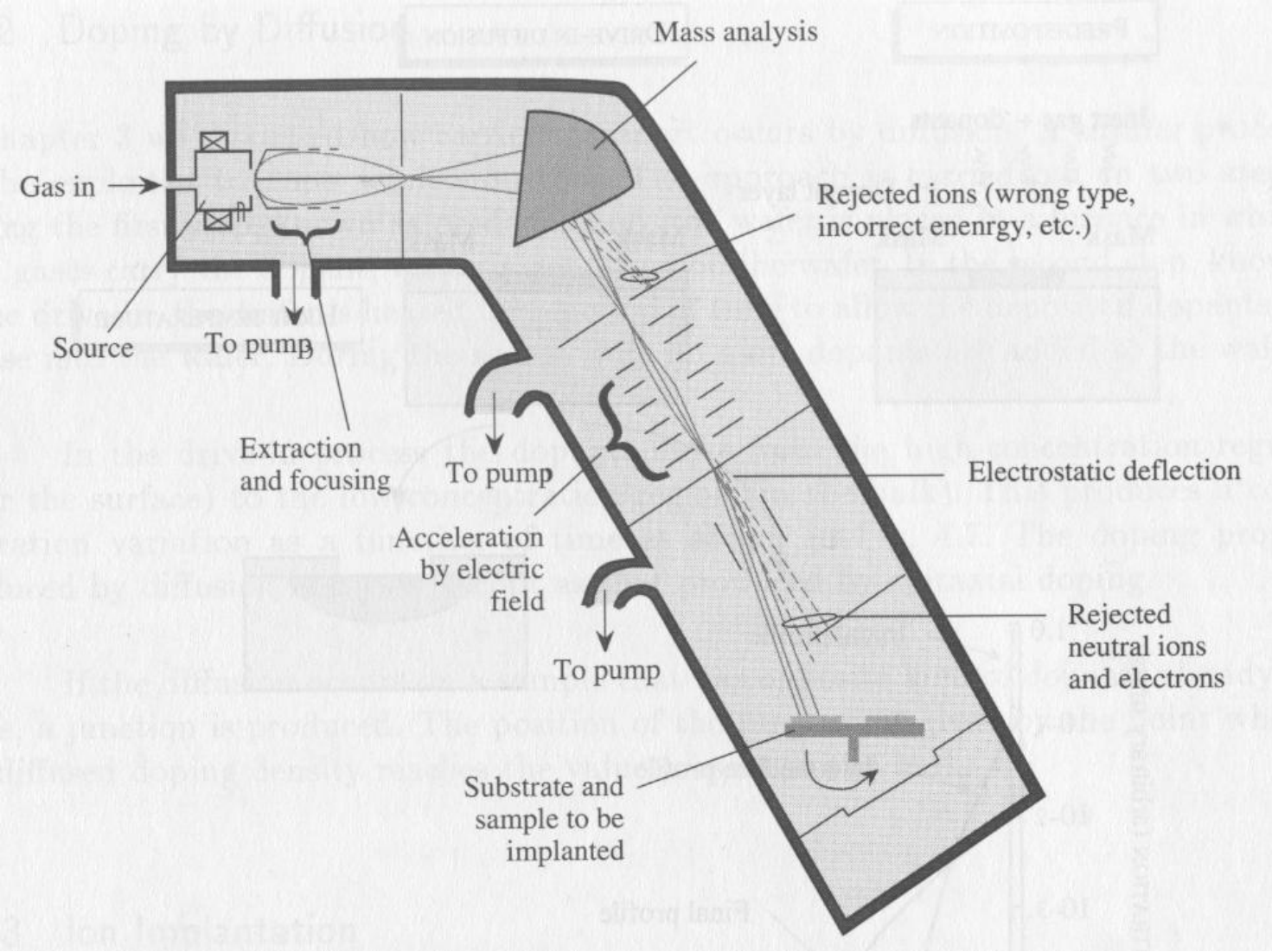
Doping: Ion Implantation

- Is the most important doping techniques used in the microelectronics industry.
- Dopant ions (accelerated to a pre-chosen energy) impinge on a wafer.
- The ion beam penetrates the semiconductor, during this process the ions suffer a series of collisions with the atoms and electrons in the solid.
- The collision process is statistical in nature and on average an ions loses its energy at a depth (range) R_p from surface.
- The ion distribution is typically Gaussian in nature, the FWHM of this defines the spatial spread of dopants.
- By controlling the energy of the ions the position of the dopants in the semiconductor can be controlled.

Doping: Ion Implantation

- The collisions the ions undergo with the host semiconductor causes a lot of damage in the implanted wafer.
- Vacancies, interstitial atoms or even locally non-crystalline regions are produced.
- The damage is removed by **annealing** the semiconductor – that is keeping the semiconductor at an elevated temperature for 20 to 30 minutes.

Doping: Ion Implantation



Summary

- The final devices and chips are the most complex systems that humans can build.
- In high density memory chips, tens of thousands of transistors are packed into a thumbnail size Si chip.
- In microprocessors, thousands of logic elements (electronic buses, registers and memory devices) are coupled by an intricate maze of interconnects.
- The features on these chips are extremely tiny, the smallest feature size on modern chips is ~0.1μm.
- The depth profile has features as thin as 2nm, just a few monolayers.

Summary of lecture 7

- Crystal growth
  - Czochralski
  - High Pressure Bridgeman
  - Epitaxial
- Lithography
- Etching
- Doping