

What temperature scenario for the SLHC?

G. Casse

Temperature scenario for Si detectors:

To face the problems induced by the increase of the current due to the high irradiation doses, it will be necessary to provide very efficient cooling to the detector systems (sensors and electronics). Providing power and extracting heat is one of the major (if not “the major”) challenges for the upgrade. It is conceivable a need for T 30°C or more cooler than the present LHC. Nonetheless, in non operation time, it might be well advantageous to let the systems rest at room T (RT = 20°C).

Temperature management:

Beam on: irradiated detectors biased at 500V and cooled to (possibly) -25°C to control the reverse current, avoid runaway and reduce the shot noise.

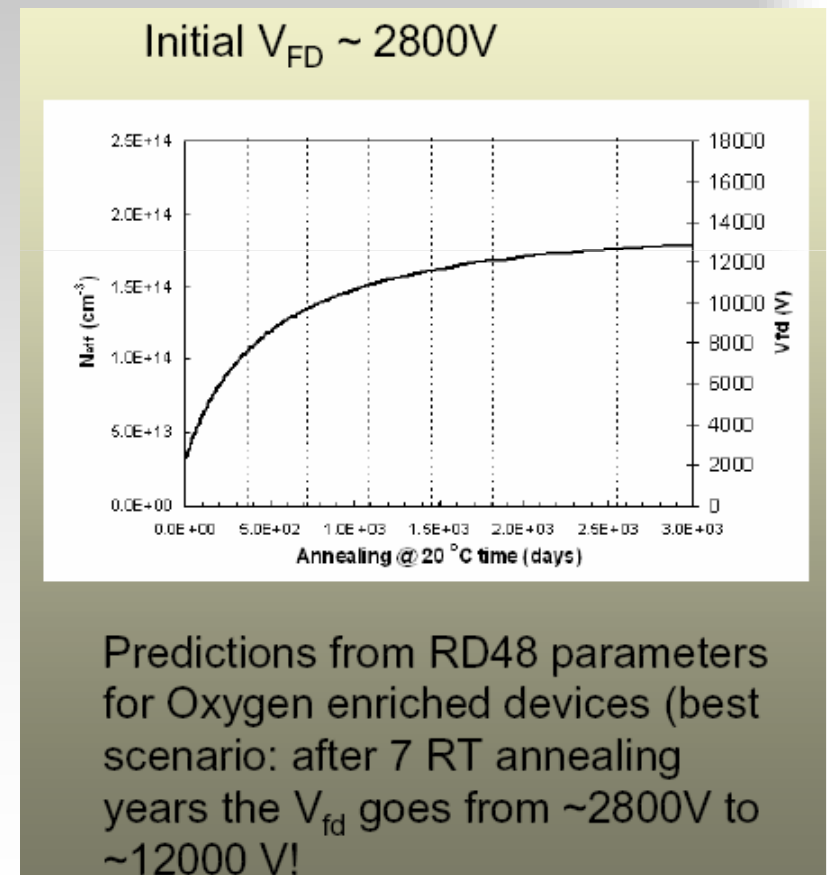
Beam off, “old” assumption:

Avoid warming up the irradiated detectors above 0°C , even during beam down and reduce maintenance at room temperature to minimum.

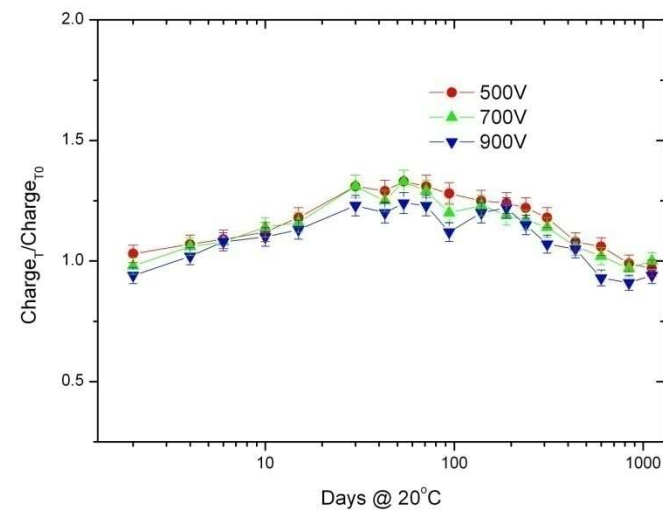
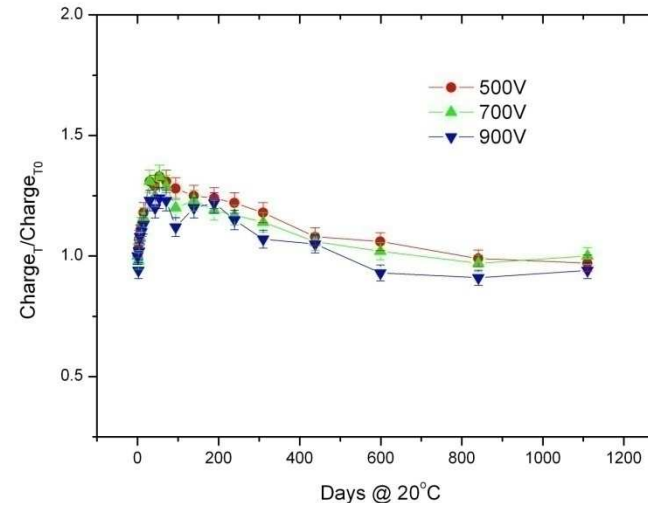
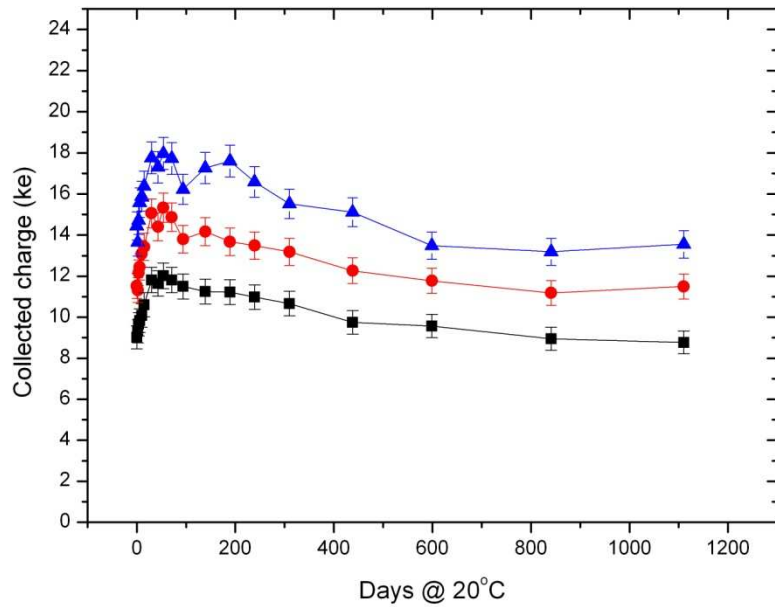
V_{FD} undergoes reverse annealing and

becomes progressively higher if the detectors are kept above 0°C .

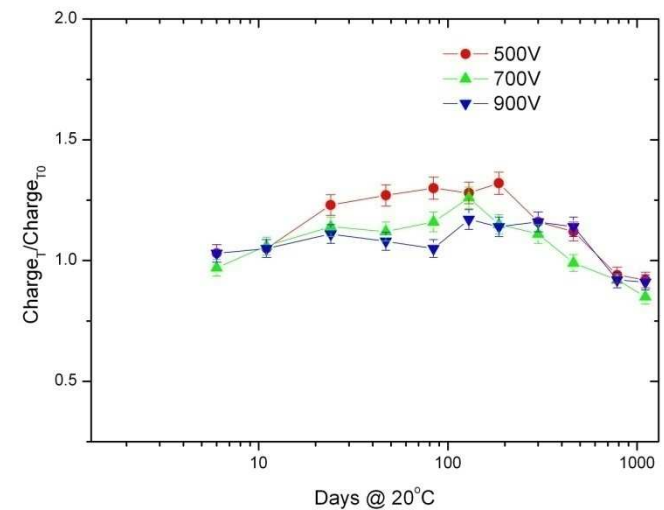
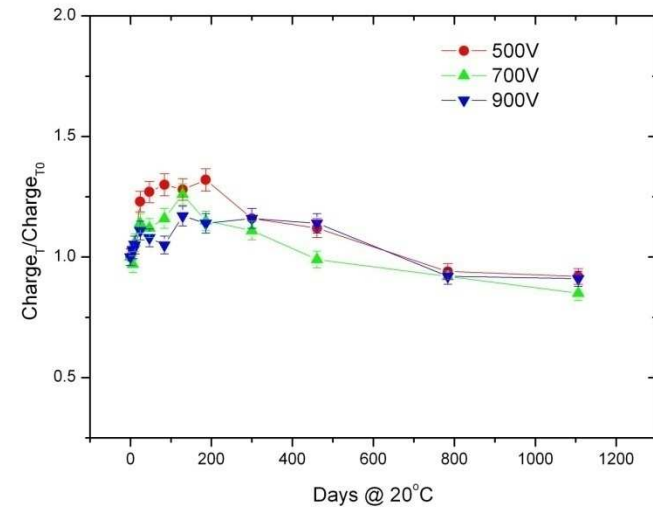
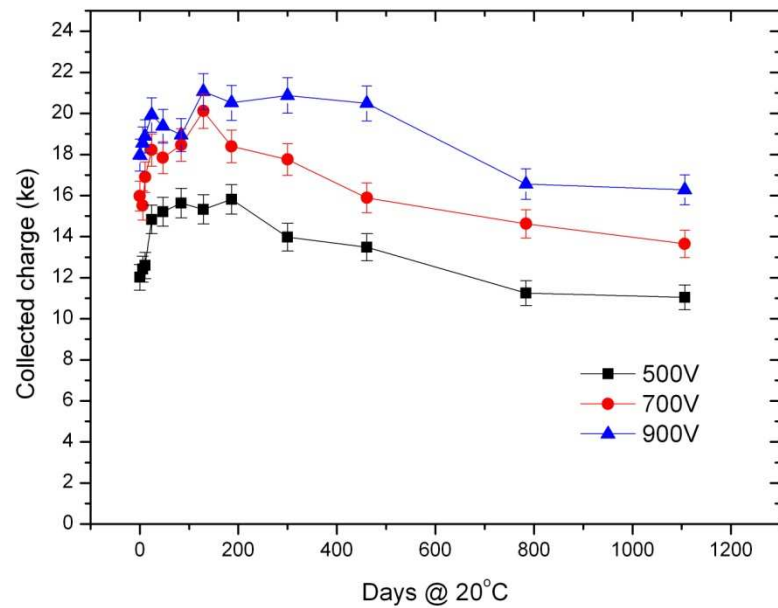
But what happens to the reverse current and the CCE of n-side readout detectors?



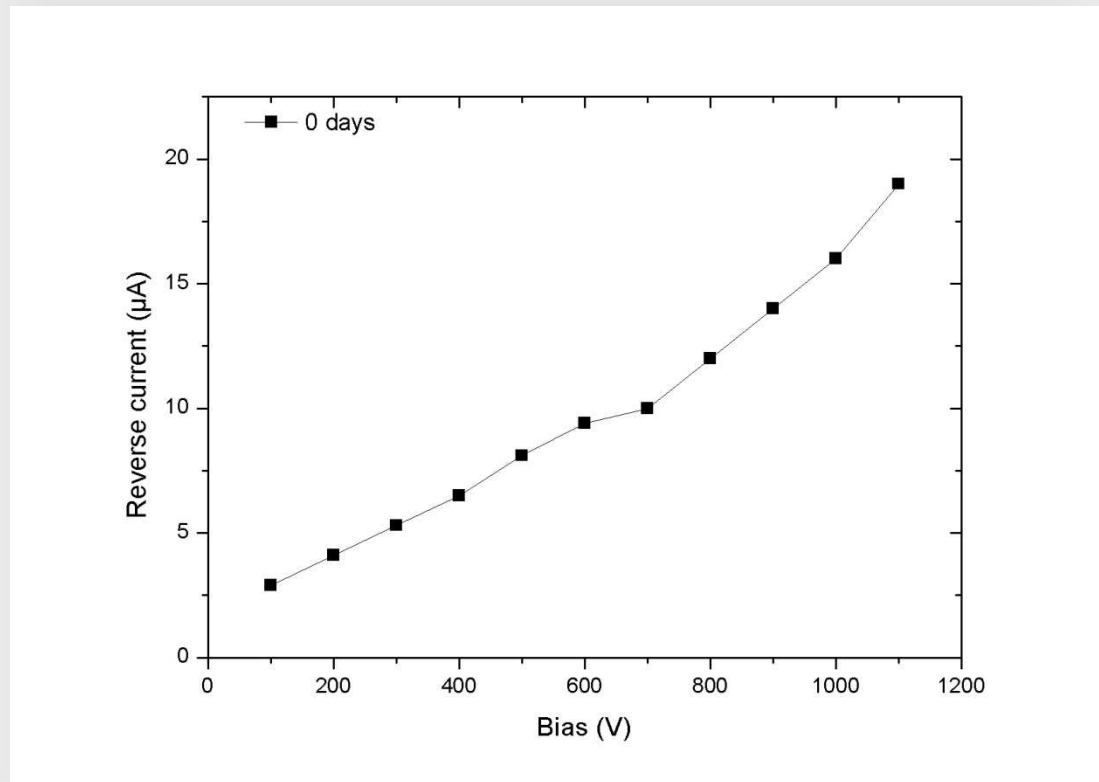
“Fine step” Annealing of the collected charge, HPK FZ n-in-p, $1E15 \text{ n cm}^{-2}$



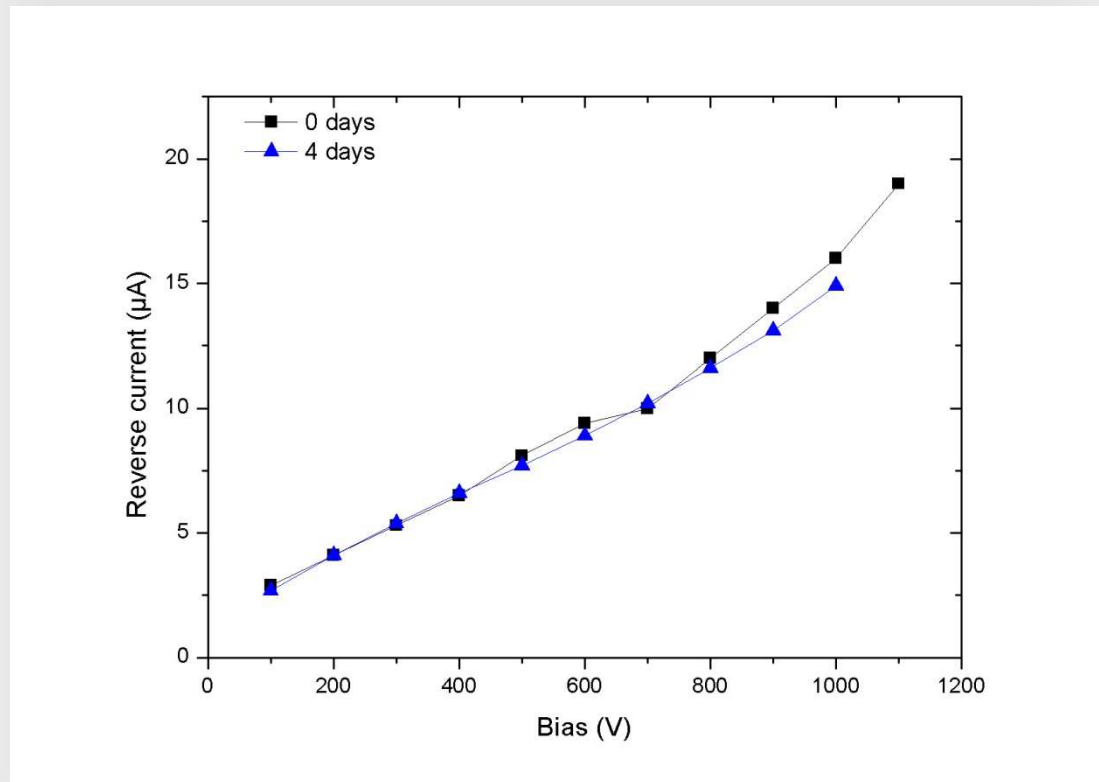
“Fine step” Annealing of the collected charge, Micron FZ n-in-p, $1E15 \text{ n cm}^{-2}$ (26MeV p irradiation)



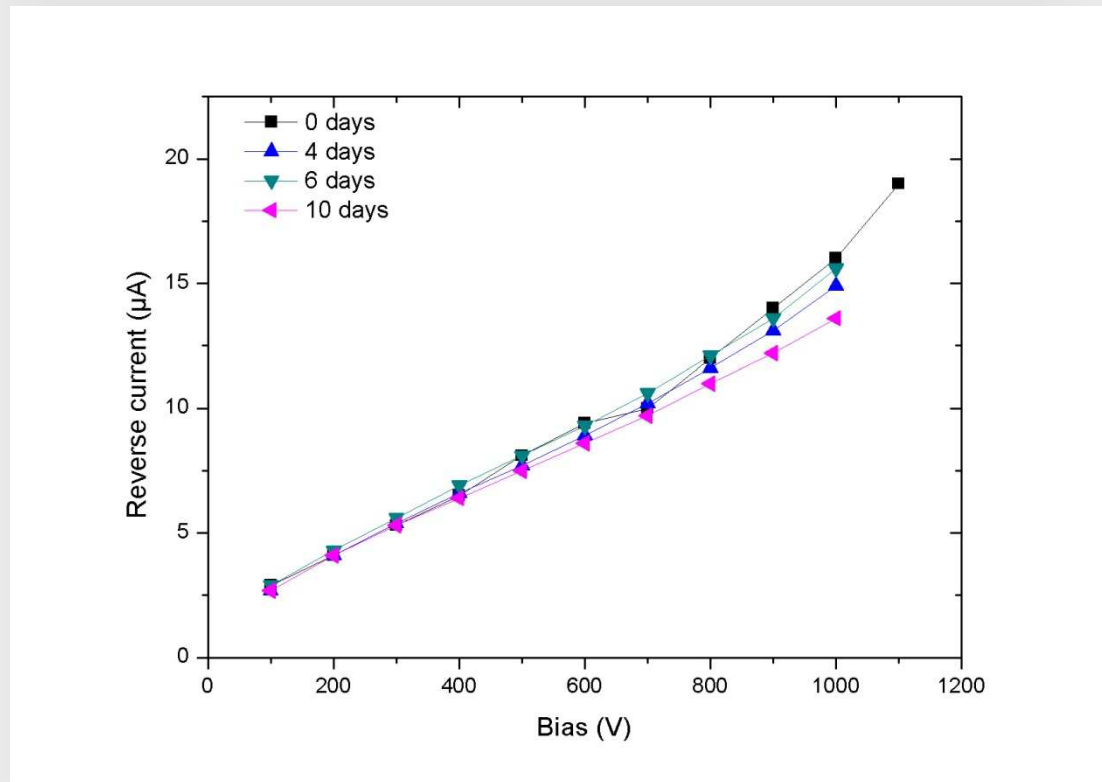
“Fine step” Annealing of the reverse current, HPK FZ n-in-p, $1E15 \text{ n cm}^{-2}$



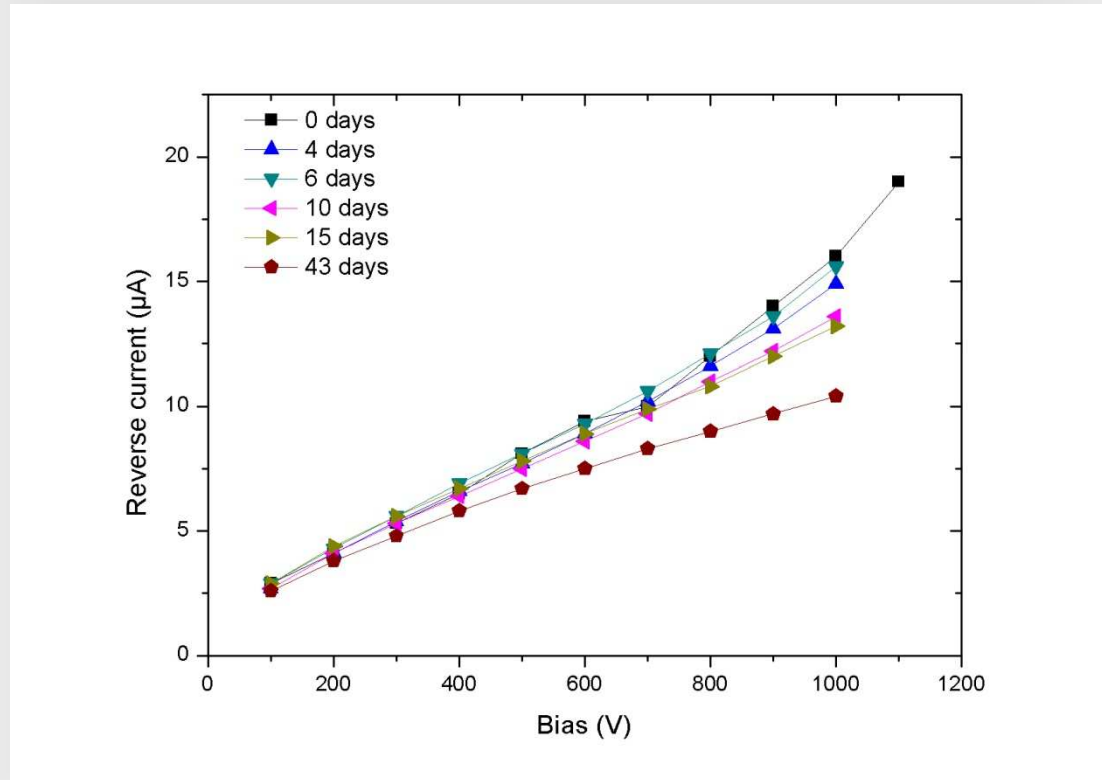
“Fine step” Annealing of the reverse current, HPK FZ n-in-p, $1E15 \text{ n cm}^{-2}$



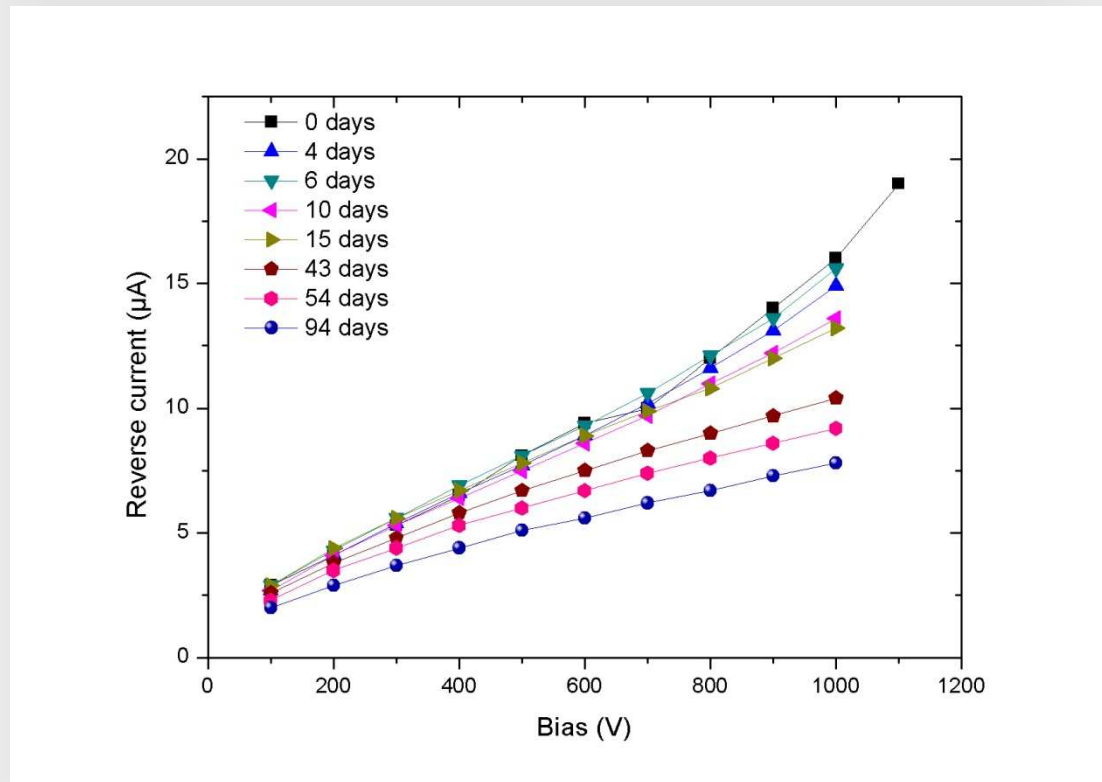
“Fine step” Annealing of the reverse current, HPK FZ n-in-p, $1E15 \text{ n cm}^{-2}$



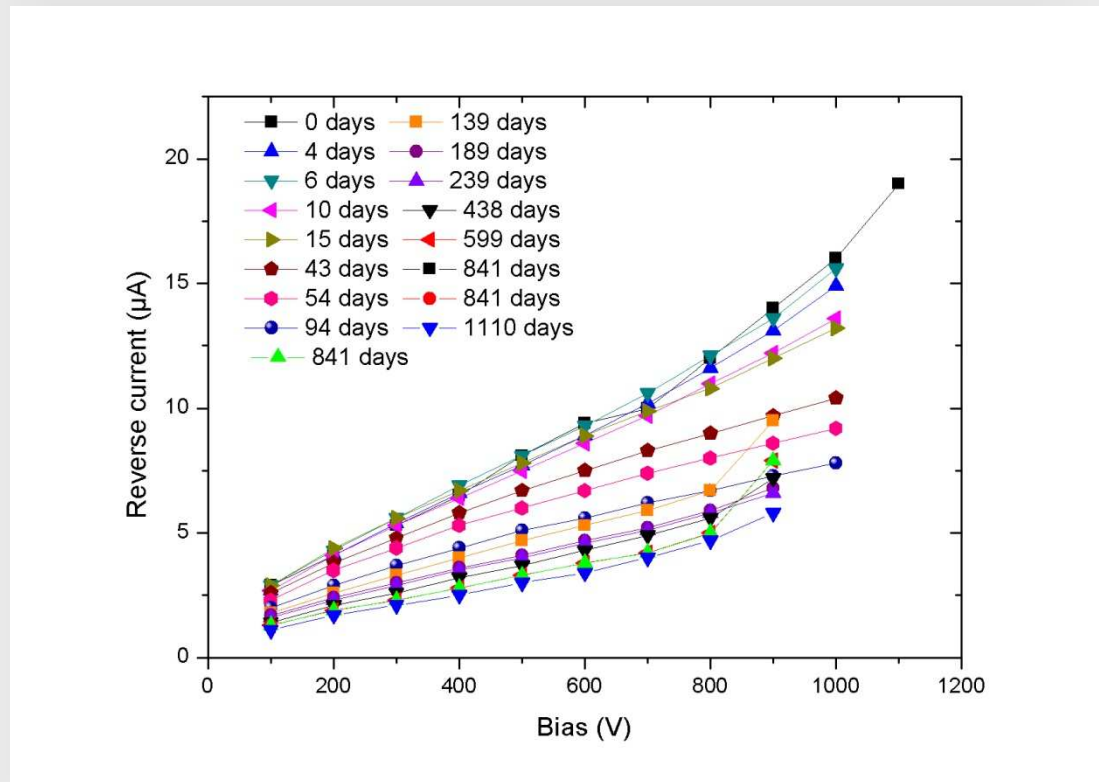
“Fine step” Annealing of the reverse current, HPK FZ n-in-p, $1E15 \text{ n cm}^{-2}$



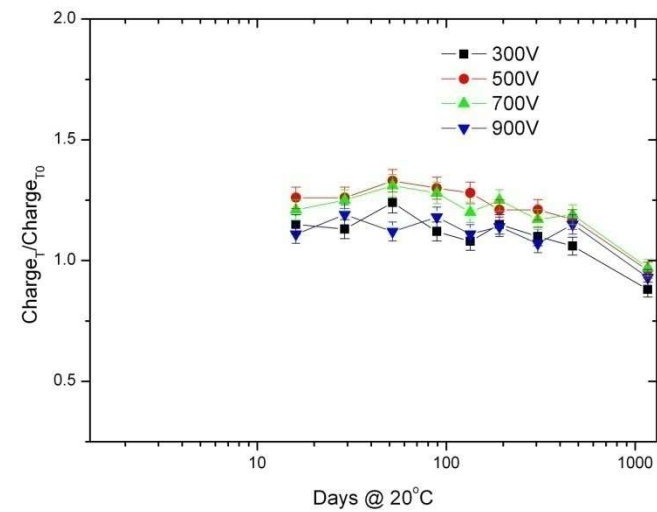
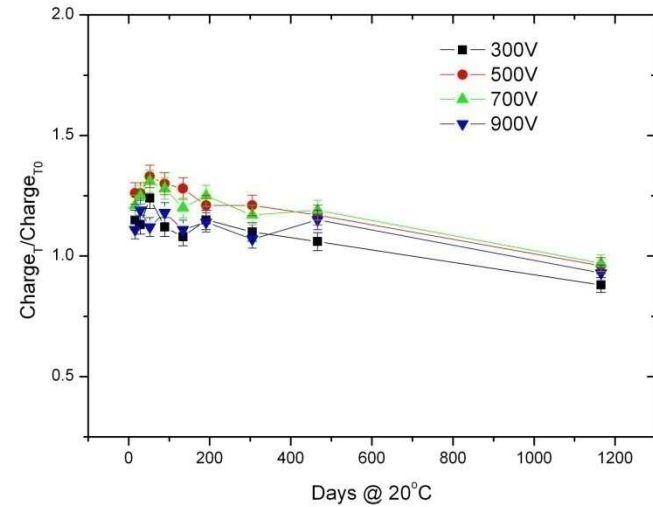
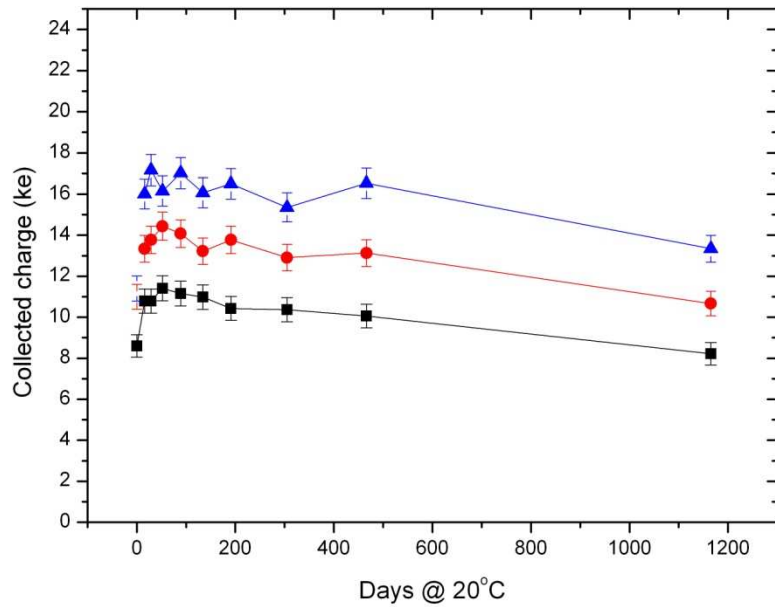
“Fine step” Annealing of the reverse current, HPK FZ n-in-p, $1E15 \text{ n cm}^{-2}$



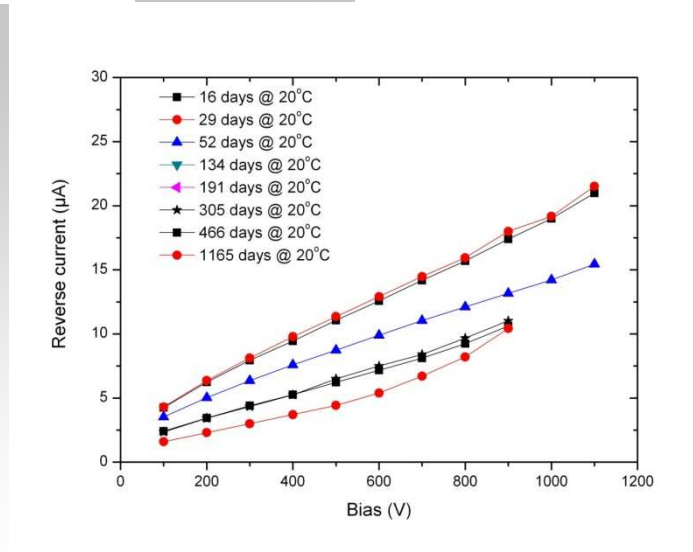
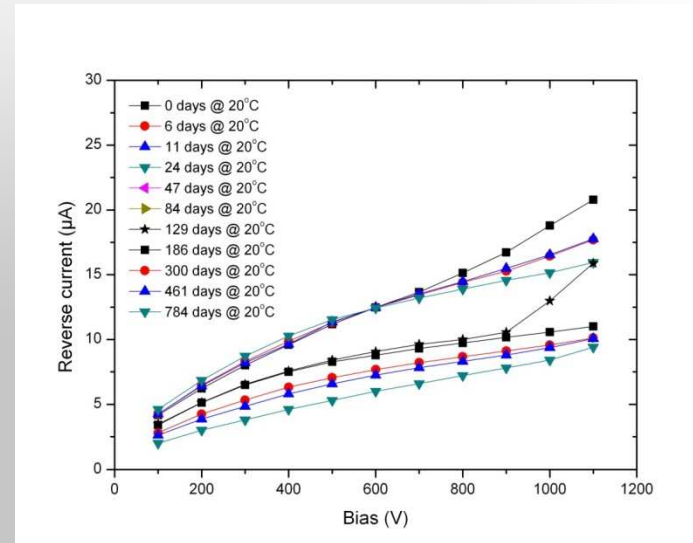
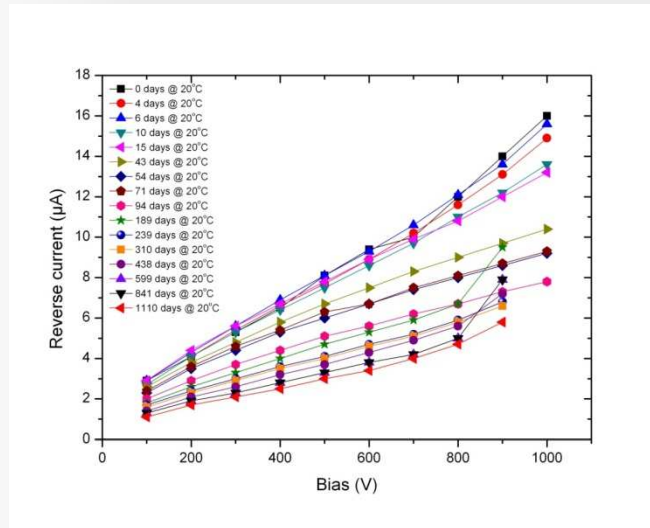
“Fine step” Annealing of the reverse current, HPK FZ n-in-p, $1E15 \text{ n cm}^{-2}$



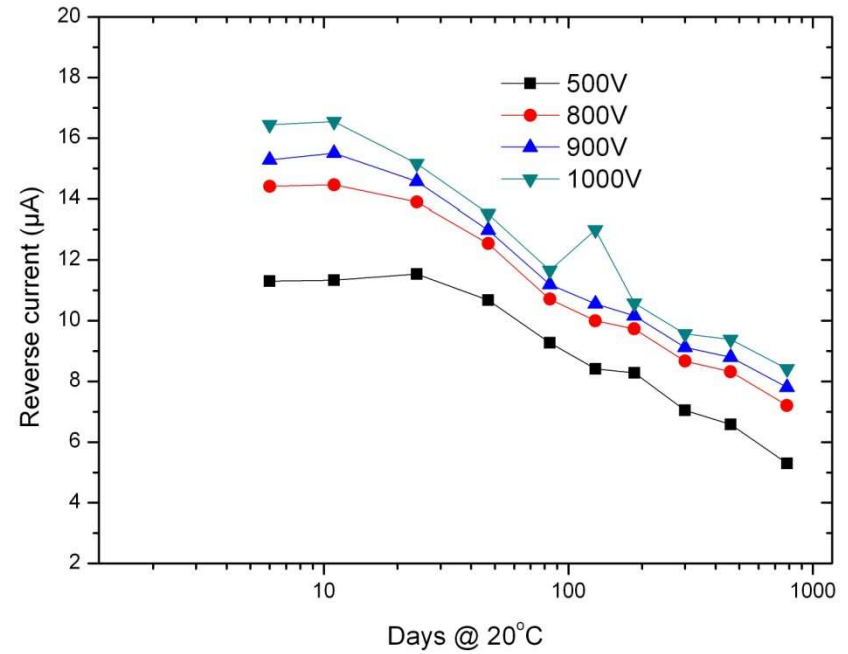
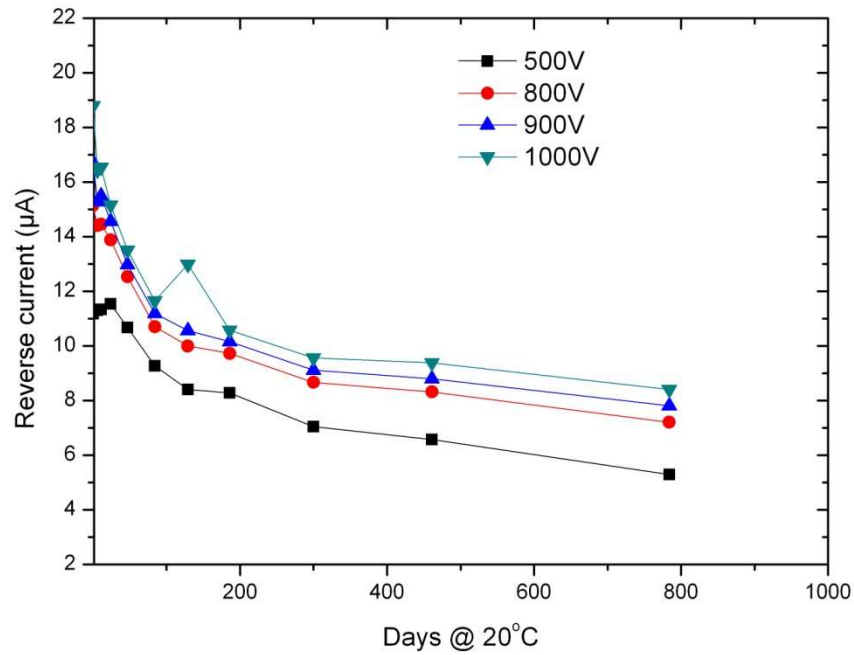
“Fine step” Annealing of the collected charge, Micron FZ n-in-n, $1.5E15 \text{ n cm}^{-2}$



“Fine step” Annealing of the reverse current, Micron FZ n-in-p, $1E15 \text{ n cm}^{-2}$ (26MeV p irradiation), Micron FZ n-in-n, $1.5E15 \text{ n cm}^{-2}$

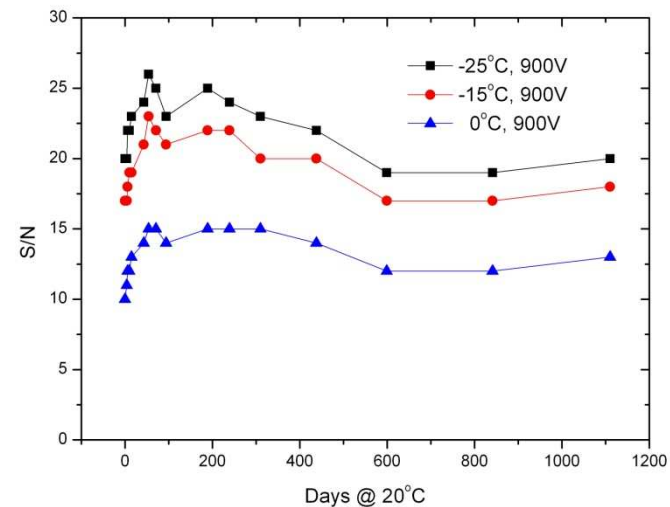
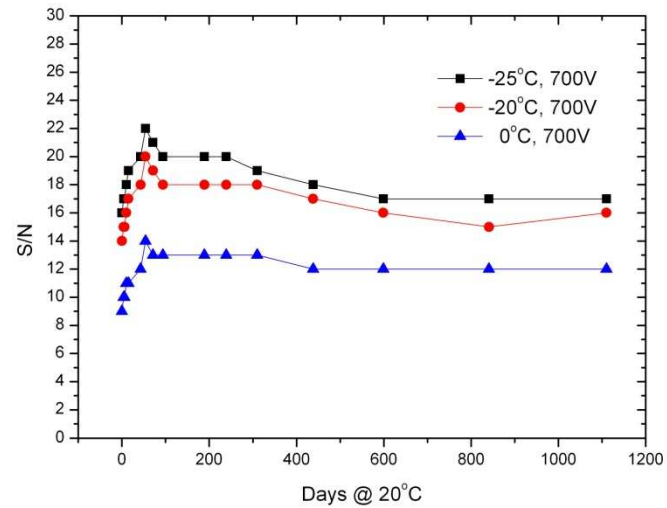
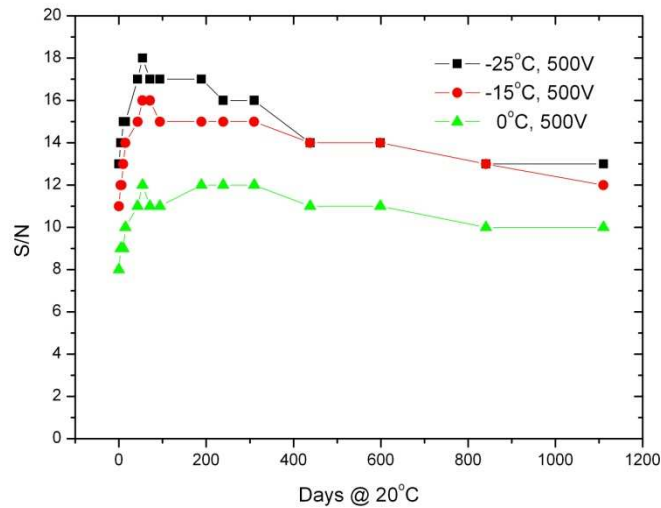


“Fine step” Annealing of the reverse current, Micron FZ n-in-p, $1E15 \text{ n cm}^{-2}$ (26MeV p irradiation)



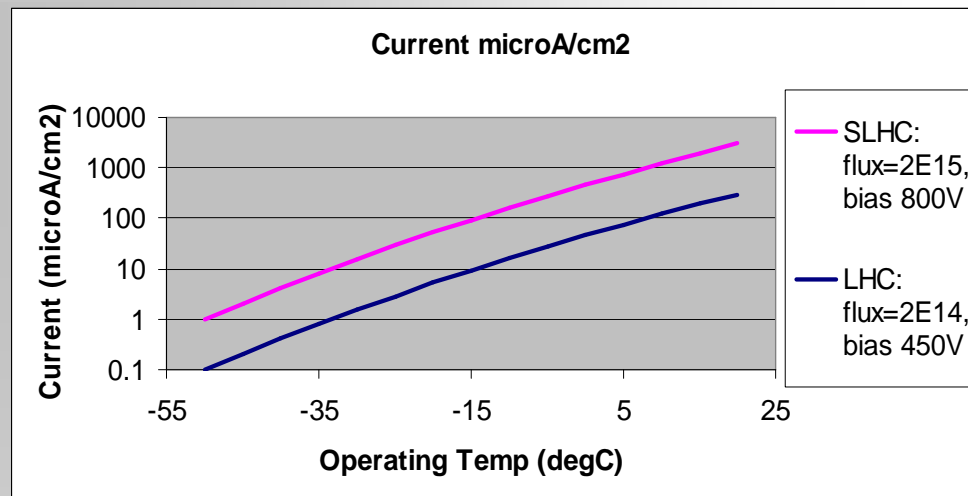
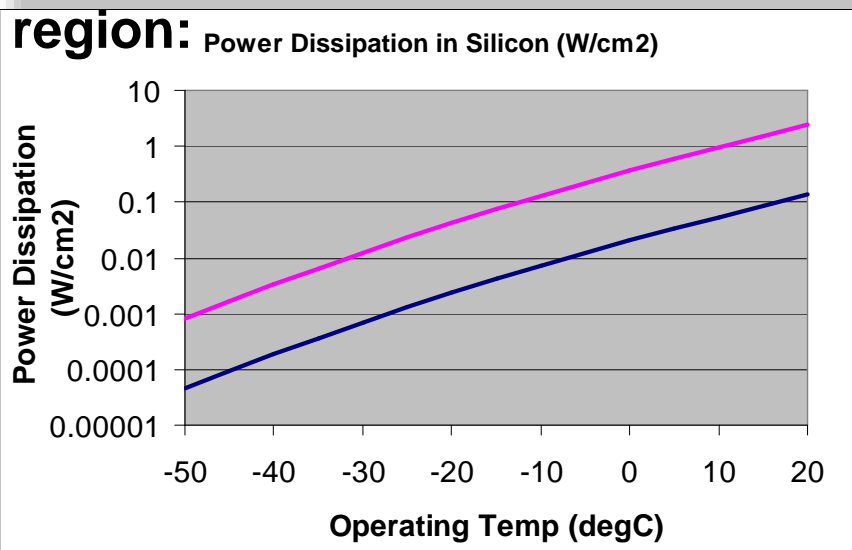
“Fine step” Annealing of S/N, $1.5E15 \text{ n cm}^{-2}$

Noise is the sum in quadrature of shot noise and parallel noise (taken from the Beetle chip specs, and estimated as 650ENC)



Current & power dissipation

Example innermost short strip region:



— LHC: flux = 2×10^{14} n_{eq}/cm², bias = 450V
 — SLHC: flux = 2×10^{15} n_{eq}/cm², bias = 800V

Current up by factor 10.
 Power up by nearly factor 20.

Temperature	-40°C	-30°C	-20°C	-10°C	0°C	10°C	20°C
LHC (mW/cm ²)	0.19	0.70	2.4	7.2	21	54	135
SLHC (mW/cm ²)	3.4	12.5	42	129	366	967	2400

LHC ⇒ SLHC: to keep similar power dissipation must run ~25°C colder.

(Note: at SLHC (n-side readout) we will not run at full depletion, i.e. reverse annealing is not a major issue, no need to keep sensors cold outside operation.)

Thermal runaway: Toy Model

Full analysis of thermal runaway requires detailed knowledge of precise cooling connection. Use toy-model instead.

Input:

- 300 μm Silicon sensor
- cooled at either end (no substrate or cooling spine)
- Assume heat exchange in 1 dimension only
- 2 Cases: 4.5cm & 9cm wide
- Assume perfect connection to cooling
- Thermal conductivity Silicon: 130 W/mK

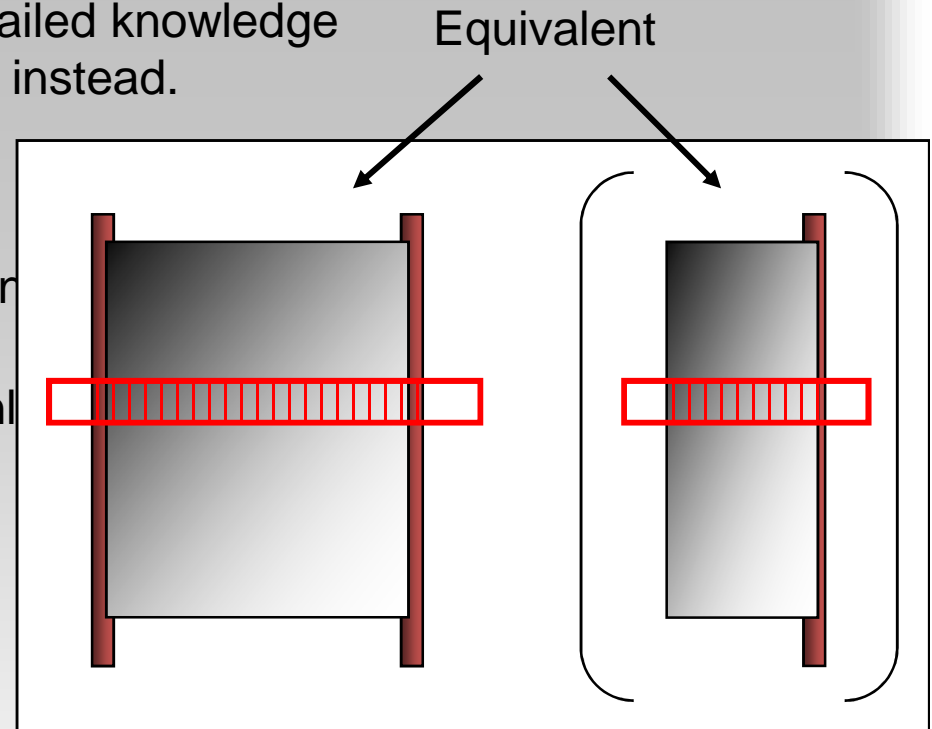
To determine the thermal runaway points:

Model:

- Take “strip” across the sensor and divide into small cells.
- Calculate power dissipation and heat exchange every 1 ms in each cell.
- Continue until it stabilises or diverges.

Alternative model (cross-check):

- Use equilibrium condition: dissipated power + heat conduction = 0



Thermal runaway results

Temperature gradient across sensor for different coolant temperatures. (NOTE: heat from ASICs or environment not included!)

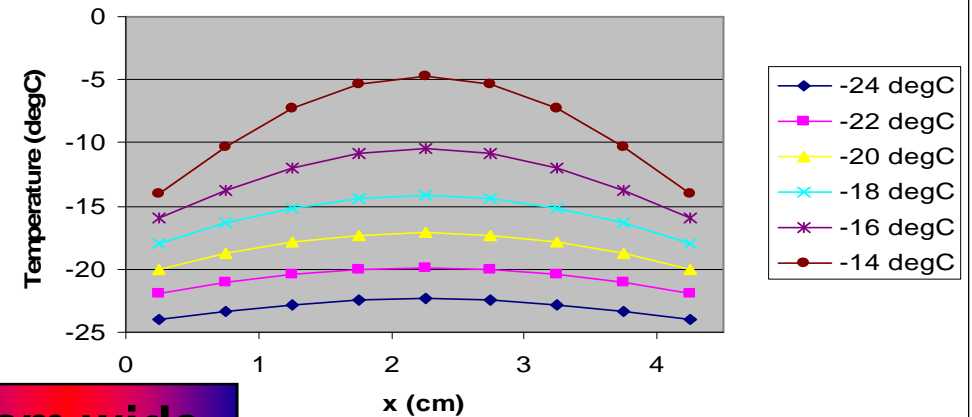
Thermal run-away points:

(curves shown up to temperature where model stops converging)

**4.5cm wide sensor: ~ -13°C
(+19 °C for LHC)**

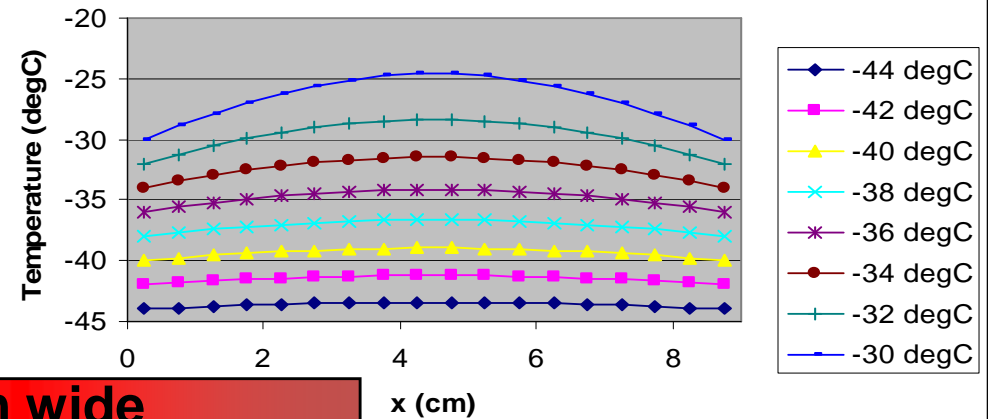
**9cm wide sensor: ~ -29°C
(+1 °C for LHC)**

Temperature gradient across sensor versus T coolant
(Flux 2E15, bias 800, width 4.5cm)



4.5cm wide

Temperature gradient across sensor versus T coolant
(Flux 2E15, bias 800, width 9cm)



9cm wide

Thermal runaway temperatures down by ~30°C (LHC⇒SLHC).

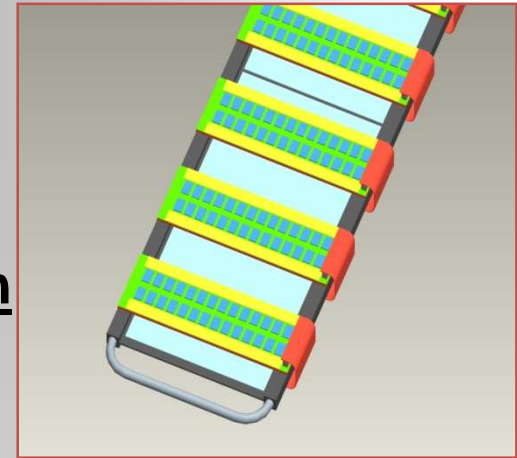
- need a spine or substrate underneath sensor for heat extraction
- need to run Silicon significantly colder than at LHC

Thermal simulation

Work done using ANSYS package (finite element thermal simulation)

Added to this package: simulation heat dissipation in Silicon (including the temperature dependence).

Work based on ladder design with single sensor layer.



In ANSYS:

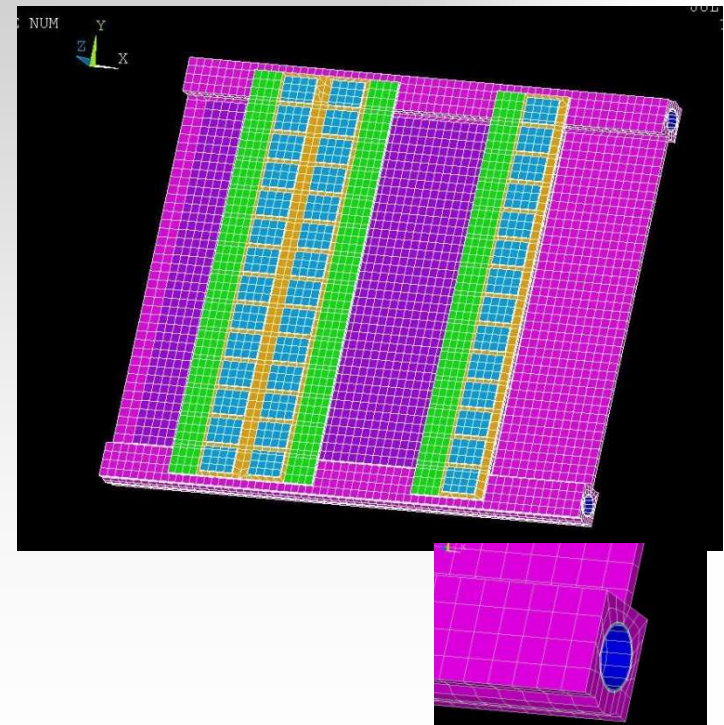
- carbon-carbon ladder
- diameter cooling pipe 5mm
- CC substrate under sensor 1mm (too thick!)

Sensor:

- 8 cm wide, 300 μ m, 3 cm length strips
- power based on: $\Phi = 2.2 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$, $V_b = 800 \text{ V}$

Hybrid:

- CC base with thin kapton layer
- 14 chips per sensors (0.5 W)
- distance to hybrid 2.7 mm (air)



Thermal runaway model: Results

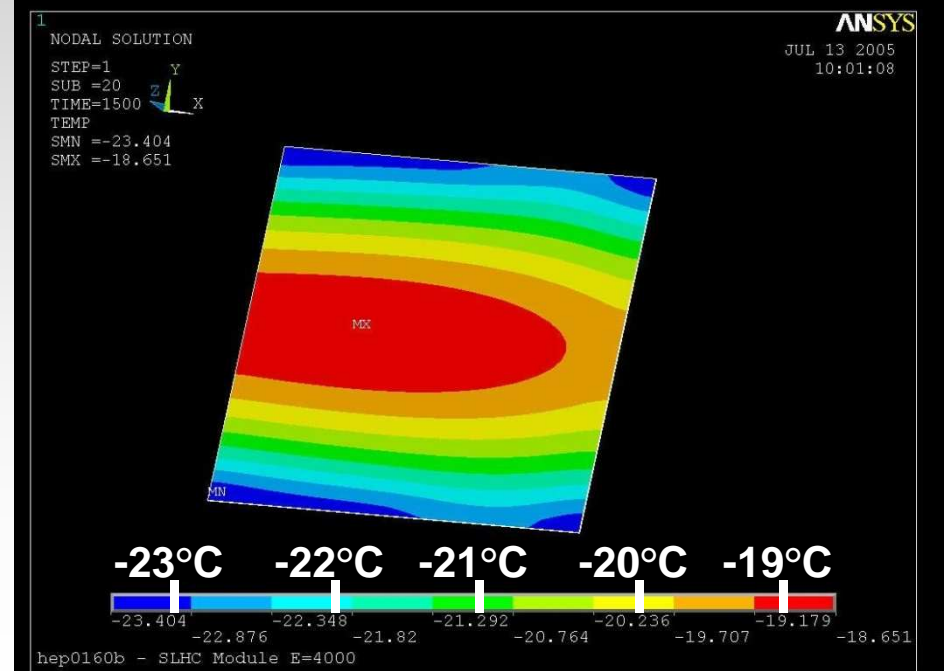
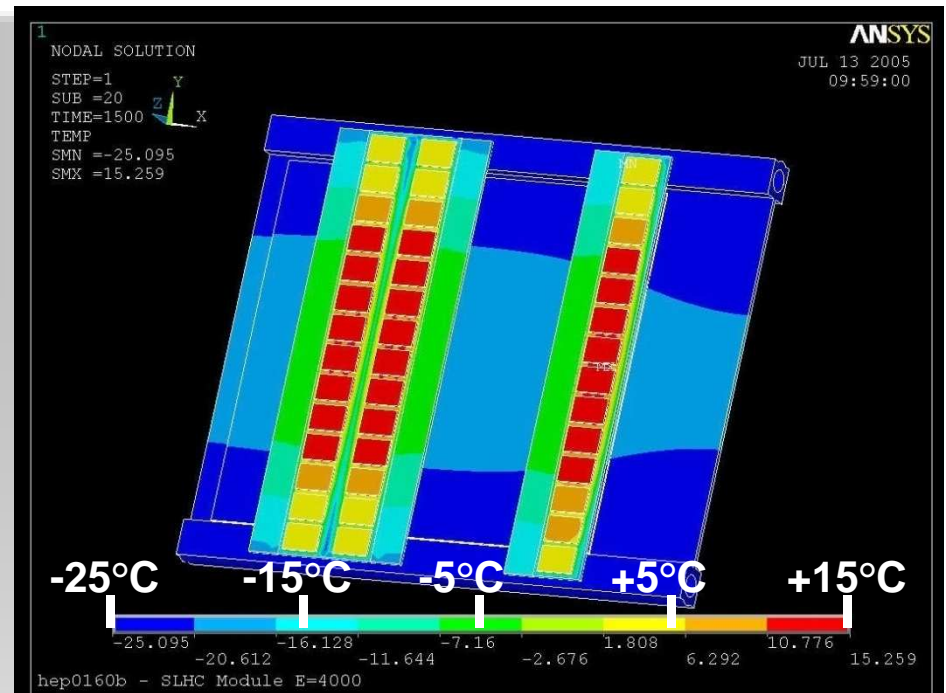
Coolant temperature: $-25\text{ }^{\circ}\text{C}$

**Sensor: hottest point $\sim -19\text{ }^{\circ}\text{C}$
Hybrid: hottest chip $\sim +14\text{ }^{\circ}\text{C}$**

**No sign of thermal runaway with $-25\text{ }^{\circ}\text{C}$
coolant temperature.**

Some caveats:

- substrate is unreasonably thick
- simulation still incomplete, e.g. heat input from electronics and environment in to silicon needs more detailed treatment.



SUMMARY

Controlled annealing (at 20⁰C) is a very useful tool to reduce power dissipation and recover fraction of S/N in heavily irradiated silicon detectors. Optimum annealing time is between 100-300 days for CCE (while no restriction is found with reverse current recovery). Nonetheless, during operation, cooling to temperature lower than -20⁰C is required for preventing thermal runaway and excessive shot noise. The operation T will depend on the radius, as well as the more stringent limiting factor (runaway or shot noise).