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Liverpool HV-CMOS test PCB (V2) for Particulars TCT

PCB design by Samuel Powell

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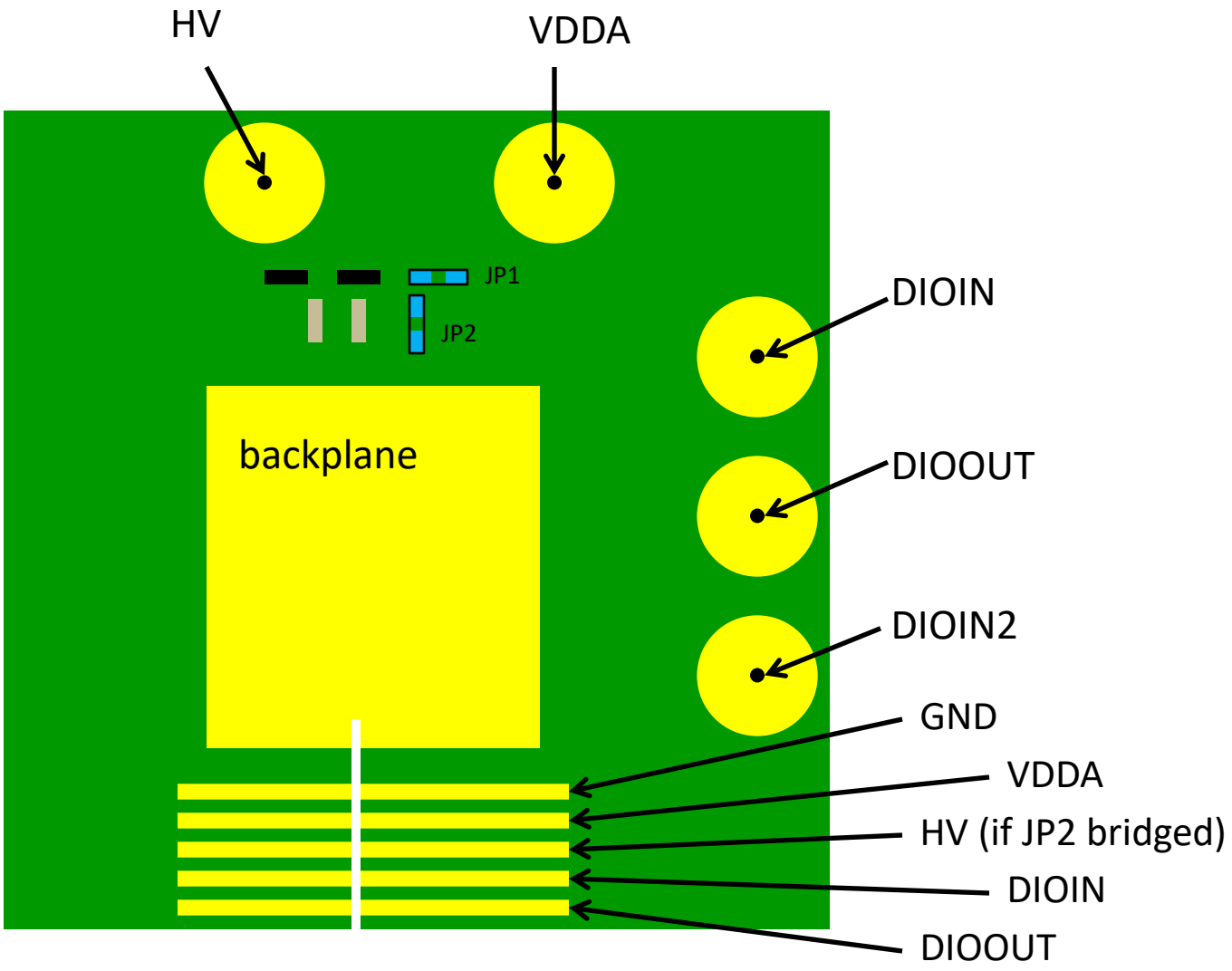
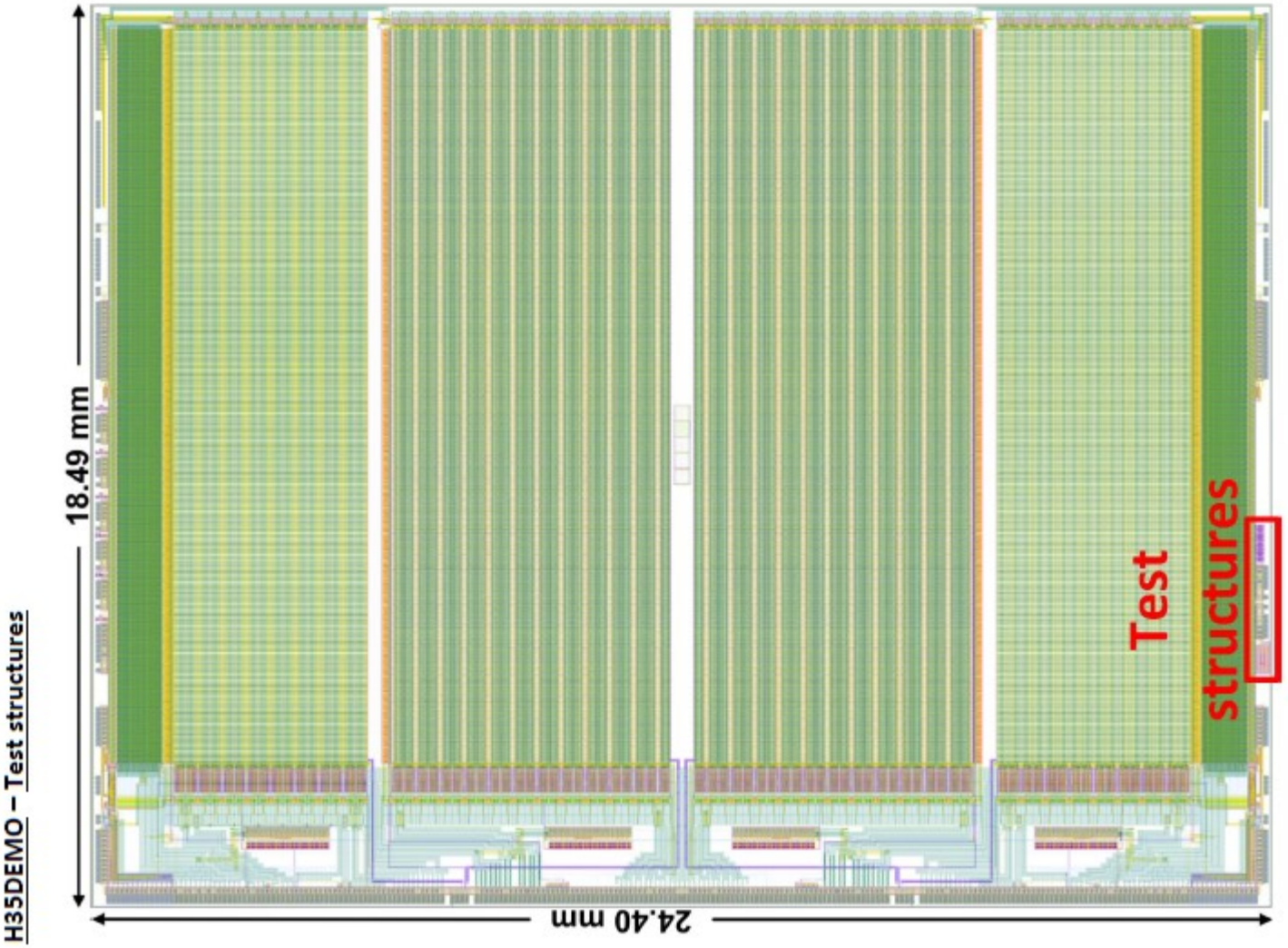
PCB pinout



JP1: bridged to connect HV SMA to backplane
JP2: bridged to connect HV SMA to trace at bottom

GND: all SMA shields connected

HV-CMOS H35DEMO



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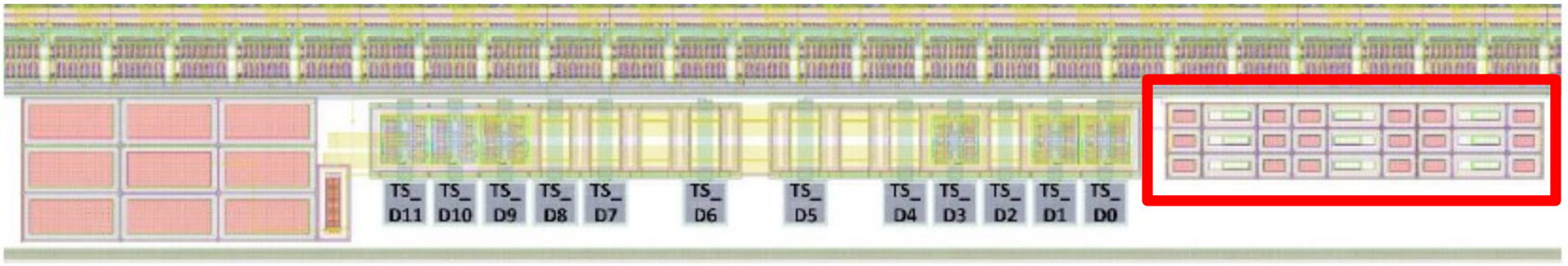
Connection Details



Pad no	Pad name	Type	Purpose
TS_D0	DioIn	Analog	Output of central diode
TS_D1	DioOut	Analog	Output of external 8 diodes
TS_D2	vdda!	Analog	Positive supply voltage for pads (3.3 V)
TS_D3	PW	Analog	Ground for PW (0 V)
TS_D4	gnda!	Analog	Negative supply voltage for pads (0 V)
100 µm gap			
TS_D5	Sub	Analog	Substrate bias voltage (HV < -50 V)

Required for test with edge-TCT of diode structure