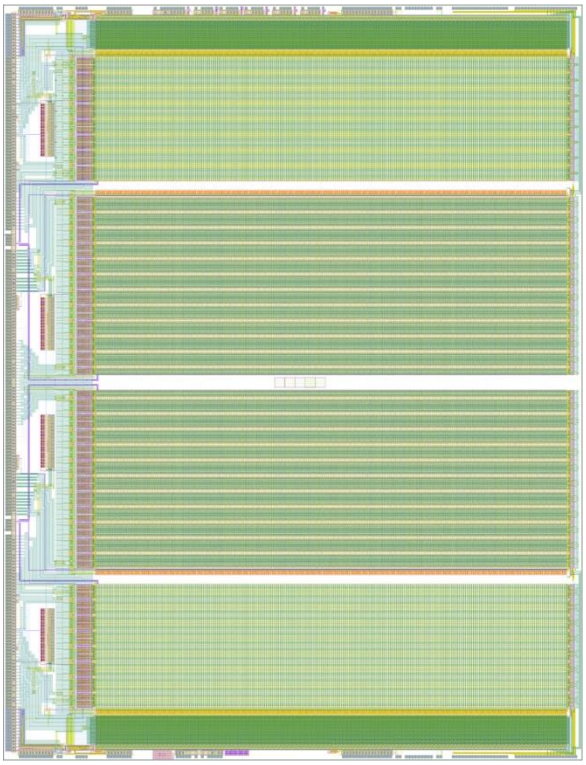

H35DEMO documentation

Date	Version	Authors	Updates
January 2016	1.0	Eva Vilella vilella@hep.ph.liv.ac.uk Raimon Casanova rcasanova@ifae.es Ivan Peric ivan.peric@kit.edu	- First stable version

Table of contents

1. Main features

Property	Value
Name of the chip	H35DEMO
Technology	0.35 µm High-Voltage CMOS (H35) from ams AG
Chip size	18490 µm x 24400 µm (without scribe line)
Tape-out	08-October-2015
Submission type	Engineering run
Fabricated resistivities	20 Ω·cm, 80 Ω·cm, 200 Ω·cm, 1k Ω·cm
Number of wafers/resistivity	6
Number of chips per wafer	60
Contents	- 4 large pixel matrices (all the pixels are 50 µm x 250 µm) - standalone nMOS matrix (16 rows x 300 columns) - first analog matrix (23 rows x 300 columns) - second analog matrix (23 rows x 300 columns) - standalone CMOS matrix (16 rows x 300 columns) - Test structures -- The arrays and the test structures are completely independent

Table I Main features of the submitted pixel demonstrator.

2. Chip layout

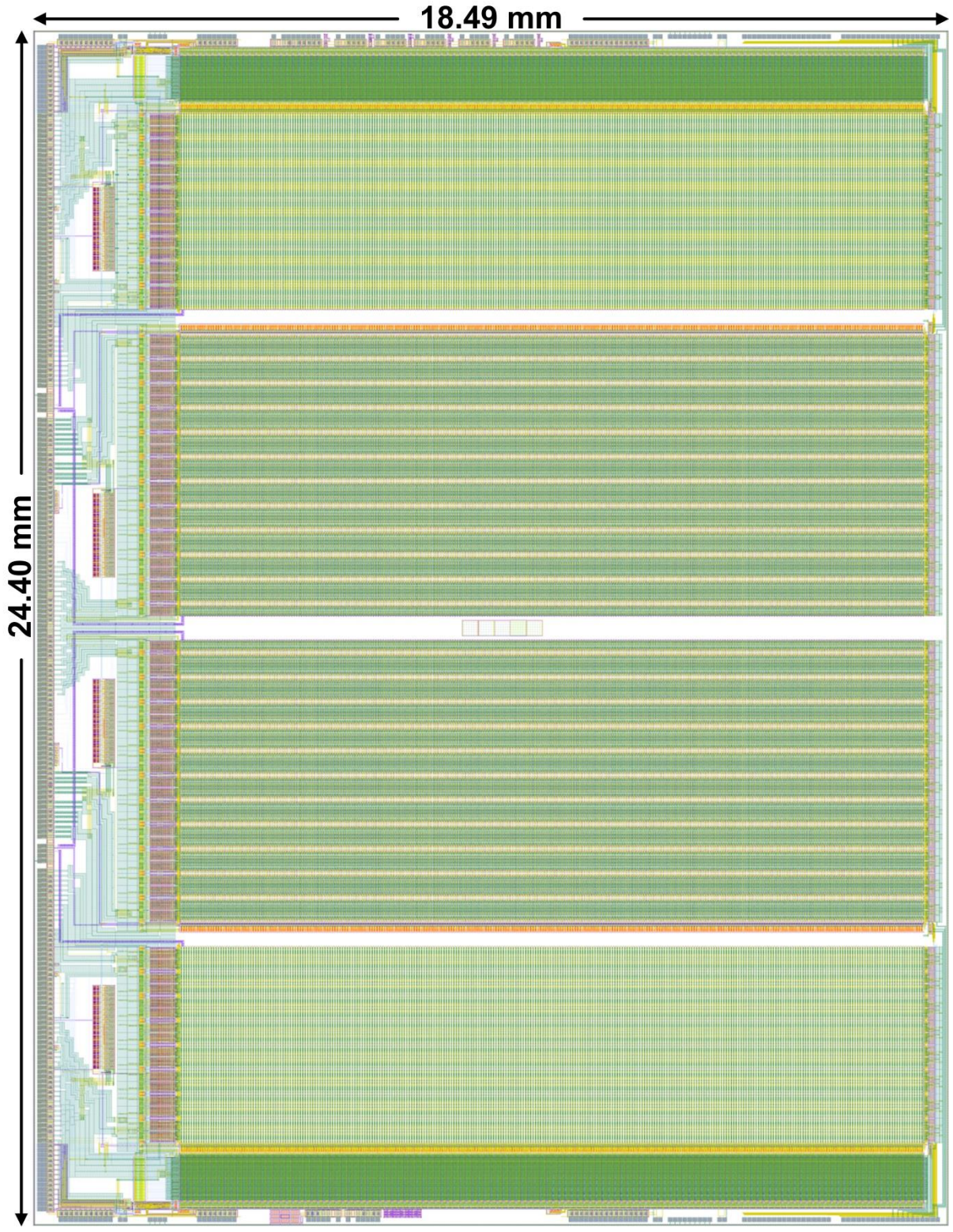

Fig. 1 H35DEMO layout.

3. Pads

3.1. Main features

- All the pads are placed on the top side of the ASIC.

- Each matrix has its own pads.

- The pads of the standalone nMOS matrix and the first analog matrix are mirrored with respect to the second analog matrix and the standalone CMOS matrix.

- Size of the passivation opening of each pad:

- Pads on the up part (see figure 2):

- Each pad has a pitch of 100 µm.
- Passivation opening is 80 µm x 80 µm.

- Pads on the left hand side (see figure 3):

- Each pad has a pitch of 100 µm.
- Passivation opening is 170 µm x 80 µm.

- Pads on the down part (see figure 2):

- Each pad has a pitch of 100 µm.
- Passivation opening is 80 µm x 80 µm.

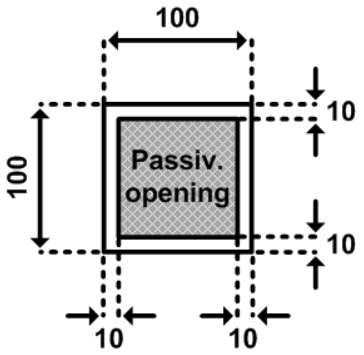

Fig. 2 Schematic diagram of one smaller pad (used in the up and down sides of the chip). All the distances are in µm.

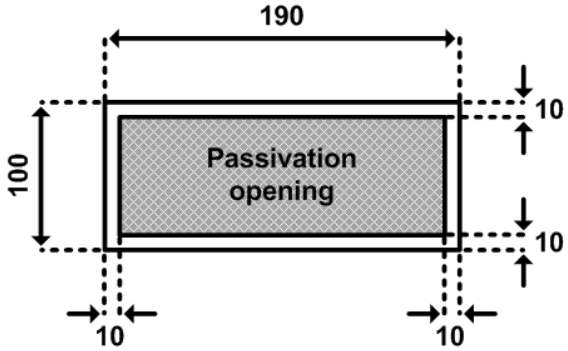

Fig. 3 Schematic diagram of one large pad (used in the left hand side of the chip). All the distances are in µm.

- Types of used pads:

(a) PAD_VP

- It has no protection.
- It is connected to the positive protection diode voltage.
- Used by vdda only.

(b) PAD_VN

- It has no protection.
- It is connected to the negative protection diode voltage.
- Used by gnda only.

(c) PAD_All_H35CCPDv1

- It has protection diodes.
- The pad and the internal connection are shorted.

(d) PAD_NoProtNoPad

- It has no protection.
- There is no passivation opening, no wire can be bonded.
- It is used to introduce a separation between low and high-voltage pads, while keeping continuity in the positive and negative protection diode voltages.

(e) PAD_NoProtAll

- It has no protection.
- It is the same pad as PAD_VP, but with less vias.
- It is used by vdda and HV. In HV, it biases the matrices and it can also bias the substrate guard ring around the pad ring.

(f) PAD_Substrat

- It has no protection.

(g) PAD_All_H35CCPDv1 + OutputBufferAnalogAll

- It is a PAD_All_H35CCPDv1 connected to a CMOS input.

(h) PAD_All_H35CCPDv1 + OutputBufferDigitalAll

- It is a PAD_All_H35CCPDv1 connected to a CMOS output.

(i) PAD_All_PullDown

- It is a PAD_All_H35CCPDv1, but with a pull-down resistor.

(j) PAD_NoProt_Simplest

- It only has a passivation opening and metals for the connections.

3.2. List of pads

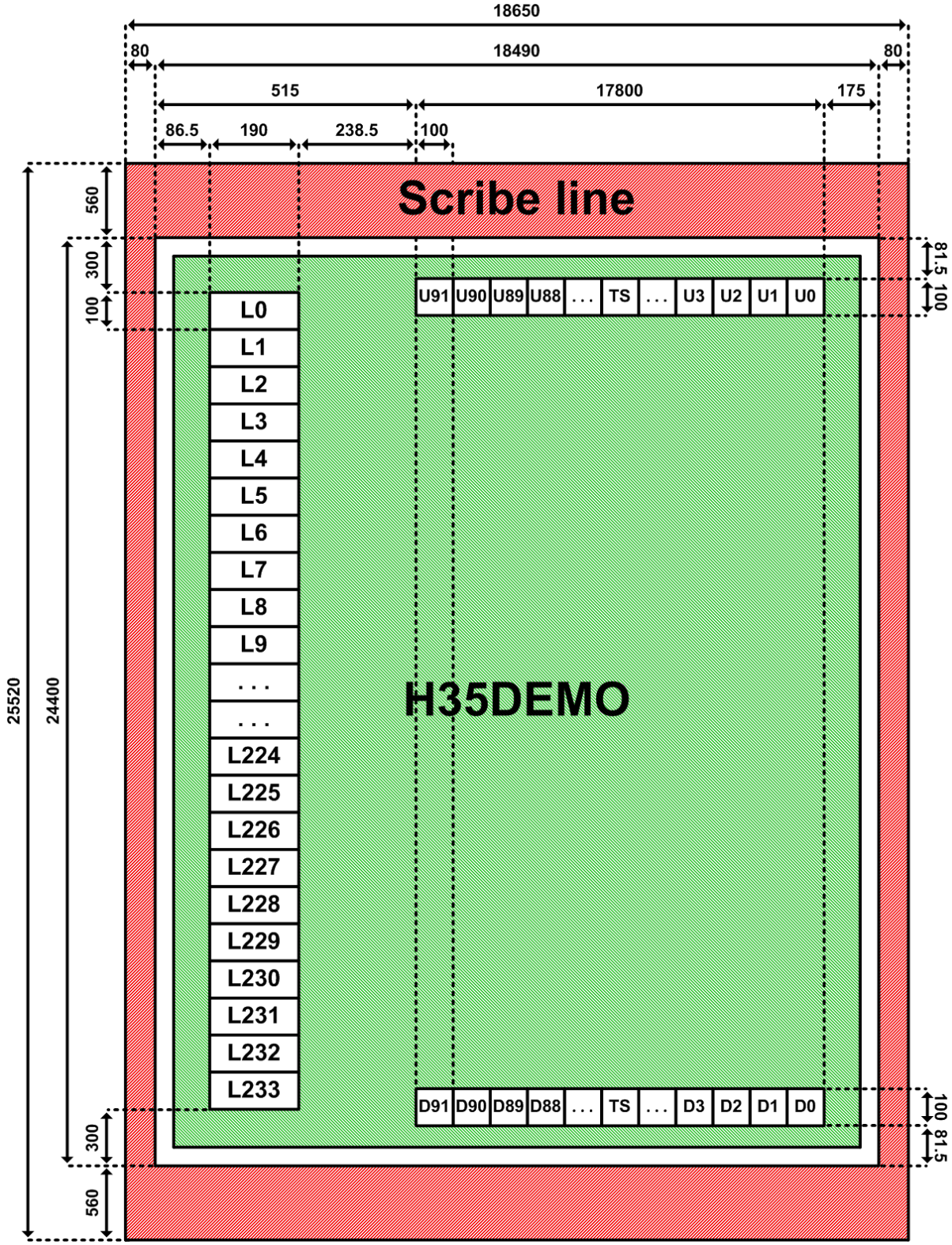

Fig. 4 Schematic diagram of the pad distribution. All the pads of the test structures are placed in the TS block - **TS contains empty gaps (please see section 3.2.4)**. All the distances are in µm.

Comments:

- In the pcb, we need the following power connectors:

Name	Value	Purpose
gnda!	0 V	- Analog power
gndd!	0 V	- Digital power of pixels
vdda!	3.3 V	- Analog power
vddd!	3.3 V	- Digital power of pixels
VSensBias, aSensBias, bSensBias, nSensBias	3.3 V	- Analog input to bias the cathode (dntub) of the sensor through an in-chip resistor. If connected to the positive power, analog or digital, it would not be possible to see particle hits. No current.
Sub	< -50 V	- Analog input to bias the anode (p-substrate) of the sensor
vssa!	2.0 V 2.5 V (in ANA1 only)	- Analog input to power the charge sensitive amplifier in the pixels
aCascGND, bCascGND, nCascGND	0.4 V	- Analog input to power the charge sensitive amplifier (except in ANA1) - Analog input to bias the charge sensitive amplifier (only in ANA1) - Current ↓↓↓
aVPBias, bVPBias, nVPBias	> 0 V < 3.3 V	- Connected to *mDac* circuit
ConnBiasPads, nConnBiasPads	0 V or 3.3 V	- CMOS control signal connected to circuit *BiasPadsSwitches*
ConnBiasPadsB, nConnBiasPadsB	0 V or 3.3 V	- CMOS control signal connected to circuit *BiasPadsSwitches*

Table II Required power and analog input connectors for all the matrices.

Name	Value	Purpose
aVGate, bVGate	3.3 V	- Analog input to pixels (named VPlus in pixel schematics)

Table III Required analog input connectors for the analog matrices.

Name	Value	Purpose
gnd!	0 V	- Digital power of digital blocks
vdd!	3.3 V	- Digital power of digital blocks
nBL	2.2 V	- Analog input to bias block and digital block. No current.
nBLPix	1.5 V	- Analog input to bias block and pixels. No current.
nTh	nBL+thr	- Analog input to digital block. The value of thr is usually 6σ (~32-35 mV). No current.
nThPix	nBLPix+thr	- Analog input to pixels. The value of thr is usually 6σ (~32-35 mV). - No current.
nThTwPix	1.334 V	- In nMOS matrix: Analog input to pixels with time-walk compensated comparator. - In CMOS matrix: To digital block with 2-threshold scheme. - No current
nVDDRAM	3.3 V	- Analog input to power comparators in standalone matrices - Current ↓
nVGatePix	3.6 V	- Analog input to comparators in pixels. No current.
nVPlusTwPix	1.6 V	- In nMOS matrix: Analog input to pixels with time-walk compensated comparator. - In CMOS matrix: Not connected. - Current ↓↓

Table IV Required analog input connectors for the standalone matrices.

- In table V, the pads connected to **nMOS** are connected to the **standalone nMOS matrix**; the pads connected to **ANA1** are connected to the **first analog matrix**.

- In table XX, the pads connected to **CMOS** are connected to the **standalone CMOS matrix**; the pads connected to **ANA2** are connected to the **second analog matrix**.

- The matrices work as four completely independent devices. Pads with the same name and belonging to different matrices (except powers) are not connected between them.

- There is no protection between the p-substrate and the exterior world.

3.2.1. Pads on the up part

Pad number	Pad name	Purpose (matrix)	Pad number	Pad name	Purpose (matrix)
U0 (j)	vssa!	Ana in (ANA1)	**U39 (j)**	gnd!	Power dig (nMOS)
U1 (j)	gnda!	Power ana (ANA1)	**Gap separation of 100 µm (equivalent to 1 pad)**		
U2 (j)	VSensBias	Ana in (ANA1)	**U40 (j)**	--	HV guard ring
U3 (j)	vssa!	Ana in (nMOS)	**U41 (j)**	--	HV guard ring
U4 (j)	VSensBias	Ana in (nMOS)	**U42 (j)**	--	HV guard ring
U5 (j)	gnda!	Power ana (nMOS)	**U43 (j)**	--	HV guard ring
U6 (j)	vdd!	Power dig (nMOS)	**U44 (j)**	--	HV guard ring
U7 (j)	gnd!	Power dig (nMOS)	**U45 (j)**	--	HV guard ring
U8 (j)	gnd!	Power dig (nMOS)	**U46 (j)**	--	HV guard ring
U9 (j)	vdd!	Power dig (nMOS)	**U47 (j)**	--	HV guard ring
U10 (j)	ConnBiasPads	Dig in (ANA1)	**U48 (j)**	--	HV guard ring
U11 (j)	ConnBiasPadsB	Dig in (ANA1)	**Gap separation of 100 µm (equivalent to 1 pad)**		
U12 (j)[1]	BiasPAD<0>	Ana out (ANA1)	**U49 (j)**	gnd!	Power dig (nMOS)
U13 (j)	BiasPAD<1>	Ana out (ANA1)	**U50 (j)**	vdd!	Power dig (nMOS)
U14 (j)	BiasPAD<2>	Ana out (ANA1)	**Gap separation of 100 µm (equivalent to 1 pad)**		
U15 (j)	BiasPAD<3>	Ana out (ANA1)	**U51 (c)**	nAddrRPAD<7>	Dig out (nMOS)
U16 (j)	BiasPAD<4>	Ana out (ANA1)	**U52 (c)**	nAddrRPAD<6>	Dig out (nMOS)
U17 (j)	BiasPAD<5>	Ana out (ANA1)	**U53 (c)**	nAddrRPAD<5>	Dig out (nMOS)
U18 (j)	BiasPAD<6>	Ana out (ANA1)	**U54 (c)**	nAddrRPAD<4>	Dig out (nMOS)
U19 (j)	BiasPAD<7>	Ana out (ANA1)	**U55 (c)**	nAddrRPAD<3>	Dig out (nMOS)
Gap separation of 200 µm (equivalent to 2 pads)			**U56 (c)**	nAddrRPAD<2>	Dig out (nMOS)
U20 (j)	nConnBiasPads	Dig in (nMOS)	**U57 (c)**	nAddrRPAD<1>	Dig out (nMOS)
U21 (j)	nConnBiasPadsB	Dig in (nMOS)	**U58 (c)**	nAddrRPAD<0>	Dig out (nMOS)
U22 (j)	nBiasPAD<11>	Ana out (nMOS)	**U59 (c)**	nTSRPAD<0>	Dig out (nMOS)
U23 (j)	nBiasPAD<12>	Ana out (nMOS)	**U60 (c)**	nTSRPAD<1>	Dig out (nMOS)
U24 (j)	nBiasPAD<13>	Ana out (nMOS)	**U61 (c)**	nTSRPAD<2>	Dig out (nMOS)
U25 (j)	nBiasPAD<14>	Ana out (nMOS)	**U62 (c)**	nTSRPAD<3>	Dig out (nMOS)
U26 (j)	nBiasPAD<15>	Ana out (nMOS)	**U63 (c)**	nTSRPAD<4>	Dig out (nMOS)
U27 (j)	nBiasPAD<0>	Ana out (nMOS)	**U64 (c)**	nTSRPAD<5>	Dig out (nMOS)
U28 (j)	nBiasPAD<1>	Ana out (nMOS)	**U65 (c)**	nTSRPAD<6>	Dig out (nMOS)
U29 (j)	nBiasPAD<2>	Ana out (nMOS)	**U66 (c)**	nTSRPAD<7>	Dig out (nMOS)
U30 (j)	nBiasPAD<3>	Ana out (nMOS)	**Gap separation of 6700 µm (equiv. to 67 pads)**[2]		
U31 (j)	nBiasPAD<4>	Ana out (nMOS)	**U67 (c)**	nPullDNPAD	Dig out (nMOS)
U32 (j)	nBiasPAD<5>	Ana out (nMOS)	**U68 (c)**	nRdPixPAD	Dig out (nMOS)
U33 (j)	nBiasPAD<6>	Ana out (nMOS)	**U69 (c)**	nLdPixPAD	Dig out (nMOS)
U34 (j)	nBiasPAD<7>	Ana out (nMOS)	**U70 (c)**	nParEnPAD	Dig out (nMOS)
U35 (j)	nBiasPAD<8>	Ana out (nMOS)	**U71 (c)**	nRoCkPAD	Dig out (nMOS)
U36 (j)	nBiasPAD<9>	Ana out (nMOS)	**U72 (c)**	nFastLdPAD	Dig out (nMOS)
U37 (j)	nBiasPAD<10>	Ana out (nMOS)	**U73 (i)**	nTSExt<0>	Dig in (nMOS)
Gap separation of 300 µm (equivalent to 3 pads)			**U74 (i)**	nTSExt<1>	Dig in (nMOS)
U38 (j)	vdd!	Power dig (nMOS)	**Gap separation of 600 µm (equivalent to 6 pads)**		

[1] For more details for pads from U12 to U19 and from U22 to U37, see table XXXII.
[2] Test structures are placed in this gap separation. Please see section 3.2.4.

Pad number	Pad name	Purpose	Pad number	Pad name	Purpose
U75 (j)	--	HV guard ring	**U83 (i)**	nTSExt<4>	Dig in (nMOS)
U76 (j)	--	HV guard ring	**U84 (i)**	nTSExt<5>	Dig in (nMOS)
U77 (j)	--	HV guard ring	**U85 (i)**	nTSExt<6>	Dig in (nMOS)
U78 (j)	--	HV guard ring	**U86 (i)**	nTSExt<7>	Dig in (nMOS)
Gap separation of 400 µm (equivalent to 4 pads)			**U87 (i)**	nRoCkExt	Dig in (nMOS)
U79 (j)	gnd!	Power dig (nMOS)	**U88 (i)**	nParEnExt	Dig in (nMOS)
U80 (j)	vdd!	Power dig (nMOS)	**U89 (i)**	nLdPixExt	Dig in (nMOS)
Gap separation of 100 µm (equivalent to 1 pad)			**U90 (i)**	nRdPixExt	Dig in (nMOS)
U81 (i)	nTSExt<2>	Dig in (nMOS)	**U91 (i)**	nPullDNExt	Dig in (nMOS)
U82 (i)	nTSExt<3>	Dig in (nMOS)			

Table V Pads on the up part of the chip. They are connected to the standalone nMOS matrix and the first analog matrix.

3.2.2. Pads on the left hand side

Standalone nMOS matrix:

Pad number	Pad name	Purpose	Pad number	Pad name	Purpose
L0 (c)	nSyRes_P	LVDS in	**L37 (c)**	gndd!	Power dig pix
L1 (c)	nSyRes_N	LVDS in	**L38 (c)**	gndd!	Power dig pix
L2 (c)	nFastCk_P	LVDS in	**L39 (c)**	nVDDRAM	Ana in
L3 (c)	nFastCk_N	LVDS in	**L40 (c)**	nBL	Ana in
L4 (c)	nAddrL_N	LVDS out[3]	**L41 (c)**	nTh	Ana in
L5 (c)	nAddrL_P	LVDS out	**L42 (c)**	nBLPix	Ana in pix
L6 (c)	nTSL_N	LVDS out	**L43 (c)**	nThPix	Ana in pix
L7 (c)	nTSL_P	LVDS out	**L44 (c)**	nVGatePix	Ana in pix
L8 (c)	nAddrR_N	LVDS out	**L45 (c)**	nThTwPix	Ana in pix
L9 (c)	nAddrR_P	LVDS out	**L46 (c)**	nVPlusTwPix	Ana in pix
L10 (c)	nTSR_N	LVDS out	**L47 (c)**	nSensBias	Ana in
L11 (c)	nTSR_P	LVDS out	**L48 (g)**	nMonitor	Ana out
L12 (c)	HB_N	LVDS out	**L49 (c)**	nInjection	Signal in
L13 (c)	HB_P	LVDS out	**L50 (h)**	nSout	Dig out CMOS
L14 (c)	vdd!	Power dig, protection	**L51 (c)**	nSIn	Dig in CMOS
L15 (a)	vdd!	Power dig	**L52 (c)**	nLd	Dig in CMOS
L16 (c)	gnd!	Power dig	**L53 (c)**	nCk2	Dig in CMOS
L17 (c)	gnd!	Power dig	**L54 (c)**	nCk1	Dig in CMOS
L18 (b)	gnd!	Power dig, protection	**L55 (c)**	gndd!	Power dig pixel
L19 (c)	gnd!	Power dig	**L56 (c)**	gndd!	Power dig pixel
L20 (e)	vdd!	Power dig	**L57 (c)**	gndd!	Power dig pixel
L21 (c)	vdd!	Power dig	**L58 (c)**	nVCascPMOS	Not used
L22 (b)	gnda!	Power ana, protection	**L59 (c)**	nCascGND	Ana in
L23 (c)	gnda!	Power ana	**L60 (c)**	vddd!	Power dig pixel
L24 (c)	gnda!	Power ana	**L61 (c)**	vddd!	Power dig pixel
L25 (c)	vssa!	Ana in	**L62 (c)**	vddd!	Power dig pixel
L26 (c)	vssa!	Ana in	**L63 (c)**	vdda!	Power ana
L27 (c)	vssa!	Ana in	**L64 (a)**	vdda!	Power ana, protection
L28 (c)	VNPix	Ana out, decoupling or n.c.	**L65 (c)**	vssa!	Ana in
L29 (c)	vdda!	Power ana	**L66 (c)**	vssa!	Ana in
L30 (a)	vdda!	Power ana, protection	**L67 (c)**	vssa!	Ana in
L31 (c)	vddd!	Power dig pix	**L68 (c)**	gnda!	Power ana
L32 (c)	vddd!	Power dig pix	**L69 (b)**	gnda!	Power ana, protection
L33 (g)	AnalogOut_0	Ana out	**(d)**	No bonding	Separation
L34 (c)	nCascGND	Ana in, power	**L70 (e)**	Sub	HV, chip ring
L35 (c)	nVPBias	Ana in, main bias: decoupling or n.c.	**L71 (f)**	Sub	HV, periphery ring
L36 (c)	gndd!	Power dig pix	**L72 (e)**	Sub	HV, pixel ring

Table VI Pads on the left hand side connected to the standalone nMOS matrix.

[3] LVDS out means open drain out. It needs a 100 Ω pull-up resistor to 3.3 V.

First analog matrix:

Pad number	Pad name	Purpose	Pad number	Pad name	Purpose
L73 (e)	Sub	HV, pixel ring	**L95 (c)**	aSIn	Dig in CMOS
(d)	No bonding	Separation	**L96 (c)**	aLd	Dig in CMOS
L74 (b)	gnda!	Power ana, protection	**L97 (c)**	aCk2	Dig in CMOS
L75 (c)	gnda!	Power ana	**L98 (c)**	aCk1	Dig in CMOS
L76 (c)	gnda!	Power ana	**L99 (c)**	aSensBias	Ana in
L77 (c)	vssa!	Ana in	**L100 (c)**	aVGate	Ana in
L78 (c)	vssa!	Ana in	**L101 (c)**	aTh	Ana out (1.5 V)
L79 (c)	vssa!	Ana in	**L102 (c)**	aBL	Ana out (1.5 V)
L80 (a)	vdda!	Power ana, protection	**L103 (c)**	aVCascPMOS	Ana out (1.6 V)
L81 (c)	vdda!	Power ana	**L104 (c)**	aCascGND	Ana in, not used
L82 (c)	aVPBias	Ana in, main bias: decoupling or n.c.	**L105 (c)**	vddd!	Power dig pixel
L83 (c)	gndd!	Power dig pixel	**L106 (c)**	vddd!	Power dig pixel
L84 (c)	gndd!	Power dig pixel	**L107 (c)**	gndd!	Power dig pixel
L85 (c)	vddd!	Power dig pixel	**L108 (c)**	gndd!	Power dig pixel
L86 (c)	vddd!	Power dig pixel	**L109 (c)**	vdda!	Power ana
L87 (c)	aCascGND	Ana in, not used	**L110 (a)**	vdda!	Power ana, protection
L88 (c)	aInjection	Signal in	**L111 (c)**	vssa!	Ana in
L89 (c)	AnalogOut_1	Ana out	**L112 (c)**	vssa!	Ana in
L90 (c)	aMonitor<0>	Ana out	**L113 (c)**	vssa!	Ana in
L91 (c)	aMonitor<1>	Ana out	**L114 (c)**	gnda!	Power ana
L92 (c)	aMonitor<2>	Ana out	**L115 (c)**	gnda!	Power ana
L93 (c)	aSOut	Dig out CMOS	**L116 (b)**	gnda!	Power ana, protection
L94 (c)	aShiftEnB	Dig in CMOS or ‘0’			

Table VII Pads on the left hand side connected to the first analog matrix.

Second analog matrix:

Pad number	Pad name	Purpose	Pad number	Pad name	Purpose
L117 (b)	gnda!	Power ana, protection	**L139 (c)**	bShiftEnB	Dig in CMOS or '0'
L118 (c)	gnda!	Power ana	**L140 (c)**	bSOut	Dig out CMOS
L119 (c)	gnda!	Power ana	**L141 (c)**	bMonitor<2>	Ana out
L120 (c)	vssa!	Ana in	**L142 (c)**	bMonitor<1>	Ana out
L121 (c)	vssa!	Ana in	**L143 (c)**	bMonitor<0>	Ana out
L122 (c)	vssa!	Ana in	**L144 (c)**	AnalogOut_2	Ana out
L123 (a)	vdda!	Power ana, protection	**L145 (c)**	bInjection	Signal in
L124 (c)	vdda!	Power ana	**L146 (c)**	bCascGND	Ana in
L125 (c)	gndd!	Power dig pix	**L147 (c)**	vddd!	Power dig pix
L126 (c)	gndd!	Power dig pix	**L148 (c)**	vddd!	Power dig pix
L127 (c)	vddd!	Power dig pix	**L149 (c)**	gndd!	Power dig pix
L128 (c)	vddd!	Power dig pix	**L150 (c)**	gndd!	Power dig pix
L129 (c)	bCascGND	Ana in	**L151 (c)**	bVPBias	Ana in
L130 (c)	bVCascPMOS	Ana out, not used	**L152 (c)**	vdda!	Power ana
L131 (c)	bBL	Ana out (1.5 V)	**L153 (a)**	vdda!	Power ana, protection
L132 (c)	bTh	Ana out (1.5 V)	**L154 (c)**	vssa!	Power ana
L133 (c)	bVGate	Ana in	**L155 (c)**	vssa!	Power ana
L134 (c)	bSensBias	Ana in	**L156 (c)**	vssa!	Power ana
L135 (c)	bCk1	Dig in CMOS	**L157 (c)**	gnda!	Power ana
L136 (c)	bCk2	Dig in CMOS	**L158 (c)**	gnda!	Power ana
L137 (c)	bLd	Dig in CMOS	**L169 (b)**	gnda!	Power ana, protection
L138 (c)	bSIn	Dig in CMOS	**(d)**	No bonding	Separation
			L160 (e)	Sub	HV, pixel ring

Table VIII Pads on the left hand side connected to the second analog matrix.

CMOS standalone matrix:

Pad number	Pad name	Purpose	Pad number	Pad name	Purpose
L161 (e)	Sub	HV, pixel ring	**L197 (c)**	gndd!	Power dig pix
L162 (f)	Sub	HV, periphery ring	**L198 (c)**	nVPBias	Ana in, main bias: decoupling or n.c.
L163 (e)	Sub	HV, chip ring	**L199 (c)**	nCascGND	Ana in
(d)	No bonding	Separation	**L200 (g)**	AnalogOut_3	Ana Out
L164 (b)	gnda!	Power ana, protection	**L201 (c)**	vddd!	Power dig pix
L165 (c)	gnda!	Power ana	**L202 (c)**	vddd!	Power dig pix
L166 (c)	vssa!	Ana in	**L203 (a)**	vdda!	Power ana pix, protection
L167 (c)	vssa!	Ana in	**L204 (c)**	vdda!	Power ana pix
L168 (c)	vssa!	Ana in	**L205 (c)**	VNPix	Ana out, decoupling or n.c.
L169 (a)	vdda!	Power ana, protection	**L206 (c)**	vssa!	Ana in
L170 (c)	vdda!	Power ana	**L207 (c)**	vssa!	Ana in
L171 (c)	vddd!	Power dig pix	**L208 (c)**	vssa!	Ana in
L172 (c)	vddd!	Power dig pix	**L209 (c)**	gnda!	Power ana
L173 (c)	vddd!	Power dig pix	**L210 (c)**	gnda!	Power ana
L174 (c)	nCascGND	Ana in	**L211 (b)**	gnda!	Power ana, protection
L175 (c)	nVCascPMOS	Ana out, not used	**L212 (c)**	vdd!	Power dig
L176 (c)	gndd!	Power dig pix	**L213 (e)**	vdd!	Power dig
L177 (c)	gndd!	Power dig pix	**L214 (c)**	gnd!	Power dig
L178 (c)	gndd!	Power dig pix	**L215 (b)**	gnd!	Power dig, protection
L179 (c)	nCk1	Dig in CMOS	**L216 (c)**	gnd!	Power dig
L180 (c)	nCk2	Dig in CMOS	**L217 (c)**	gnd!	Power dig
L181 (c)	nLd	Dig in CMOS	**L218 (a)**	vdd!	Power dig, protection
L182 (c)	nSIn	Dig in CMOS	**L219 (c)**	vdd!	Power dig
L183 (h)	nSout	Dig out CMOS	**L220 (c)**	HB_P	LVDS out
L184 (c)	nInjection	Signal in	**L221 (c)**	HB_N	LVDS out
L185 (g)	nMonitor	Ana out	**L222 (c)**	nTSR_P	LVDS out
L186 (c)	nSensBias	Ana in	**L223 (c)**	nTSR_N	LVDS out
L187 (c)	nVPlusTwPix	Ana in pix, not used	**L224 (c)**	nAddrR_P	LVDS out
L188 (c)	nThTwPix	Ana in pix	**L225 (c)**	nAddrR_N	LVDS out
L189 (c)	nVGatePix	Ana in pix	**L226 (c)**	nTSL_P	LVDS out
L190 (c)	nThPix	Ana in pix	**L227 (c)**	nTSL_N	LVDS out
L191 (c)	nBLPix	Ana in pix	**L228 (c)**	nAddrL_P	LVDS out
L192 (c)	nTh	Ana in	**L229 (c)**	nAddrL_N	LVDS out
L193 (c)	nBL	Ana in	**L230 (c)**	nFastCk_N	LVDS in
L194 (c)	nVDDRAM	Ana in	**L231 (c)**	nFastCk_P	LVDS in
L195 (c)	gndd!	Power dig pix	**L232 (c)**	nSyRes_N	LVDS in
L196 (c)	gndd!	Power dig pix	**L233 (c)**	nSyRes_P	LVDS in

Table IX Pads on the left hand side connected to the standalone CMOS matrix.

3.2.3. Pads on the down part

Pad number	Pad name	Purpose (matrix)	Pad number	Pad name	Purpose (matrix)
D0 (j)	vssa!	Ana in (ANA2)	**D39 (j)**	gnd!	Power dig (CMOS)
D1 (j)	gnda!	Power ana (ANA2)	**Gap separation of 100 µm (equivalent to 1 pad)**		
D2 (j)	VSensBias	Ana in (ANA2)	**D40 (j)**	--	HV guard ring
D3 (j)	vssa!	Ana in (CMOS)	**D41 (j)**	--	HV guard ring
D4 (j)	VSensBias	Ana in (CMOS)	**D42 (j)**	--	HV guard ring
D5 (j)	gnda!	Power ana (CMOS)	**D43 (j)**	--	HV guard ring
D6 (j)	vdd!	Power dig (CMOS)	**D44 (j)**	--	HV guard ring
D7 (j)	gnd!	Power dig (CMOS)	**D45 (j)**	--	HV guard ring
D8 (j)	gnd!	Power dig (CMOS)	**D46 (j)**	--	HV guard ring
D9 (j)	vdd!	Power dig (CMOS)	**D47 (j)**	--	HV guard ring
D10 (j)	ConnBiasPads	Dig in (ANA2)	**D48 (j)**	--	HV guard ring
D11 (j)	ConnBiasPadsB	Dig in (ANA2)	**Gap separation of 100 µm (equivalent to 1 pad)**		
D12 (j)[4]	BiasPAD<0>	Ana out (ANA2)	**D49 (j)**	gnd!	Power dig (CMOS)
D13 (j)	BiasPAD<1>	Ana out (ANA2)	**D50 (j)**	vdd!	Power dig (CMOS)
D14 (j)	BiasPAD<2>	Ana out (ANA2)	**Gap separation of 100 µm (equivalent to 1 pad)**		
D15 (j)	BiasPAD<3>	Ana out (ANA2)	**D51 (c)**	AddrRPAD<7>	Dig out (CMOS)
D16 (j)	BiasPAD<4>	Ana out (ANA2)	**D52 (c)**	AddrRPAD<6>	Dig out (CMOS)
D17 (j)	BiasPAD<5>	Ana out (ANA2)	**D53 (c)**	AddrRPAD<5>	Dig out (CMOS)
D18 (j)	BiasPAD<6>	Ana out (ANA2)	**D54 (c)**	AddrRPAD<4>	Dig out (CMOS)
D19 (j)	BiasPAD<7>	Ana out (ANA2)	**D55 (c)**	AddrRPAD<3>	Dig out (CMOS)
Gap separation of 200 µm (equivalent to 2 pads)			**D56 (c)**	AddrRPAD<2>	Dig out (CMOS)
D20 (j)	ConnBiasPads	Dig in (CMOS)	**D57 (c)**	AddrRPAD<1>	Dig out (CMOS)
D21 (j)	ConnBiasPadsB	Dig in (CMOS)	**D58 (c)**	AddrRPAD<0>	Dig out (CMOS)
D22 (j)	BiasPAD<11>	Ana out (CMOS)	**D59 (c)**	TSRPAD<0>	Dig out (CMOS)
D23 (j)	BiasPAD<12>	Ana out (CMOS)	**D60 (c)**	TSRPAD<1>	Dig out (CMOS)
D24 (j)	BiasPAD<13>	Ana out (CMOS)	**D61 (c)**	TSRPAD<2>	Dig out (CMOS)
D25 (j)	BiasPAD<14>	Ana out (CMOS)	**D62 (c)**	TSRPAD<3>	Dig out (CMOS)
D26 (j)	BiasPAD<15>	Ana out (CMOS)	**D63 (c)**	TSRPAD<4>	Dig out (CMOS)
D27 (j)	BiasPAD<0>	Ana out (CMOS)	**D64 (c)**	TSRPAD<5>	Dig out (CMOS)
D28 (j)	BiasPAD<1>	Ana out (CMOS)	**D65 (c)**	TSRPAD<6>	Dig out (CMOS)
D29 (j)	BiasPAD<2>	Ana out (CMOS)	**D66 (c)**	TSRPAD<7>	Dig out (CMOS)
D30 (j)	BiasPAD<3>	Ana out (CMOS)	**Gap separation of 6700 µm (equiv. to 67 pads)**[5]		
D31 (j)	BiasPAD<4>	Ana out (CMOS)	**D67 (c)**	PullDNPAD	Dig out (CMOS)
D32 (j)	BiasPAD<5>	Ana out (CMOS)	**D68 (c)**	RdPixPAD	Dig out (CMOS)
D33 (j)	BiasPAD<6>	Ana out (CMOS)	**D69 (c)**	LdPixPAD	Dig out (CMOS)
D34 (j)	BiasPAD<7>	Ana out (CMOS)	**D70 (c)**	ParEnPAD	Dig out (CMOS)
D35 (j)	BiasPAD<8>	Ana out (CMOS)	**D71 (c)**	RoCkPAD	Dig out (CMOS)
D36 (j)	BiasPAD<9>	Ana out (CMOS)	**D72 (c)**	FastLdPAD	Dig out (CMOS)
D37 (j)	BiasPAD<10>	Ana out (CMOS)	**D73 (i)**	TSExt<0>	Dig in (CMOS)
Gap separation of 300 µm (equivalent to 3 pads)			**D74 (i)**	TSExt<1>	Dig in (CMOS)
D38 (j)	vdd!	Power dig (CMOS)	**Gap separation of 600 µm (equivalent to 6 pads)**		

[4] For more details for pads from D12 to D19 and from D22 to D37, see table XXXII.
[5] Test structures are placed in this gap separation. Please see section 3.2.4.

Pad number	Pad name	Purpose	Pad number	Pad name	Purpose
D75 (j)	--	HV guard ring	**D83 (i)**	TSExt<4>	Dig in (CMOS)
D76 (j)	--	HV guard ring	**D84 (i)**	TSExt<5>	Dig in (CMOS)
D77 (j)	--	HV guard ring	**D85 (i)**	TSExt<6>	Dig in (CMOS)
D78 (j)	--	HV guard ring	**D86 (i)**	TSExt<7>	Dig in (CMOS)
Gap separation of 400 µm (equivalent to 4 pads)			**D87 (i)**	RoCkExt	Dig in (CMOS)
D79 (j)	gnd!	Power dig (CMOS)	**D88 (i)**	ParEnExt	Dig in (CMOS)
D80 (j)	vdd!	Power dig (CMOS)	**D89 (i)**	LdPixExt	Dig in (CMOS)
Gap separation of 100 µm (equivalent to 1 pad)			**D90 (i)**	RdPixExt	Dig in (CMOS)
D81 (i)	TSExt<2>	Dig in (CMOS)	**D91 (i)**	PullDNExt	Dig in (CMOS)
D82 (i)	TSExt<3>	Dig in (CMOS)			

Table X Pads on the down part of the chip. They are connected to the standalone CMOS matrix and the second analog matrix.

3.2.4 Pads connected to the test structures

Up part of the chip:

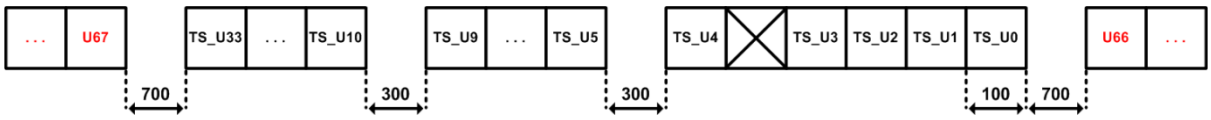

Fig. 5 Schematic diagram of the pad distribution on the up part. All the distances are in µm.

Pad number	Pad name	Purpose	Pad number	Pad name	Purpose
. . .			**TS_U17 (c)**	ConnLow	Pulse signal
U66 (c)	TSRPAD<7>	Dig out (nMOS)	**TS_U18 (c)**	VLow	Ana in (gnda!)
Gap separation of 700 µm (equiva. to 7 pads)			**(d)**	No bonding	Separation
TS_U0 (c)	VHi	Ana in (vdda!)	**TS_U19 (e)**	Sub	HV
TS_U1 (c)	ConnHi	Pulse signal	**Gap separation of 200 µm (equiva. to 2 pads)**		
TS_U2 (c)	ConnLow	Pulse signal	**TS_U20 (c)**	VHi	Ana in (vdda!)
TS_U3 (c)	VLow	Ana in (gnda!)	**TS_U21 (c)**	ConnHi	Pulse signal
(d)	No bonding	Separation	**TS_U22 (c)**	ConnLow	Pulse signal
TS_U4 (e)	Sub	HV	**TS_U23 (c)**	VLow	Ana in (gnda!)
Gap separation of 300 µm (equiva. to 3 pads)			**(d)**	No bonding	Separation
TS_U5 (c)	VHi	Ana in (vdda!)	**TS_U24 (e)**	Sub	HV
TS_U6 (c)	ConnHi	Pulse signal	**Gap separation of 300 µm (equiva. to 2 pads)**		
TS_U7 (c)	ConnLow	Pulse signal	**TS_U25 (c)**	VHi	Ana in (vdda!)
TS_U8 (c)	VLow	Ana in (gnda!)	**TS_U26 (c)**	ConnHi	Pulse signal
(d)	No bonding	Separation	**TS_U27 (c)**	ConnLow	Pulse signal
TS_U9 (e)	Sub	HV	**TS_U28 (c)**	VLow	Ana in (gnda!)
Gap separation of 300 µm (equiva. to 3 pads)			**TS_U29 (c)**	vdda!	Power ana
TS_U10 (c)	VHi	Ana in (vdda!)	**TS_U30 (a)**	vdda!	Power ana
TS_U11 (c)	ConnHi	Pulse signal	**TS_U31 (c)**	gnda!	Power ana
TS_U12 (c)	ConnLow	Pulse signal	**TS_U32 (b)**	gnda!	Power ana
TS_U13 (c)	VLow	Ana in (gnda!)	**(d)**	No bonding	Separation
(d)	No bonding	Separation	**TS_U33 (e)**	Sub	HV
TS_U14 (e)	Sub	HV	**Gap separation of 700 µm (equiva. to 7 pads)**		
Gap separation of 200 µm (equiva. to 2 pads)			**U67 (c)**	nPullDNPAD	Dig in (nMOS)
TS_U15 (c)	VHi	Ana in (vdda!)	. . .		
TS_U16 (c)	ConnHi	Pulse signal			

Table XI Pads on the up part of the chip that are connected to the test structures.

Down part of the chip:

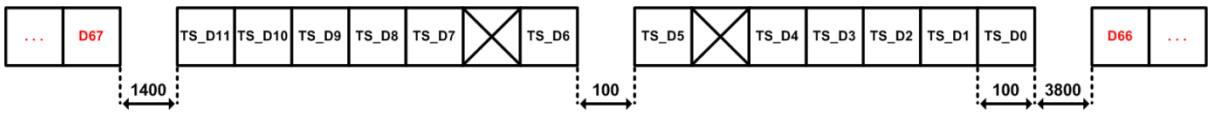

Fig. 6 Schematic diagram of the pad distribution on the down part. All the distances are in µm.

Pad number	Pad name	Purpose	Pad number	Pad name	Purpose
. . .			**TS_D6 (e)**	Sub	HV
D66 (c)	TSRPAD<7>	Dig out (CMOS)	**(d)**	No bonding	Separation
Gap separation of 3800 µm (equiva. to 38 pads)			**TS_D7 (b)**	gnda!	Power ana
TS_D0 (c)	DioIn	Ana in	**TS_D8 (a)**	vdda!	Power ana
TS_D1 (c)	DioOut	Ana out	**TS_D9 (c)**	DioBias	Ana in
TS_D2 (a)	vdda!	Power ana	**TS_D10 (c)**[6]	VHi	Ana in
TS_D3 (c)	PW	Ana in	**TS_D11 (c)**[7]	DioIn	Ana out (to Res)
TS_D4 (b)	gnda!	Power ana	**Gap separation of 1400 µm (equiva. to 14 pads)**		
(d)	No bonding	Separation	**D67 (c)**	PullDNPAD	Dig in (CMOS)
TS_D5 (e)	Sub	HV	. . .		
Gap separation of 100 µm (equiva. to 1 pad)					

Table XII Pads on the down part of the chip that are connected to the test structures.

[6] The pads used in TS_D10 and in TS_D11 are PAD_All_H35CCPDv1, but without MET3. In this circuit, MET3 is used for the connections (very wide lines) between the readout circuit and the pads.
[7] The pads used in TS_D10 and in TS_D11 are PAD_All_H35CCPDv1, but without MET3. In this circuit, MET3 is used for the connections (very wide lines) between the readout circuit and the pads.

4. General block diagrams

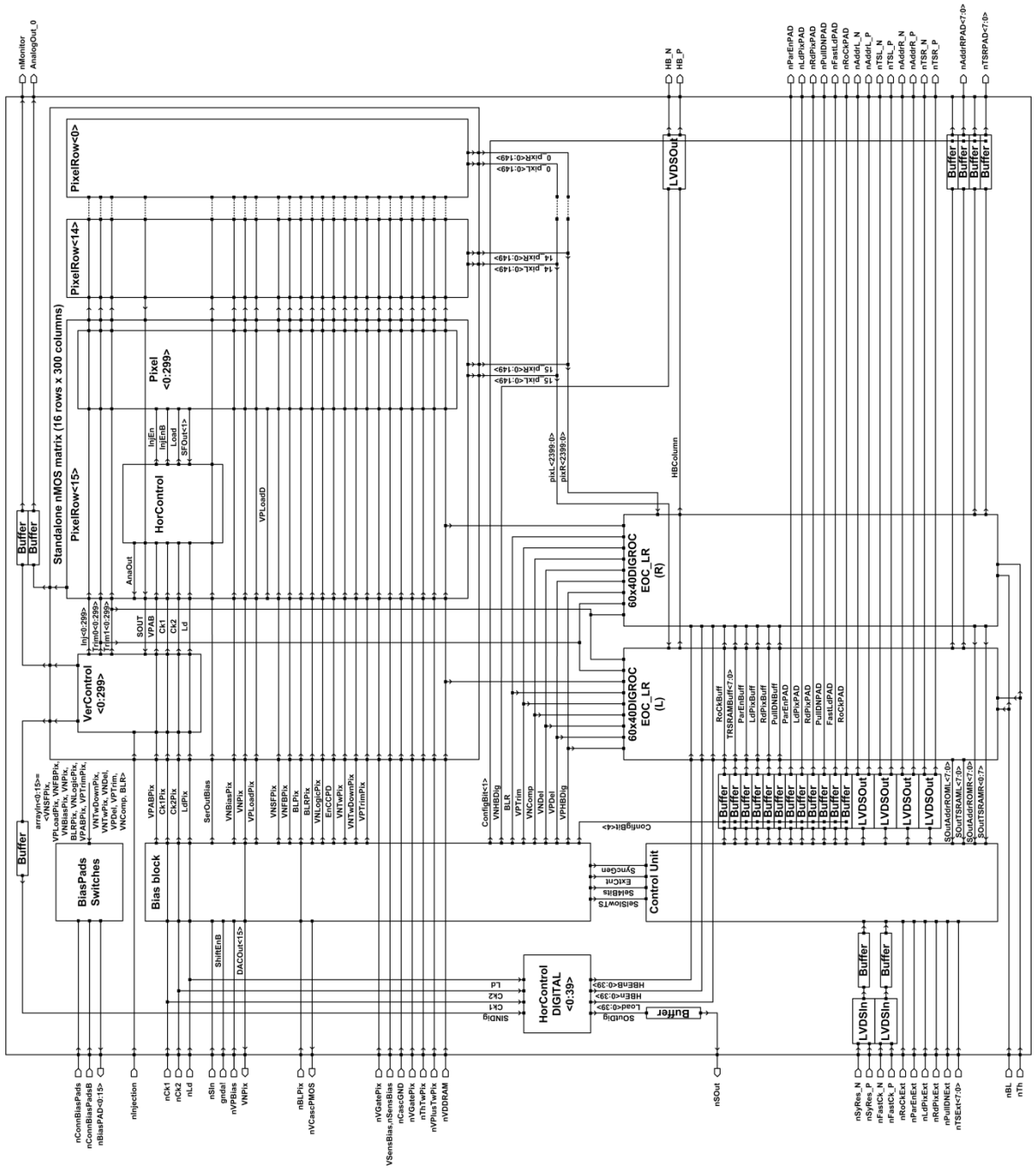

Fig. 7 Simplified block diagram of the standalone nMOS matrix. Global powers (gnda!, gndd!, gnd!, vdda!, vddd! and vdd!), vssa! and HV are not included in this diagram.

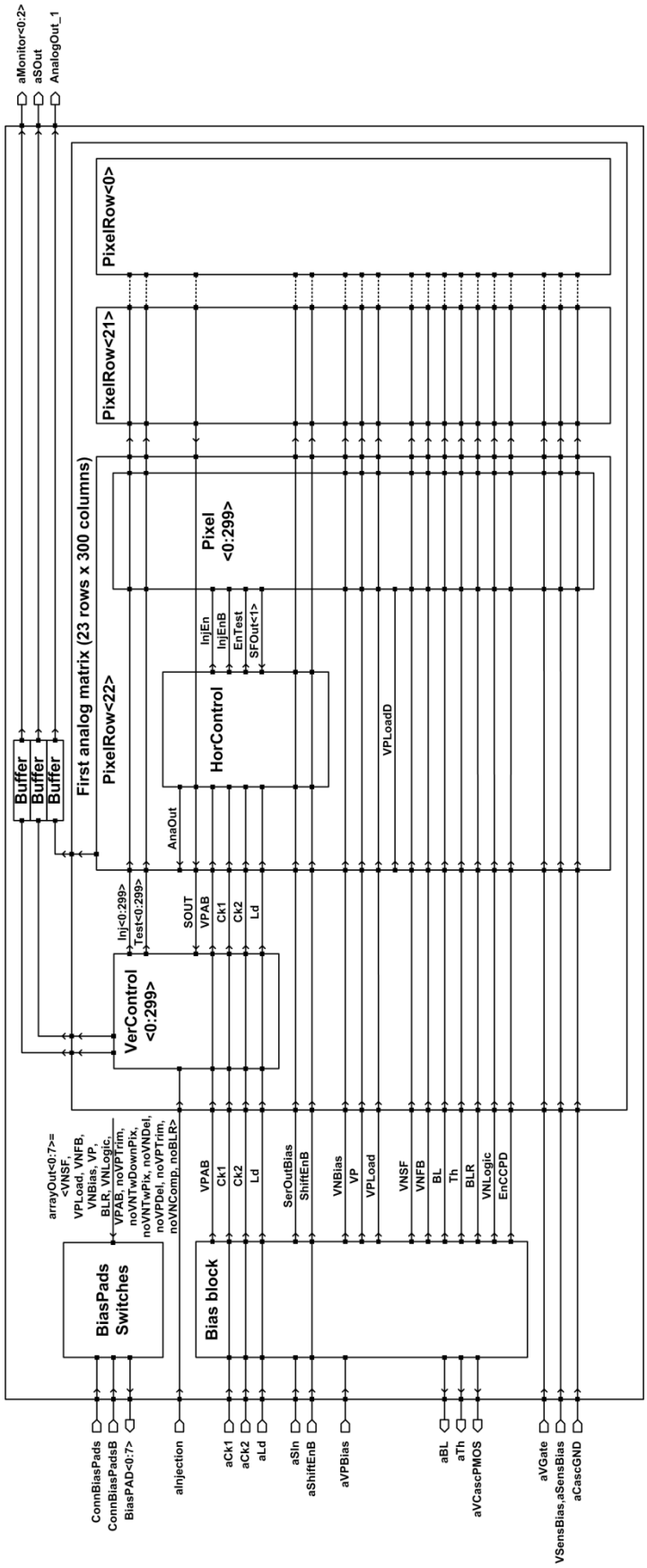

Fig. 8 Simplified block diagram of the first analog matrix. Global powers (gnda!, gndd!, gnd!, vdda!, vddd! and vdd!), vssa! and HV are not included in this diagram.

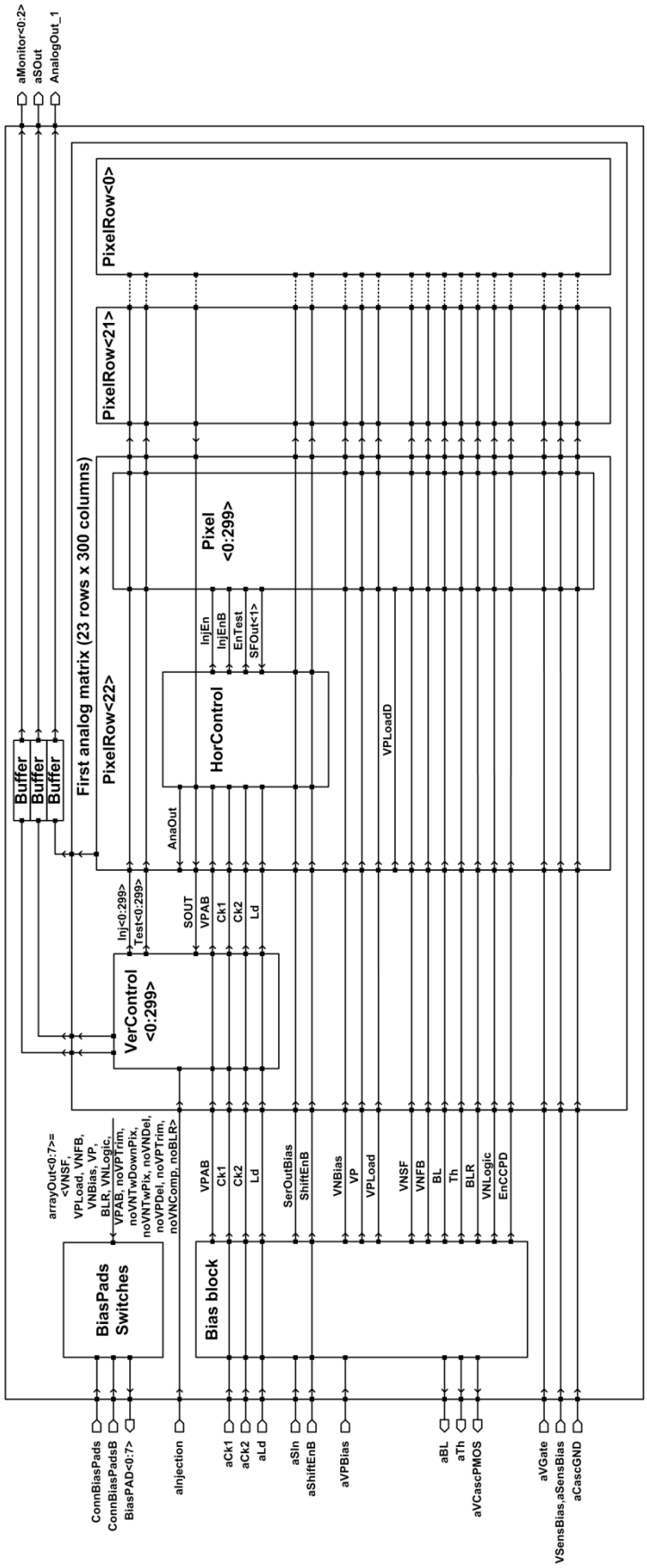

Fig. 9 Simplified block diagram of the second analog matrix. Global powers (gnda!, gndd!, gnd!, vdda!, vddd! and vdd!), vssa! and HV are not included in this diagram.

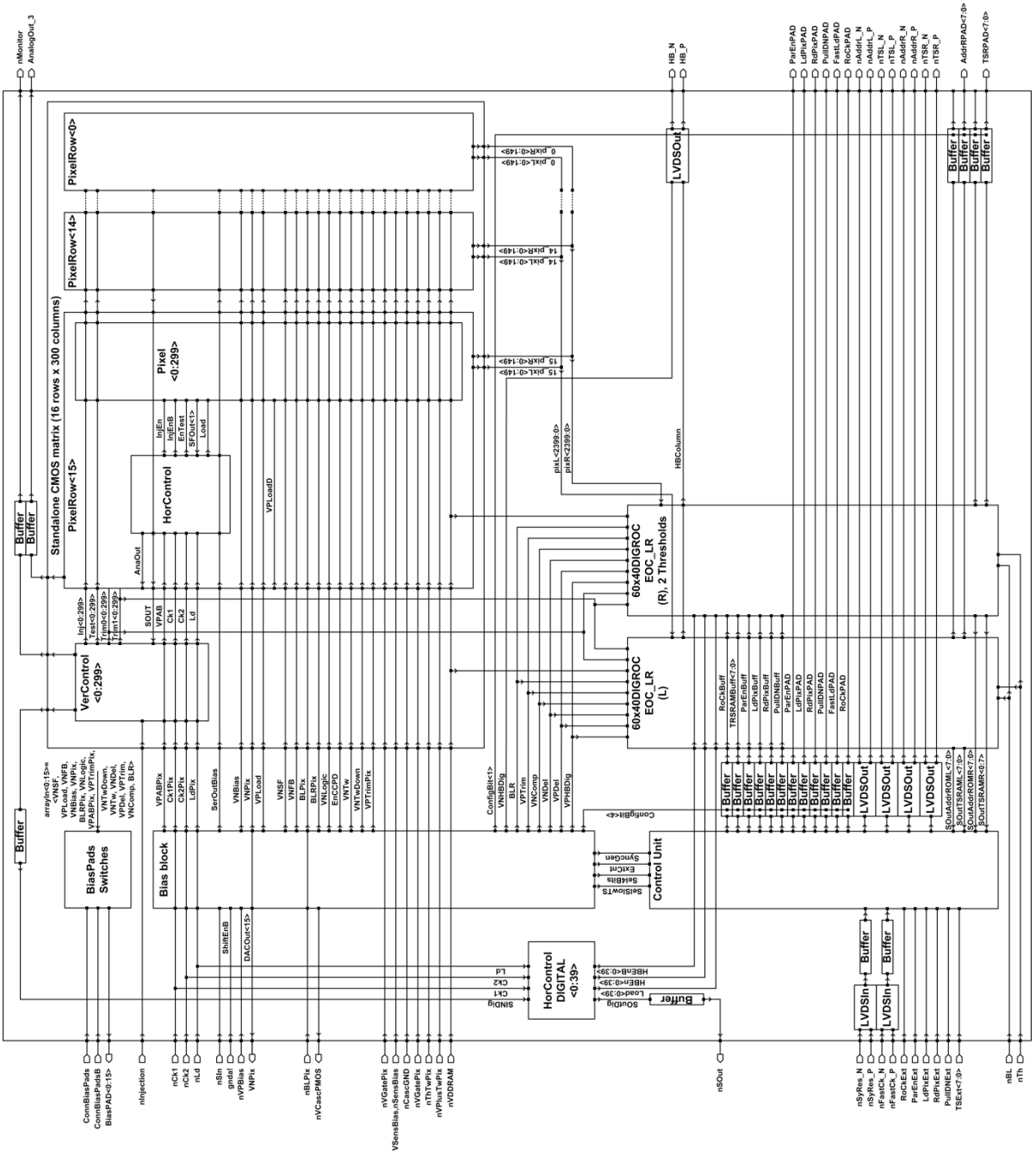

Fig. 10 Simplified block diagram of the standalone CMOS matrix. Global powers (gnda!, gndd!, gnd!, vdda!, vddd! and vdd!), vssa! and HV are not included in this diagram.

5. Standalone nMOS matrix

Property	Value
Number of pixels	16 rows x 300 columns of pixels
Type of pixels	- 150 columns with a simple nMOS comparator - 150 columns with a time-walk compensated nMOS comparator

Table XIII Main features of the standalone nMOS matrix.

5.1. Pixel schematic without comparator

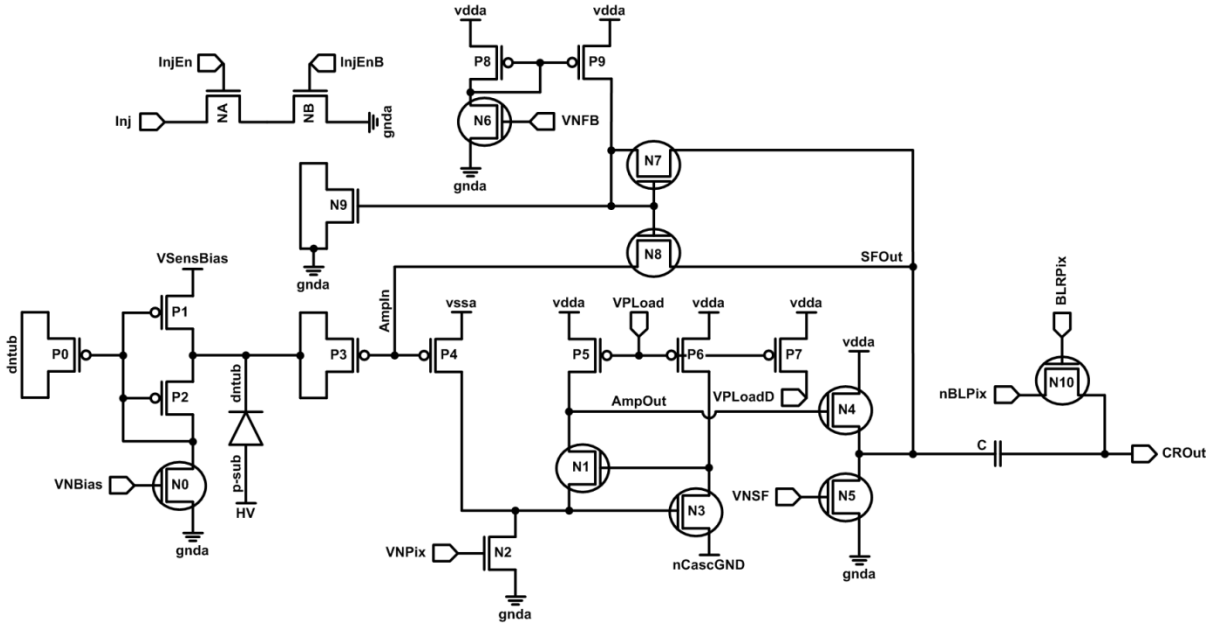

Fig. 11 Schematic of one pixel (without comparator) from the standalone nMOS matrix.

Component	Value	Component	Value
P0	(3.9/3.65)	**N0**	(6/1)
P1-P2	(1/3)	**N1**	(5/0.4)
P2	(1/3)	**N2**	(2/3)
P3	(10.6/12.2)	**N3**	(5/0.4)
P4	(40/0.4)	**N4**	(5/0.4)
P5-P6-P7	(0.7/3)	**N5**	(6/1)
P8-P9	(0.7/3)	**N6**	(6/1)
P9	(0.7/3)	**N7-N8**	(5/0.4)
		N9	(0.8/9.7)
C	150.84 fF	**N10**	(5/0.4)
		NA-NB	(1/0.4)

Table XIV Values of components of one pixel (without comparator) from the standalone nMOS matrix.

5.1.1. Schematic of the simple nMOS comparator

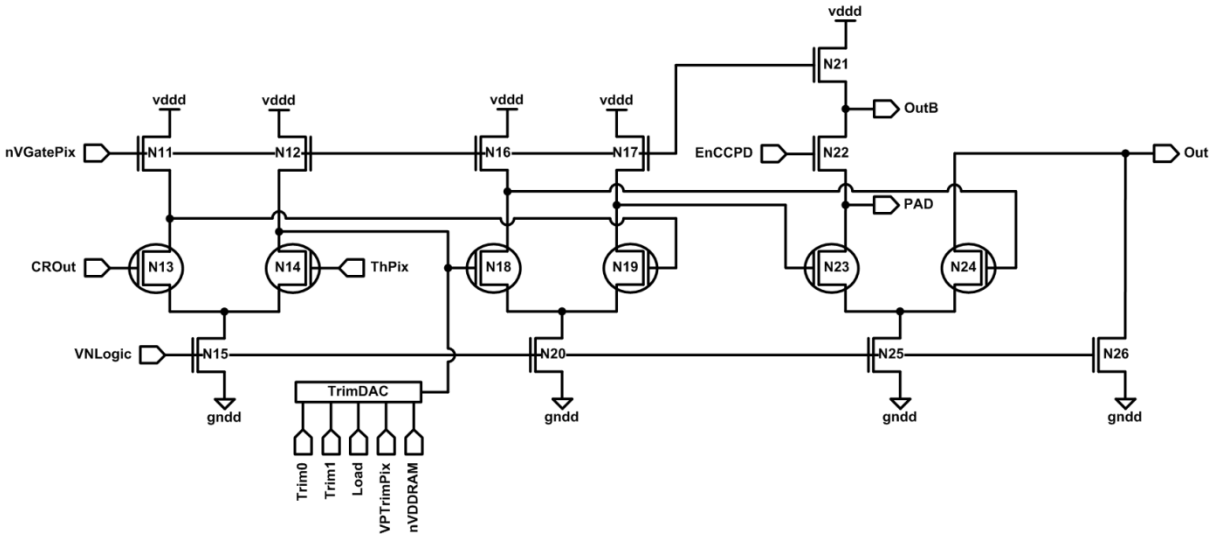

Fig. 12 Schematic of the simple nMOS comparator.

Component	Value
N11-N12	(0.4/17.8)
N13-N14	(6/1)
N15	(1.85/7.5)
N16-N17	(0.4/8.9)
N18-N19	(6/1)
N20	(1.85/4)
N21	(0.4/7.7)
N22	(0.4/0.35)
N23-N24	(6/1)
N25	(1.85/4)
N26	(0.9/3.9)
dntub_1	231 µm x 30 µm
dptub_1	55 µm x 16.65 µm
dptub_2	57.75 µm x 17.1 µm

Table XV Values of components from the simple nMOS comparator.

5.1.2. Schematic of the time-walk compensated comparator

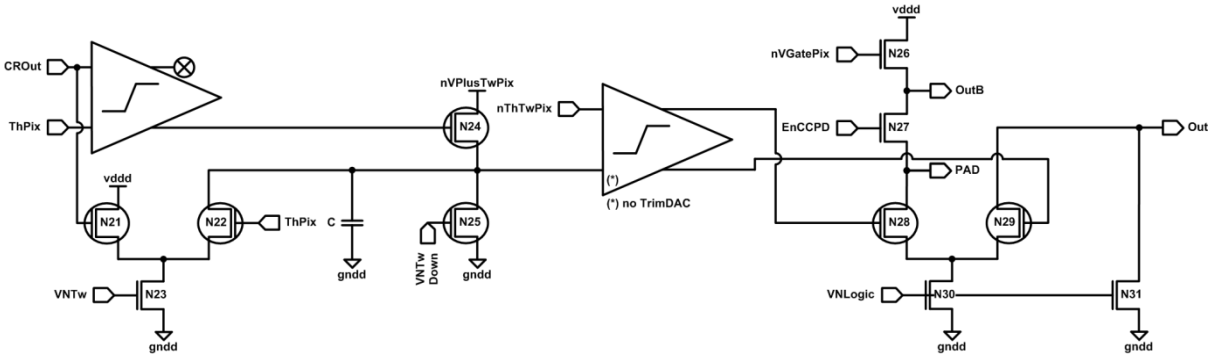

Fig. 13 Schematic of the time-walk compensated nMOS comparator. The first and second comparators within the time-walk compensated comparator are based on 2 differential amplifiers each, like in the simple nMOS comparator, but with different (W/L) and without the output stage.

Component	Value	Value
N11-N12	(0.4/17.8)	(0.4/17.8)
N13-N14	(6/1)	(6/1)
N15	(1.85/7.5)	(1.85/8)
N16-N17	(0.4/17.8)	(0.4/8.9)
N18-N19	(6/1)	(6/1)
N20	(1.85/8)	(1.85/4)

Table XVI Values of components from the first (1st column) and second (2nd column) simple nMOS comparators included in the time-walk compensated comparator.

Component	Value
N21-N22	(6/1)
N23	(1.85/8)
N24	(5/0.4)
N25	(1.85/8)
N26	(0.4/7.7)
N27	(0.4/0.35)
N28-N29	(5/0.4)
N30	(1/1.8)
N31	(0.5/1.8)
C	235.26 fF
dntub_1	231 µm x 30 µm
dptub_1	55 µm x 16.65 µm
dptub_2	109 µm x 17.1 µm

Table XVII Values of components from the time-walk compensated nMOS comparator.

5.2. Pixel power, input and configuration signals

5.2.1. Pixel with the simple nMOS comparator

Power name	Value	Input name	Value	Configuration	Value
nCascGND	0.4 V	**BLPix**	1.5 V (10)	**BLRes**	1
gnda	0 V	**BLRPix**	Bias block	**BLResDig**	10
gndd	0 V	**EnCCPD**	vdda	**NAmp**	60
HV	< - 50 V	**EnTest**	gnda	**NBiasRes**	1
vdda	3.3 V	**Inj**	--	**NcompDig**	10
vddd	3.3 V	**InjEn**	vdda	**NDelDig**	10
vssa	2.0 V	**InjEnB**	gnda	**NFB**	5
VSensBias	3.3 V	**nVGatePix**	3.3 V	**NFoll**	50
		VNPix	Bias block	**NLogic**	20
		VNBias	Bias block	**NTrim1**	10
		VNFB	Bias block	**NTw**	15
		VNLogic	Bias block	**NTwDown**	30
		VNSF	Bias block	**PDelDig**	10
		VPLoad	Bias block	**PLoad**	5
		VPLoadD	VPLoad	**PTrimDig**	10
		Test	3.3 V	**thr**	35m
		ThPix	BLPix	**VPAB**	10

Table XVIII Values of power and input/output signals of the standalone pixels with simple nMOS comparator.

5.2.2. Pixel with the time-walk compensated comparator

Power name	Value	Input name	Value	Output name	Value
nCascGND	0.4 V	**BLPix**	1.5 V (5)	**BLRes**	1
gnda	0 V	**BLRPix**	Bias block	**BLResDig**	10
gndd	0 V	**EnCCPD**	vdda	**NAmp**	60
HV	< - 50 V	**EnTest**	gnda	**NBiasRes**	1
vdda	3.3 V	**Inj**	--	**NcompDig**	10
vddd	3.3 V	**InjEn**	vdda	**NDelDig**	10
vssa	2.0 V	**InjEnB**	gnda	**NFB**	5
VPlusTw	--	**nVGatePix**	3.3 V	**NFoll**	50
VSensBias	3.3 V	**VNPix**	Bias block	**NLogic**	20
		VNBias	Bias block	**NTrim1**	10
		VNFB	Bias block	**NTw**	15
		VNLogic	Bias block	**NTwDown**	30
		VNSF	Bias block	**PDelDig**	10
		VPLoad	Bias block	**PLoad**	5
		VPLoadD	VPLoad	**PTrimDig**	10
		Test	3.3 V	**thr**	35m
		ThPix	BLPix	**VPAB**	10

Table XIX Values of power and input/output signals of the standalone pixels with time-walk compensated nMOS comparator.

5.3. Pixel layout

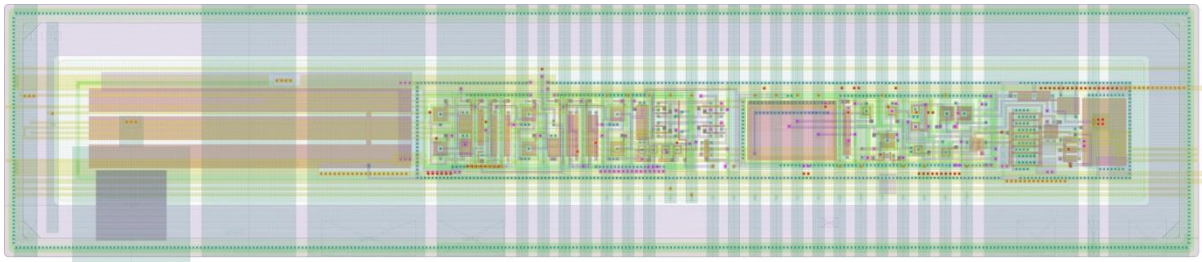

Fig. 14 Layout of the pixel with the simple nMOS comparator.

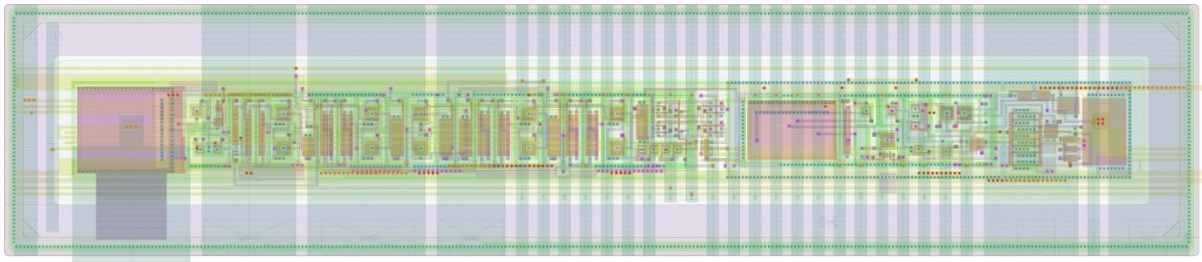

Fig. 15 Layout of the pixel with the time-walk compensated nMOS comparator.

5.4. Post-layout simulation

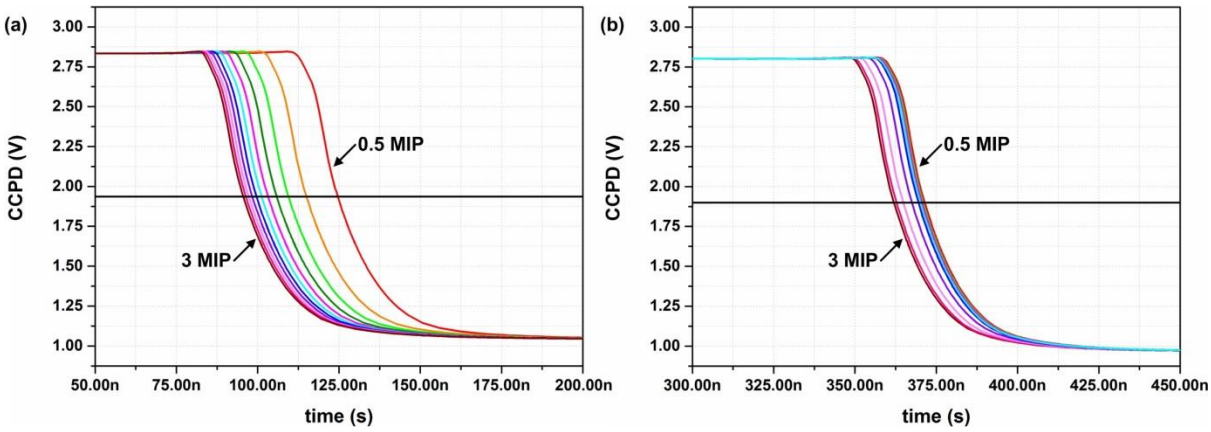

Fig. 16 Transient post-layout simulation of node CCPD in the standalone nMOS pixel (a) with a simple comparator and (b) with a time-walk compensated comparator.

6. First analog matrix

Property	Value
Number of pixels	23 rows x 300 columns of pixels
Type of pixels	- 100 columns columns with extra DPTUB for HV and ELTs in FB - 100 columns without DPTUB for HV and ELTs in FB - 100 columns without DPTUB for HV and linear transistors in FB

Table XX Main features of the first analog matrix.

6.1. Pixel schematic

6.1.1. Pixel schematic with ELTs in the FB block

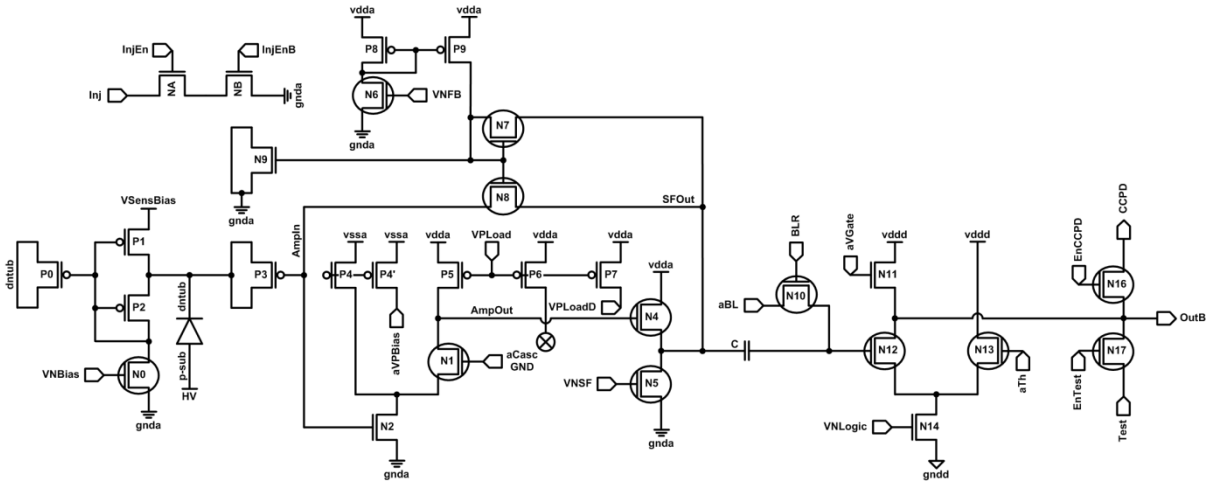

Fig. 17 Schematic of one pixel from the first analog matrix. The feedback block uses enclosed transistors.

Component	Value	Component	Value
P0	(3.9/3.65)	**N0**	(6/1)
P1	(1/3)	**N1**	(5/0.4)
P2	(1/3)	**N2**	(5/0.4)
P3	(8.6/14.2)	**N3**	--
P4	(2.8/2)	**N4**	(5/0.4)
P4'	(0.7/2)	**N5**	(6/1)
P5-P6-P7	(0.7/3)	**N6**	(6/1)
P8-P9	(0.7/3)	**N7-N8**	(5/0.4)
		N9	(4.7/3.8)
C	80.66 fF	**N10**	(5/0.4)
		N11	(1/8.9)
dntub_1	103 µm x 30 µm	**N12-N13**	(6/1)
dntub_2	37 µm x 30 µm	**N14**	(1.85/3.8)
dntub_3	50 µm x 30 µm	**N15**	--
dptub_1	64.55 µm x 16.65 µm	**N16-N17**	(5/0.4)
		NA-NB	(1/0.4)

Table XXI Values of components of one analog pixel from the first analog matrix.

6.1.2. Pixel schematic with linear transistors in the FB block

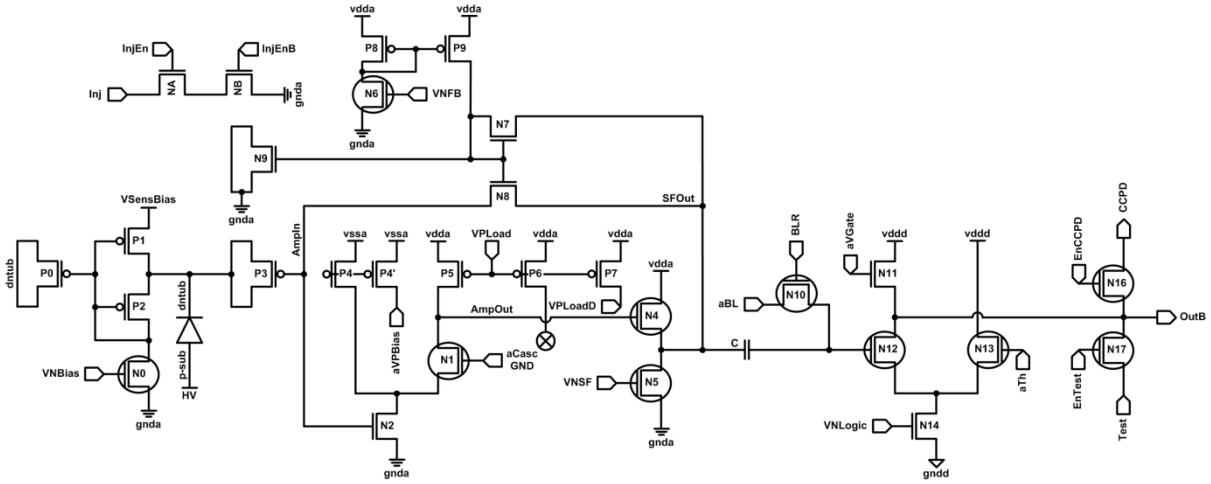

Fig. 18 Schematic of one pixel from the first analog matrix. The feedback block uses linear transistors.

Component	Value	Component	Value
P0	(3.9/3.65)	**N0**	(6/1)
P1	(1/3)	**N1**	(5/0.4)
P2	(1/3)	**N2**	(5/0.4)
P3	(8.6/14.2)	**N3**	--
P4	(2.8/2)	**N4**	(5/0.4)
P4'	(0.7/2)	**N5**	(6/1)
P5-P6-P7	(0.7/3)	**N6**	(6/1)
P8-P9	(0.7/3)	**N7-N8**	(5/0.4)
		N9	(4.7/3.8)
C	80.66 fF	**N10**	(5/0.4)
		N11	(1/8.9)
dntub_1	103 µm x 30 µm	**N12-N13**	(6/1)
dntub_2	37 µm x 30 µm	**N14**	(1.85/3.8)
dntub_3	50 µm x 30 µm	**N15**	--
dptub_1	64.55 µm x 16.65 µm	**N16-N17**	(5/0.4)
		NA-NB	(1/0.4)

Table XXII Values of components of one analog pixel from the first analog matrix.

6.2. Pixel power, input and configuration signals

Power name	Value	Input name	Value	Output name	Value
aCascGND	0.4 V	**nBL**	1.5 V (10)	**BLRes**	1
gnda	0 V	**BLR**	Bias block	**BLResDig**	1
gndd	0 V	**EnCCPD**	vdda	**NAmp**	30
HV	< - 50 V	**EnTest**	gnda	**NBiasRes**	1
vdda	3.3 V	**Inj**	--	**NcompDig**	30
vddd	3.3 V	**InjEn**	vdda	**NDelDig**	10
vssa	2.0 V	**InjEnB**	gnda	**NFB**	10
VSensBias	3.3 V	**aVGate**	3.3 V	**NFoll**	30
		VN	Bias block	**NLogic**	20
		VNBias	Bias block	**NTrim1**	10
		VNFB	Bias block	**NTw**	15
		VNLogic	Bias block	**NTwDown**	30
		VNSF	Bias block	**PDelDig**	10
		VPLoad	Bias block	**PLoad**	10
		VPLoadD	VPLoad	**PTrimDig**	10
		Test	3.3 V	**thr**	32m
		aTh	nBL	**VPAB**	10

Table XXIII Values of power and input/output signals of the pixels from the first analog matrix.

6.3. Pixel layout

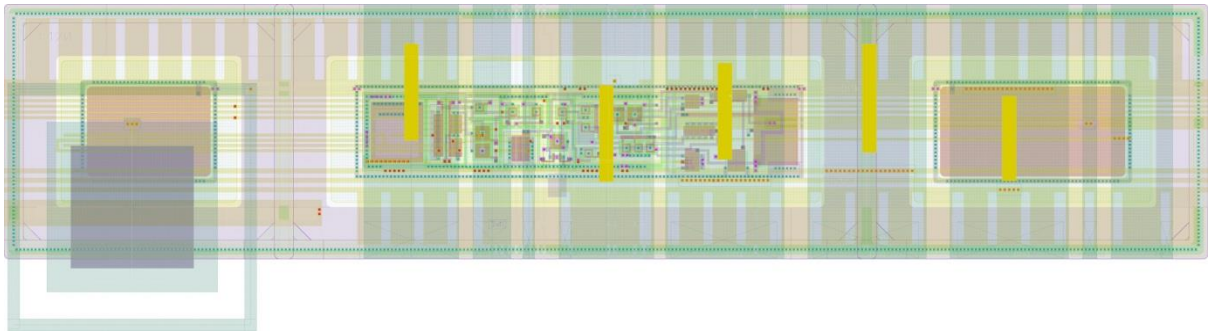

Fig. 19 Layout of the analog pixel with the extra DPTUB and ELTs in the FB block.

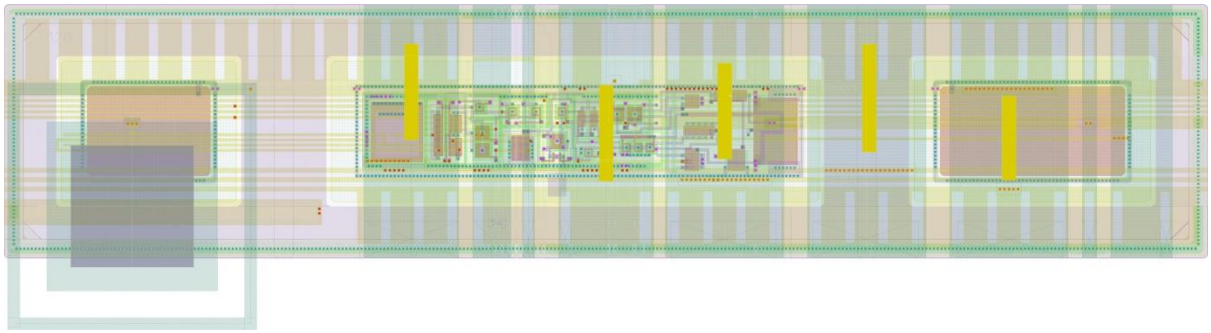

Fig. 20 Layout of the analog pixel without the extra DPTUB and linear transistors in the FB block.

7. Second analog matrix

Property	Value
Number of pixels	23 rows x 300 columns of pixels
Type of pixels	- 100 columns with extra DPTUB for HV and high gain - 100 columns without extra DPTUB for HV and high gain - 100 columns without extra DPTUB for HV and low gain

Table XXIV Main features of the second analog matrix.

7.1. Pixel schematic

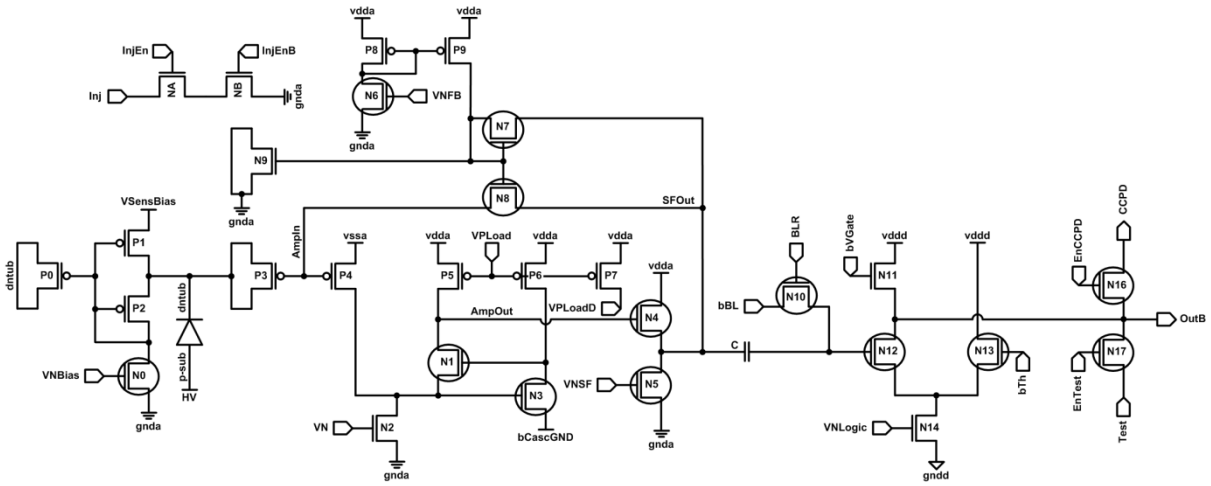

Fig. 21 Schematic of one pixel from the second analog matrix. The three pixel types present the same schematic. The high speed pixel, at the expenses of a low gain, is achieved by adding a capacitor between SFOut and dntub.

Component	Value	Component	Value
P0	(3.9/3.65)	**N0**	(6/1)
P1	(1/3)	**N1**	(4.9/0.35)
P2	(1/3)	**N2**	(2/3)
P3	(8.6/14.2)	**N3**	(5/0.4)
P4	(40/0.4)	**N4**	(5/0.4)
P5- P6-P7	(0.7/3)	**N5**	(6/1)
P8-P9	(0.7/3)	**N6**	(6/1)
		N7- N8	(5/0.4)
C	80.66 fF	**N9**	(4.7/3.8)
		N10	(5/0.4)
dntub_1	103 µm x 30 µm	**N11**	(1/8.9)
dntub_2	37 µm x 30 µm	**N12-N13**	(6/1)
dntub_3	50 µm x 30 µm	**N14**	(1.85/3.8)
dptub_1	64.55 µm x 16.65 µm	**N15**	--
		N16-N17	(5/0.4)
		NA-NB	(1/0.4)

Table XXV Values of components of one analog pixel from the second analog matrix.

7.2. Pixel power, input and configuration signals

Power name	Value	Input name	Value	Configuration	Value
bCascGNDA	0.4 V	**bBL**	1.5 V	**BLRes**	1
gnda	0 V	**BLR**	Bias block	**BLResDig**	1
gndd	0 V	**EnCCPD**	vdda	**NAmp**	30
HV	< - 50 V	**EnTest**	gnda	**NBiasRes**	1
vdda	3.3 V	**Inj**	--	**NcompDig**	30
vddd	3.3 V	**InjEn**	vdda	**NDelDig**	10
vssa	2.0 V	**InjEnB**	gnda	**NFB**	10
VSensBias	3.3 V	**aVGate**	3.3 V	**NFoll**	30
		VN	Bias block	**NLogic**	20
		VNBias	Bias block	**NTrim1**	10
		VNFB	Bias block	**NTw**	15
		VNLogic	Bias block	**NTwDown**	30
		VNSF	Bias block	**PDelDig**	10
		VPLoad	Bias block	**PLoad**	10
		VPLoadD	VPLoad	**PTrimDig**	10
		Test	3.3 V	**thr**	32m
		bTh	bBL	**VPAB**	10

Table XXVI Values of power and input/output signals of the pixels from the second analog matrix.

7.3. Pixel layout

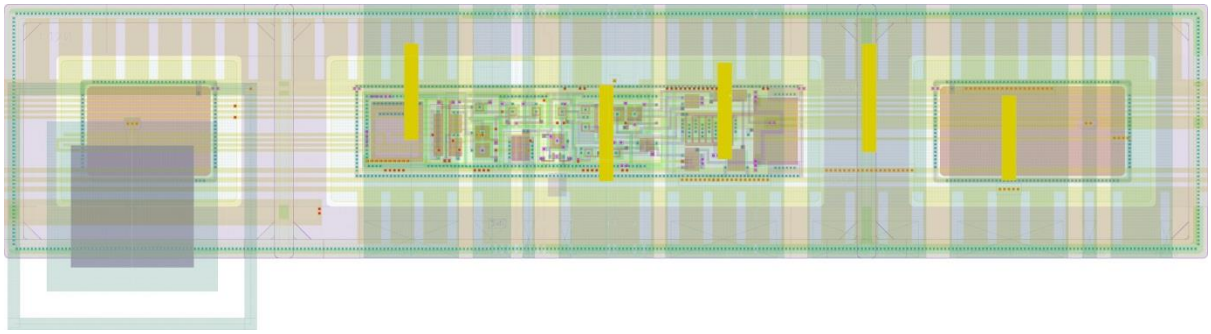

Fig. 22 Layout of the analog pixel with the extra DPTUB and high gain.

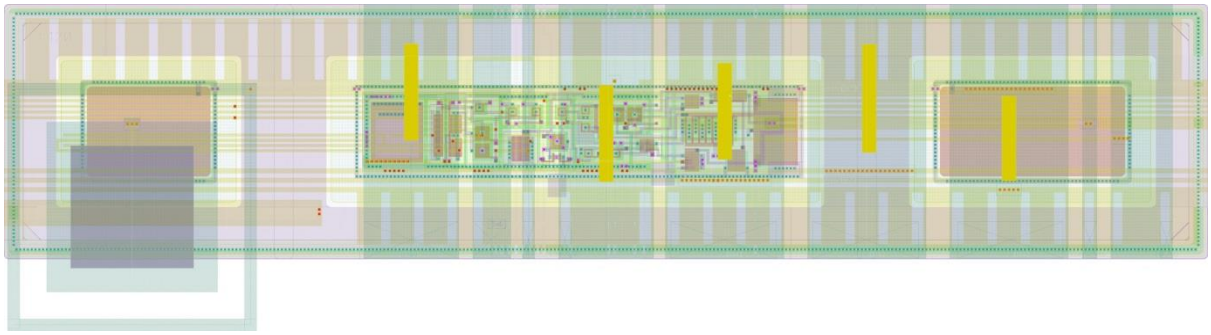

Fig. 23 Layout of the analog pixel without the extra DPTUB and low gain.

7.4. Post-layout simulation

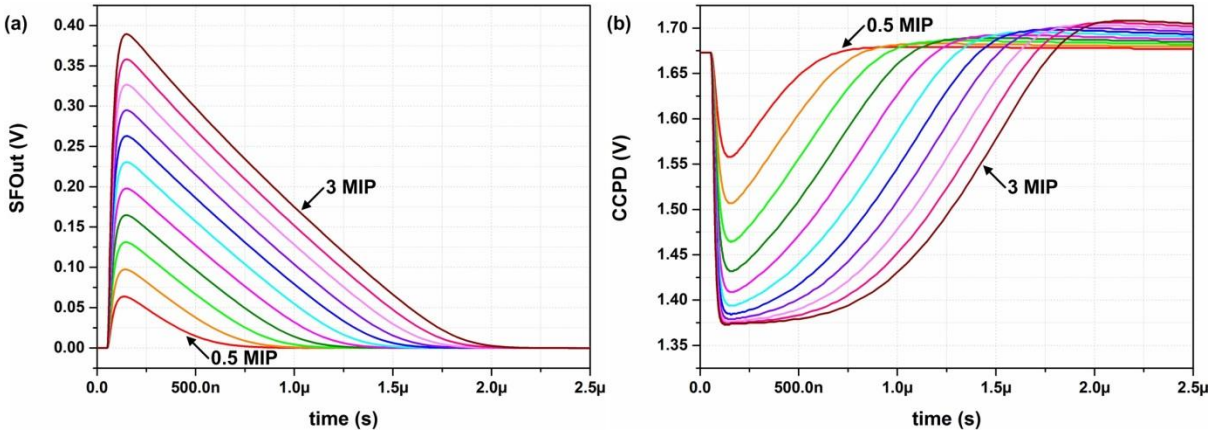

Fig. 24 Transient post-layout simulation of nodes (a) SFOut and (b) CCPD in the analog pixel without the extra DPTUB and high gain. The input energy ranges from 0.5 MIP (750 e^-) to 3 MIP (4500 e^-).

8. Standalone CMOS matrix

Property	Value
Number of pixels	16 rows x 300 columns of pixels
Type of pixels	- 1 pixel type

Table XXVII Main features of the standalone CMOS matrix.

8.1. Pixel schematic

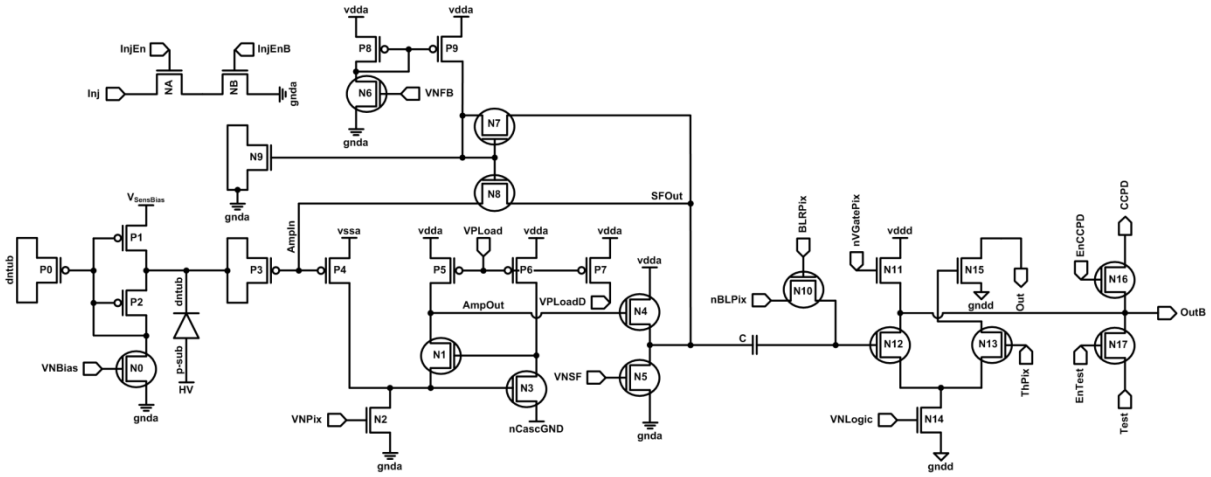

Fig. 25 Schematic of one pixel (without comparator) from the standalone CMOS matrix.

Component	Value	Component	Value
P0	(3.9/3.65)	**N0**	(6/1)
P1	(1/3)	**N1**	(4.9/0.35)
P2	(1/3)	**N2**	(2/3)
P3	(10.6/12.2)	**N3**	(5/0.4)
P4	(40/0.4)	**N4**	(5/0.4)
P5- P6-P7	(0.7/3)	**N5**	(6/1)
P8-P9	(0.7/3)	**N6**	(6/1)
		N7- N8	(5/0.4)
C	80.66 fF	**N9**	(4.7/3.8)
		N10	(5/0.4)
dntub_1	107.1 µm x 30 µm	**N11**	(1/8.9)
dntub_2	36.9 µm x 30 µm	**N12-N13**	(6/1)
dntub_3	46 µm x 30 µm	**N14**	(1.85/3.8)
dptub_1	64.3 µm x 16.65 µm	**N15**	(0.9/3.9)
		N16-N17	(5/0.4)
		NA-NB	(1/0.4)

Table XXVIII Values of components of one pixel (without comparator) from the standalone CMOS matrix.

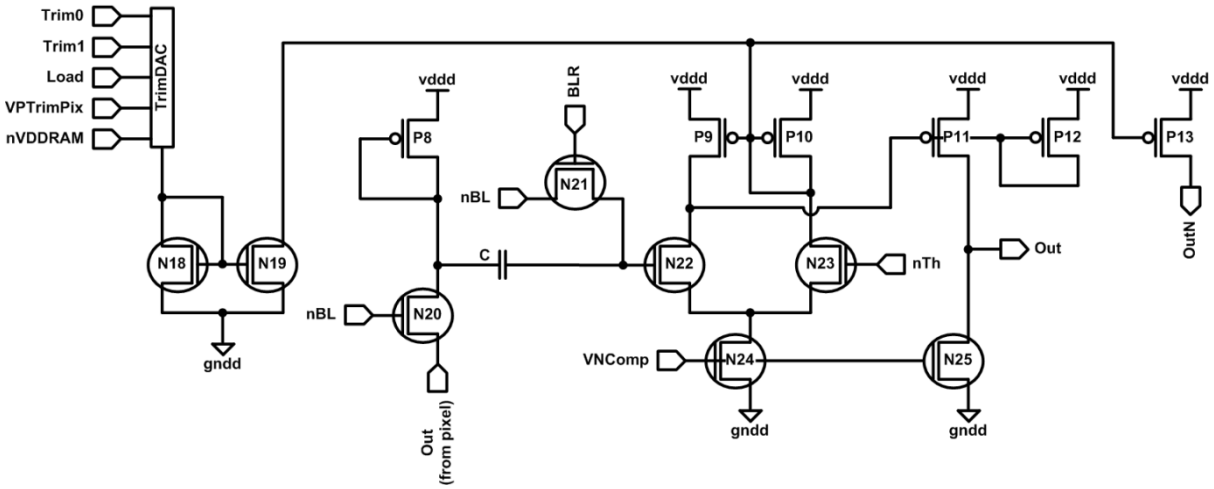

Fig. 26 Schematic of the CMOS comparator. It is included in the standalone readout digital part, and not in the pixel area.

Component	Value	Component	Value
P8	(1/0.5)	**N18**	(5/0.4)
P9	(1.6/2)	**N19**	(5/0.4)
P10	(1.6/2)	**N20**	(6/1)
P11	(1.6/2)	**N21**	(5/0.4)
P12	(0.7/0.8)	**N22**	(6/1)
P13	(1.6/2)	**N23**	(6/1)
		N24	(6/1)
C	137.13 fF	**N25**	(6/1)

Table XXIX Values of components from the CMOS comparator.

8.2. Pixel power, input and configuration signals

Power name	Value	Input name	Value	Output name	Value
nCascGND	0.4 V	**nBLPix**	1.5 V	**BLRes**	1
gnda	0 V	**BLRPix**	Bias block	**BLResDig**	1
gndd	0 V	**EnCCPD**	vdda	**NAmp**	30
HV	< - 50 V	**EnTest**	gnda	**NBiasRes**	1
vdda	3.3 V	**Inj**	--	**NcompDig**	30
vddd	3.3 V	**InjEn**	vdda	**NDelDig**	10
vssa	2.0 V	**InjEnB**	gnda	**NFB**	5
VSensBias	3.3 V	**nVGatePix**	3.3 V	**NFoll**	50
		VNPix	Bias block	**NLogic**	40
		VNBias	Bias block	**NTrim1**	10
		VNFB	Bias block	**NTw**	15
		VNLogic	Bias block	**NTwDown**	30
		VNSF	Bias block	**PDelDig**	10
		VPLoad	Bias block	**PLoad**	10
		VPLoadD	VPLoad	**PTrimDig**	10
		Test	3.3 V	**thr**	32m
		ThPix	BL	**VPAB**	10

Table XXX Values of power and input/output signals of the standalone pixels with simple CMOS comparator.

8.3. Pixel layout

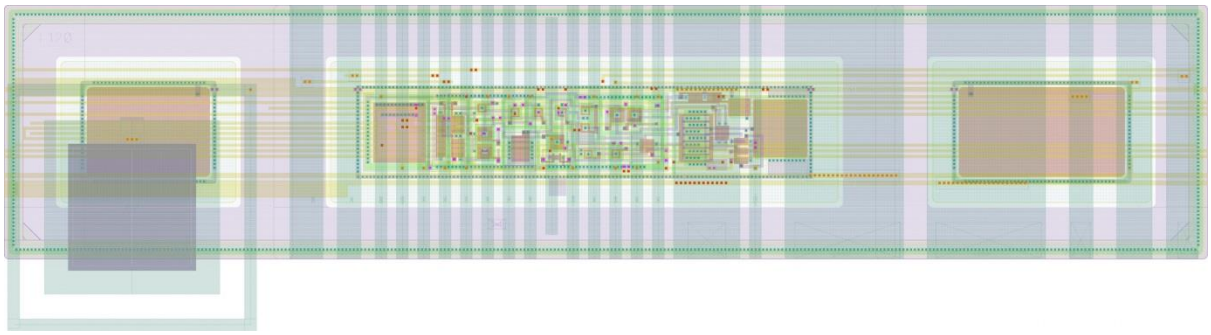

Fig. 27 Layout of one pixel from the standalone CMOS matrix.

9. Standalone readout digital block

The H35DEMO chip includes two standalone matrices, nMOS and CMOS. The size of these matrices, the pixel geometry, the number of pixels and how are read out are the same for both of them. The differences are on the pixel electronics. This section describes first the standalone common circuits and operation. At the end of the section, the differences between both matrices are described.

9.1. General overview

The standalone digital circuit purpose is to generate the time stamp and address of each hit pixel of a matrix of 4800 pixels and send that information off chip. For such a purpose the circuit is divided into 4 main regions as shown in the block diagram of figure 28. These are:

- Matrix of pixels
- ReadOut Cells (ROC)
- End Of Column cells (EOC)
- Control Unit (CU)

A standalone matrix includes two pixel matrices of 16 rows per 300 columns each, Left (L) matrix and Right (R) matrix. The analog output of each pixel is connected to a ROC cell. The purpose of this cell is to detect if there is a hit or not in a bunch crossing. A discriminator inside the cell checks if the analog output of the pixel is above a threshold voltage. In case of hit, the time stamp is stored into an 8 bits RAM memory. The address of the ROC cell is stored into an 8 bit ROM memory. The ROC cell at the bottom of the column has the lower address. The ROC cells are arranged in columns of 40 cells forming two groups of 60 columns. One is connected to the L matrix and the other one to the R matrix. Each readout column is connected to 2.5 columns of pixels.

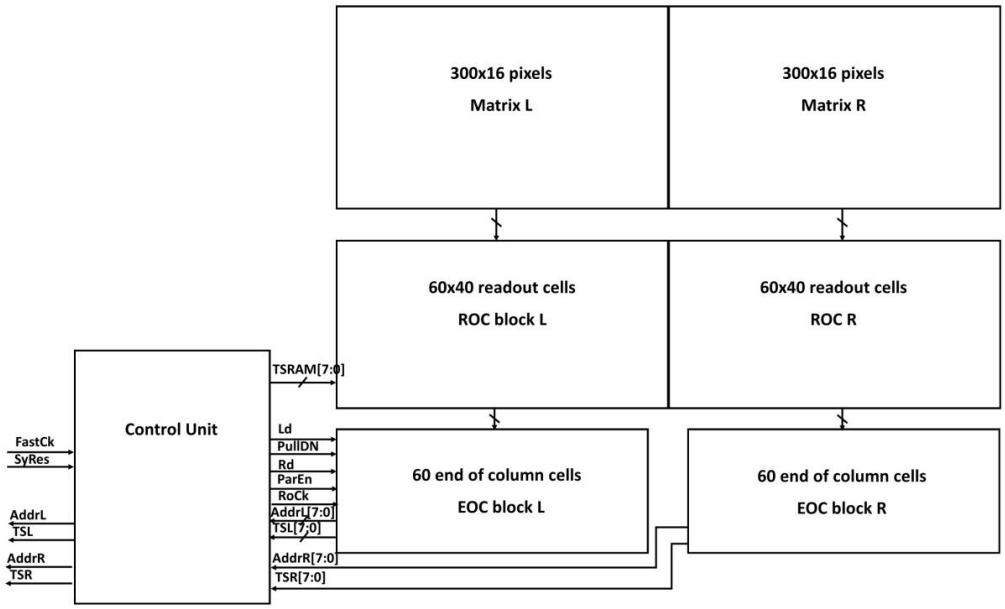

Fig. 28 Block diagram of a standalone matrix.

Every ROC in a column is connected to a time stamp and address bus. It includes a priority AND-OR circuit in order to avoid conflicts when accessing to the buses so that only one of the cells in a column

can access the bus at a time. The hit cell with the largest address has the largest priority so columns are read out from top to bottom. The address and time stamp bus of each column goes to an end of column cell. Its function is to sample the address and time stamp and then to pass those values in parallel to the next EOC cell. The EOC cells are connected in series forming two large 16 bits parallel shift register of 60 cells each. Data moves from the right to the left. Every clock cycle, each register sends a time stamp and address in parallel to the control unit, which samples and serializes those values. Data are transmitted with a clock 8 times faster than the clock of the registers.

9.1.1. Standalone matrices differences

The main difference between the nMOS and CMOS matrices are the pixel electronics. The pixels of the nMOS matrix are divided into two categories. Pixels from columns 0 to 149 include a CSA plus an nMOS discriminator. The threshold voltage is set with the global signal ThPix. Pixels from columns 150 up to 299 include a CSA plus an nMOS discriminator with time-walk compensation. In this case 2 threshold voltages are need, ThPix and ThTwPix (see figures 11, 12 and 13). The threshold level of the ROC discriminators is set with the global signal Th. The pixels of the CMOS matrix include a CSA and a second amplifier instead of a discriminator. But in this case there is a difference in the ROC cells. The ROC of matrix R includes 2 discriminators instead of 1. The threshold voltage is fixed with Th and ThTw. The name of the second threshold voltage, ThTw, is confusing. During the design of the chip, the same name in the nMOS matrix was reused for the CMOS matrix but it does not mean that the CMOS pixels have an nMOS discriminator with time-walk compensation in the pixel.

9.2. Operation

The control unit is responsible for generating the global time stamp, handling the EOC and ROC cells and transmitting the time stamp and address of each hit pixel. There is a specific circuit for each feature as shown in the block diagram of figure 29. All blocks are synchronous and operate with an external clock FastCk or with an internal one, RoCk, generated by the external clock with a clock divider. The RoCk is 8 times slower than the FastCk. The control unit has a clock tree so FastCk has a latency. Hence, all circuits operate with a delayed clock FastCkInt.

The control unit generates a global 8 bits gray encoded time stamp TSRAM. It can be configured to operate at a quarter of the FastCk frequency or at an eighth of FastCk through the 4th bit of the configuration register ConfigBit[3]. The time stamp can also by divided in two time stamps of 4 bits each. For that, the 7th bit of the configuration register, ConfigBit[6], is used. This option is only used by the CMOS matrix with two discriminators. In this matrix it is necessary to store two time stamps of 4 bits, one for each discriminator.

The synchronous logic block generates a sequence of control signals to read out the data stored in the readout cells: Ld, PullDN, Rd and ParEn. This sequence is shown in figure 30. Note that the sequence lasts 60 RoCk clock cycles, that is, the length of one of the shift registers. During the sequence 4 events occur. First, the hit of the pixel with higher priority is validated (Ld asserted). Then, the address and time stamp of each hit pixel in a column are prepared to be stored in the corresponding EOC (PullDN and Rd asserted). Finally, the addresses and time stamps are stored (ParEn asserted). During each clock cycle, data is shifted so that at the first clock of the sequence the address and time stamp of the first column are passed to the control unit. At the next clock cycle, the address and time stamp of the second column are sent to the control unit, and so on. The control sequence can be restarted with the external reset signal SyRes, which also resets the time stamp. It is active high and must be asserted during a FastCk clock cycles. SyRes goes through two flip-flops D

to avoid metastabilities[8]. The sequence starts to be generated (5+2) FastCk clock cycles after deasserting the SyRes signal.

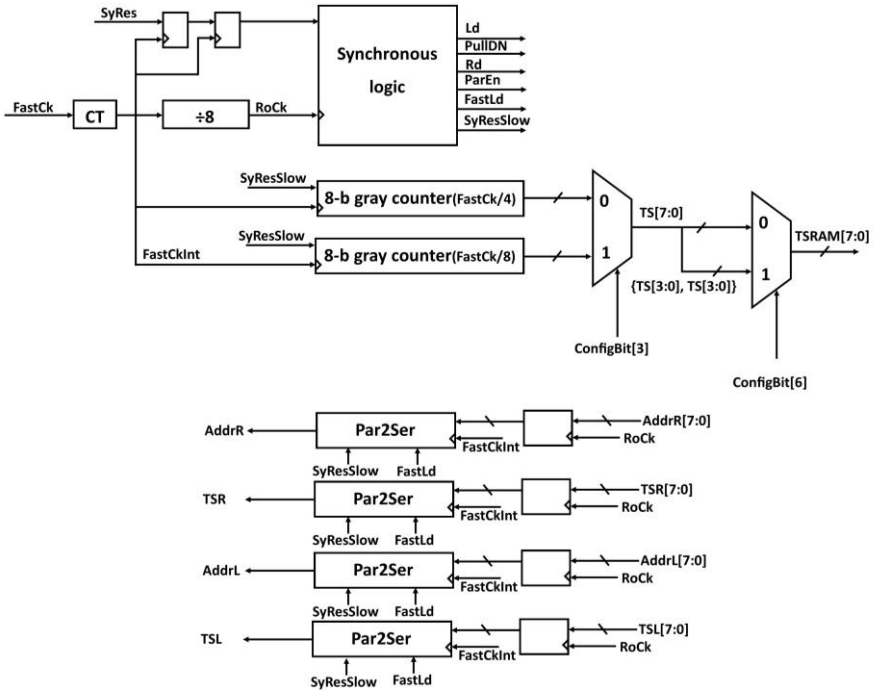

Fig. 29 Block diagram of the control unit.

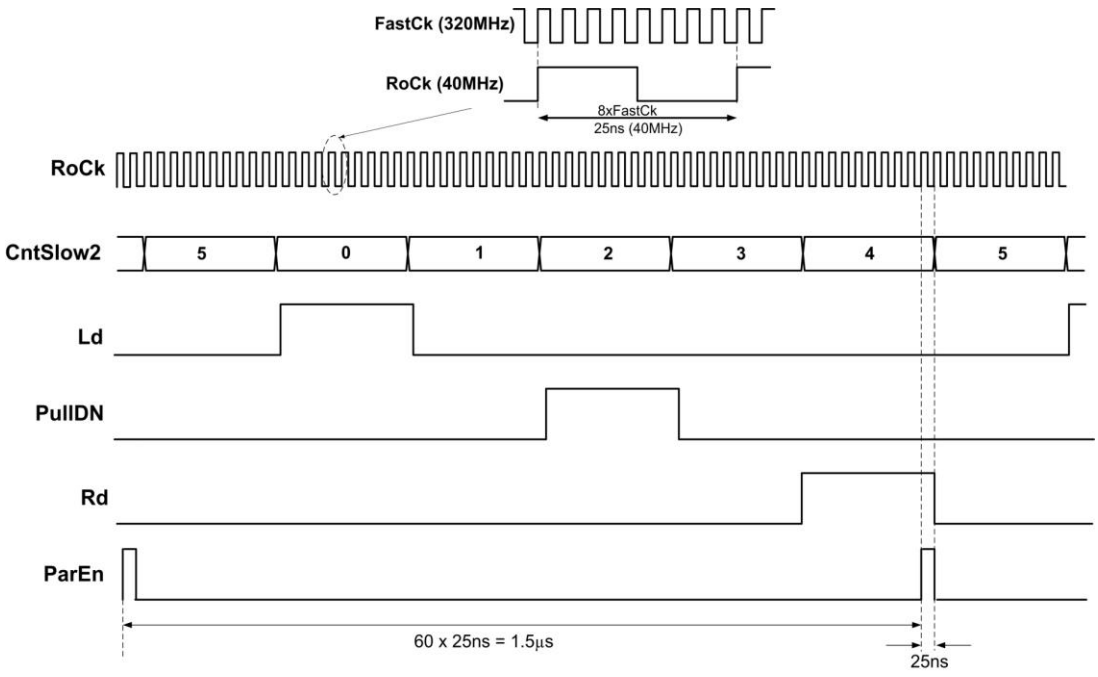

Fig. 30 Sequence of control signals to read out the data stored in the readout cells.

[8] In fact, SyRes is synchronous with FastCk and hence with the on-chip logic. Nevertheless, there is a clock tree inside the chip so there is a latency. The synchronizers were included for safety.

The control unit receives an 8 bit address and time stamp from each shift register: AddrR, TSR, AddrL and TSL. The data is first stored temporally into a register and then sent to a serializer. The data is transmitted in series. The process takes 8 FastCk clock cycles and then a new sample is stored and serialized.

The serializers start transmitting correct data after 421 FastCk clock after deasserting the SyRes signal. This value is correct for slow and moderate clock frequencies (< 50 MHz). For frequencies of 320 MHz, this value must be changed to 422. The internal clock tree has a latency that causes this. Note that the clock tree latency introduces a phase shift between the external clock signal and any synchronous signal generated by the H35DEMO. Therefore, it is recommended to work at low clock frequencies to avoid such issues. At higher frequencies these issues need to be taken into account.

9.3. I/O signals

The digital part standalone matrices are handled through two groups of control signals: main and auxiliary signals. The main signals are used to read data out. These are FastCk, SyRes, AddrR, TSR, AddrL and TSL. All these signals are LVDS. For simplicity, all main signals are depicted in the figures as single and not differential. The auxiliary signals are used to monitor the correct operation of the digital part of the standalone matrices and to bypass the control unit. Figure 31 shows a block diagram of the auxiliary signals and how they can be configured. The TSRAM, RoCk, Ld, PullDN, Rd and ParEn signals generated by the control unit can be probed by asserting the 5th bit of the configuration register ConfigBit[4]. These signals can be bypassed and use some externals by asserting the 3th bit of the configuration register ConfigBit[3].

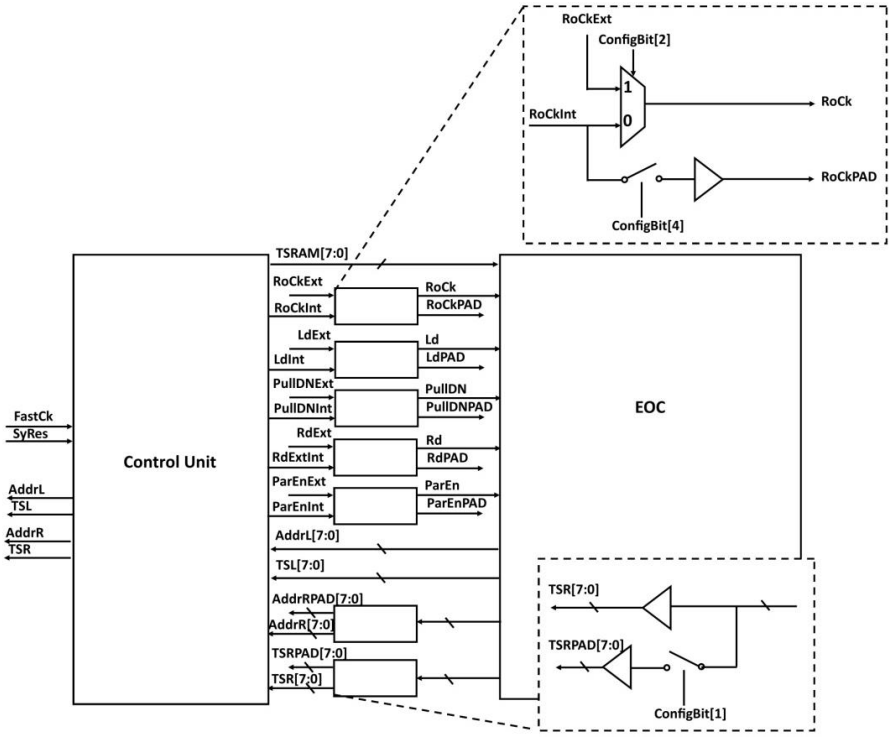

Fig. 31 Block diagram of the digital I/O signals of a standalone matrix.

10. Bias block

- The bias voltages for the current sources are generated by 17 on-chip 6-bit DACs.

- Bits DAC#(5:0) control one DAC with bit 5 connected to MSB. Each DAC register segment (7 bits) has one spare bit.

- Each DAC is written using a shift register.

- To write a DAC, the signals SIN, Ck1, Ck2 and Load are needed (see Fig. 32). After Load is issued, the content of the shift register is stored in the latches. There is one latch memory cell attached to each bit of the shift register. The outputs of the latches are connected to the circuits.

- It is also possible to implement read back. For this, an additional signal ShiftEnB is needed. This works in the analog matrices only, as ShiftEnB is connected to gnda! in the standalone matrices.

- Each matrix has its own bias block. The 4 bias blocks in the chip are identical.

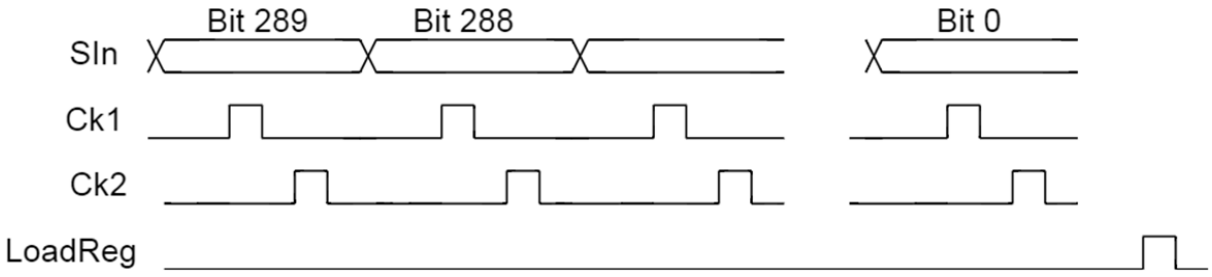

Fig. 32 Configuration writing sequence.

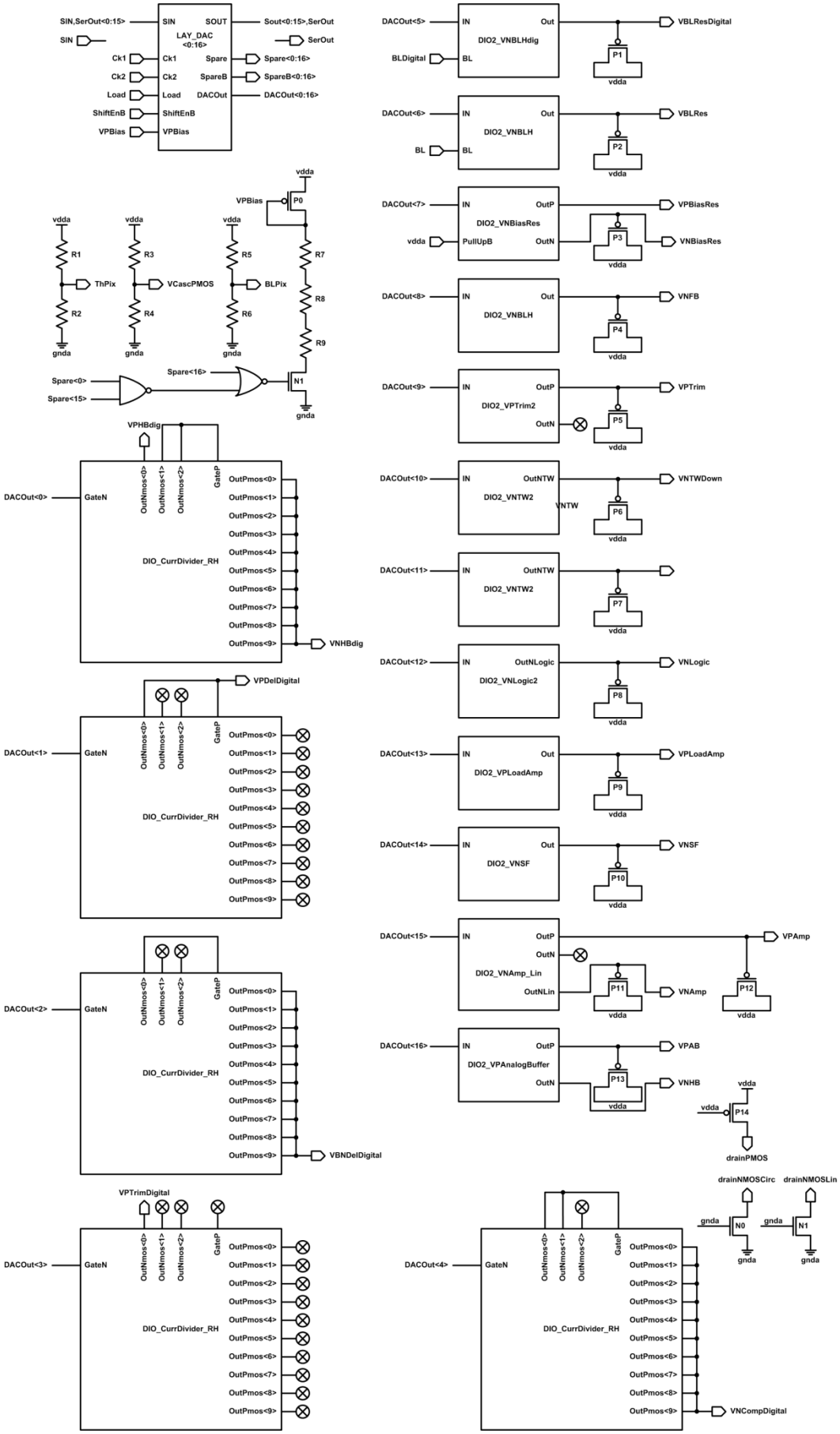

Fig. 33 Block diagram of *BiasBlock2*.

Generated by	Signal name	nMOS	ANA1	ANA2	CMOS
DACOut<0>	VNHBdig/ VPHBdig	VNHBdig/ VPHBdig	NC/ NC	NC/ NC	VNHBdig/ VPHBdig
DACOut<1>	VPDelDigital	VPDel	NC	NC	VPDel
DACOut<2>	VNDelDigital	VNDel	NC	NC	VNDel
DACOut<3>	VPTrimDigital	VPTrim	NC	NC	VPTrim
DACOut<4>	VNCompDigital	VNComp	NC	NC	VNComp
DACOut<5>	VBLResDigital	BLR	NC	NC	BLR
DACOut<6>	VBLRes	BLRpix	BLR	BLR	BLRpix
DACOut<7>	VPBiasRes/ VNBiasRes	NC/ VNBiasPix	NC/ VNBias	NC/ VNBias	NC/ VNBiasPix
DACOut<8>	VNFB	VNFBPix	VNFB	VNFB	VNFBPix
DACOut<9>	VPTrim	VPTrimPix	NC	NC	NC
DACOut<10>	VNTWDown	VNTwDownPix	NC	NC	NC
DACOut<11>	VNTW	VNTwPix	NC	NC	NC
DACOut<12>	VNLogic	VNLogicPix	VNLogic	VNLogic	VNLogicPix
DACOut<13>	VPLoadAmp	VPLoadPix	VPLoad	VPLoad	VPLoadPix
DACOut<14>	VNSF	VNSFPix	VNSF	VNSF	VNSFPix
DACOut<15>	VPAmp/ VNAmp	NC/ VNPix	VP/ NC	NC/ VN	NC/ VNPix
DACOut<16>	VPAB/ VNHB	VPABPix/ NC	VPAB/ NC	VPAB/ NC	VPABPix/ NC
--	BLPix	NC	BL	BL	NC
--	drainNMOSCirc	NC	NC	NC	NC
--	drainNMOSLin	NC	NC	NC	NC
--	drainPMOS	NC	NC	NC	NC
--	SerOut	SerOutBias	SerOutBias	SerOutBias	SerOutBias
--	Spare<0:16>	<1>=BufferEn <2>=ExtCnt <3>=SelSlowTS <4>=BufferEn <5>=EnCCPD <6>=Sel4Bits <7>=SyncGen	<5>=EnCCPD	<1>=BufferEn <2>=ExtCnt <3>=SelSlowTS <4>=BufferEn <5>=EnCCPD <6>=Sel4Bits <7>=SyncGen	<5>=EnCCPD
--	SpareB<0:16>	NC	NC	NC	NC
--	TestGate	NC	NC	NC	NC
--	ThPix	NC	Th	Th	NC
--	VCascPMOS	VCascPMOS	VCascPMOS	VCascPMOS	VCascPMOS

Table XXXI Bias signals generated by *BiasBlock2* and their name in each one of the matrices.

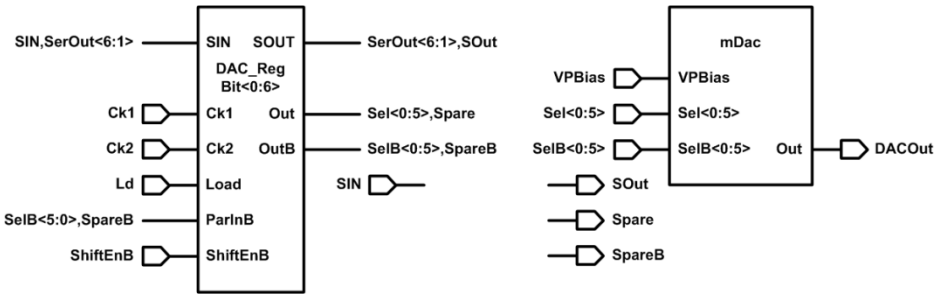

Fig. 34 Block diagram of *LAY_DAC*. In each bias block, there are seventeen *LAY_DAC* cells.

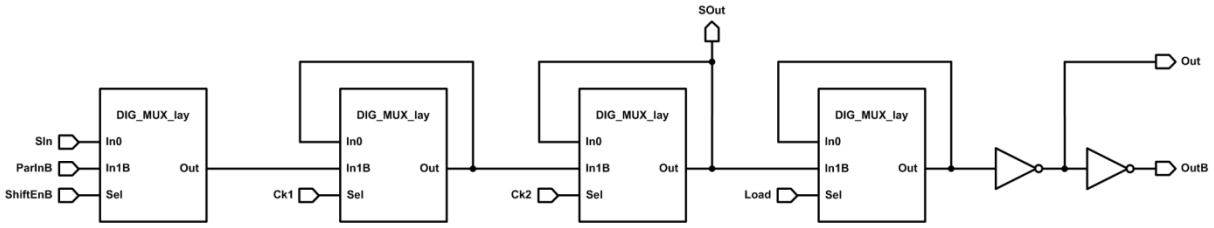

Fig. 35 Block diagram of *DAC_RegBit*.

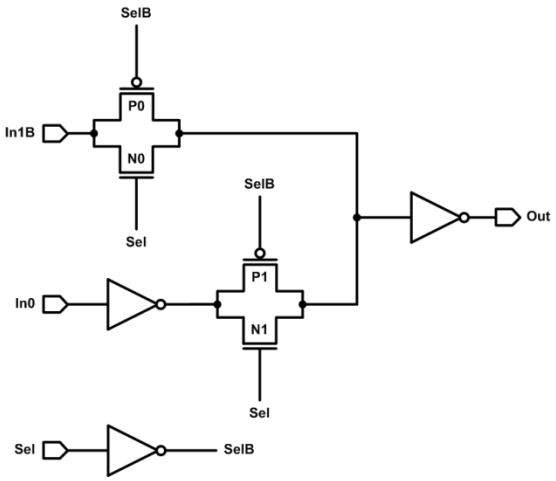

Fig. 36 Block diagram of *DIG_MUX_lay*.

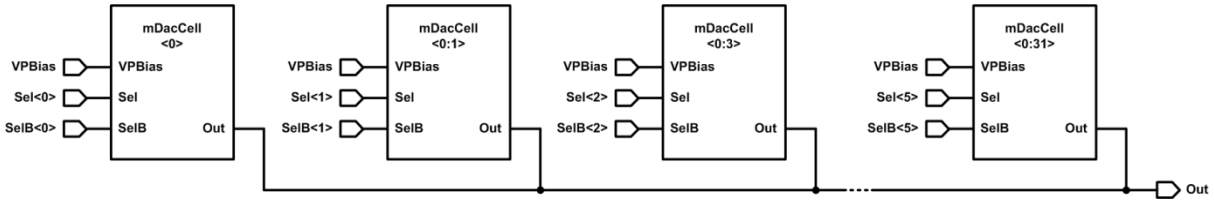

Fig. 37 Block diagram of *mDac*. In *mDac*, the first block is composed of one *mDacCell*; the second block, two *mDacCells*; the third block, four *mDacCells*; and so on until the sixth block, which is composed of thirty-two *mDacCells*.

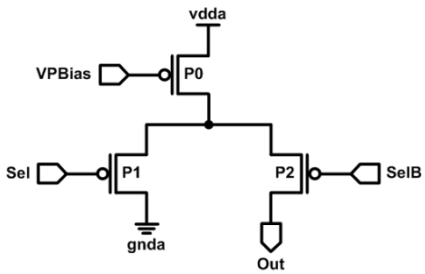

Fig. 38 Schematic of *mDacCell*.

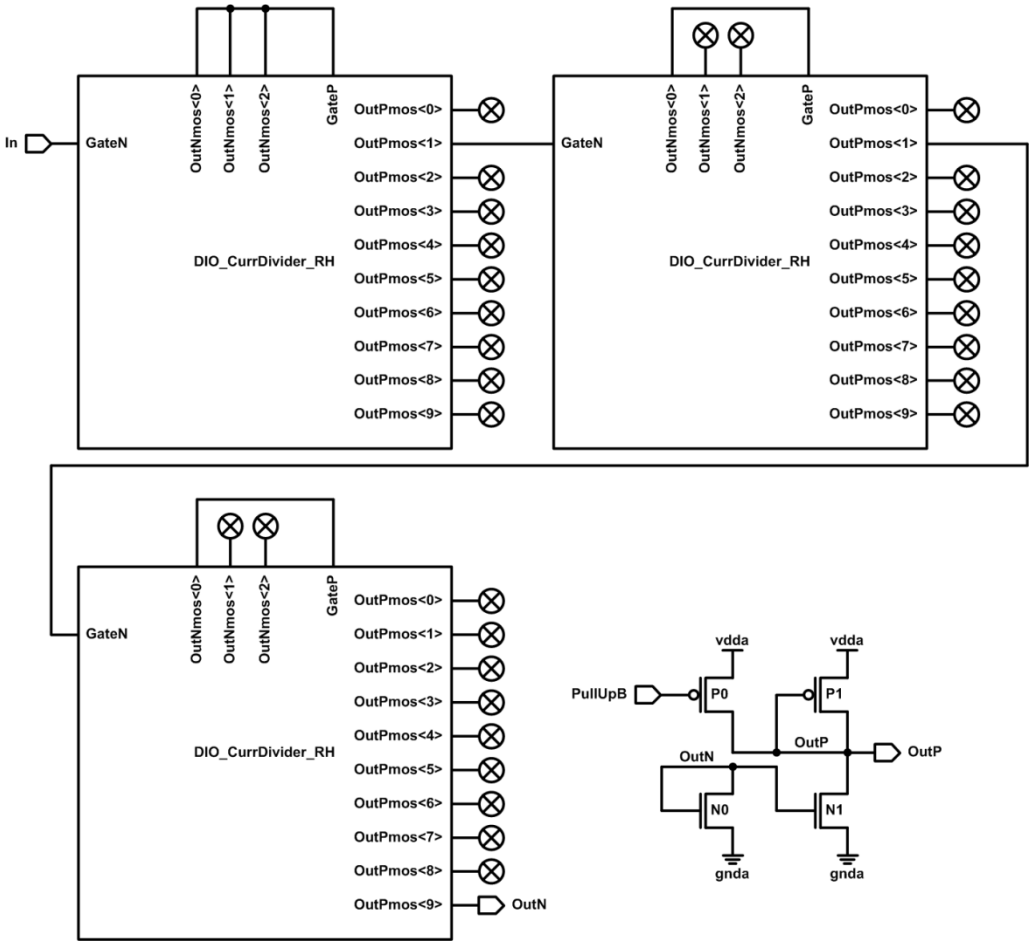

Fig. 39 Block diagram of *DIO2_VNBiasRes*. The other *DIO2_xxx* circuits present a similar scheme, but not necessarily the same.

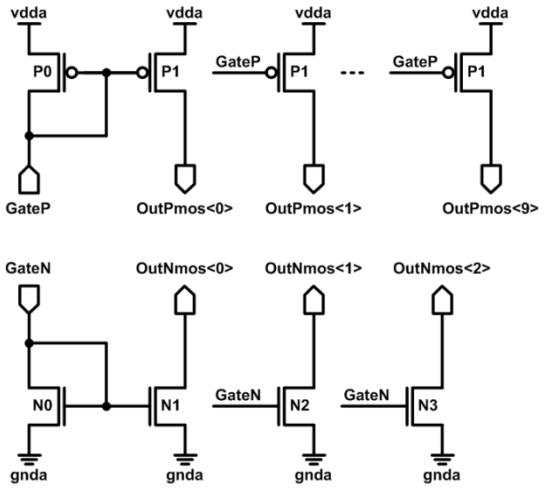

Fig. 40 Block diagram of *DIO2_CurrDivider_RH*.

- For testing purposes, some of the outputs of the bias block are connected to monitor pads through the circuit *BiasPadsSwitches*. This circuit contains one CMOS transmission gate per signal that we can monitor. It is controlled by the signals ConnBiasPads (to matrices ANA1, ANA2 and CMOS)/nConnBiasPads (to matrix nMOS) and ConnBiasPadsB (to matrices ANA1, ANA2 and CMOS)/nConnBiasPadsB (to matrix nMOS). Although the control signals to monitor the matrices ANA1, ANA2 and CMOS have the same names, there 2 different physical pads for each matrix (see table V and table X). When <ConnBiasPads,ConnBiasPadsB>=<0,1> (or when <nConnBiasPads,nConnBiasPadsB>=<0,1>), the signals BiasPAD<x> (or nBiasPAD<X>) are in high impedance. Alternatively, when <ConnBiasPads,ConnBiasPadsB>=<1,0> (or when <nConnBiasPads,nConnBiasPadsB>=<1,0>), when can monitor the signals BiasPAD<x> (or nBiasPAD<X>).

Chip output	nMOS	ANA1	ANA2	CMOS
BiasPAD<0>	VNSFPix	VNSF	VNSF	VNSFPix
BiasPAD<1>	VPLoadPix	VPLoad	VPLoad	VPLoadPix
BiasPAD<2>	VNFBPix	VNFB	VNFB	VNFBPix
BiasPAD<3>	VNBiasPix	VNBias	VNBias	VNBiasPix
BiasPAD<4>	VNPix	VP	VN	VNPix
BiasPAD<5>	BLRPix	BLR	BLR	BLRPix
BiasPAD<6>	VNLogicPix	VNLogic	VNLogic	VNLogicPix
BiasPAD<7>	VPABPix	VPAB	VPAB	VPABPix
BiasPAD<8>	noVPTrimPix	noVPTrim	noVPTrim	noVPTrimPix
BiasPAD<9>	noVNTwDownPix	noVNTwDonPix	noVNTwDonPix	noVNTwDownPix
BiasPAD<10>	noVNTwPix	noVNTwPix	noVNTwPix	noVNTwPix
BiasPAD<11>	VNDel	noVNDel	noVNDel	VNDel
BiasPAD<12>	VPDel	noVPDel	noVPDel	VPDel
BiasPAD<13>	VPTrim	noVPTrim	noVPTrim	VPTrim
BiasPAD<14>	VNComp	noVNComp	noVNComp	VNComp
BiasPAD <15>	BLR	noBLR	noBLR	BLR

Table XXXII Monitor pads with their corresponding signals from *BiasBlock2*.

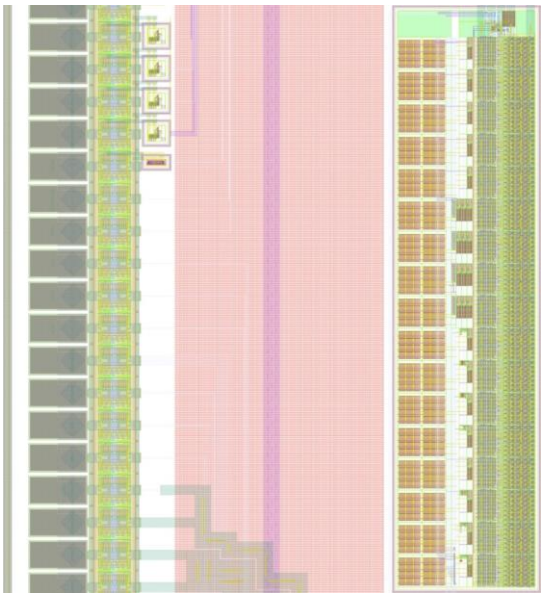

Fig. 41 Layout of the bias block with pads on the left hand side for reference.

11. Configuration registers

- The configuration register consists of the following:

  - DAC register
  - Horizontal control register
  - Vertical control register
  - Digital horizontal control register (in the standalone matrices only)

11.1. Horizontal control register

- For each pixel, 4 bits are needed. These enable:

  - Bit 1. Injection in the corresponding row.
  - Bit 2. Test measurement.
  - Bit 3. Amplifier output measurement.
  - Bit 4. To load the RAM bits in the corresponding row in the case of pixels with comparators. In analog pixels, the fourth bit is not necessary.

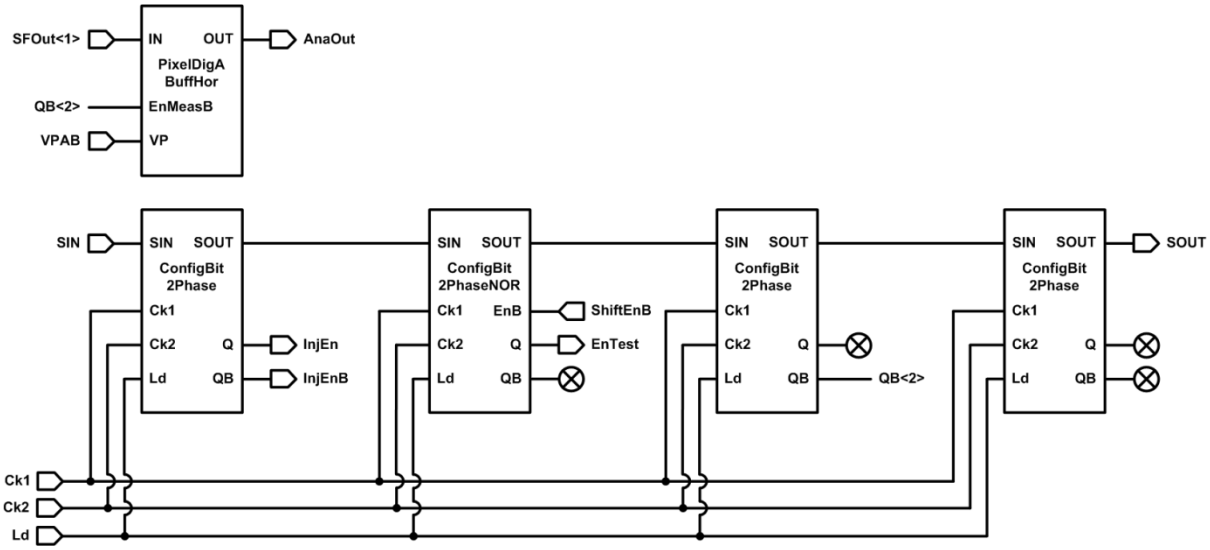

Fig. 42 Block diagram of the horizontal control circuit. In each matrix there is one of these circuits per row, i.e., HorControl<x> with 0<x<22. SIN in HorControl <0> is SerOutBias generated by the bias block. SOUT in HorControl <0> is connected to SIN in HorControl <1>, SOUT in HorControl <1> is connected to SIN in HorControl <2>, etc. SOUT in HorControl <22> is named SOUT1 and connected to SIN in the vertical control circuit.

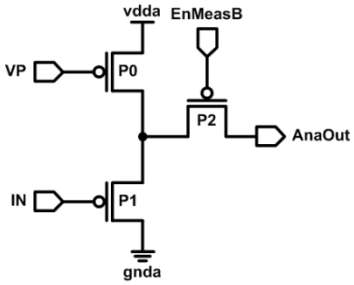

Fig. 43 Schematic of *PixelDigABuffHor*.

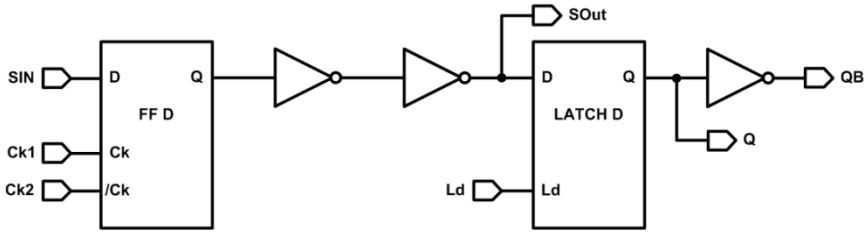

Fig. 44 Block diagram of *ConfigBit2Phase*.

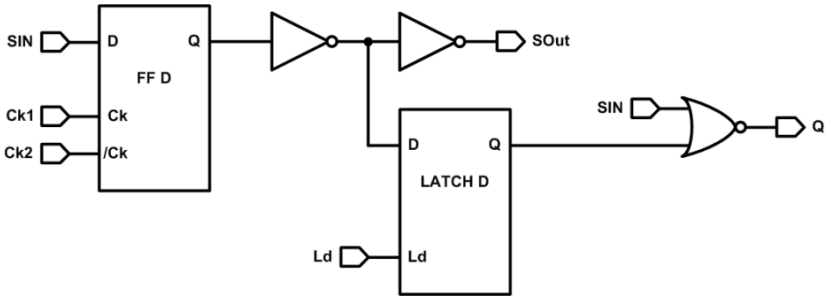

Fig. 45 Block diagram of *ConfigBit2PhaseNOR*.

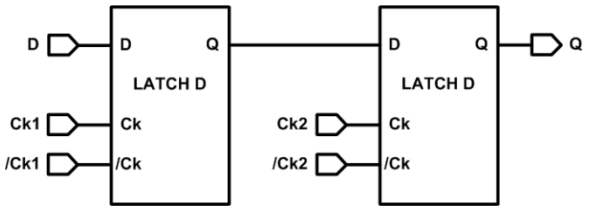

Fig. 46 Block diagram of *LATCHD*. /Ck1 and /Ck2 are generated in *LATCHD* with two inverters connected to Ck1 and Ck2, respectively.

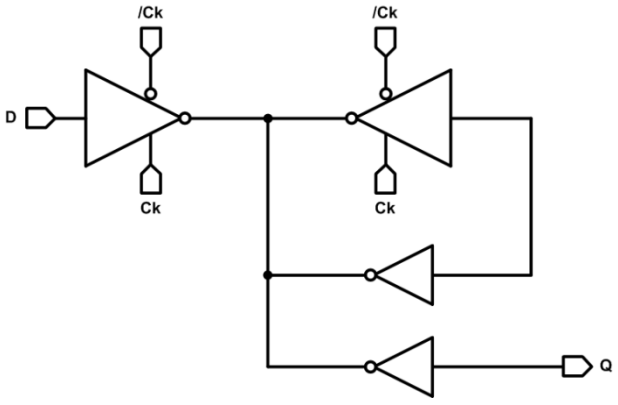

Fig. 47 Block diagram of *FFD*.

11.2. Vertical control register

- For each row, 4 bits are needed. These enable:

  - Bit 1. Calibration of the analog buffer (source follower) by connecting the injection signal (externally generated) to its input.
  - Bit 2. Connection between the analog buffer and the test line. The test line is connected to the bump bond pad by the corresponding horizontal control register.
  - Bit 3. Vertical injection line by connecting it to the externally generated injection pulse.
  - Bits 3 and 4. Writing the pixel 2-bit RAM. They are connected to RAM inputs. The RAM cell is written by issuing bit 4 in the horizontal register part.

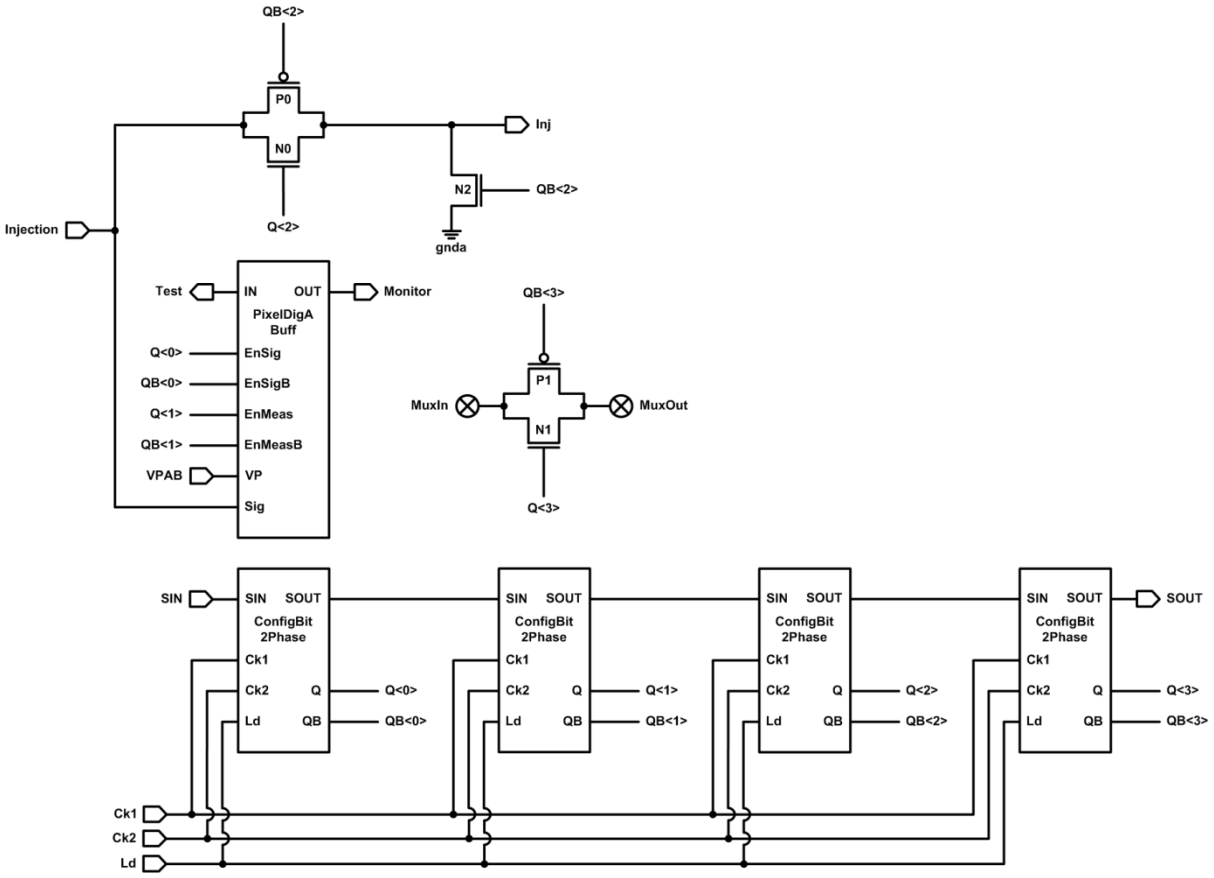

Fig. 48 Block diagram of the vertical control circuit. In each matrix there is one of these circuits per column, i.e., VerControl<x> with 0<x<299. SIN in VerControl<0> is SOUT1 from HorControl<22>; SIN<x> with 0<x<299 is SOUT1, si2<1:299>. SOUT in VerControl<299> is an output of the matrix at the ASIC level; SOUT<x> with 0<x<299 is si2<1:299>, SOUT. There are 300 signals Inj and Test. There are 100 signals Monitor<0:2>.

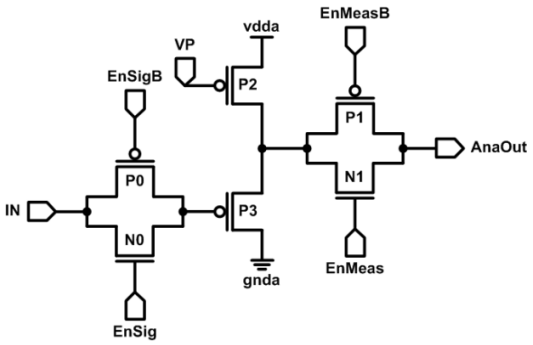

Fig. 49 Schematic of *PixelDigABuff*.

11.3. Digital horizontal control register

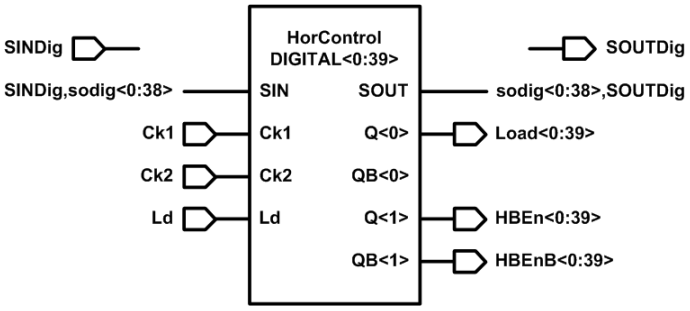

Fig. 50 Top of *HorControlDIGITAL* used to control the digital block.

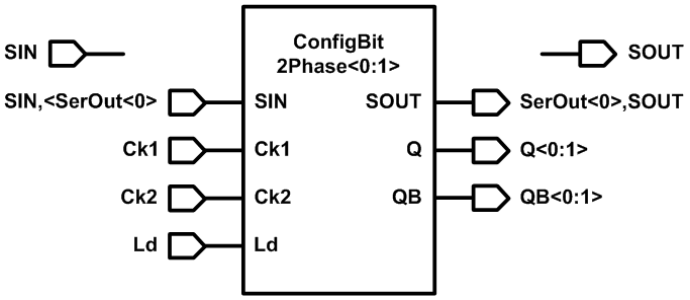

Fig. 51 Block diagram of *HorControlDIGITAL*.

12. Test structures

12.1. Circuit to measure the sensor capacitance

We have six different circuits, with the same electronics but different sensor features. From right to left, (i.e., from TS_U0 to TS_U33) these circuits are:

- *Dio_Cap_meas_NoSegmentedNoGR_PAD*. The sensor is made of one big DNTUB without DPTUB.

- *Dio_Cap_meas_SegmentedNoGR_PAD*. The sensor is made of four small DNTUBs without DPTUB between them.

- *Dio_Cap_meas_Segmented_PAD*. The sensor is made of four small DNTUBs with DPTUB between them.

- *Dio_Cap_meas_circ_nMOS_comparator_with_TW_pad_ring*. The sensor has the same features as in the pixel with an nMOS comparator and without time-walk compensation (standalone nMOS matrix).

- *Dio_Cap_meas_circ_nMOS_comparator_no_TW_pad_ring*. The sensor has the same features as in the pixel with an nMOS comparator and with time-walk compensation (standalone nMOS matrix).

- *Dio_Cap_meas_circ_nMOS _pad_ring*. The sensor has the same features as in the analog pixel in the analog matrices and the analog pixel for standalone readout in the standalone CMOS matrix. There is no additional DPTUB between the different DNTUBs that make the sensor.

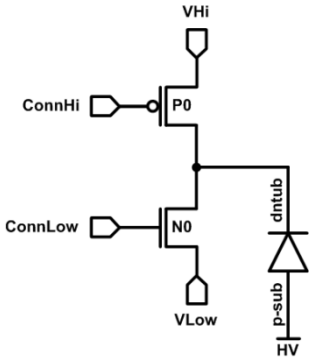

Fig. 52 Schematic of the circuit to measure the sensor capacitance. VHI is vdda! and VLow is gnda!. ConnHi and ConnLow are square voltage signals with a small delay between them. By measuring the current that flows through P0 and/or N0, we can measure the capacitance of the diode.

Component	Value	Component	Value
P0	(2/0.35)	**N0**	(5/0.4)

Table XXXIII Values of components of the test structure to measure the sensor capacitance.

Circuit	DNTUB area (μm^2)	DPTUB area (μm^2)
Dio_Cap_meas_NoSegmentedNoGR_PAD	30 x 230	0
Dio_Cap_meas_SegmentedNoGR_PAD	4 x 30 x 42.5	0
Dio_Cap_meas_Segmented_PAD	4 x 30 x 42.5	0$^{(*)}$
Dio_Cap_meas_circ_nMOS_comparator_with_TW_pad_ring	30 x 231	16.65 x 55 + 17.1 x 109
Dio_Cap_meas_circ_nMOS_comparator_no_TW_pad_ring	30 x 231	16.65 x 55 + 17.1 x 57.75
Dio_Cap_meas_circ_nMOS _pad_ring	30 x 50 + 30 x 103 + 30 x 37	16.65 x 64.55

Table XXXIV Values of components of one pixel (without comparator) from the standalone nMOS matrix.
$^{(*)}$ There's DPTUB only between the different DNTUBs that make the sensor, but only to apply the HV.

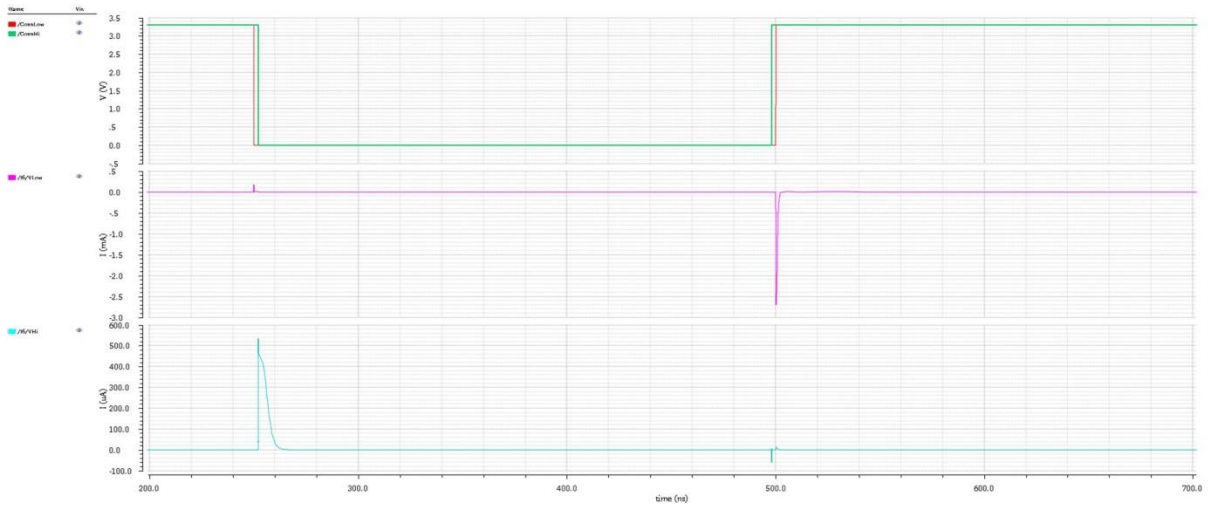

Fig. 53 Transient simulation of circuit to measure the sensor capacitance.

12.2. Circuit for fast measurements

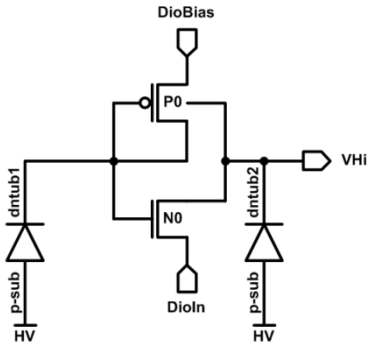

Fig. 54 Schematic of circuit for fast measurements. It is a matrix of 3 x 3 diodes and there is DPTUB between the sensors to apply the HV. DioBias is vdda!, VHi can be connected to 3.3 V and DioIn is connected to an external low value resistor (i.e., 10 Ω). The current that flows through DioIn can be as high as 100 mA (maximum). The fall time in DioIn upon particle hit/light detection should be extremely fast (< 1 ns, according to simulations).

Component	Value	Component	Value
P0	(20/0.4)	**N0**	(10/1)
		dntub1	76 µm x 176 µm
		dntub2	8 x 76 µm x 176 µm

Table XXXV Values of components of test structure for fast measurements.

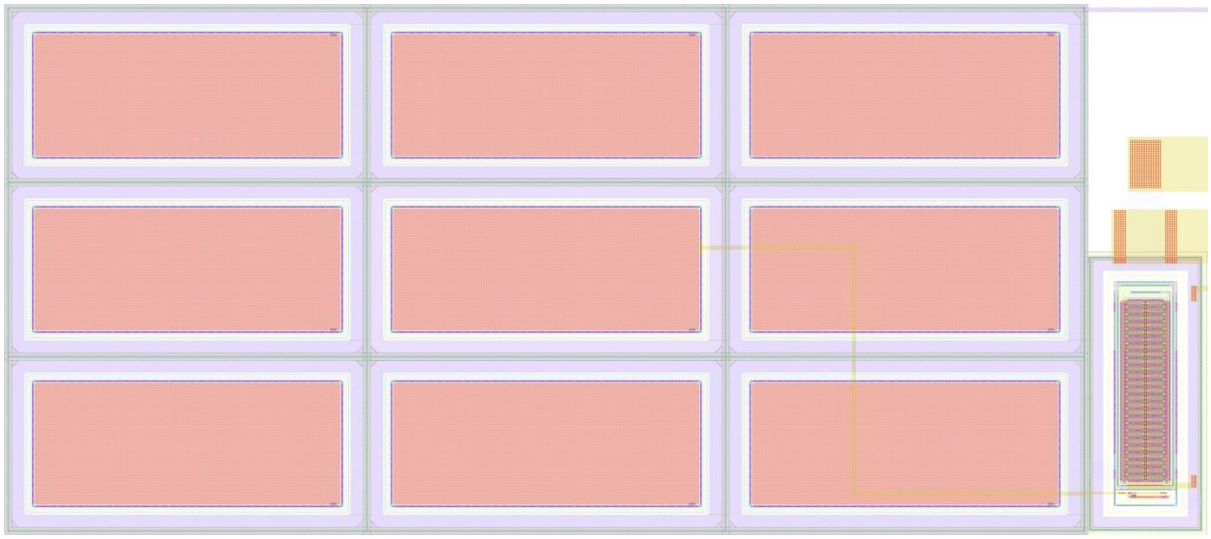

Fig. 55 Layout of circuit for fast measurements.

12.3. Circuit for sensor measurement without electronics

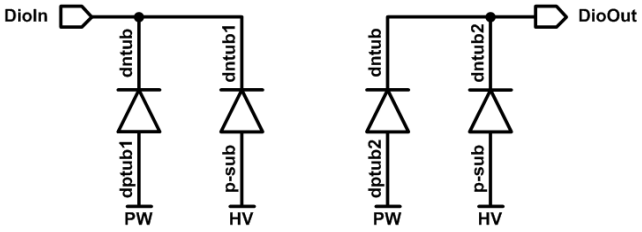

Fig. 56 Schematic of circuit for measurements without electronics. It is a matrix of 3 x 3 diodes. The diode connected to DioIn is placed at the middle of the matrix. PW is connected to gnda!, DioIn should be connected to 3.3 V and DioOut is the output of the circuit.

Component	Value
dptub1	16.65 µm x 53.3 µm
dntub1	30 µm x 90 µm + 2 x 30 µm x 50 µm
dptub2	8 x 16.65 µm x 53.3 µm
dntub2	8 x 30 µm x 90 µm + 16 x 30 µm x 50 µm

Table XXXVI Values of components of test structure without electronics.

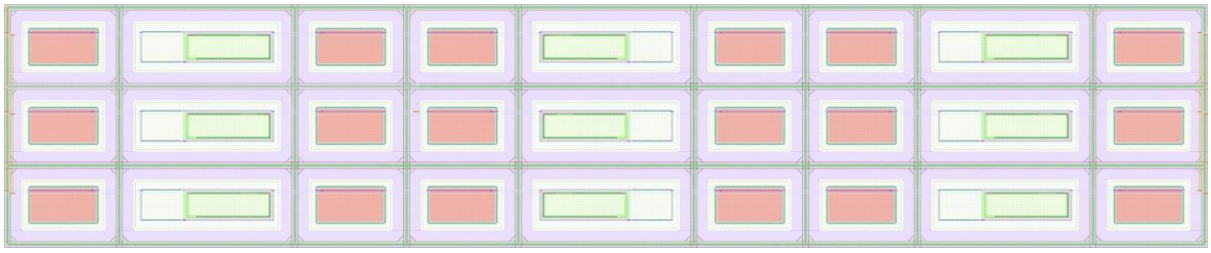

Fig. 57 Layout of circuit for measurements without electronics.