Recommendations for the Design of Layer 00

1 Introduction

This document is a summary of our studies to date and presents our conclusions on design features of Layer 00. The document is in five sections. This introduction is the first section. In the second section, the expected performance of an 8-fold detector is compared to that of a 12-fold detector. In the third section, a possible 12-fold design is described which we believe to be feasible, as demonstrated by the full-scale mock-up we have built. In the fourth section, we highlight some other issues which are of importance to the design of Layer 00. A summary is presented in the fifth section.

2 Comparison of 8-fold and 12-fold design

The modularity of the detector is an issue which must be resolved soon so that the overall design, cable layouts, hybrid design and cooling can be completed. The general rule which we derived previously [1] is that the modularity should be as high as possible and the pitch as small as possible. Because each readout chip has 128 channels, and the total number of chips should be about 100, there are two [1] principal designs:

- 8-fold modularity with $\approx 50\mu$m pitch;
- 12-fold modularity with $\approx 70\mu$m pitch.

We note that the 12-fold design matches the modularity of SVXII. The impact of each of these designs on the physics has been presented in a number of previous reports. [1, 2, 3, 4, 5] Our studies of the detector performance are discussed in the following subsections: Resolution; Two-track Resolution; Trigger Efficiency; and Alignment.

2.1 Resolution

2.1.1 Our simulation

We have written a realistic simulation of a silicon detector in order to calculate the intrinsic resolution as a function of crossing angle, intermediary strip, signal to noise, and strip pitch.

[1] Two further designs should also be mentioned: A 16-fold modularity with $\approx 50\mu$m pitch and a 12-fold wide/narrow design with $\approx 50\mu$m pitch. This document does not address these designs; our impression is that the mechanical construction of either of these is too difficult, particularly with respect to hybrid placement.

Our results are contained in [5] and have been presented and discussed at a number of video-conferences.

Some doubts were raised as to the reliability of the simulation, due to the fact that the resolutions predicted did not agree well with results from CDF RunI data. We have addressed this point by comparing our results to a number of published papers on test-beam data. We believe that this is the best way to address the question, as test-beam data is relativity free of extraneous effects such as conversions and mis-alignments.

- In Figure 1 we compare our results to n-strip detectors with 100μm pitch, no intermediary strip, and a signal-to-noise of 27:1 [6].
- In Figure 2 we compare our results to n-strip detectors with 50μm pitch, no intermediary strips, and a signal-to-noise of 12:1 [7]
- In Figure 2 we compare our results to n-strip detectors with 100μm pitch, no intermediary strips, and a signal-to-noise of 12:1 [7]
- In Figure 3 we compare our results to ATLAS prototype p-strip detectors with 50μm pitch, no intermediary strips, and a binary threshold set at 1fC, corresponding to S/N of 4:1. [8]
- In Figure 3 we compare our results to ATLAS prototype p-strip detectors with 100μm pitch, with an intermediary strip, and a binary threshold set at 1fC, corresponding to S/N of 4:1. [8]
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In all cases, the agreement is good and the trend of the resolution as a function of angle is established. We therefore conclude that our simulation reflects the intrinsic resolution that one would expect from the Layer00 detector. Not having analysed the CDF RunI data, we are not in a position to explain the disagreement of this data with our simulation, except to comment that our simulation also disagrees with data taken by another running experiment, namely DELPHI. Our agreement with test-beam data and our disagreement with running experiments, suggests a further contribution which is not linked to the intrinsic performance of the silicon. Possible causes may be conversions in other materials apart from the silicon plaquettes, or alignment effects. We return to this point in section 2.4.

The large point precision in the CDF data is unlikely to be due to delta-rays produced in the silicon. Figure 4a shows the charge deposited in each layer of the DELPHI micro-vertex detector during the 1992 running period. It can be seen that the right-hand tails contribute no more than about 5% of the data. Furthermore, the effect on resolution has been examined by plotting the intrinsic resolution as a function of deposited charge in the silicon. Figure 4b shows that as expected the best resolution is obtained at, and just above the peak of the Landau. For very low and very high charge deposits, the resolution degrades by up to a factor of two. Note however that very little data is in these regions as witnessed by the large error bars.

2.1.2 Results on Resolution from our Simulation

We return now to the results on the resolution of Layer00 obtained from our simulation. A few plots are sufficient to summarise the situation.

Figure 5 shows the resolution as a function of crossing angles, with and without intermediary strips for detectors with signal-to-noise of 10:1.

Figure 6 compares an 8-fold 50μm pitch detector without intermediary strip, with a 12-fold 70μm pitch [2] detector with variable intermediary strip, and shows the fraction of tracks as a function of resolution. The 12-fold response is uniform. Irrespective of angle, the intrinsic resolution is about 8μm. The 8-fold design often has tracks with better resolution, but also has tracks with considerably worse resolution. 40% of the tracks would have a resolution $\geq$ 10μm, and 15% have a resolution $\geq$ 15μm. On account of the small numbers of top, Higgs and supersymmetric events which may be produced, we believe it is important for the physics to have excellent resolution throughout the acceptance of Layer00.

Figure 7 allows these point precisions to be converted to an impact parameter resolution. This plot assumes 8.5μm point precision in the SVXII and 32μm point precision in ISL. At very high momenta, a point precision of 5μm rather than 8μm in Layer00 means that the IP resolution improves from 8μm to 6μm, while for tracks with a p_T of 1GeV, the IP resolution improves from 24μm to 20μm.

From these studies we conclude as in [1]:

- It is extremely beneficial to use an intermediary readout strip at small angles ($< 7^o$);
- It is better *not* to use an intermediary strip at larger angles, especially if we have poor signal-to-noise;
- For large angles ($> 15^o$), the resolution is independent of readout pitch;
- For large angles ($> 15^o$), the resolution is poor ($> 10\mu$m). For this reason, unless there are overwhelming mechanical reasons, we would advise against an 8-fold geometry.

[2] At one point, we presented a variable pitch design for the 12-fold detector, which gave better resolution at small crossing angles. We do not yet understand why this is so very difficult for the trigger, and wish to investigate this option further at some future time.

2.2 Two track resolution

Because much of the interesting physics will occur in tightly collimated jets, it is important to be able to distinguish between clusters coming from nearby tracks. We have defined a mis-measured track as one whose charge deposits in the silicon overlap with the deposits of another track. We have already shown in [1, 2, 3, 4] that the mis-measurement rate for b-tracks coming from top decays is quite high, at about 30%. The situation gets worse as the crossing angle increases. Lowering the strip pitch makes the situation better for small crossing angles, but has no effect at large crossing angles where the charge is deposited over many strips. Comparing the 8-fold with the 12-fold, the 8-fold design is better at small angles, but worse at large angles as shown in Figure 8. The two effects are roughly of the same size, so that the average mis-measurement is the same in both designs.

2.3 Efficiency

A further consideration is the efficiency for reconstructing clusters, which is especially important if Layer 00 were to be used in the trigger. This only becomes important if we have to operate at poor signal-to-noise ratios (see section 4.1).

For a signal-to-noise of 10:1, both 8-fold and 12-fold designs are $> 99\%$ efficient with a 3:1 threshold. However if the signal-to-noise is 7:1, the efficiency of the 8-fold design would deteriorate to 87% while the 12-fold design would remain higher than 99%.

If it was necessary to run with a single strip threshold of 4:1, then the efficiency for the 8-fold deteriorates to 60% while for 12-fold it would be 94%.

2.4 Radial Alignment

The issue of the radial alignment of the detectors is important since for tracks which cross the detector at an angle of θ, a mis-alignment of δR in the R co-ordinate translates into a transverse alignment error of $\delta R \tan\theta$. Furthermore, it may be very difficult to obtain δR to better than 30μm or so. This was the experience in DELPHI [9] where various mechanical effects such as bowing of the detectors, or charge collection effects such as barycentric shifts, meant that the R co-ordinate was only known to this order.

This may be a contributing factor to the disagreement of the resolution of CDF data with our simulation. It is certainly the case if we compare our model to DELPHI data (see Figure 9) Despite the fact that our model agrees well with large crossing angles from test-beam data, it does not describe DELPHI data at large crossing angles. Clearly some other affect is at work. If we assume it is due to a mis-alignment in the R co-ordinate at the level of 30μm, then this gives a transverse misalignment of $30\tan\theta$. Adding this in quadrature to the intrinsic resolution, we can fit the DELPHI data well as is shown in Figure 9.

There are implications from this for Layer 00. Assuming a mis-alignment of 30μm in R, an 8-fold detector would have a transverse misalignment of 12.4μm at large angles, while for a 12-fold detector, a transverse misalignment of 8μm would be found. This is another reason to favour a detector with smaller crossing angles.

2.5 Conclusions from simulation

Our conclusions from our simulations are:

- Better and more uniform intrinsic precision is obtained with the 12-fold rather than the 8-fold design;
- The two-track separations are similar for both designs;
- The trigger efficiency is better for 12-fold, and the modularity better matches SVXII;
- Radial misalignment will affect a 12-fold design less than they will an 8-fold design.

We therefore conclude that a 12-fold design is to be preferred in terms of physics output.

3 Construction

Based on our studies, we have proceeded to make mechanical designs of our preferred solution: a 12-fold detector. We note two general points in our comparison with 8-fold.

- Because a 12-fold polygon of given radius has a smaller circumference than an 8-fold polygon, any 8-fold design which fits around the beam-pipe can be transformed into a 12-fold design which will fit, and with greater clearance. For example, a 12-fold design can be generated from the 8-fold design, if the inner silicon radius is fixed at 13.35mm and the gap between the inner silicon layer radius and the outer silicon layer radius is fixed at 0.94mm. In this case, the gap between the outer layer and SVXII (at a diameter of 39.5mm) is increased from 0.62mm in the 8-fold scheme to 1.85mm in the 12-fold scheme.

  Alternatively, holding the gap between SVXII (at a diameter of 41mm) and the outer layer fixed at 1.88mm, and the gap between outer and inner layers fixed at 0.94mm, Figure 10 shows that the gap between the beam-pipe and the inner layer radius can be increased from .72mm to 1.89mm. Space considerations therefore also favour 12-fold.
- To a large extent the designs are driven by the size of the hybrids. The 8-fold design manages to put 8 hybrids around the beam-pipe. Because there are 25% less channels in the 12-fold design, only 6 hybrids now need to be placed around the beam-pipe. This eases the construction, freeing up more space.

3.1 Our favoured design

Our design uses silicon sensors with 128 readout lines at 70μm pitch. The central 64 channels have an intermediary strip; the outer 64 do not. Two sensors are bonded head-to-tail to produce a 15cm module. Six modules together form a ladder which extends from -45cm to 45cm in the z co-ordinate. 12 ladders are placed around the beam-pipe in a castellated design which provides an overlap of 5 readout lines between ladders. The ladders are readout at each end; each set of three modules in $\pm z$ are connected to one hybrid which consists of a master plus two slaves. In total, 12 hybrids are required to readout each side of the detector. These are placed in two rings of six hybrids which encircle the beam-pipe. One ring is placed on the 'narrow' section of the beam-pipe, and one on the 'wide'. Every alternate ladder has cables connecting to the nearer set of hybrids, while the remaining ladders connect to the far set. One ring is rotated by $2\pi/12$ with respect to the other which ensures that all cables run straight from the silicon to the hybrids without any problematic dog-legs or bending. Two cables are used to readout each module. This allows the signal wires to be fanned out to double the strip pitch along the length of the cable, thus reducing the capacitance. The cable layout and hybrid positions is shown schematically in Figure 11.

The $R\phi$ view of our favoured 12-fold design is shown in Figure 14. We have assumed that the silicon sensors are 300μm thick, the cables are 25μm thick, spacers between the cables are 100μm thick, bondwires are 250μm thick, the beam-pipe has a radius of 1.262cm and the SVXII inner wall is at 1.975cm.

The silicon sensors are placed alternatively at radii of 1.44cm and 1.662cm. The support structure is 0.47mm wide at its narrowest point. The gap between the sensors on the inner ring with their cables on top, and the modules on the outer ring is .5mm. The gap between the sensors on the outer ring and SVXII is 1.25mm. For the cooling we have used 12 equally spaced tubes with a diameter of 1.6cm.

3.2 Mechanical Mock-Up

We have constructed a mechanical mock-up of a 12-fold design which firstly, gives us an indication of scale, secondly, has given us insight into the construction problems we will face, thirdly, allows us to check all clearances, and fourthly, allows us to test the installation.

The design of the mock-up is very similar to our favoured 12-fold design described above. The main difference is that the cooling tubes in the mock-up are placed at the centre of the silicon modules, rather than at the edges. (The design which has cooling tubes at the edges, provides even more clearance than in the mock-up, which itself looks eminently buildable.) The mechanical drawing of the mock-up is shown in Figure 12. A comparison of the dimensions and clearances of the Fermilab 8-fold, our favoured 12-fold, and the mock-up are given in Table 1.

The beam-pipe has been constructed from a cylinder of aluminium and is mounted on a solid aluminium base-plate. Rails are mounted on the base plate on which can slide a cylinder of the same inner radius as the inner wall of SVXII. The support structure of Layer00 is simulated by a series of aluminium clam-shells, two of which encircle the beam-pipe. Holes are drilled in the clam-shells through which cooling pipes, simulated by 1.6cm thick wire, are passed. We foresee the real detector being assembled from two continuous clam-shells which run the full length of z. All the cooling would be taken out on one end. This solution eases problems of installation with the whole detector being installed into the middle of SVXII from one end only.

The silicon modules are simulated by 300μm thick aluminium sheets cut to size with small 300μm thick pieces glued on top to simulate bondwires. The modules are placed on the supporting clam-shells. Kapton cables are glued onto the modules and run between them and the hybrids, which are cut out of a block of aluminium according to Carl's latest design. The cables are 125μm thick which simulates the thickness of the true cables with a 100μm spacer. Because the longest cable which can be manufactured is 400mm, the two longest cables in our design are split in two and joined together over a 5mm long, 300μm high support. An additional 300μm is added to the height of the cables at this point in order to simulate bond-wires.

A photograph of the mockup is shown in Figure 13, and more are available at [10] and have already been shown at meetings, but for a full appreciation we hope to be able to transport the model to Padova. We believe that this mock-up shows that a 12-fold Layer00 detector is buildable.

There are two major differences between this mockup and the real detector. They concern firstly, the support structure and secondly, the cooling. In an ideal world, we would replace our aluminium support structure with a massless one. We have not yet resolved how this is to be accomplished: presumably thin walled carbon fibre is the material of choice, but we have not yet performed the necessary studies of its rigidity or its thermal properties. We have also not finalised ideas on how to cool the modules. One solution is to place the silicon modules directly onto the cooling pipes, thus using the pipes (which must anyway be present) as a support structure. The pipes in turn would be supported on the beam-pipe at either end, outside the silicon acceptance, and reinforced with thin carbon fibre staves along the length of the beam-pipe.

We hope to be able to use the Padova workshop for discussions and ideas on possible support and cooling structures. These issues apply equally well to either 8-fold or 12-fold detectors.

4 Other Issues

We have studied a number of other issues which are important to the design of Layer00, and in this section we recapitulate our conclusions.

4.1 Signal-To-Noise

The expected signal-to-noise is an important input to the design as it affects the resolution and efficiency of the detector. In particular, the problems for tracks which cross the detector at large angles are somewhat mitigated if a very high signal-to-noise was obtainable.

The noise of the Honeywell SVX3D chip [11] after 2MRad irradiation can be expressed as $800 + 60\times$(Capacitance in pF).

We have evaluated the capacitance of cables with varying strip pitch [12], and have checked our calculations against experimental data to ensure their validity. We find that for 100μm pitch cables the capacitance is 0.33 pF/cm while for 150μm pitch, it is 0.27 pf/cm.

The capacitance of irradiated silicon has been measured by the RD20 collaboration [13] as well as for various different detectors with differing strip thickness by CMS [14]. Both collaborations obtain capacitances close to 1.2pF/cm for detectors with 50μm pitch and no intermediary strip. In particular, CMS obtain 1.2pF/cm for unirradiated detectors with a strip width which is 20% of the strip pitch. Even extrapolating their data to an infinitely narrow strip width, the capacitance is greater than 1pF/cm. This data on 50μm pitch detectors implies capacitances of 1.3pF/cm for detectors with 70μm pitch and an intermediary strip [15].

The capacitance for the longest element of our 12-fold design is thus $1.3 \times 15 + 0.27 \times 44.5 =$ 30pF. This translates to 2700 electron noise equivalents which gives a signal to noise of 12:1.

4.2 Radiation-Hard Technology

We recall our studies [1] which concluded that, assuming an operating temperature of -10C, radiation doses up to 3fb^{-1} would require operating voltages less than 150V, which is probably acceptable.

4.3 Operating Temperature

Figure 15 from [1] shows that the depletion voltage varies very little whether Layer00 is maintained at -10C, or if it is operated at the temperature of the rest of SVXII (10C). It is only at room temperature operation (20C) that appreciable differences in the voltage are observed.

We also calculated that the shot noise for a detector running at -10C would be about 400 enc, while at 10C it would be about 900 enc. When added in quadrature to the noise coming from the capacitance, the shot noise makes a very small contribution to the total noise for either operating temperature.

We thus see no compelling reason to run Layer00 at a different temperature from SVXII, and expect that choosing the same temperature would simplify matters. However, a full study has not yet been undertaken to evaluate the effects of differential contraction and cooling.

5 Summary

Liverpool favour a 12-fold symmetric design with $\approx 70\mu$m pitch, which we believe is buildable, as demonstrated by our mechanical mock-up. We expect the signal-to-noise of the detector in the worst case to be 12:1. This decision is based firstly, on simulation studies which agree with data from both test-beams and a running experiment; secondly, on our estimates of depletion voltages and radiation damage as studied by ATLAS; thirdly on signal-to-noise values from RD20, CMS and the performance of the SVX3D chip; and fourthly, from our mechanical mock-up which gives us confidence that this detector can be successfully built and installed.

There are a number of issues however which are still to be resolved. Detailed studies have not yet been performed on the differential expansion and cooling of the detector at a particular temperature. Nor have we completed a material budget or a stress analysis of the detector. However, we do not expect that such issues depend crucially on the modularity or pitch of the detector, and so hopefully, at least these two issues can already be resolved at the Padova workshop.

References

[1] 'Discussion of Some Design Issues for the Layer00 Detector' to be found at `http://hep.ph.liv.ac.uk/cdf/ip3.ps`

[2] 'A first look at occupancies in Layer00' which can be found at `http://hep.ph.liv.ac.uk/cdf/occupancy.ps`

[3] 'Variation 1 on A first look at occupancies in Layer00' which can be found at `http://hep.ph.liv.ac.uk/cdf/var1.ps`

[4] 'Further Variations on A first look at occupancies in Layer00' which can be found at `http://hep.ph.liv.ac.uk/cdf/var2.ps`

[5] 'Resolution of the Layer00 Silicon Detector for Various Configurations ' which can be found at `http://hep.ph.liv.ac.uk/cdf/sidesign.ps`

[6] R.Brenner et al./ ,*Nucl. Inst. and Meth.* **A326** (1993) 189.

[7] P.Weilhammer, *Nucl. Inst. and Meth.* **A342** (1994) 1.

[8] Y.Unno et al., *Nucl. Inst. and Meth.* **A383** (1996) 211.

Component	8-fold	12-fold	Mock-up
Diameter of SVXII Carbon Fibre Sleeve	42	39.5	39.5
Radius of inner silicon layer	13.35	14.4	14.83
Radius of outer silicon layer	16.5	16.62	17.06
Diameter of cooling pipe	1.6	1.6	1.6
Distance from beam-pipe to cooling pipe	0.40	0.47	0.3
Silicon Sensor Width	12.8	8.96	9.22
Silicon Sensor Thickness	0.3	0.3	0.3
Guardring Width	2.1	2.1	2.1
Bond-wire Height	0.25	0.25	0.25
Cable Height	.050	.025	.025
Spacers between cables	0.1	0.1	0.1
Maximum silicon + cable stack height	1.45	1.05	1.05
Gap from outer layer to SVXII assuming 39.5mm Sleeve	0.63	1.25	0.79
Gap between inner and outer silicon layers	0.94	0.5	0.5
Gap between the beam-pipe and inner layer	.48	1.28	2.2

Table 1: Table comparing dimensions of the 8-fold, 12-fold and mock-up. All dimensions are in mm.

[9] V. Chabaud et al., *Nucl. Inst. and Meth.***A368** (1996) 314.

[10] See `http://hep.ph.liv.ac.uk:80/cdf/jan26.html`

[11] See `http://cdfsg6.lbl.gov/ dfish/cdf/chips/svx3d/hd2_noise. gif`

[12] See `http://hep.ph.liv.ac.uk/cdf/cables.html`

[13] A.Holmes-Siedle, ‘Radiation tolerance of single-sided silicon micro-strips.’, RD20 Coll., *Nucl. Inst. and Meth.***A339** (1994) 511.

[14] The CMS Technical Design Report.

[15] P.Allport, Private Communication.

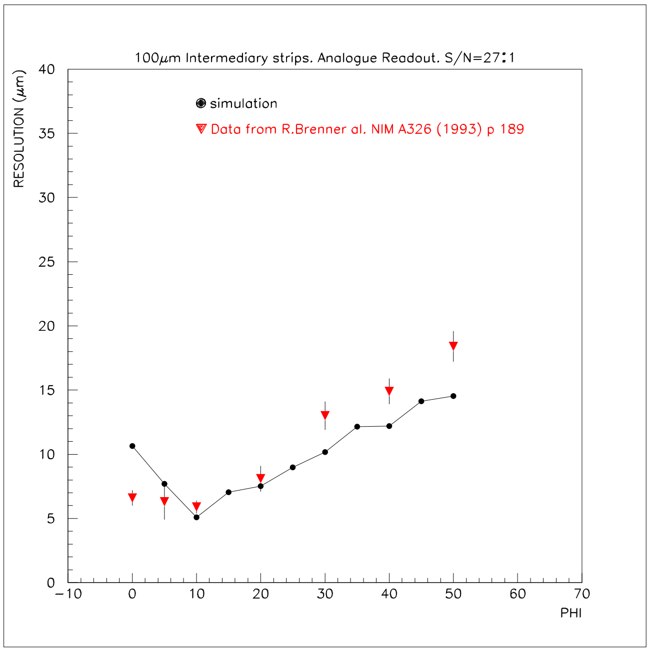

Figure 1: Comparison of our simulation with test-beam data

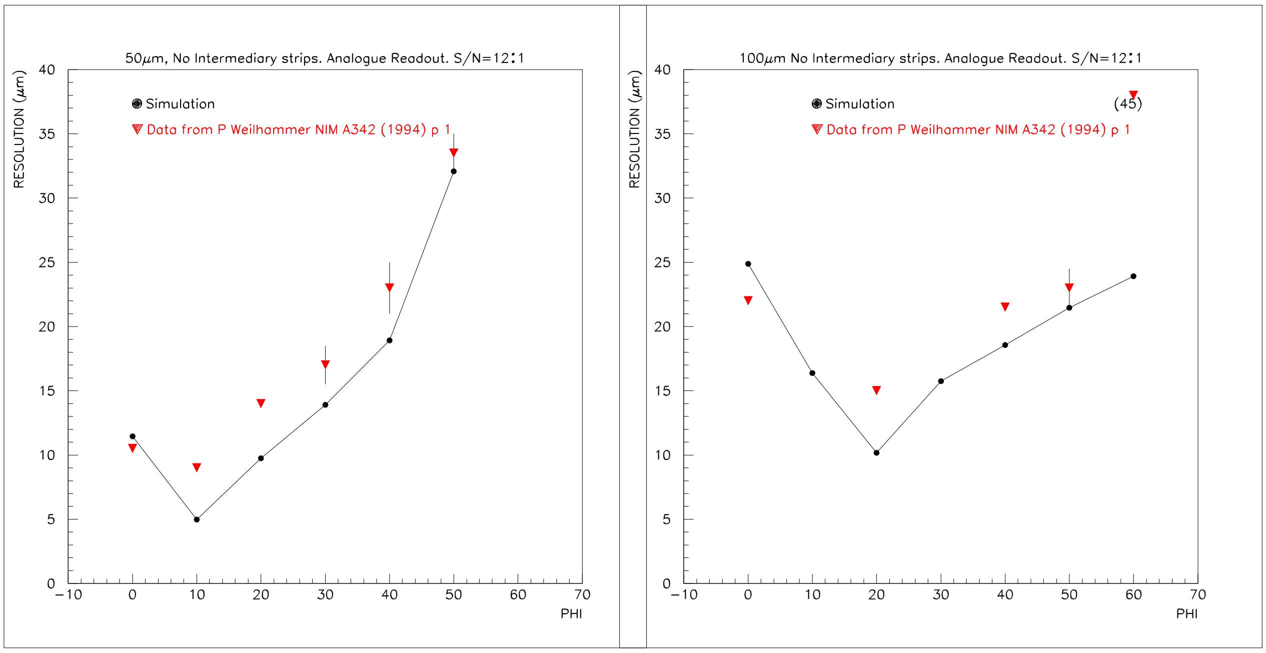

Figure 2: Comparison of our simulation with test-beam data

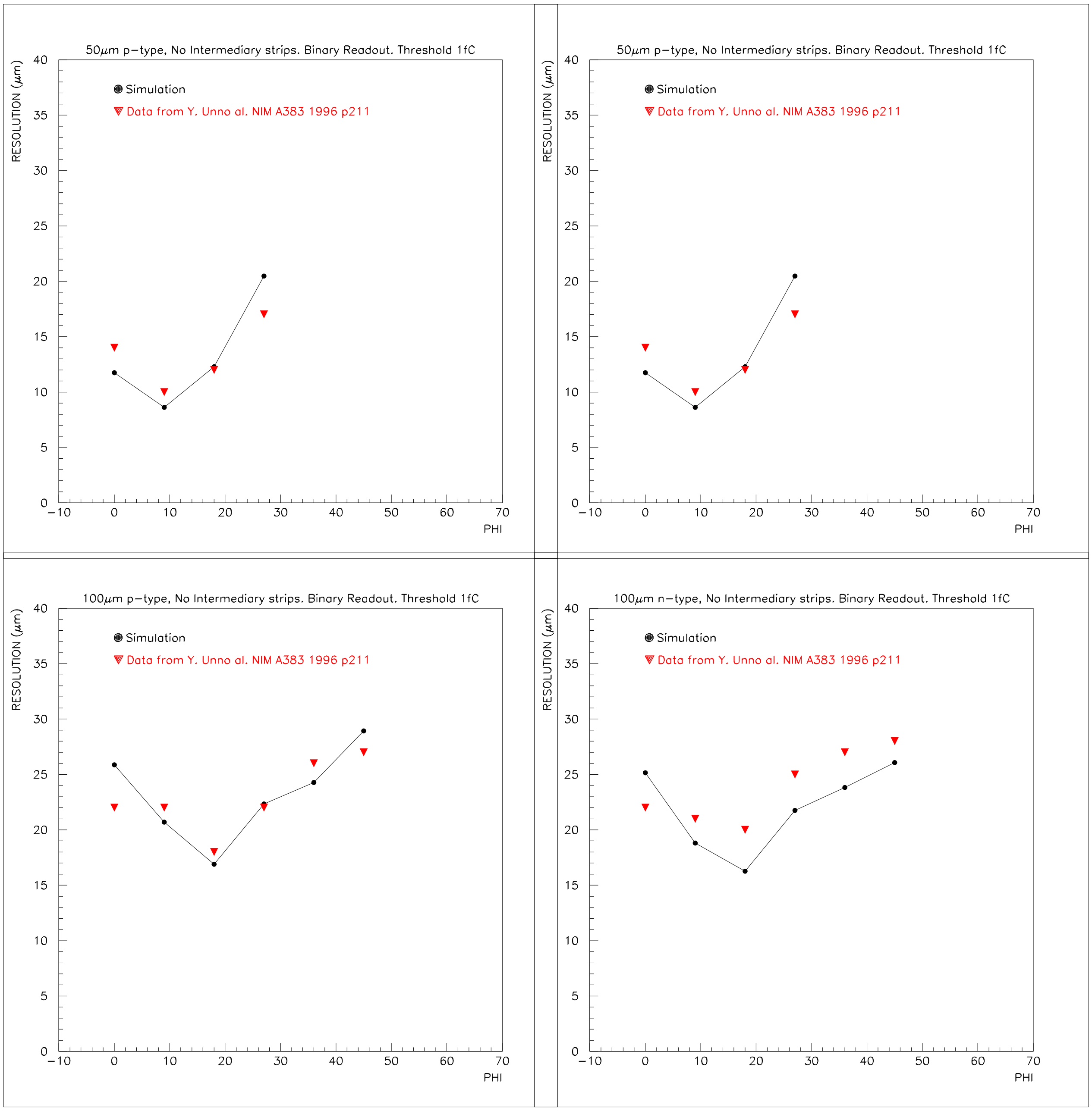

Figure 3: Comparison of our simulation with test-beam data

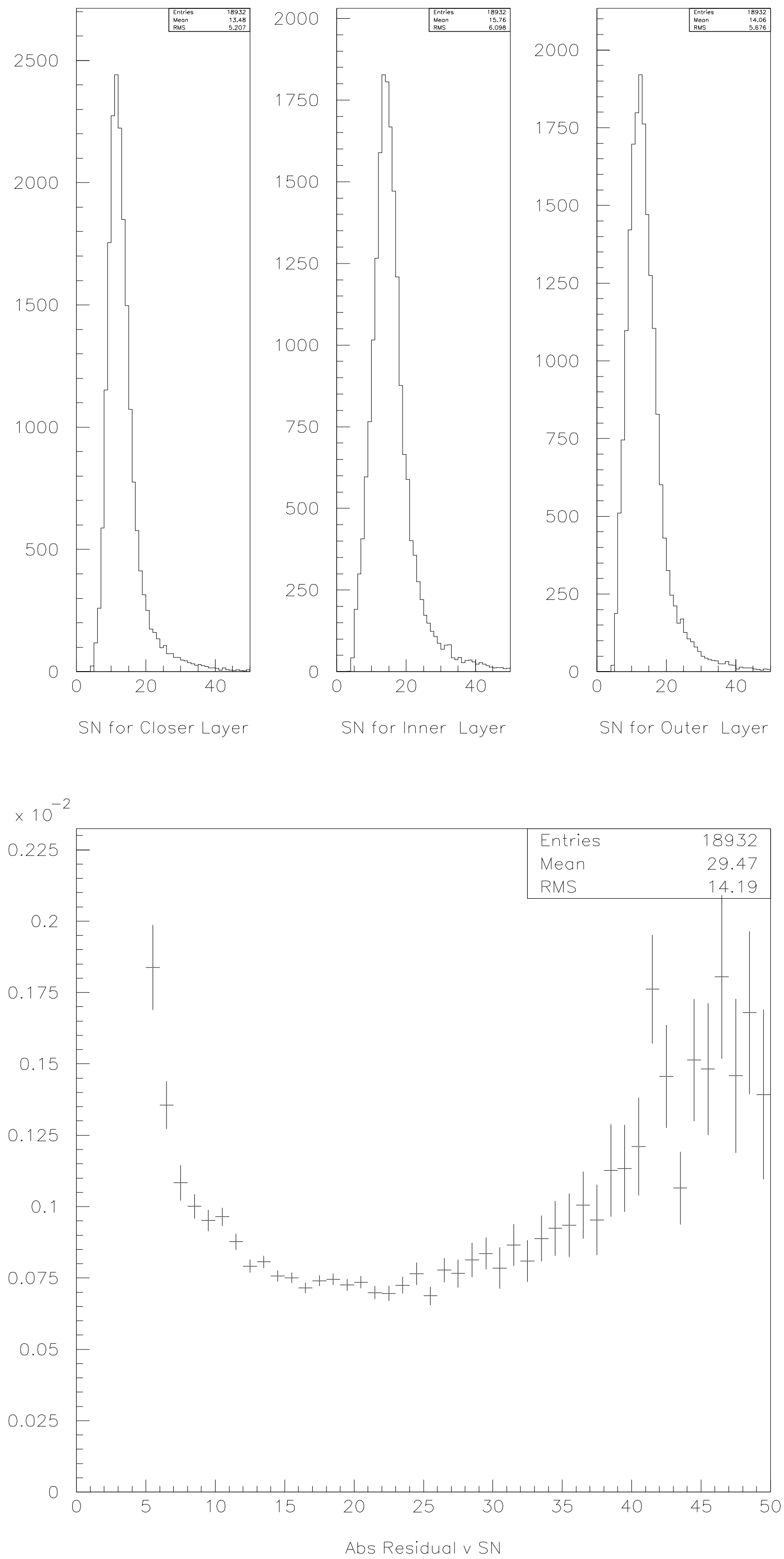

Figure 4: Top plot: Signal deposited in each of the three layers of the DELPHI vertex detector during the 1992 running period.
Bottom plot: Resolution as a function of signal deposited during the 1992 running period.

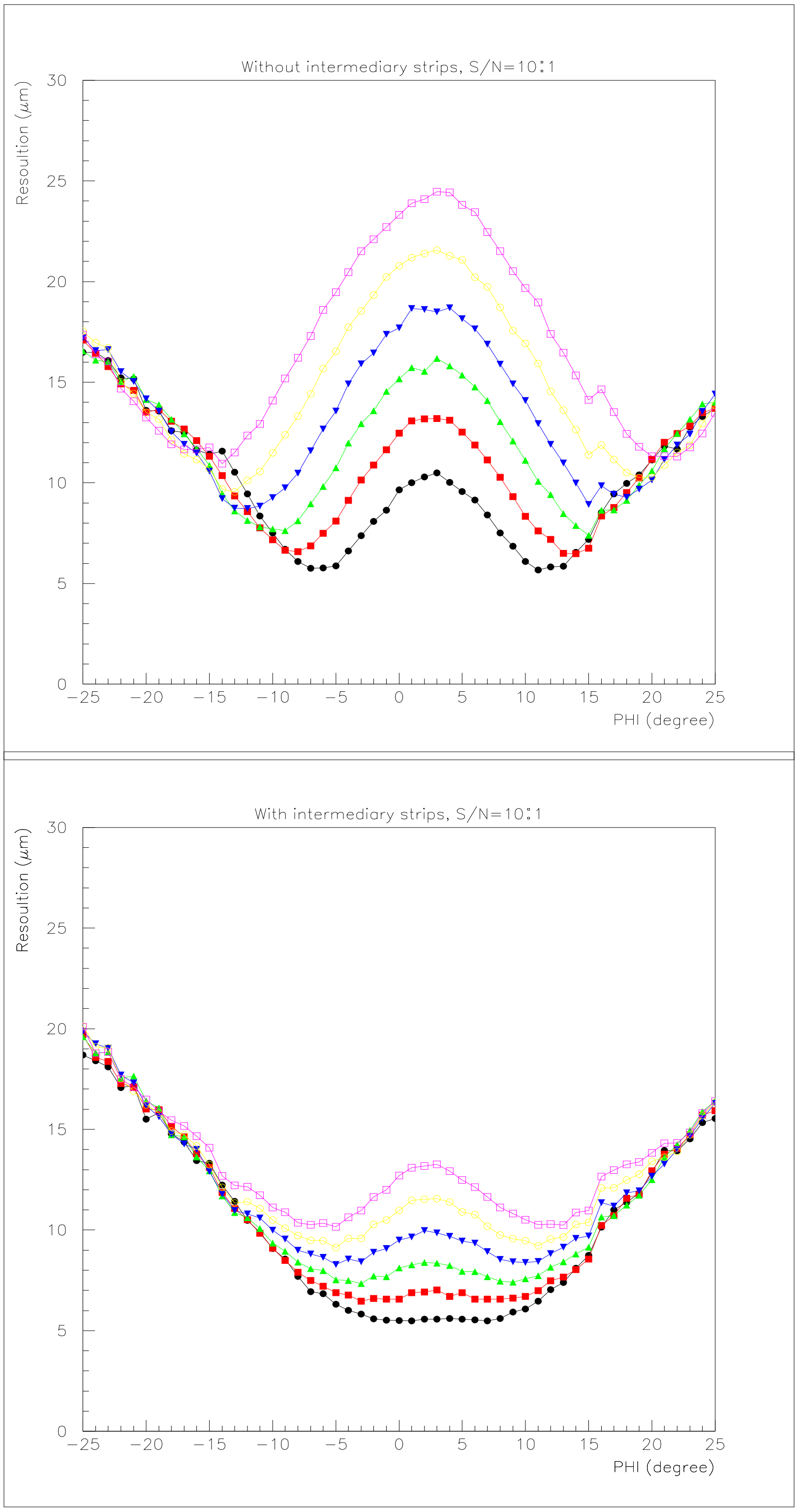

Figure 5: Intrinsic resolution in the silicon as a function of track crossing angle, with and without intermediary strips for detectors with signal-to-noise of 10:1.
Closed circles are for 50μm pitch
Closed squares are for 60μm pitch
Triangles are for 70μm pitch
Inverted triangles are for 80μm pitch
Open circles are for 90μm pitch
Open squares are for 100μm pitch

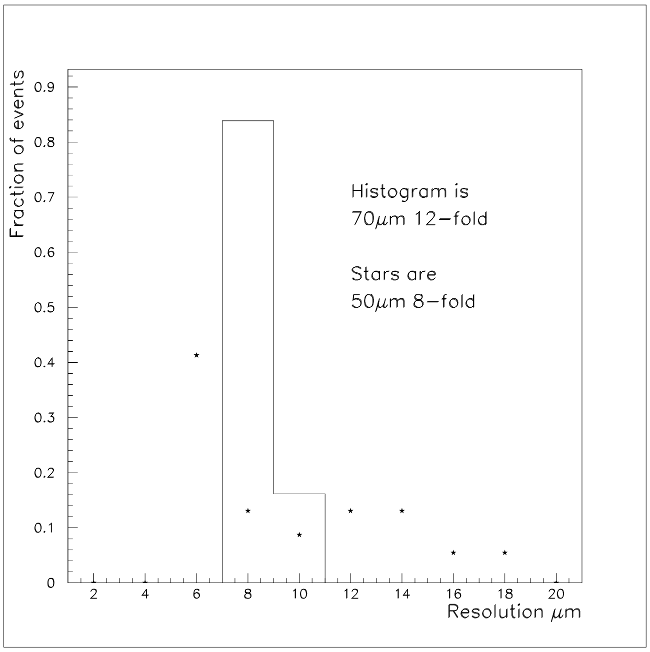

Figure 6: Fraction of events at a given resolution for a 12-fold design, and an 8-fold design.

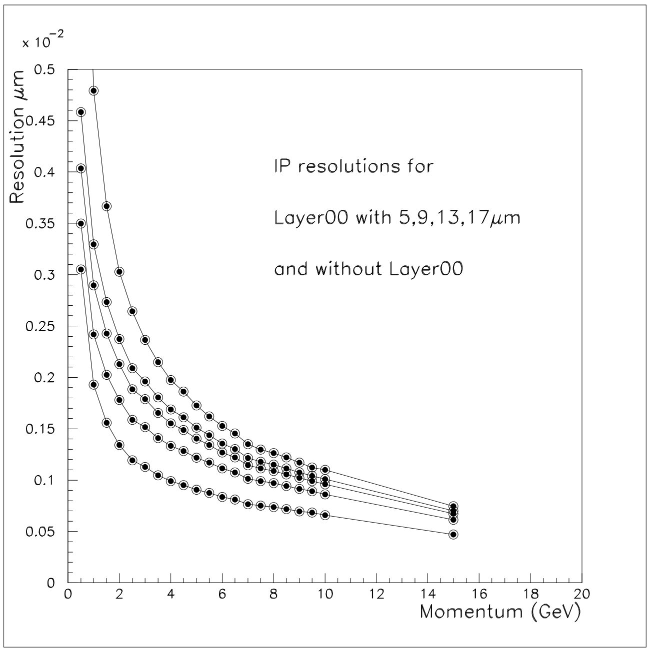

Figure 7: The relationship between impact parameter resolution and transverse momentum assuming hits in SVXII and ISL, with a point precision on Layer00 points of $5, 9, 13, 17\mu$m and also without a Layer00 point. Note the point which is plotted at a p_t of 15GeV is the asymptotic resolution for an infinite momentum.

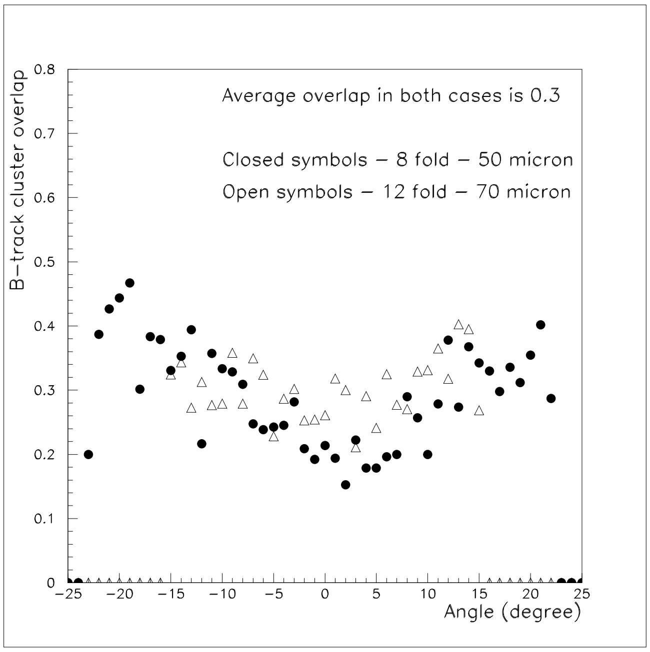

Figure 8: The fraction of b-tracks coming from top decays which are mis-measured due to overlapping clusters for an 8-fold and a 12-fold design.

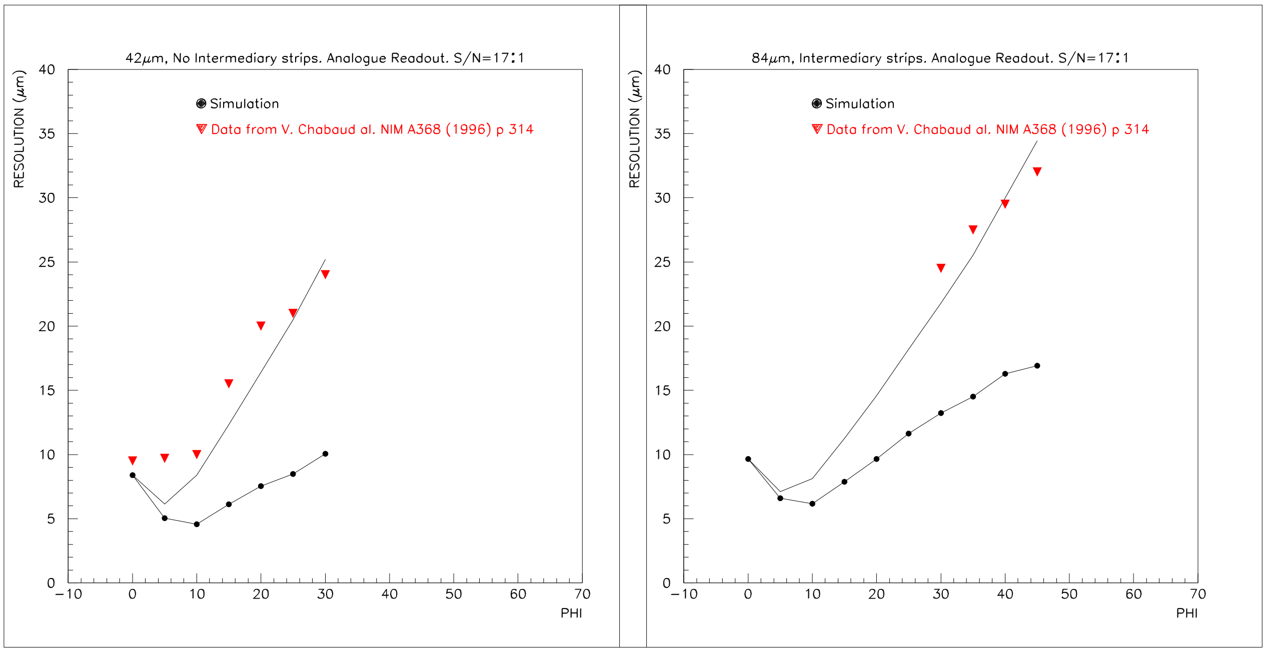

Figure 9: The comparison of our simulation with the DELPHI data taken during the 1994 running period. In both cases, the lower curve is the direct comparison. The upper curve assumes a 40μm and 30μm radial alignment error for upper and lower plots respectively, as explained in the text.

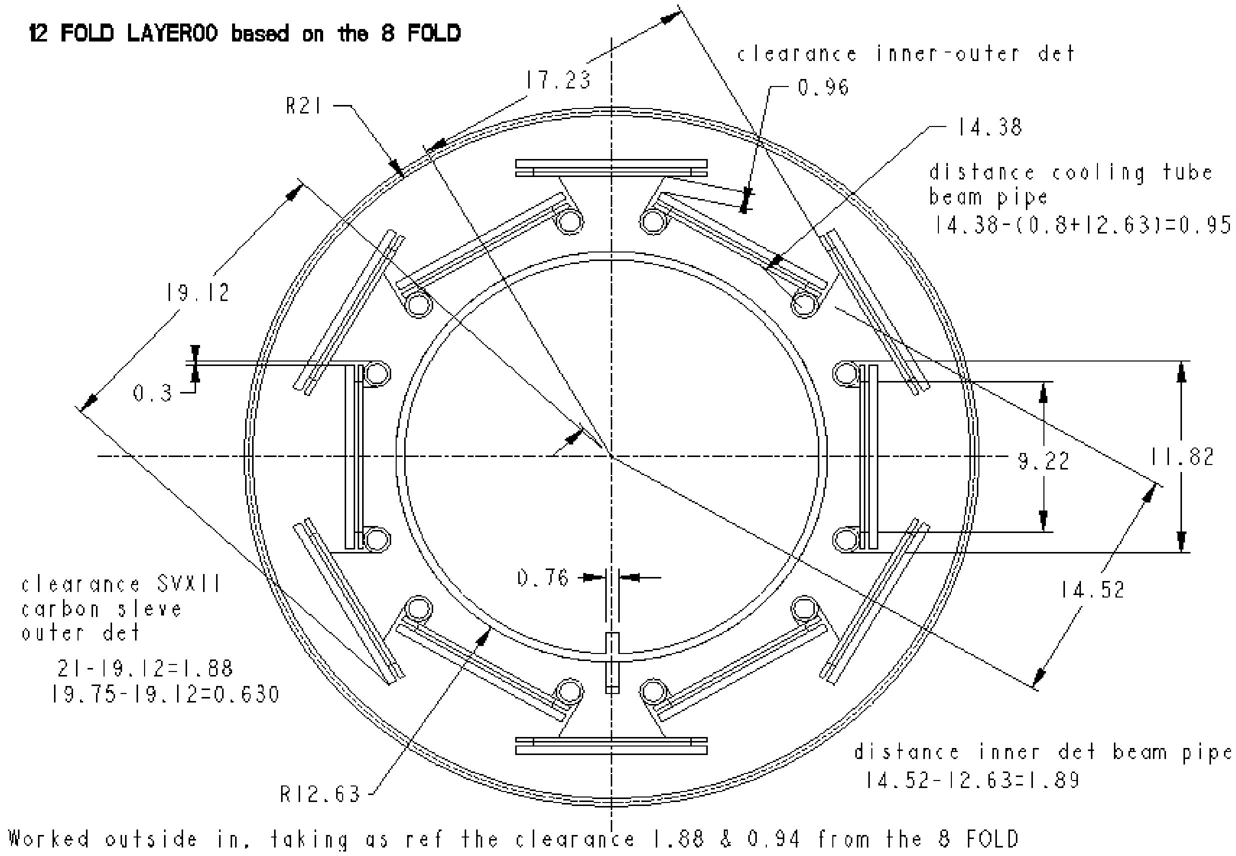

Figure 10: The $R\phi$ view of Layer00 in which a 12-fold design has been created from the 8-fold design by holding two dimensions fixed: the difference between the inner silicon radius and the outer silicon radius; and the difference between the outer silicon radius and the SVXII inner wall radius (at 21mm).

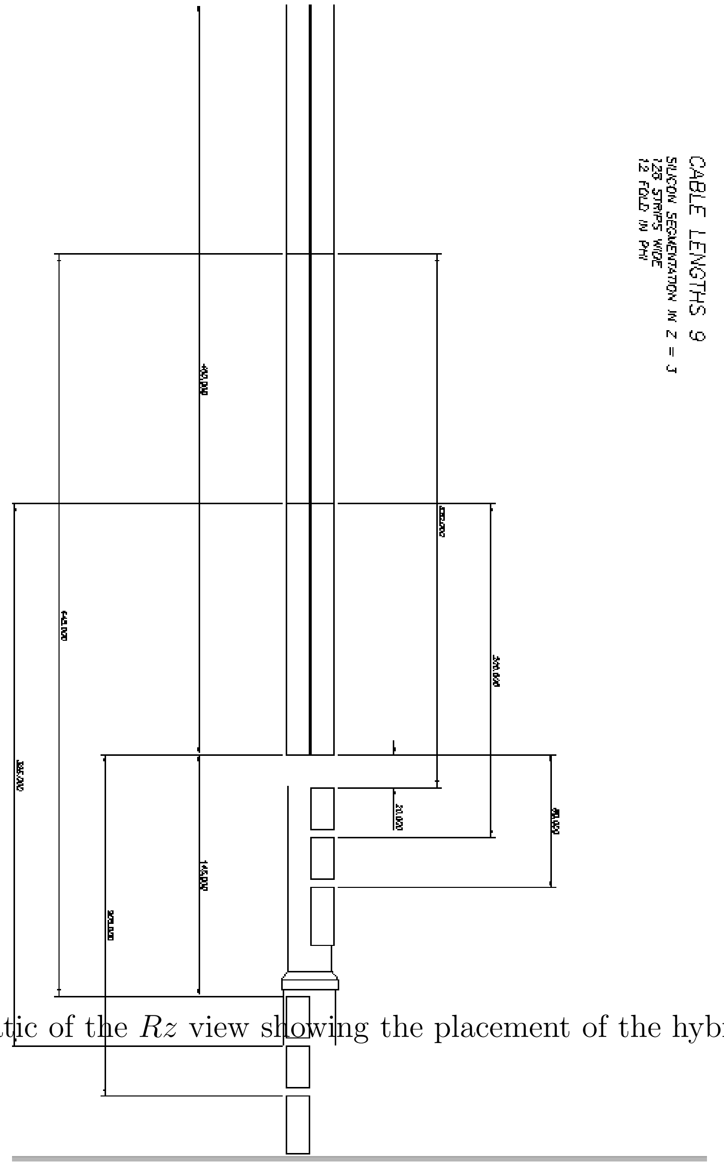

Figure 11: A schematic of the Rz view showing the placement of the hybrids and the cable lengths.

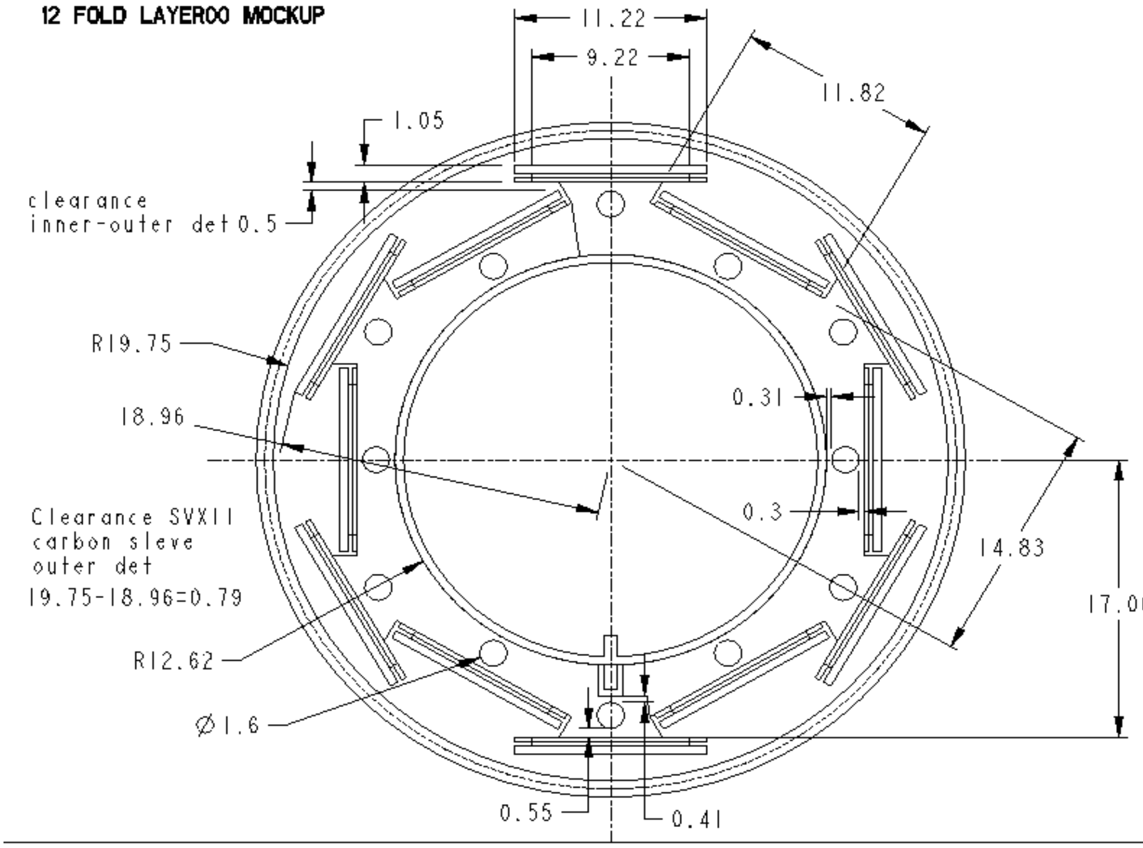

Figure 12: The mechanical drawing for the $R\phi$ projection of our mock-up.

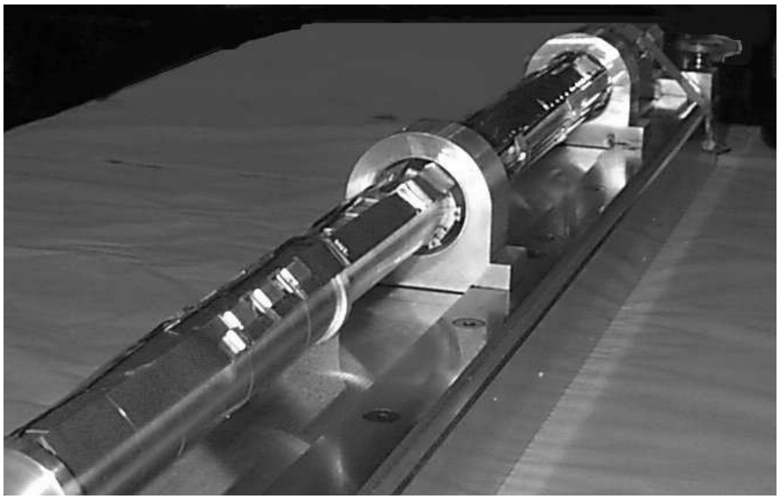

Figure 13: A photograph of the mechanical mock-up.

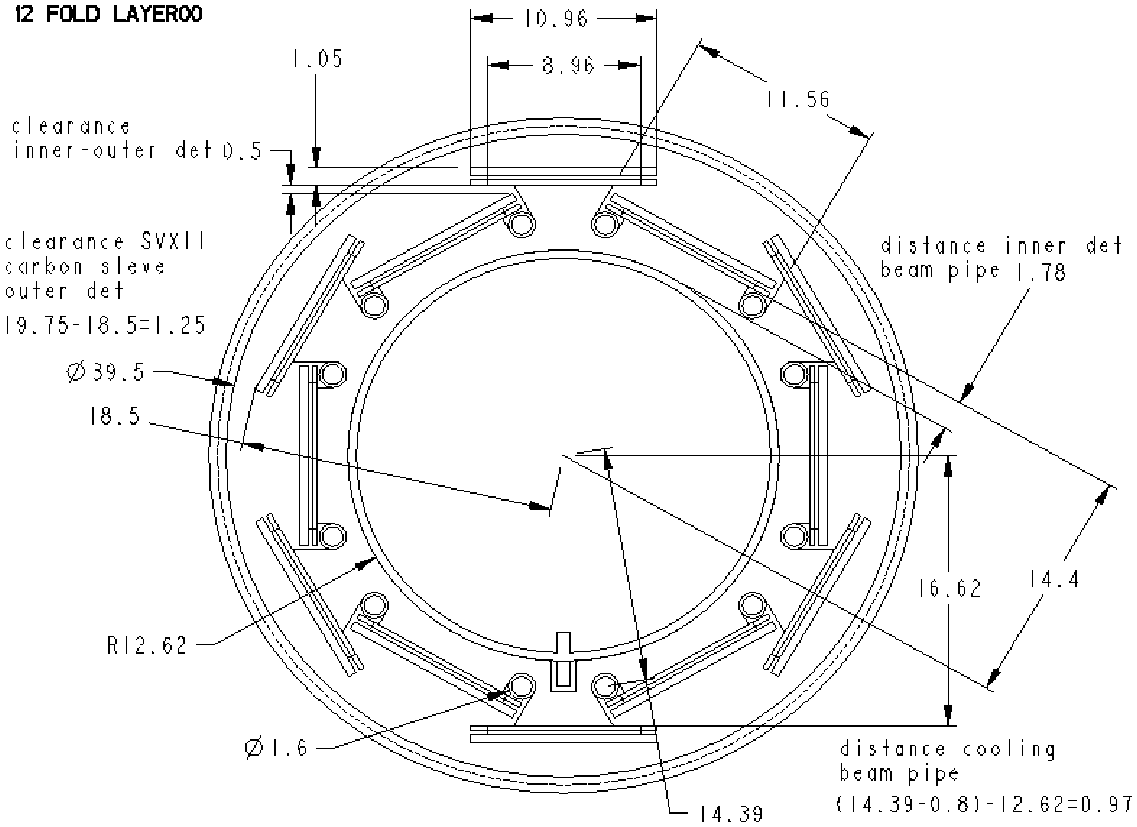

Figure 14: A possible design in which the sensors are mounted directly on the cooling pipes. The pipes are supported by end rings outside of the silicon acceptance and by thin carbon fibre staves within the acceptance.

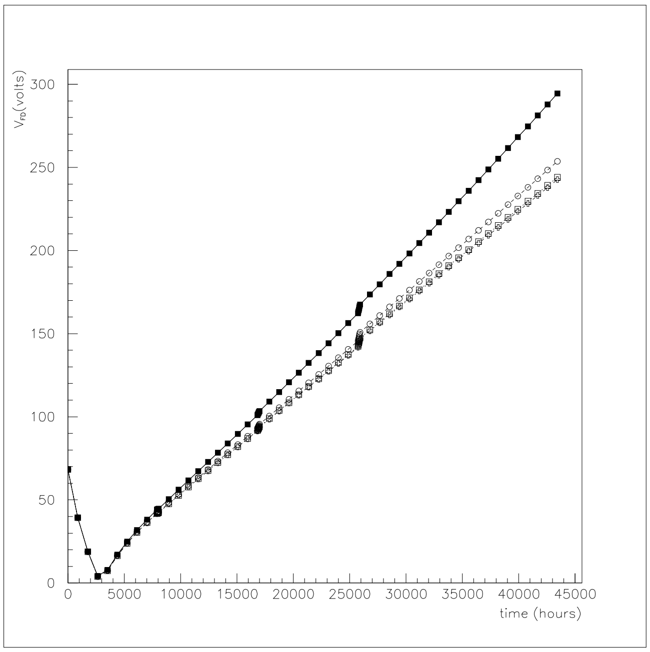

Figure 15: The depletion voltage as a function of time for detectors at temperatures, reading from top to bottom, of 20C, 10C, 0C, -10C. This plot assumes 1fb^{-1} per year. (There are 8760 hours in one year.)