Summary of Constraints and Performance

1 Introduction

From our studies at Liverpool, a number of points have become clear and certain arguments crystallised, so that we are now in a position to focus on a relatively small number of solutions and examine their respective merits.

The major constraints and performance related issues are discussed and conclusions drawn.

2 Mechanical Constraints

There may be mechanical constraints on building a very small detector. We need to think how the silicon will be mounted, how the cables will be taken out, and how the detector will be cooled. Some degree of overlap between plaquettes is needed: firstly, to allow for dead regions at the edge of the plaquettes due to guard rings and the silicon manufacture; and secondly, to provide overlap for alignment. We assume a dead region of 1mm and require an overlap of 10%.

Three designs amongst many present themselves (Figure 1.)

- An angled design: Each side of a regular polygon is tilted through an angle and the width of the plaquette extended.
- A castellated design: Every other side of a regular polygon is displaced outwards by δR which allows the width of the plaquettes to be extended.
- An overlapping design: Each side of a regular polygon is extended, but in one direction only.

Although an angled or overlapping design may make fanning out the cables easier, it appears from sections 3 & 8 that a castellated design may be necessary in order to reduce the crossing angles although the effects of the Lorentz angle require further study.

Another mechanical concern to be addressed, is whether the small width detectors (dependent on r-phi modularity) pose any problems from the point of view of handling and testing by the manufacturer. To assess this, it is urgent to agree final dimensions in time to get any adverse feed-back on this point quickly from potential suppliers.

3 Crossing Angles

The modularity of the detector and the pitch of the strips must be matched so that the majority of tracks deposit their charge over one, two or three strips. Designs in which a large number ($> 20\%$) of tracks spread their charge over greater than three strips give degraded performance.

A reasonable criterion is that the strip pitch should be no smaller than the projected distance in the silicon of the largest angled track, i.e. for a 300μm width detector, the modularity N, and the pitch p are related via

$$p > 300\Big(\tan(\pi/N + \theta) + y\Big) \tag{1}$$

where θ is the angle through which the modules are tilted and $y = 0.1/1.6$ for an overlapping design implies a sideways shift per plaquette of 1mm. Reducing the pitch below this number would only compromise efficiency without much significant gain in resolution.

The table below calculates an approximate minimum strip pitch for a given R-phi modularity, for three geometries as in Fig.1.

Modularity	Minimum strip pitch		
	Angled Tilt $= 10^o$	Castellated Tilt $= 0^o$	Overlapping $y = 0.1/1.6$
8	191μm	124μm	143μm
9	173μm	109μm	127μm
10	160μm	97μm	115μm
11	149μm	88μm	106μm
12	140μm	80μm	98μm
13	132μm	74μm	92μm
14	126μm	68μm	86μm
15	121μm	64μm	82μm
16	117μm	60μm	78μm

This effectively eliminates the 8-fold 50μm pitch solution since, as section 8 will show, 38% of tracks spread their charge over 4 or more strips. We must go to a) greater modularity and/or b) larger strip pitches.

4 Readout Chip Constraints

Given that there is a reasonably hard limit of about 128 readout chips, only a limited number of solutions exist in terms of modularity N, and strip pitch p. If the radius of the detector is assumed to be 1.6cm and an overlap of 10% is requested for alignment purposes; then the minimum strip pitch allowed can be calculated:

$$p > \Big(2 \times 1.6 \times 1.1 \times f \tan(\pi/N)\Big)/128 \tag{2}$$

where f is a factor of about 1.1 to ensure 2π coverage. For a castellated design with alternate plaquettes offset by δR then $f = 1 + \delta R/(2 \times 1.6)$ while for an angled design $f = \cos(\pi/N)/cos(\pi/N + \theta)$.

The following table shows the results for an angled design of 10^o and a castellated design with $\delta R = 2mm$.

Modularity	Angled Design			Castellated Design			No.Chips
	Circumference (cm)	Width Plaq. (cm)	Minimum Pitch (μm)	Circumference (cm)	Width Plaq. (cm)	Minimum Pitch (μm)	
8	12.77	1.597	125 (62)	12.39	1.549	121 (60)	64 (128)
9	12.51	1.390	109 (55)	12.25	1.361	106 (53)	72 (144)
10	12.32	1.232	96	12.15	1.215	95	80
11	12.17	1.107	86	12.08	1.098	86	88
12	12.06	1.005	78	12.03	1.002	78	96
13	11.97	0.921	72	11.98	0.922	72	104
14	11.90	0.850	66	11.95	0.854	67	112
15	11.83	0.789	62	11.92	0.795	62	120
16	11.79	0.737	58	11.90	0.744	58	128

Numbers in brackets are for **two** readout chips per plaquette

Whatever solution we choose must conform, more or less, to these limits: small variations on these numbers can be obtained by reducing the overlaps or the tilt.

5 Rad-Hard Technology Constraint

We have looked at the increase in voltage which would be necessary to fully deplete the detectors as they become progressively more damaged due to radiation.

An integrated luminosity of 1fb^{-1} per year was assumed, which corresponds to 1MRad per year which is equivalent to 1.7×10^{13} neutrons per cm^2 or $3. \times 10^{13}$ protons per cm^2 using the parameterisation of the ATLAS TDR [1]. The detector was assumed to run at -10C. The short term favourable annealing effects were ignored, while reverse annealing was calculated assuming that the detectors were allowed to heat to 25C for one week at the end of each year for maintenance purposes.

Figure 2 shows the predicted evolution of the full depletion voltage for 300μm thick detectors. After 2 years (2fb^{-1}) the detectors would need to be run at a minimum of 100 volts, while after 3 years (3fb^{-1}) it would be necessary to rise to a minimum of 150 volts.

A comparison of this prediction with a parameterisation from recent test-beam data [2] gives similar results. A further comparison has been made with the figures in the CMS TDR [3] (reproduced in the Layer00 proposal [4],) which predict very similar behaviour after inversion.

If we are only designing for 2fb^{-1}, p-in-n technology can be used. For luminosities above this value, the voltage must be raised well above the 100V which constitutes the maximum specification of the capacitor dielectric.

We would probably be safe up to 3fb^{-1} (150 volts) as there is experience with Hamamatsu detectors performing reliably at this voltage. Above this value however, we run the risk of irreversible damage to the capacitors should bad beam conditions, for example, lead to large local ionisation in the silicon. The resulting permanent damage to the dielectric leaves the affected region dead with large currents flowing into the front-end of the CMOS pre-amplifier (usually also killing neighbouring channels.) Up to now, no HEP detectors have needed to operate well above the rating of the capacitors so no relevant experience of the magnitude of this problem exists.

With n-in-n technology, this risk can be avoided by running the detectors partially depleted below the voltage rating of the dielectric. Figures 3&4 show an analysis by the Cambridge group of various n-in-n and p-in-n detectors run in a test-beam at CERN [2]. The efficiency for registering a hit at a 1fC single strip threshold (which corresponds to three times the noise for 2000 enc, or four times for 1500 enc), is plotted as a function of voltage, after irradiation at a fluence of 3×10^{14} protons/cm^2. Running p-in-n detectors at 100 to 150 volts gives poor performance (<50% efficiency) while n-in-n detectors can be run at 150 volts with >90% efficiency. The full depletion voltages for these detectors was about 300V, confirming earlier studies showing that n-side read-out allows efficient operation well below the depletion voltage. If high operating voltages are undesirable, this is a strong argument for adopting the n-in-n solution.

5.1 N-in-N Technology

We do not have time for a prototyping run for the sensors for Layer 00. This means we must work with proven solutions adapted only in terms of external geometry to fit the needs of Layer 00.

If we require n-in-n technology, we are confident that a design based on a pitch of 70μm to 90μm pitch will work, as these detectors have already been extensively prototyped and tested, giving excellent performance both before and after irradiation up to 10MRad in test-beam studies. N-side read-out designs with 50μm pitch have been prototyped for RD20 and SDC and results after irradiation can be found in the literature, but little is available on results after irradiation with fast read-out electronics.

Double metal n-in-n detectors for LHCb with variable pitch down to 40μm have been designed at Liverpool and produced by Hamamatsu. They work well pre-irradiation but the study of their post-irradiation properties is only just starting. We would conclude that the most reliable and systematic results with full read-out of irradiated detectors are those of ATLAS at $70 - 90\mu$m pitch [2].

5.2 P-in-N Technology

For the p-in-n technology, working prototypes already exist for a range of strip pitches between 50μm and 100μm. This follows from the work of RD20, ATLAS and CMS. In ATLAS, detectors irradiated up to 10MRad have been studied extensively in beam with fast electronics and found to work satisfactorily albeit with voltages >300V.

6 The Operating Temperature of Layer 00

It may be that the limiting design feature is not given from physics arguments but from mechanical constraints. For example, there may not be enough room to embed a cooling system within the silicon support structure. We therefore ask what effect higher operating temperatures have on the depletion voltage and reverse current.

6.1 Depletion Voltage

Figure 5 shows the operating voltage as a function of running time at a fluence of 1MRad/year, for temperatures of -10, 0, 10 and 20C. It is assumed that in addition, the detector is brought to 25C for one week per year for maintenance.

As regards the voltage required, there is very little difference between the performance with Layer 00 maintained at -10C, and Layer 00 operating at the temperature of the rest of SVX (10C). It is only at room temperature operation (20C) that appreciable differences in the voltage are observed. These observations may mean that a much simplified cooling system could be designed for Layer 00.

6.2 Reverse Current

Figure 6 shows the strip current for a fully depleted, 50μm readout pitch, 8cm long, 300μm thick detector, as a function of running time, for temperatures of -10, 0, 5, 7.5, 10 and 20C. The current increases with increasing trap concentration due to irradiation, and with increasing temperature. For detectors with 75μm readout pitch, these currents should be increased by 50%.

7 Noise Calculation

Estimation of the total noise with an intermediate strip and/or at a higher temperature are discussed below for a 50 micron readout pitch detector. The noise induced by the reverse current is assumed to add in quadrature with the input noise for a given capacitive load.

$$N = N_{ir} \oplus N_{cap} \tag{3}$$

7.1 Shot Noise

Running the detector at 10C rather than -10C has a small effect on the depletion voltage due to radiation damage but a larger effect in the reverse current with corresponding implications for the noise.

A simple model [5, 6] to relate the current to the noise in equivalent electrons is given by

$$N_{ir} = sqrt\frac{I_r \times \Delta t}{q_e} \tag{4}$$

where Δt is the sampling time,conservatively taken here to be 132ns, the time between beam crossings. From Fig. 6, the reverse current after two years would be 0.2μA at -10C and 0.9μA at 10C, yielding

$$N_{ir} = 400 \text{ enc. at } -10\text{C or } 900 \text{ enc. at } 10\text{C} \tag{5}$$

These rough estimates need to be better quantified.

7.2 Intermediate Strip

The addition of an intermediate strip helps to linearise the distribution of charge on neighbouring strips for tracks which are close to normal. For crossing angles less than 0.05 radians (about one quarter of all tracks) this would improve the resolution from 8 or 9μm to 7μm. As [7] already implies an average resolution of 10μm, which is dominated by other effects, the improvement which the intermediate strip provides is small.

On the other hand, an intermediate strip results in a larger noise component. Assuming that the noise of the Honeywell SVX3D chip [8] after 2MRad irradiation in units of electron noise equivalents can be expressed as $800 + 60\times$ (Capacitance in pF). From [9], the silicon will have a capacitance of 1.2 pF/cm while including an intermediary strip can add a further 0.4pF/cm[4] Consequently an intermediate strip could contribute a further 200enc to the noise.

7.3 Total Noise

Assuming the above parameterisation of the performance of the electronics and taking into account an additional 13pF capacitance from the cables, we obtain Ncap between 2200 and 2400 enc with and without an intermediate strip.

With these noise estimates, the additional effect of operating at 10C does not seriously further degrade the performance.

8 Occupancy Studies (Summary)

We come now to the impact the design will have on the physics. The myriad of numbers in the previous reports [10] are condensed and the salient points are reproduced in the table below. The results are for $t\bar{t}$ events with one minimum bias event superimposed. The numbers are similar for $b\bar{b}$ events; Percentages are similar for events with five minimum bias events superimposed.

Modu-larity	Pitch	Tracks spreading over				Strip Sharing	B-Strip Sharing	Track Sharing	B-Track Sharing
		2-strips	3-strips	4-strips	5-strips				
Castellated Design									
8	50μm	21%	41%	33%	5%	4.0%	?	12 (10%)	3.2 (26%)
8	100μm	41%	57%	2%	0%	6.2%	?	16 (14%)	4.1 (34%)
12	75μm	48%	51%	1%	0%	4.8%	18%	13(11%)	3.4(28%)
16	50μm	42%	55%	2%	0%	3.5%	13%	9.8(8.4%)	2.7(21%)
Angled Design									
8	50μm	22%	39%	21%	19%	4.4%	?	13 (11%)	3.4 (28%)
8	100μm	41%	48%	12%	0%	6.4%	?	17 (15%)	4.2 (36%)
12	75μm	40%	48%	14%	0%	5.3%	19%	14(12%)	3.7(31%)
16	50μm	25%	42%	32%	3%	4.1%	15%	12(10%)	3.3(27%)

Increasing the modularity and decreasing the pitch gives a small but nonetheless significant improvement. Going from 12-fold 75μm to 16-fold 50μm for the castellated design improves the doubley hit B-strips from 18% to 13% and improves the mis-measured b tracks from 3.4 to 2.7. That is an improvement of 0.7 tracks per event or 25% less badly measured b tracks.

However, It is important to ensure that the relationship between modularity and pitch, as described in section 3, is adhered to. As can be seen in the table above, the 8-fold 50μm solution, although giving reasonable occupancy numbers, fails on account of the large number of tracks depositing their charge over 4 or more strips.

9 Impact Parameter Resolution

The most important reason for Layer00 however is in recovering good impact parameter resolution for low momentum tracks. To evaluate the effect of different strip pitches for Layer00, a simulation has been performed. Tracks were followed outwards from the interaction point, scattered randomly on passing through the beam-pipe and the layers of silicon, and measured with the expected resolution in Layer00, SVX2 and ISL. Then the process was reversed, and a full track fit performed including the (correlated) effects of multiple scattering. Finally, the results were parameterised according to the formula $A \oplus B/p_T$. Note, this is a very *poor* parameterisation for the particular geometry we are considering. Therefore, results are also given for the average resolution at 1,2,3 and 4 GeV. These are considerably *worse* than you would expect from the formula.

The inputs to the simulation are as given in Joe's talk [7]: The radius of Layer00 is taken to be 1.6cm and the radius of the inner layer of SVX2 is 2.615cm. The resolution in SVX2 is 12μm and in ISL is 32μm. The Molière scattering formula [11], $\theta_0 = .0136\sqrt{X}_0(1 + .038 \log X_0)$, is used but the log term is neglected.

Pitch	Parameterisation	Resolution at			
		1 GeV	2 GeV	3 GeV	4 GeV
50μm	$8 \oplus 29/P_T$	29μm	20(37)μm	17(45)μm	15(51)μm
75μm	$9 \oplus 36/P_T$	35μm	25(47)μm	21(57)μm	18(62)μm
100μm	$10 \oplus 42/P_T$	40μm	28(52)μm	23(62)μm	20(69)μm
No L00	$10 \oplus 63/P_T$	57μm	37(74)μm	30(90)μm	24(96)μm

The numbers in brackets are the implied values of B in the formula $A \oplus B/p_T$

Reducing the strip pitch clearly affects both the asymptotic term and the multiple scattering term. It is felt that the asymptotic term improvement is somewhat irrelevant, especially as we read in the Layer 00 proposal [4] "The intrinsic asymptotic resolution of 9-10μm will of course not be realized in practice." The multiple scattering term is the important parameter and it improves from 42μm for 100μm pitch to 29μm for 50μm pitch which is significant. Just as importantly, for 2GeV tracks it reduces from 28μm to 20μm.

With the inputs to the simulation detailed above, we were successful in reproducing the numbers in the Layer 00 proposal [4]. These numbers may however be somewhat pessimistic. There are two inputs which could be better than has been assumed: firstly, why is the log term in Molière scattering ignored; secondly, why is the resolution 12μm for a 60μm pitch detector? At LEP a 7μm resolution is obtained for a 50μm pitch, a number which includes alignment effects. In the table below, the effect that altering these inputs has on the impact parameter resolution is examined.

Pitch	Description	Resolution at		
		Infinity	1 GeV	2 GeV
No L00	As in Proposal	10μm	55μm	37μm
No L00	Include log term	10μm	50μm	34μm
No L00	8.5μm precision for SVXII	8μm	50μm	32μm
No L00	8.5μm for SVXII & log term log	8μm	45μm	29μm
100μm L00	“”	7μm	28μm	21μm
75μm L00	“”	6μm	25μm	19μm
50μm L00	“”	6μm	19μm	15μm

From this parameterisation of the scattering and with a more realistic detector resolution, there is perhaps a less compelling reason for going to smaller strip pitches. Nonetheless, a multiple scattering term of $18/p_T$ as derived from the last line of this table, would be truly excellent, approaching the level to which the alignment was successful in Run1.

10 Discussion

In terms of the physics, both occupancies and impact parameter resolutions, it is clear that as the pitch reduces, so too do the occupancies and resolutions. In order to maintain efficiency however, the modularity of the detector must be correspondingly increased.

A continuous improvement is seen with smaller strip pitches and increased modularity; there are no hard cut-offs. We see a sliding scale of progressive benefits from increasing the granularity and the improvements, though small, are significant.

Therefore, it seems reasonable to aim for the smallest strip pitch which is technically feasible and which can confidently be built in the time-scales allowed. The physics gains from the best granularity. One must now factor in what is technically possible.

We have a hard limit for the modularity at 16-fold from the cost of the readout chain. Can we therefore take on a 16-fold, 50μm pitch detector ?

The crucial issue here would appear to be the radiation dose. If we are only planning for 2fb^{-1}, then p-in-n sensors are sufficient. If however we wish to plan for higher luminosities, or foresee Layer 00 as providing a clearly defined upgrade path for Run-III, then we would recommend n-in-n sensors. In that case, given the time-scales, 75μ pitch sensors are known to work and we would propose building a 12-fold detector which would provide almost as good physics output.

A further issue, which may be important, is the technical difficulty of cooling the detector to -10C, given the space at our disposal. With the assumptions as given in section 7.1, it would appear that running the detector at +10C is a distinct possibility.

11 Conclusion

In summary, we see two design options.

- A 16-fold, $\approx 50\mu$m pitch detector based on p-in-n technology.
- A 12-fold, $\approx 75\mu$m pitch detector based on n-in-n technology.

Notwithstanding the above, we still have a number of issues which need resolving: castellated versus angled design; Lorentz angle effects; how to fan the cables out; cable capacitances; cooling........

This document is intended to provide a possible starting point for our discussions on Nov.23rd-25th. We feel it is important to finalise the geometry and detector technology as soon as possible in view of feedback on timescales we have received from silicon manufacturers and of the overall timescale of the Layer 00 project. We understand that if we were to order p-in-n sensors from Hamamatsu this November, delivery could not be expected until mid-April at the earliest, while for n-in-n sensors, delivery would be in mid-June or later.

References

[1] The ATLAS TDR.

[2] P.Allport et al., 'ATLAS Irradiation Studies of n-in-n and p-in-n Silicon Microstrip Detectors', *submitted to NIM*

[3] The CMS TDR.

[4] P.Azzi-Bacchetta et al., 'Proposal for a Very Low Mass, Very Small Radius Silicon Layer in the CDFII Upgrade.'

[5] C.Leroy et al., 'Study of Charge Collection and Noise in Non-Irradiated and Irradiated Silicon Detectors', *Nucl. Inst. and Meth.* **A388** (1997) 289.

[6] H. Spieler 'Electronic Noise and Pulse Shaping in Radiation Detector Systems', *3rd Int. (Hiroshima) Symposium on the Development and Application of Semiconductor Tracking Detectors, Melbourne, Dec. 9-12, 1997*

[7] J.Incandela & R.Snider, 'Effect of material on SVXII impact parameter resolution', Transparencies to the Upgrade Meeting Jan 9th, 1998. Available at `http://www-cdf.fnal.gov/internal/upgrades/xvsii/Mechanical/Mass/mass.html`

[8] See `http://cdfsg6.lbl.gov/ dfish/cdf/chips/svx3d/hd2_noise.gif`

[9] A.Holmes-Siedle, 'Radiation tolerance of single-sided silicon microstrips.', RD20 Coll., *Nucl. Inst. and Meth.* **A339** (1994) 511.

[10] 'The third study' on occupancies at `http://hep.ph.liv.ac.uk:80/cdf`

[11] Particle Data Group Book.

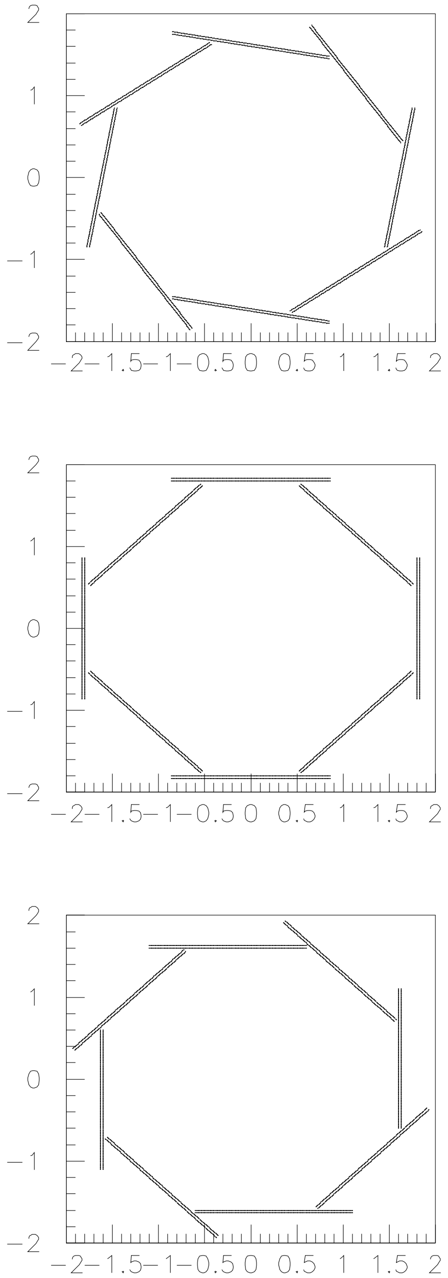

Figure 1: Three possible designs. From top to bottom: An angled design; a castellated design; an overlapping design.

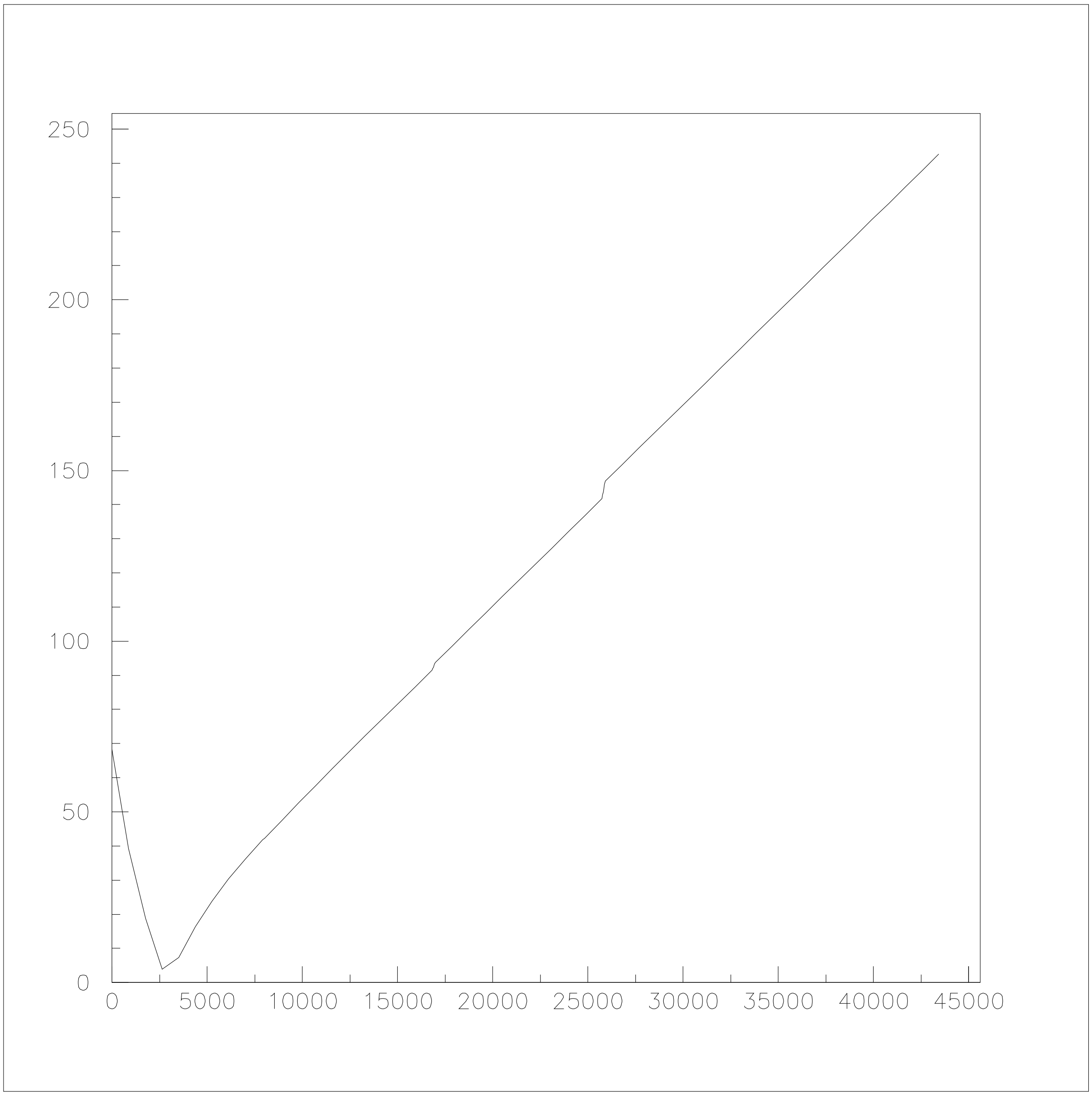

Figure 2: Full Depletion Voltage (vertical axis) as a function of time in hours (horizontal axis.)

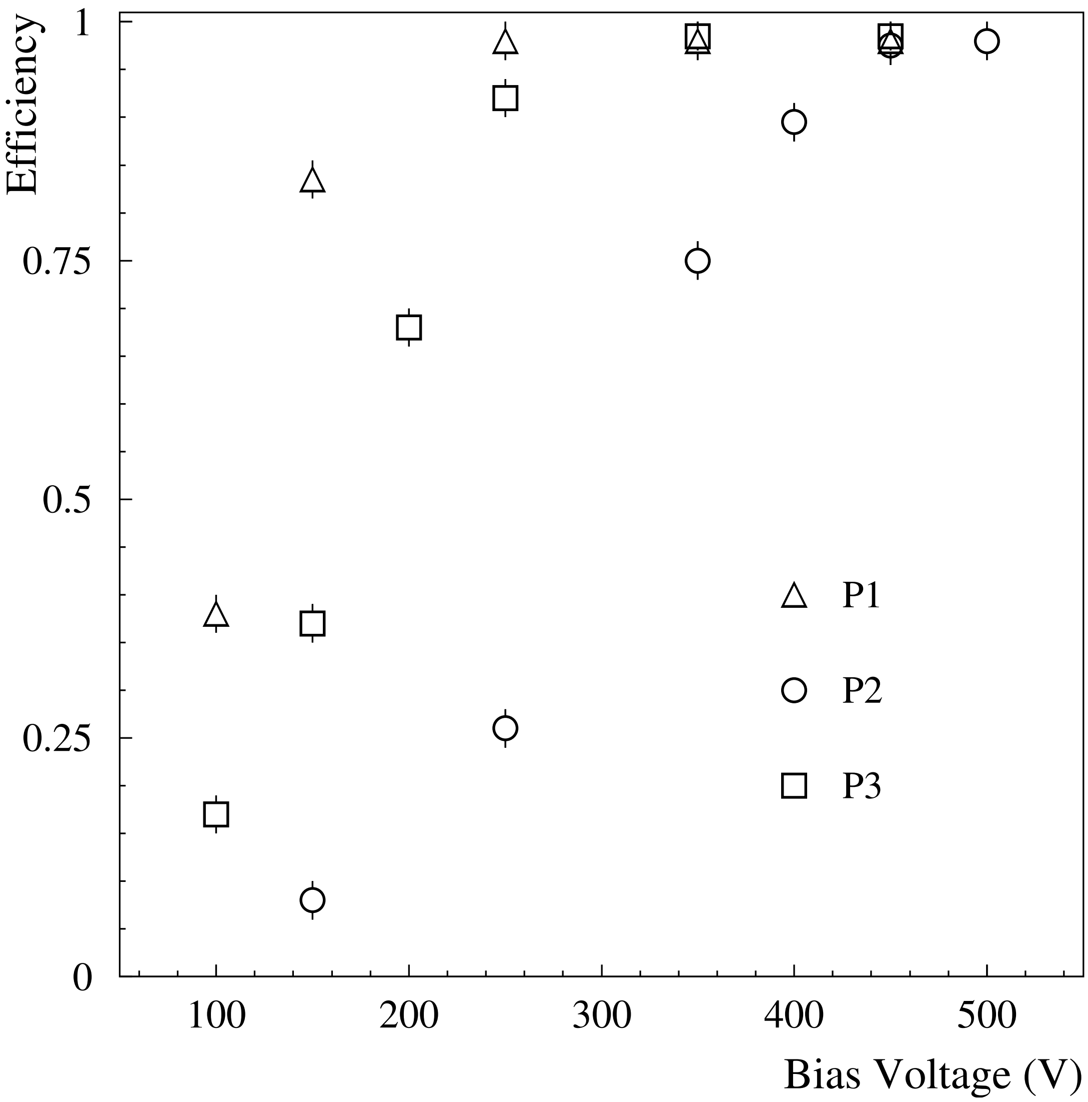

Figure 3: Measured efficiency as a function of bias voltage for three irradiated p-in-n detectors. This figure for **p-in-n** detectors is taken directly from [2].

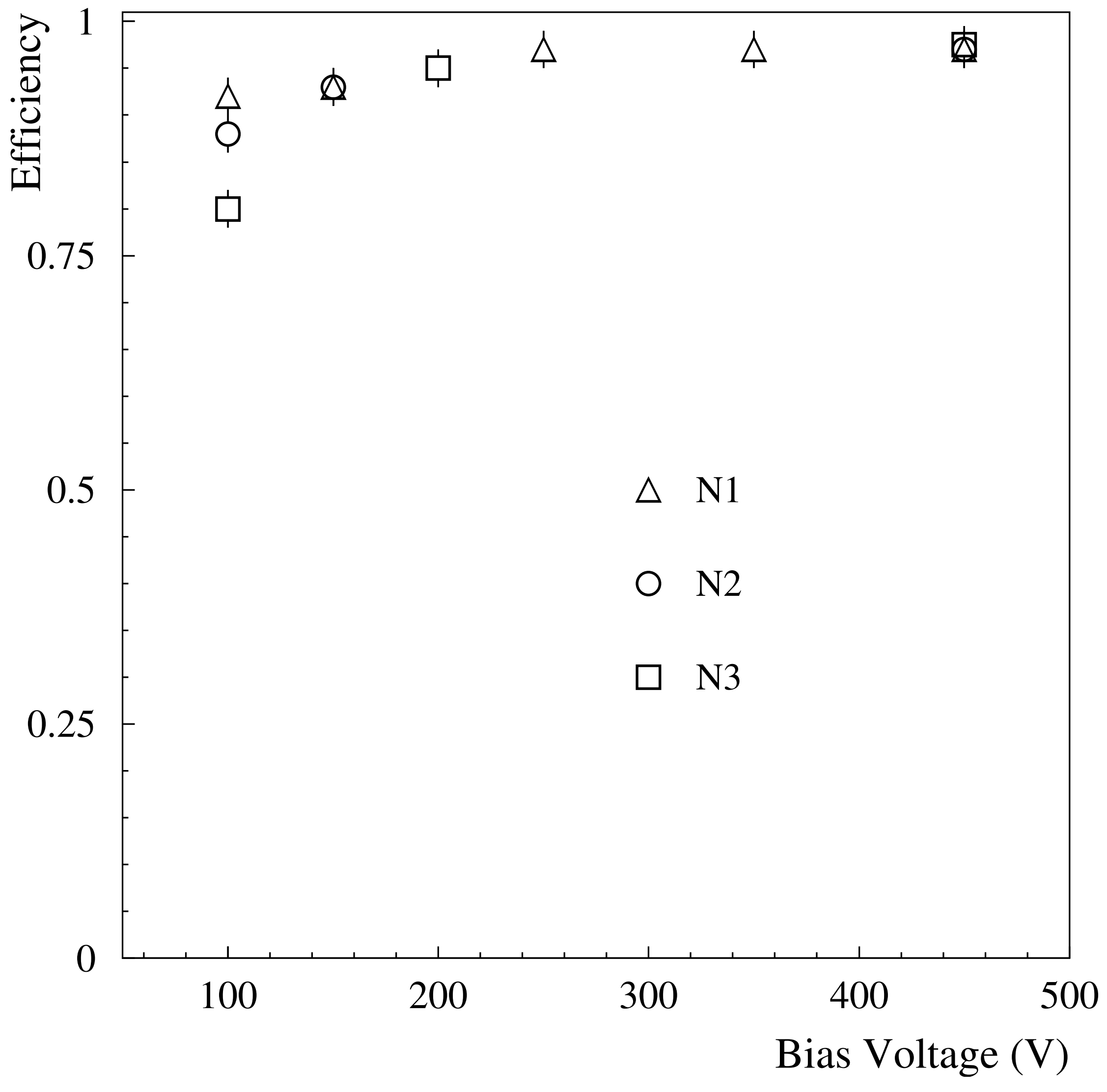

Figure 4: Measured efficiency as a function of bias voltage for three irradiated n-in-n detectors. This figure for **n-in-n** detectors is taken directly from [2].

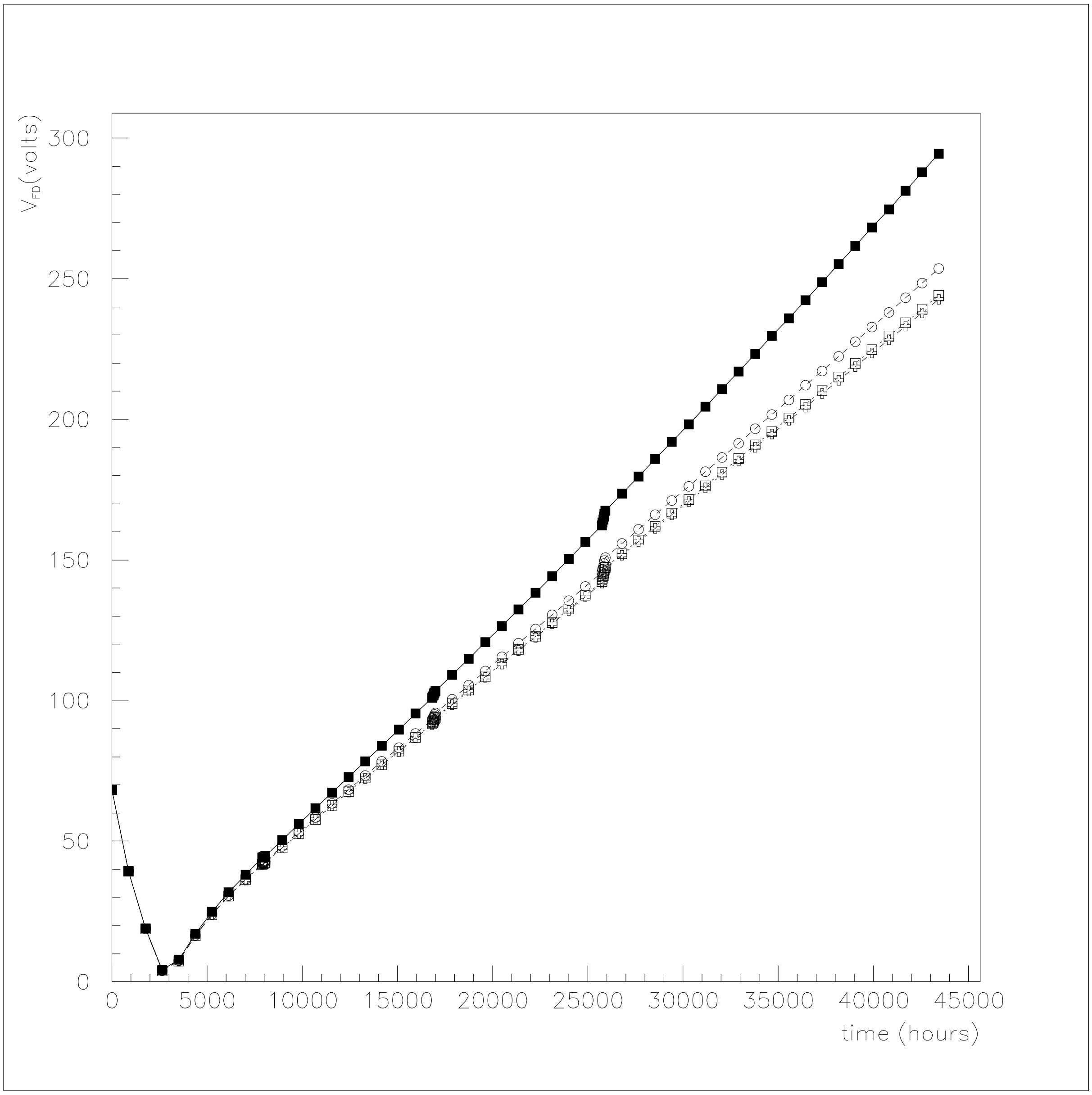

Figure 5: The depletion voltage as a function of time for detectors at temperatures, reading from top to bottom, of 20C, 10C, 0C, -10C.

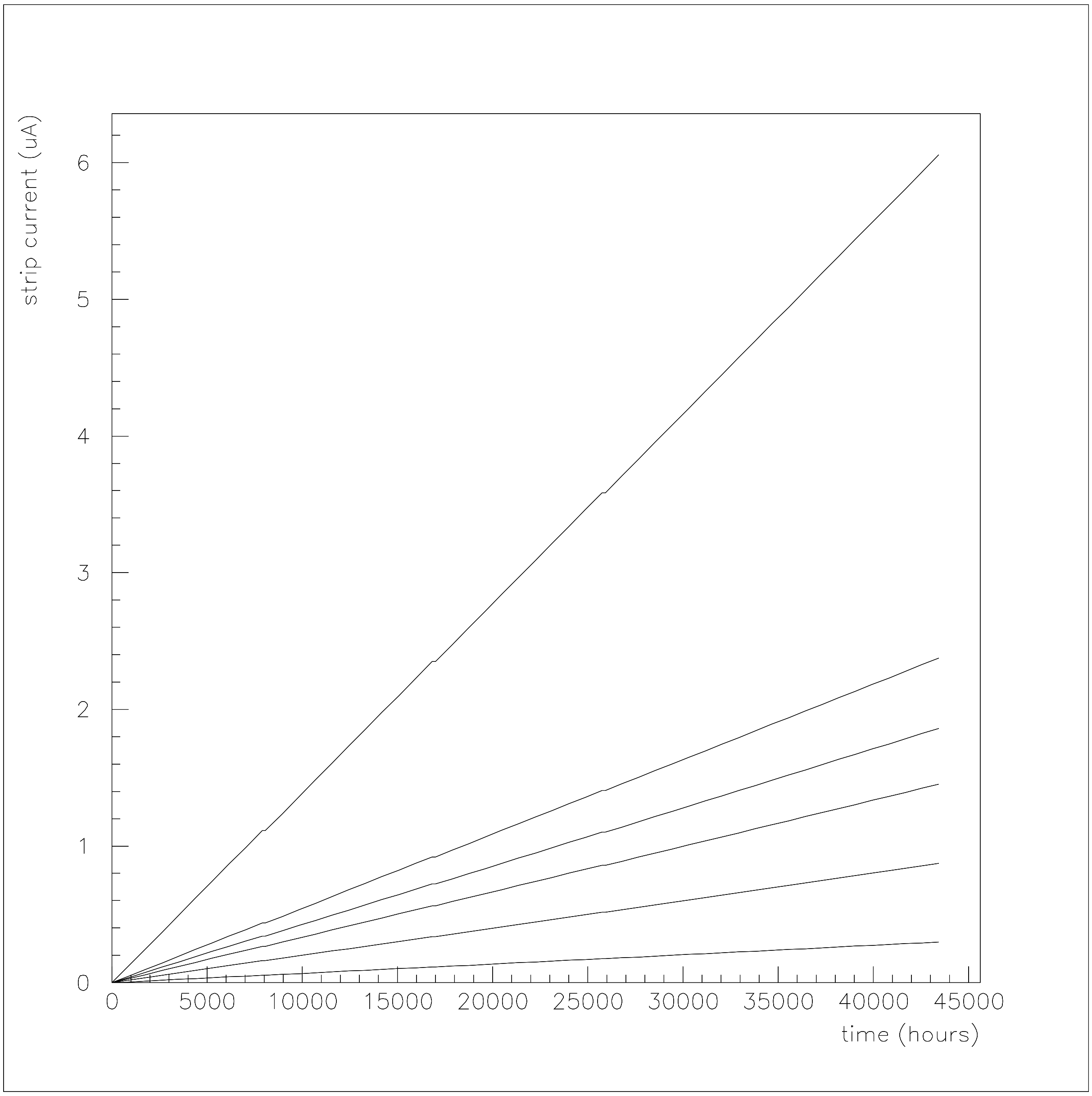

Figure 6: The strip current as a function of time for detectors at temperatures, reading from top to bottom, of 20C, 10C, 7.5C, 5C, 0C, -10C.