Velo HV slow ramp-down circuit

LHCB Technical Note

Issue: Draft
Revision: 1

Reference: EDMS xxxxxxxx
Created: 10th Feb 2009
Last modified: 10th Feb 2009

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Abstract

A protective RC circuit is designed and implemented in the Velo HV counting house patch panel. The purpose of the circuit is to slow down the ramp-down of the sensor high voltage to more than 1 s. This document presents an electrical model of the system and describes the design of the circuit. The issues about human and silicon sensor safety are addressed and a list of components is presented.

1. Introduction

The high voltages of the LHCb Velo sensors are supplied by a commercial ISEG power supply [1][2]. To ensure the safety of the detector in case of a failure of the control software the Velo is protected by a hardware interlock system [3]. This receives signals internal to the Velo (e.g. from temperature monitoring and cooling) and external signals (e.g. from BCM) and will switch off high and low voltages in case of an emergency.

When the ISEG HV power supply looses the interlock signal it will immediately switch off the high voltage without a ramp. The transition from 500 V to 0 V is in the order of 100 ms, which is deemed to be a too rapid change in voltage to be safe for the silicon sensors. Hence an additional circuit, located in the counting house patch panel, is implemented to slow down the ramp to acceptable levels. The aim is to keep the time constant of the circuit above 1 second.

2. Electrical circuit

2.1. Electrical model of the system

And electrical model of the system is necessary to predict the behaviour of the system in different scenarios and to design the appropriate protection circuit. Figure 1 shows the model of the system including the power supply, the hybrid, the silicon sensor and the protective RC circuit. The values of the components external to the protective RC circuit are approximately as follows:

- $\mathbf{R_{PS}}$ and $\mathbf{C_{PS}}$ are the output resistance and capacitance of the ISEG power supply. $\mathbf{C_{PS}}$ is approximately 10 nF estimated from the voltage decay at interlock when connected to an oscilloscope (100 ms ramp-down over 10 MΩ). $\mathbf{R_{PS}}$ is considered being small compared to all other resistances.

- $\mathbf{R_{LP}}$ and $\mathbf{C_{LP}}$ is the LP filter on the hybrid, where $\mathbf{R_{LP}}$ = 5 kΩ and $\mathbf{C_{LP}}$ = 10 nF.

- In the sensor is modelled by an ideal diode with the detector capacitance in parallel ($\mathbf{C_{det}}$) and a resistor ($\mathbf{R_{det}}$) to model the leakage current. $\mathbf{C_{det}}$ is approximately 1 nF and $\mathbf{R_{det}}$ will vary between 100 MΩ for a non-irradiated detector and 500 kΩ for a fully irradiated detector. Assuming that the leakage current increases from 5 µA to 1 mA at 500 V bias.

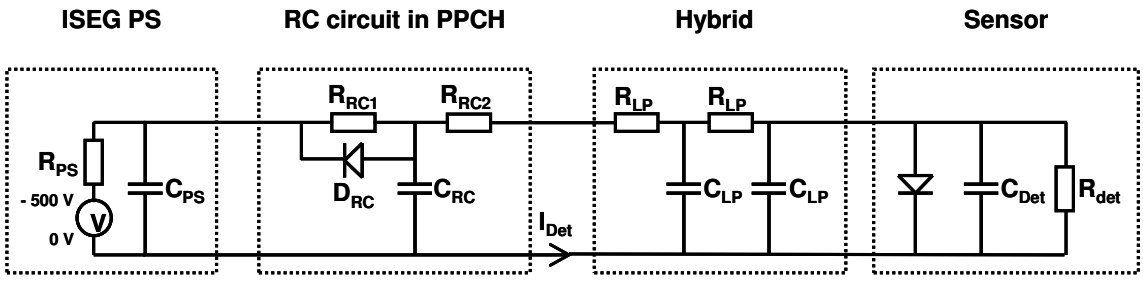

Figure 1: Schematic model of the system where all components are considered to be ideal

2.2. The RC circuit design

The concept of the protective RC circuit is to ensure a slow ramp-down by maintaining the voltage on a capacitor that is discharging in an appropriate rate. The rate of the discharge is determined by the effective RC constant. When an interlock is fired the voltage source in the ISEG is assumed to instantaneously go to 0 V. The capacitor $\mathbf{C_{RC}}$ will then discharge via two paths: via $\mathbf{R_{RC1}}$ and the power supply or $\mathbf{R_{RC2}}$ and the sensor. The values of these components are chosen to provide a good performance throughout the lifetime of the experiment. An additional constraint is that circuit have to fit in the counting house patch panel, giving a PCB surface area of 130 by 220 mm^2 for each group of 16 channels. Since high voltage capacitors grow very rapidly in size with increasing capacitance practical values for $\mathbf{C_{RC}}$ is maximum of a couple of µF.

For a non-irradiated circuit the discharge will be predominately via $\mathbf{R_{RC1}}$ and the power supply. Since this current goes in opposite direction of the normal detector leakage current, a diode $\mathbf{D_{RC}}$ is put in parallel with $\mathbf{R_{RC1}}$ to avoid a voltage drop over $\mathbf{R_{RC1}}$ in normal operation. Hence this resistance can be chosen to be very large. A choice of $\mathbf{R_{RC1}}$ = 5 MΩ and $\mathbf{C_{RC}}$ = 2 uF gives a time constant of 10 seconds.

When the equivalent detector resistance goes below 5 MΩ the discharge will be dominated by the detector current. Here it is not possible to put a large resistance in series since it can't be shunted by a diode in normal operation and hence will introduce a large voltage drop. So the RC constant will given by $\mathbf{C_{RC}}$ and the equivalent detector resistance $\mathbf{R_{det}}$. For a value of $\mathbf{C_{RC}}$ = 2 uF and $\mathbf{R_{det}}$ = 500 kΩ this gives a time constant of 1 second.

A resistor of moderate size ($\mathbf{R_{RC2}}$ = 10 kΩ) is added in series on the sensor side to limit the current in case of a short circuit at the between the bias line and bias return. The value is chose as large as possible while maintaining an acceptable voltage drop at high leakage currents. The voltage drop would be 10 V at 1 mA detector current. The resistor has a further benefit of limiting the current in case of sensor breakdown, see Section 3.2.

3. Safety implications

3.1. Human safety

Storing electrical charge at high voltage constitutes a safety issue in case of accidental discharge through the body of a human being. The safety limit at CERN for electrical discharge is a maximal stored energy of 10 Joule [4]. The energy stored in a capacitor is

$$E = \tfrac{1}{2} C U^2 .$$

The absolute maximum voltage that the ISEG HV power supply can deliver is 700 V, hence the maximal allowed capacitance for $\mathbf{C_{RC}}$ is 40 µF. The design value of 2 µF corresponds to 0.5 Joule stored energy at 700V, which is well below this limit.

3.2. Silicon sensor safety

3.2.1. Thermal run-away

In the case of thermal run-away, a delayed ramp-down of the high voltage will allow the temperature to increase further. Assuming that the energy of 10 Joule is transformed to heat in the silicon, the 2g silicon sensor will increase its temperature by 7 ˚C which is still acceptable. The design value of 500 V and 2 μF the stored energy is 0.25 Joule which will result in a temperature increase of 0.02 ˚C.

3.2.2. Voltage gradient

The maximal voltage gradient for a discharging RC circuit is given by

$$\left.\frac{dU}{dt}\right|_{\max} = U_0 / RC \quad \left[V/s\right].$$

At a bias voltage of 500 V and RC = 1 second this is 500 V/s. This value is significantly smaller in the early operation of the Velo when the RC constant is dominated by $\mathbf{R_{RC1}}$. For example before irradiation at 150 V and RC = 10 seconds the maximal voltage gradient is 15 V/s.

3.2.3. Maximal current

The current will be limited by $\mathbf{R_{RC2}}$ and $\mathbf{R_{LP}}$ in case of break down of some sort in the silicon sensor. The design values of these resistors are $\mathbf{R_{RC2}}$ = 10 k Ω and $\mathbf{R_{LP}}$ = 5 kΩ, giving a total series resistance of 20 kΩ. For a shorted detector ($\mathbf{R_{det}}$ = 0) the time constant becomes 40 ms and with 500 V bias the maximal instantaneous current becomes

$$I_{\max} = \left.\frac{dQ}{dt}\right|_{\max} = C \cdot \left.\frac{dU}{dt}\right|_{\max} = 25\,mA\,.$$

If this current is spread over the whole sensor surface area (27 cm^2) it does not damage the sensor. However, spread over a sufficiently small surface area it could cause damage. The size of the affected area depends on the nature of the break-down. The influence of the protective RC circuit on fast processes in the silicon is somewhat moderated by the fact that it is located 70 m cable distance away.

QUESTION: at what current density do we start to worry about sensor damage?

4. Physical implementation

The protective circuit is located in the counting house patch panel, where each PCB handles 16 HV channels. Three of these are mounted in each patch panel which limits the size of each PCB to 130 by 220

mm^2. For each channel two resistors, one capacitor and one diode are required. The proposed components are the following:

- **R_{RC1}**: KOA HV733ATTD4704F, Farnell order code 1627941. Resistor 4.7 MΩ, case SMD 2512, 3000V rating. http://www.farnell.com/datasheets/121943.pdf. Price GBP 0.24 e.a.

- **R_{RC2}**: WELWYN PWC2512-10KJI, Farnell order code 1100131. Resistor 10 kΩ, case SMD 2512, 500V rating. http://www.farnell.com/datasheets/80991.pdf. Price GBP 0.44 e.a.

- **D_{RC}**: VISHAY BYG10M, Farnell order code 9549170. Diode, case DO-214AC, 1000V, 1.5 A rating. http://www.vishay.com/docs/88957/byg10d.pdf. Price GBP 0.116 e.a.

- **C_{RC}**: ILLINOIS CAPACITOR 225MABA05KJS, Farnell code 9681485. Capacitor 2.2 uF, 1150 VDC rating, size 42.5x37x28 mm^3 (LxHxW). Array of 4x4 diodes needs area 180 x 120 mm^2. http://www.illinoiscapacitor.com/search/main/pdf2/Series/MAB.pdf. Price GBP 5.37 e.a.

Cost estimate for passive components: GBP 620

Cost estimate for 10 PCBs: 300 Euro

Cost estimate for box connector cases: CHF 660

Cost estimate for box connector pins: CHF 1000

Cost for PCB connectors and pins on PCB: ???

Total cost: minimum CHF 3200

5. References

[1] 'Characterisation of the VELO High Voltage System', B. Rakotomiaramanana et al., LHCb Internal Note 2008-009

[2] 'High voltage Connectivity', B. Rakotomiaramanana et al., EDMS document 836439

[3] 'Velo interlocks', A. van Lysebetten et al., EDMS document 706629

[4] 'Dangers due to electricity', TIS, EDMS document 335796