Characterisation of the VELO Low Voltage System

Internal Note

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Abstract

The low voltage system of the VELO and Pile Up is required to supply voltage to the repeater board and hybrid for 88 modules. The system is based on the CAEN Embeddeed Assembly System where the voltage is supplied by a CAEN A3009 power supply board. The boards were tested to ensure that were within the CAEN specifications using a dummy load with and without the final cables. The system was then tested using the final low voltage slice. The C side has been extensively tested and is ready to power the modules.

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+3.3V +5.3V -5.3V

3 VELO Low Voltage System

The VELO Low Voltage system is based on the CAEN EASY3000 Embedded Assembly System[**?**]. The system is controlled by two A1676A branch controllers which are plugged into a SY1527 mainframe. The EASY3000 crate is populated with A3009 12 channel 8V power supply boards. One crate can contain up to 5 A3009 boards. The crates are powered by an external 48V supply. A CAEN A3486 48V supply is used to provide two independent 48V supplies: one channel gives the 48V power to the regulators and the other provides the 48V power to the control logic (48V Service).

3.1 CAEN A3009 Power Supply board

The CAEN A3009 power supply board has 12 floating 8V/9A/45W output channels and is described in [1]. The version used in the VELO has APP30[a] output connectors and the front panel is shown in figure 1. The output channels of the A3009 boards have a remote sensing line to compensate for the voltage drop over the cables. The voltage sensing circuit is shown in figure 2.

There are a number of parameters which can be set: V0Set is the voltage at the load; SVMax is a software protection limit above which the voltage cannot to be set; I0Set is the over current threshold; Trip is the trip time[b]. A number of parameters can be read back: VMon is the voltage on the load; VCon is the voltage on the output connector; Imon is the current delivered by the channel. The channel output characteristics of the board are summarised in figure 3.

4 Testing the A3009 Modules in D3

4.1 Dummy Load

A dummy load was constructed to test the 8V supplies. It contained of 6 resistor chosen to mimic the expected current on the hybrid and repeater board. The PCB inside the load is shown in figure 4. The loads were enclosed in a box and cooled using a fan inside. There also external connections to the loads referenced to a common ground. In total two modules were made corresponding to one A3009 board.

4.2 Test Setup

The functionality of the A3009 boards was by tested by connecting each board to dummy loads in D3 using 1m cables connected directly to the supply. The dummy loads rested on a table in front of the rack and the board was controlled from a keyboard and monitor connected directly to the Sys1527 mainframe. The same slot on the Easy crate was used to test each board in turn. The test setup is shown in figure 5.

[a] Anderson Powerpole®30 Amp connector
[b] By default this is set to 1000s so had to be changed on every board.

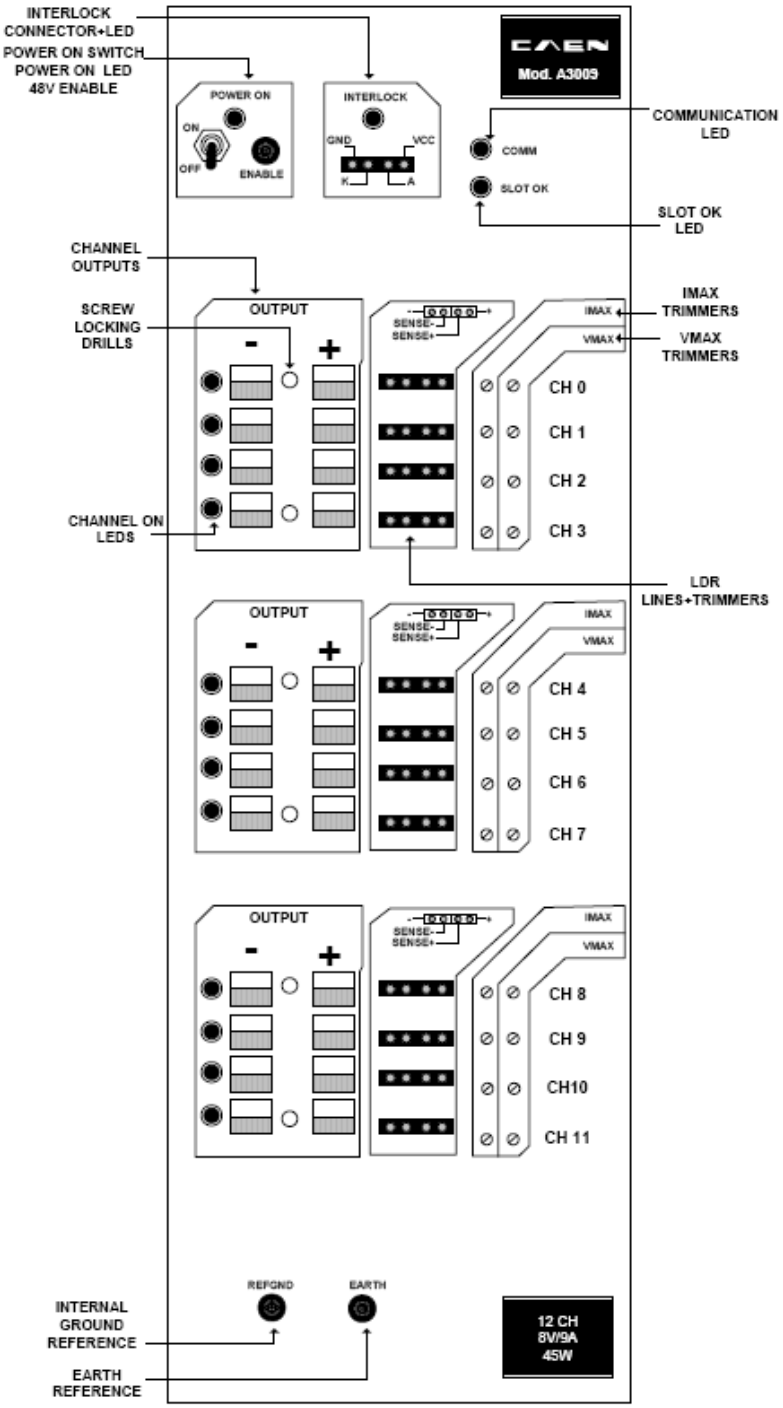

Figure 1 A3009 front panel[1].

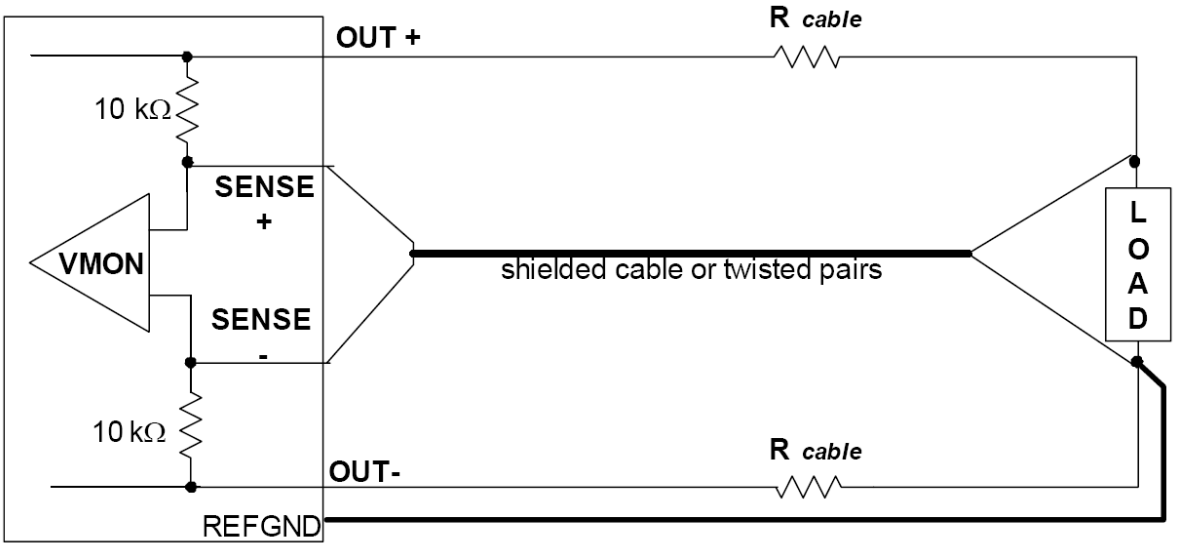

Figure 2 Remote voltage sensing scheme[1].

4.3 Linearity of the Supplies

4.3.1 Voltage Set

The linearity of the supplies was tested by changing the value of V0set to different values up to the nominal voltage on each channel. The value of the monitored voltage (Vmon) versus the set value is show in figure 6 for one module. The mean value of the difference between the measured and expected voltages was calculated for each channel and is shown as function of the module number in figure 7. The mean value per channel averaged over all modules is shown in figure 8. Two channels on one A3009 board are marginally outside the CAEN specifications.

The data was stored in excel spreadsheets until a PVSS panel was developed to automatically scan the channels with the different values of V0Set.

4.3.2 Current Trip Limit

The value of I0set was changed on each channel until the channel went into an over current state. The difference between I0Set and IMon was taken and is shown as a function of module number in figure 9. This difference was averaged over all supplies and is shown as a function of channel in figure 10.

4.4 Ramping Rates

An oscilloscope was configured to trigger on signal with an slope. Each channel was turned on and the scope was used to measure the time taken until the nominal voltage was reached. The time taken to turn off the channel was measured by configuring the scope to trigger on a down slope. The time taken to turn off the voltage after an interlock was measured in the same way. Typical trace plots for ramping up and down the channels are shown in figures 11 and 12. The average times per channel is shown in figure 14.

4.5 Noise

The noise on every channel was measured using an oscilloscope and a screen dump was taken. A typical trace plot from is shown in figure 15. There are peaks which appear with a frequency of around 155 kHz. The voltage ripple should be below 20 mV pp on 10μF.

Polarity:	Floating
Output Voltage[3]**:**	1.5 ÷ 8 V (connector output)
Max. Output Current:	9 A
Voltage Set/Monitor Resolution:	5 mV
Current Set/Monitor Resolution:	10 mA
VMAX hardware:	1.5 ÷ 8 V
VMAX hardware accuracy:	± 2% of FSR
VMAX software:	1.5 ÷ 8 V
VMAX software resolution:	5 m V
Voltage Ripple: [4]	<20mV pp on 10µF //0.1 µF 10Hz-15MHz
Voltage Monitor vs. Output Voltage Accuracy: [5]	max. ±30 mV ±0.3% of reading
Voltage Set vs. Output Voltage Accuracy: [5]	max. ±30 mV ±0.3% of reading
Current Monitor vs. Output Current Accuracy: [5]	± 0.05A ± 2% of reading
Current Set vs. Output Current Accuracy: [5]	± 0.05A ± 2% of reading
Load Regulation: [5]	± 0.3 % (with sense wires) ± 2 % (without sense wires)
Output power:	45 W per channel
Test Set Up:	cable: length = 20~30m; ∅= 10mm (for both output and return) with sense wires connected test load: 250÷2000 W (nominal) load capacitance: 100µF electrolytic // 100nF ceramic (// to the load)
48Vin (Power & Service)	45÷51Vdc

Figure 3 Channel characteristics of the A3009 power supply board[1].

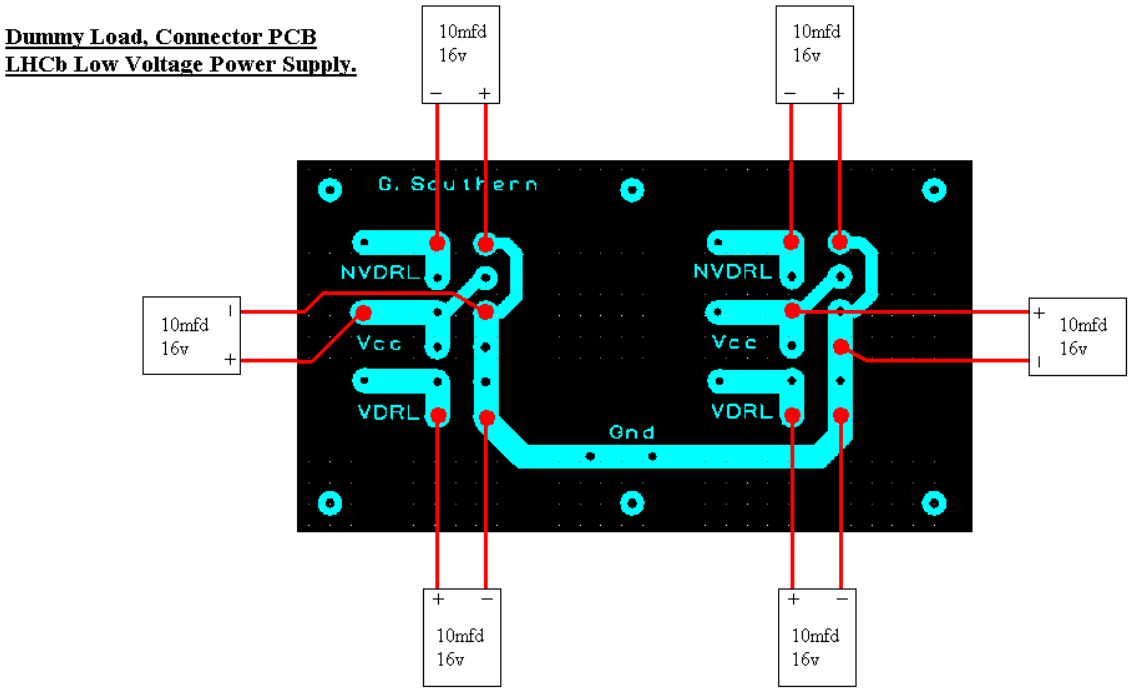

Figure 4 PCB for dummy load.

One problem channel was found in this way where there was a 350 mV oscillation found on a single channel in the module. This is shown in figure 16. The module was sent back to the manufacturer for repair.

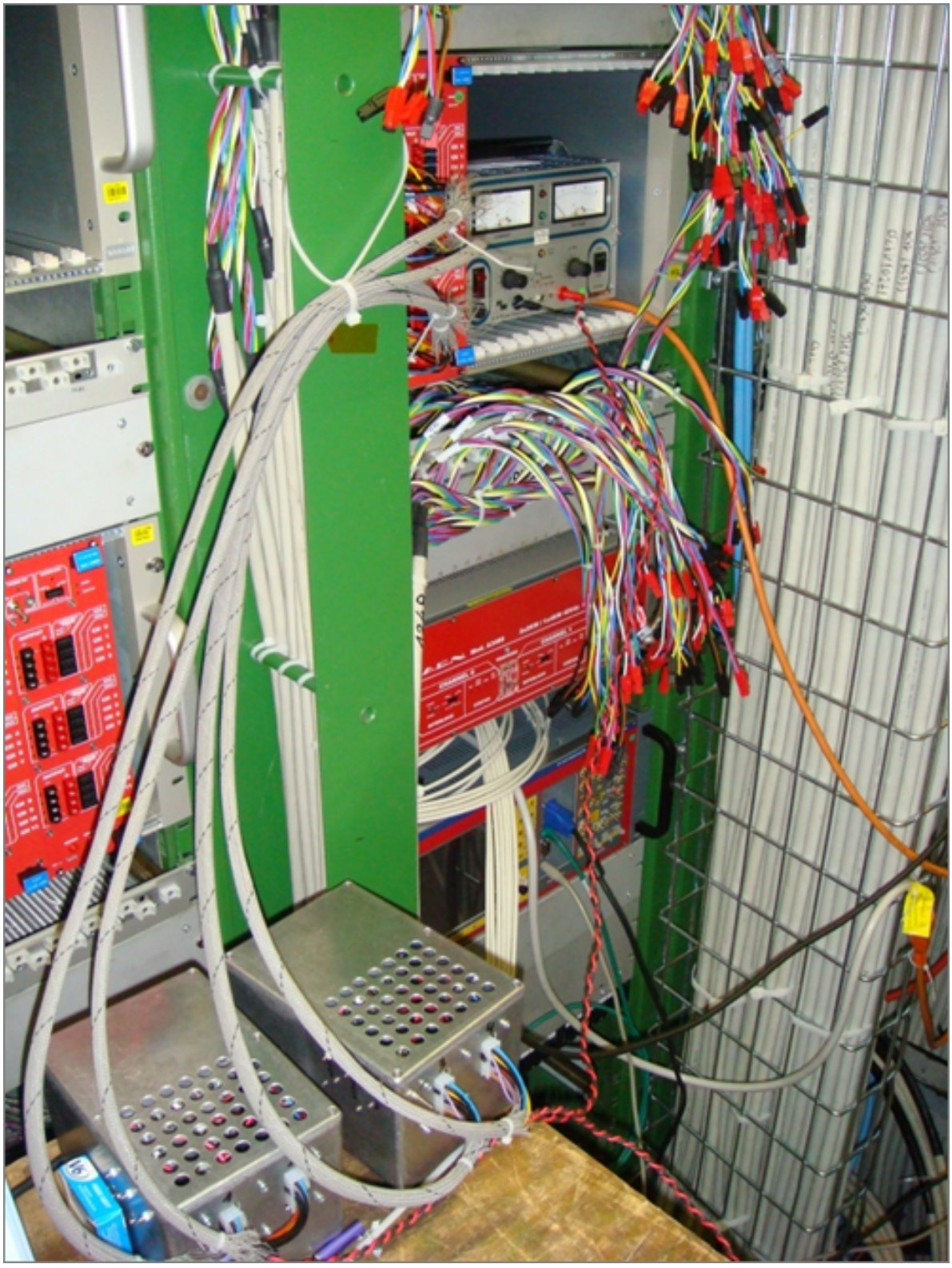

Figure 5 The test setup in D3.

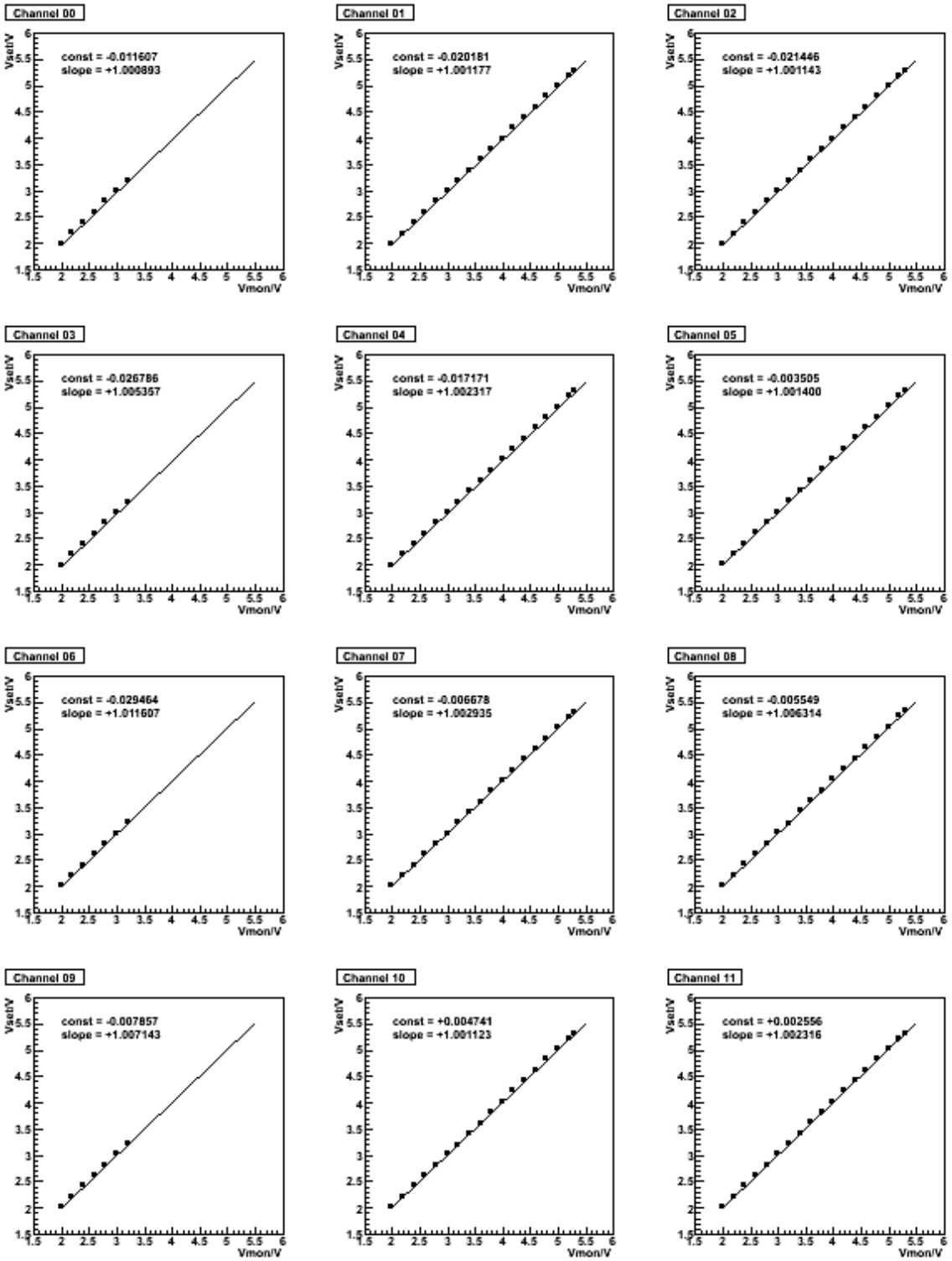

Figure 6 Vmon vs V0set for each channel of module 70620142.

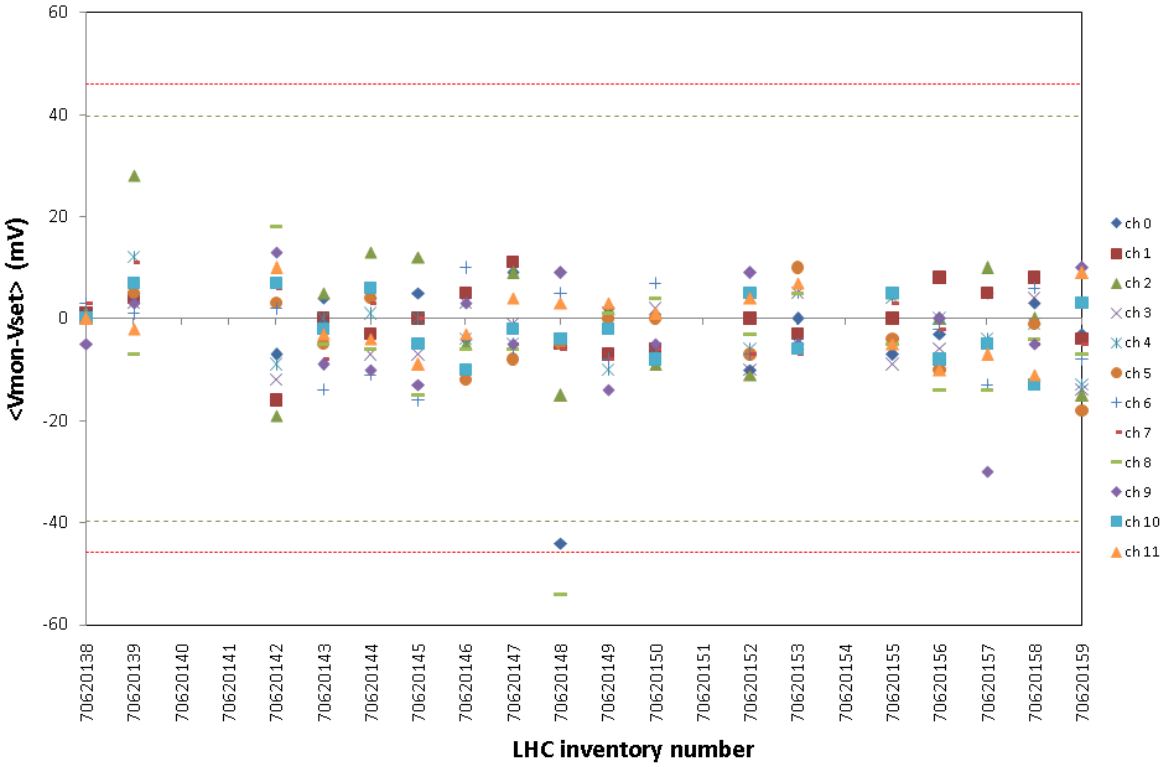

Figure 7 The mean value of the difference between Vmon and Vset for each channel as a function of the module number. The dashed lines are the maximum expected output voltage accuracy for +3.3V (green) and +5.3V (red).

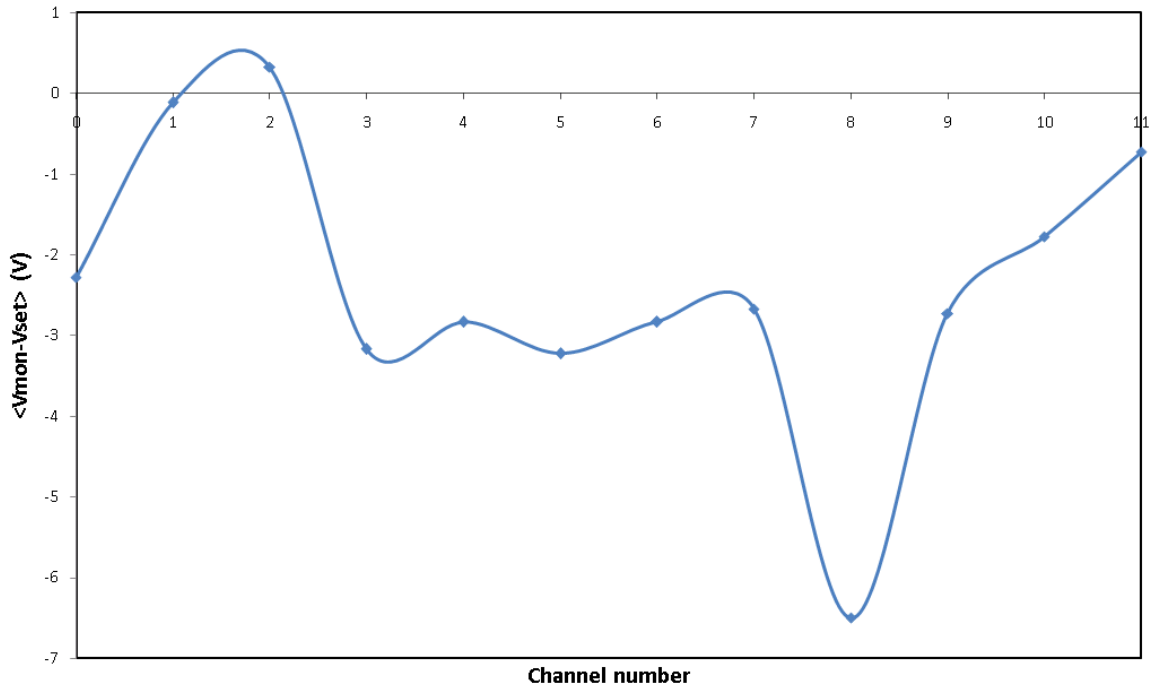

Figure 8 The mean value of the difference between Vmon and Vset averaged over all of the A3009 supplies as a function of channel.

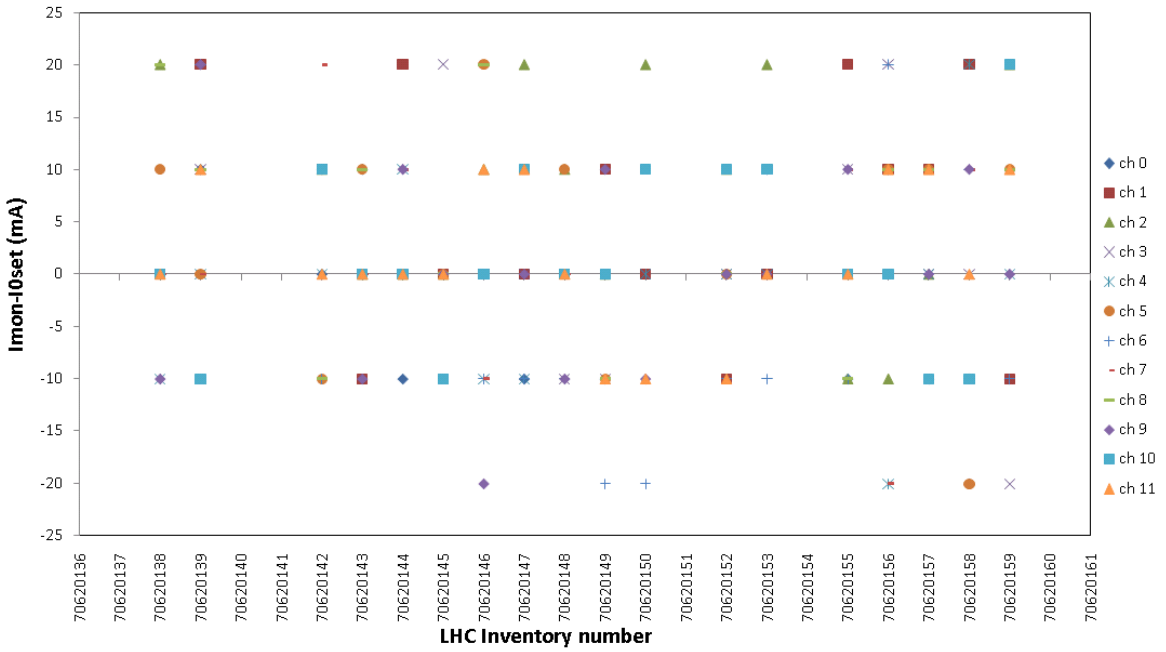

Figure 9 The difference between Imon and I0set as a function of LHC inventory number for each channel.

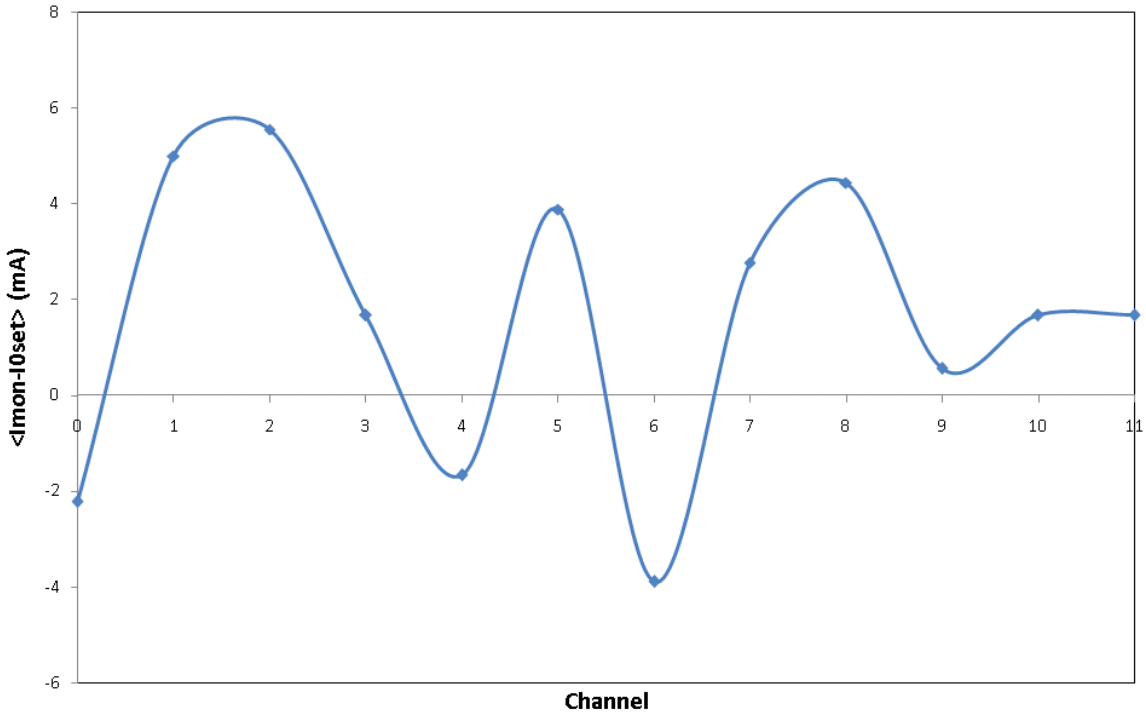

Figure 10 The mean value of the difference between Imon and I0set averaged over the all supplies as a function of channel.

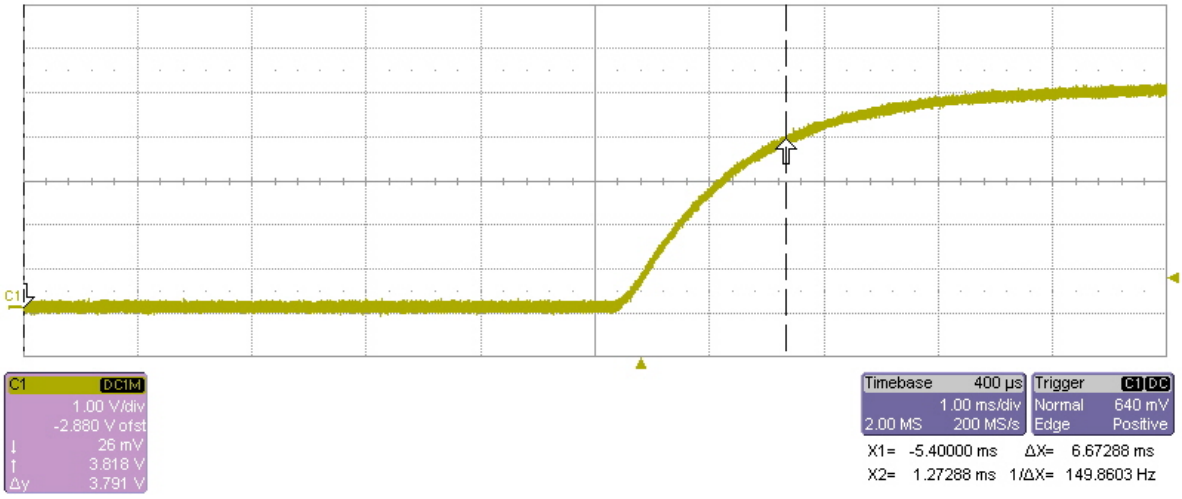

Figure 11 A typical scope trace of the time taken to ramp up a channel to its nominal voltage.

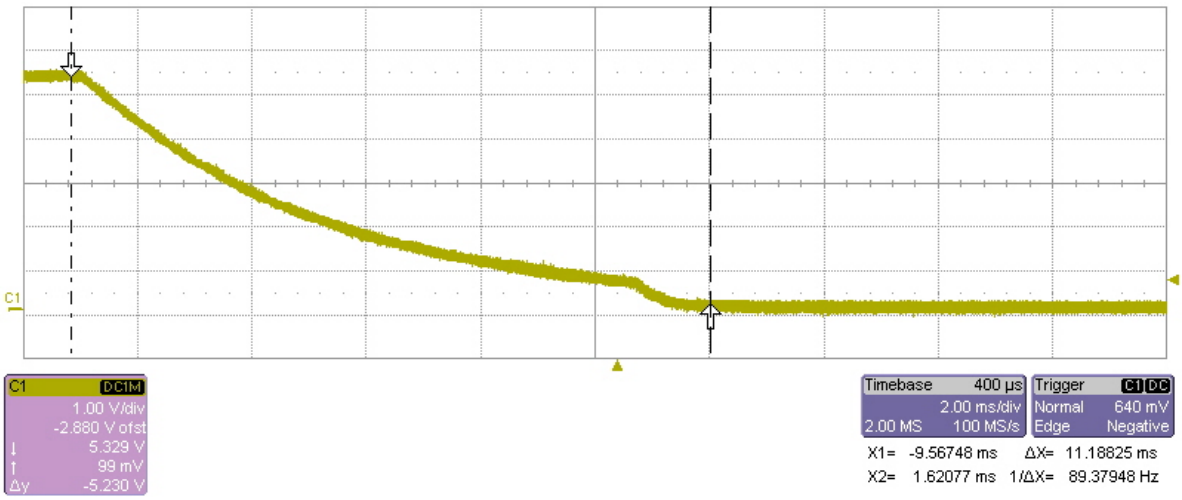

Figure 12 A typical scope trace of the time taken to ramp down a channel to its nominal voltage.

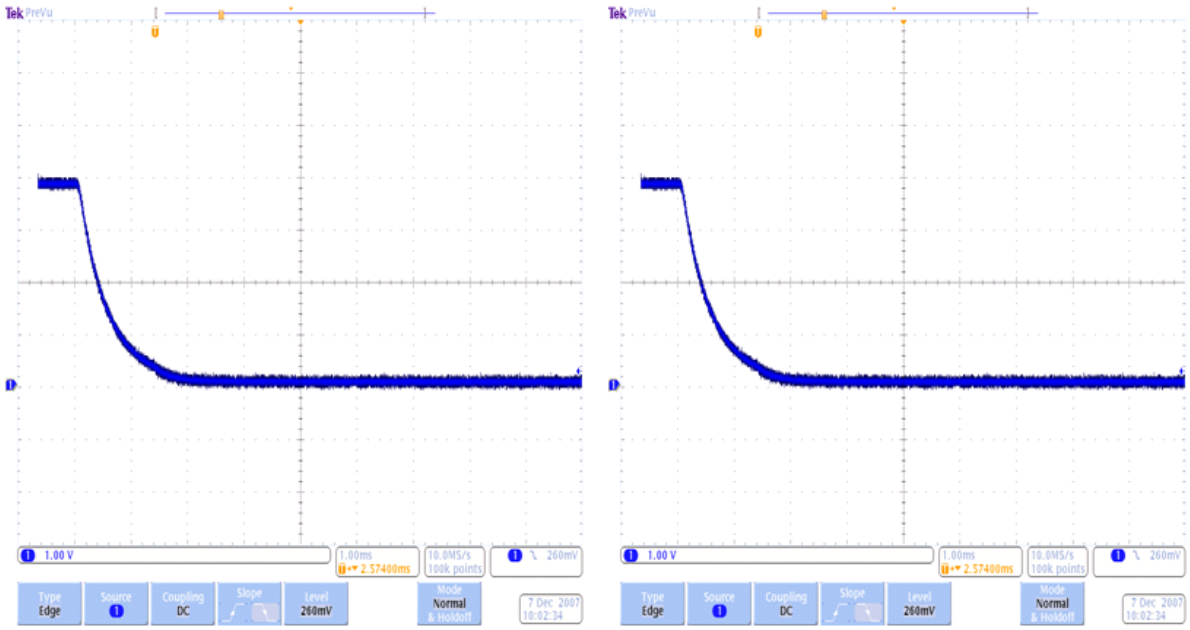

Figure 13 Typical trace plots of the time taken to ramp down a module in normal operation (left) and after an interlock signal was forced (right). The traces are identical.

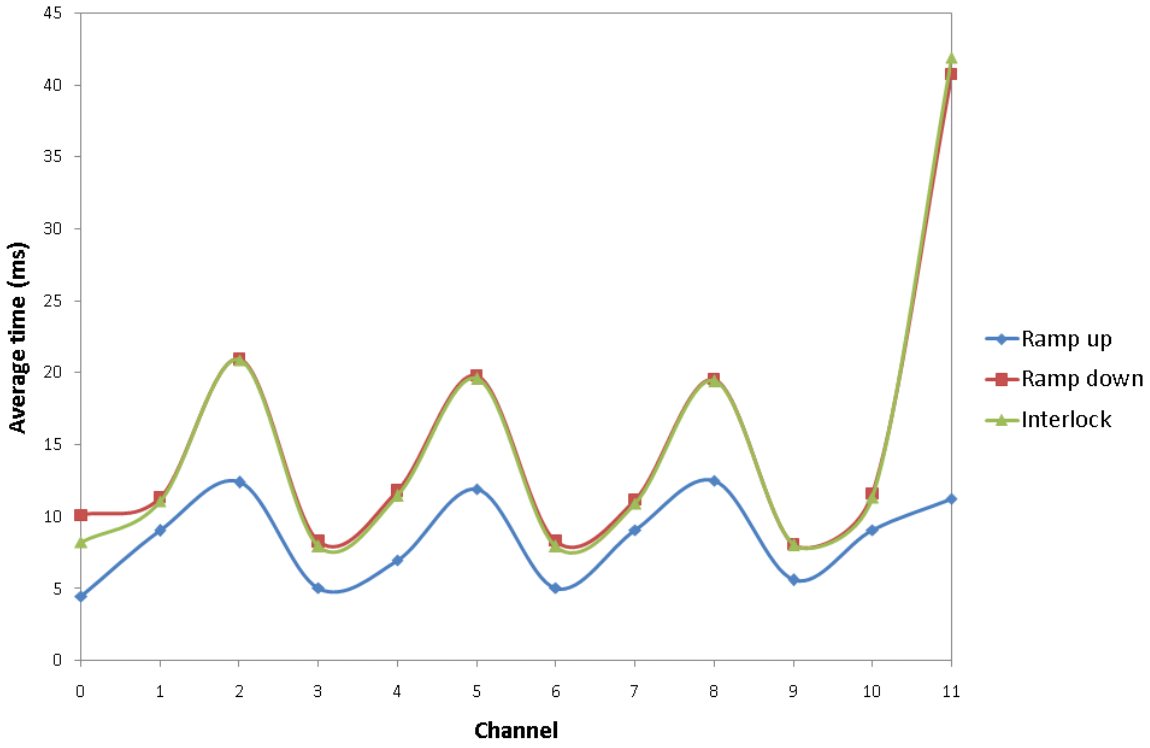

Figure 14 Average ramping times per channel.

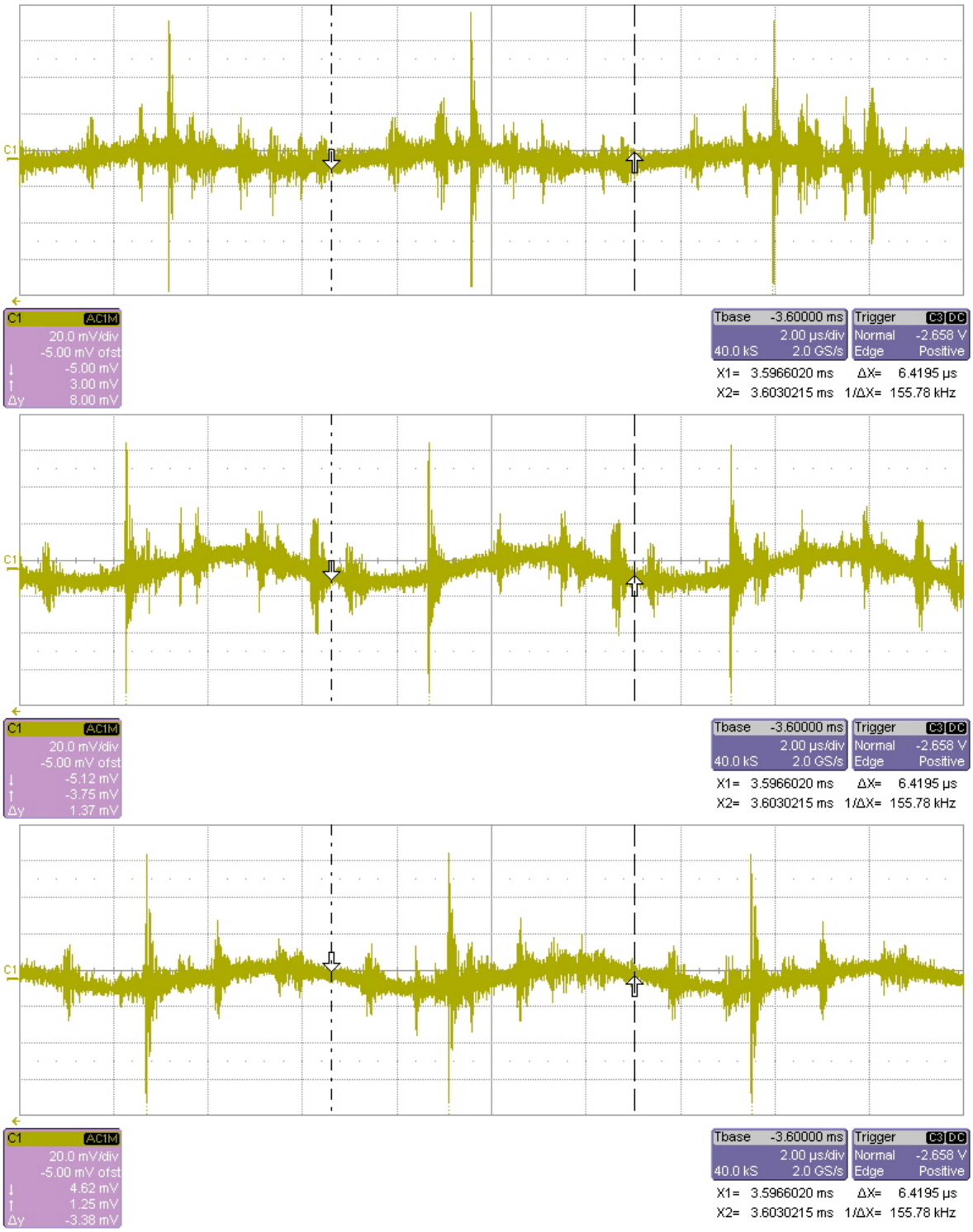

Figure 15 Typical noise measured on channels corresponding to the hybrid (top), positive driver (middle) and negative driver (bottom) voltages .

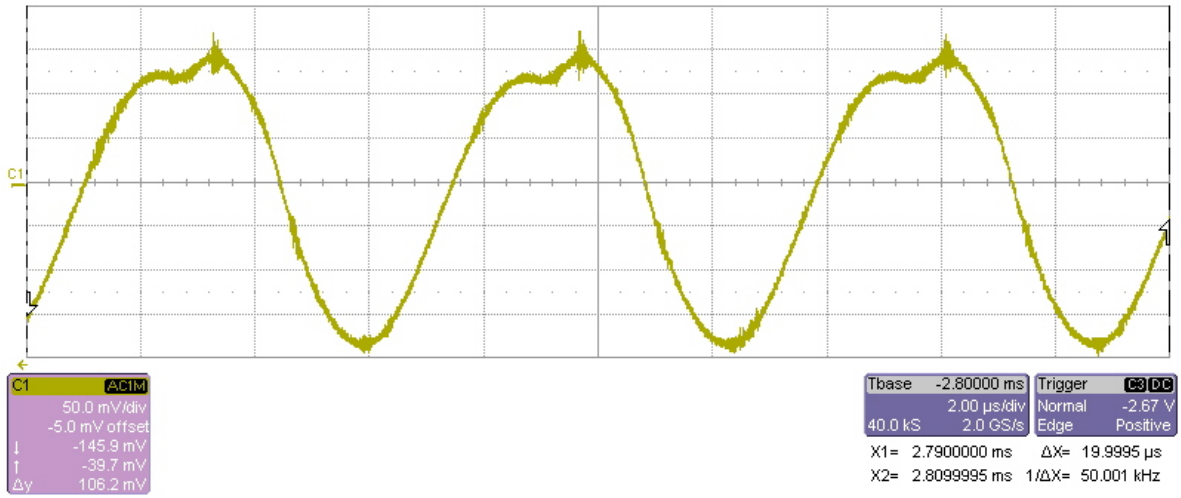

Figure 16 A problematic channel found by measuring the noise on an oscilloscope. The voltage ripple should be below 20 mV but it was around 350 mV on this channel.

5 Testing the A3009 Performance at the VELO

The A3009 modules were put in position in the Easy crate and connected to the long cables and sense lines. Teh branch controller corresponding to teh C side was configured with two fully populated Easy3000 crates and a 48 power supply. This meant that 20 VELO modules could be fully powered.

5.1 Testing the Long Cables with Dummy Load

5.1.1 Monitoring the Supplies

The dummy load was connected to each low voltage cable on the C side of the VELO. The three corresponding channels were switched on to their nominal voltage. The values of Vmon, Vcon and Imon were measured and they are shown in figures 17 to 20. The voltage drop across the cables is measured by taking the difference between the voltage on the output connector (Vcon) and the voltage on the load (Vmon). This value was then used to calculate the resistance of the cables/connectors as shown in figure 21.

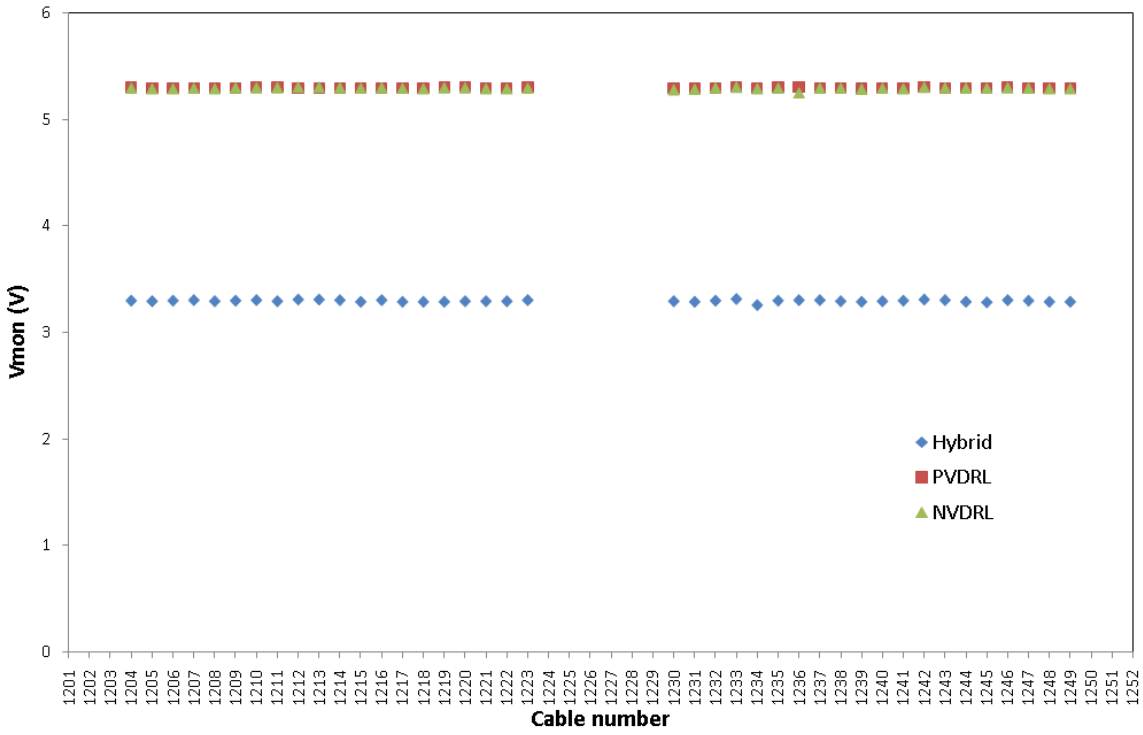

Figure 17 The voltage measured at the load (Vmon) as a function of cable number with the supply connected to the dummy module at the end of the long cables.

The value of the monitored voltage is stable. The variations in the supply voltage and the resistance of the cables was traced to bad connections between the anderson connector and the board. The effect can be demonstrated by moving the cables in D3. After moving the cables, one or more channels could go in HVMax state which happens when the supply voltage increases to compensate for the voltage drop along the cables. The cables should be shielded on the crate.

5.1.2 Noise Measurements

The noise on every channel was measured with an oscilloscope when the dummy load was connected to the long cables. The spikes seen in figure 15 were filtered by the 60m cables. Typical trace plots can be seen in figure 22.

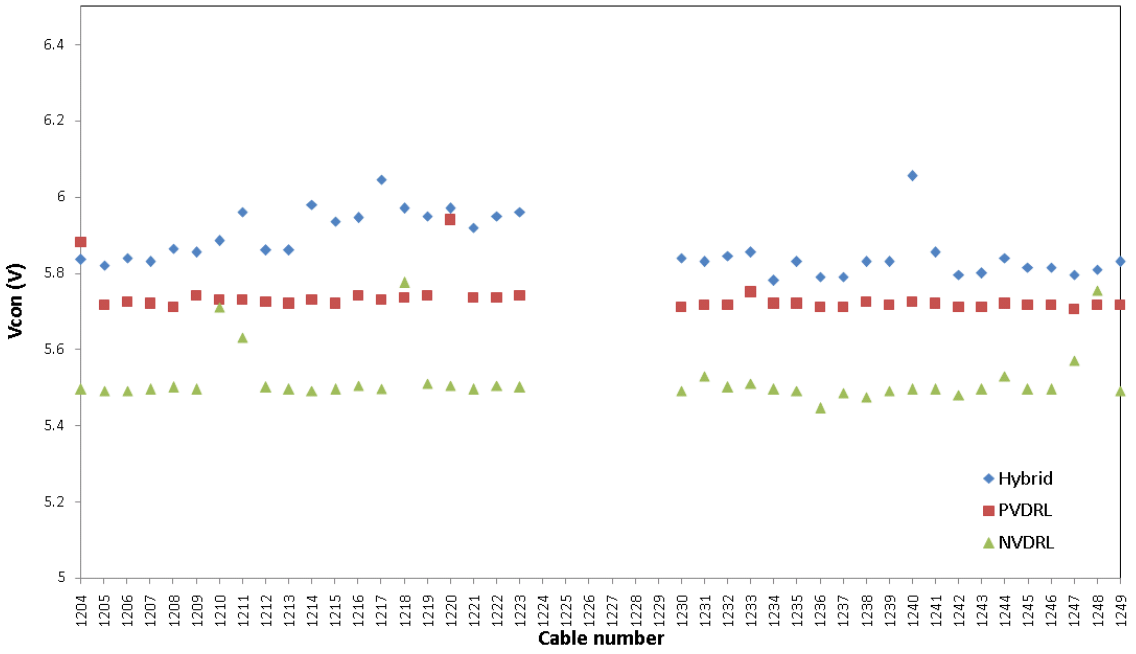

Figure 18 The voltage measured at supply (Vcon) as a function of cable number with the dummy module connected to the long cables.

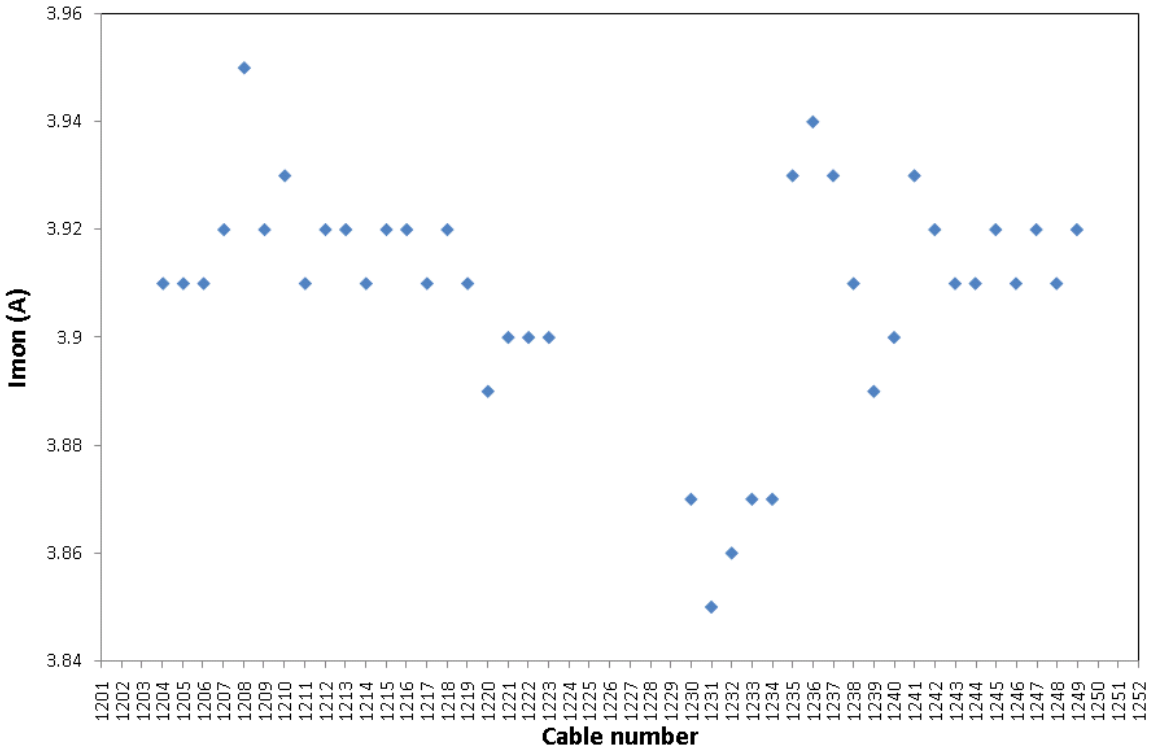

Figure 19 The current measured on the hybrid channel of the dummy load as a function of cable number with the load connected to the long cables.

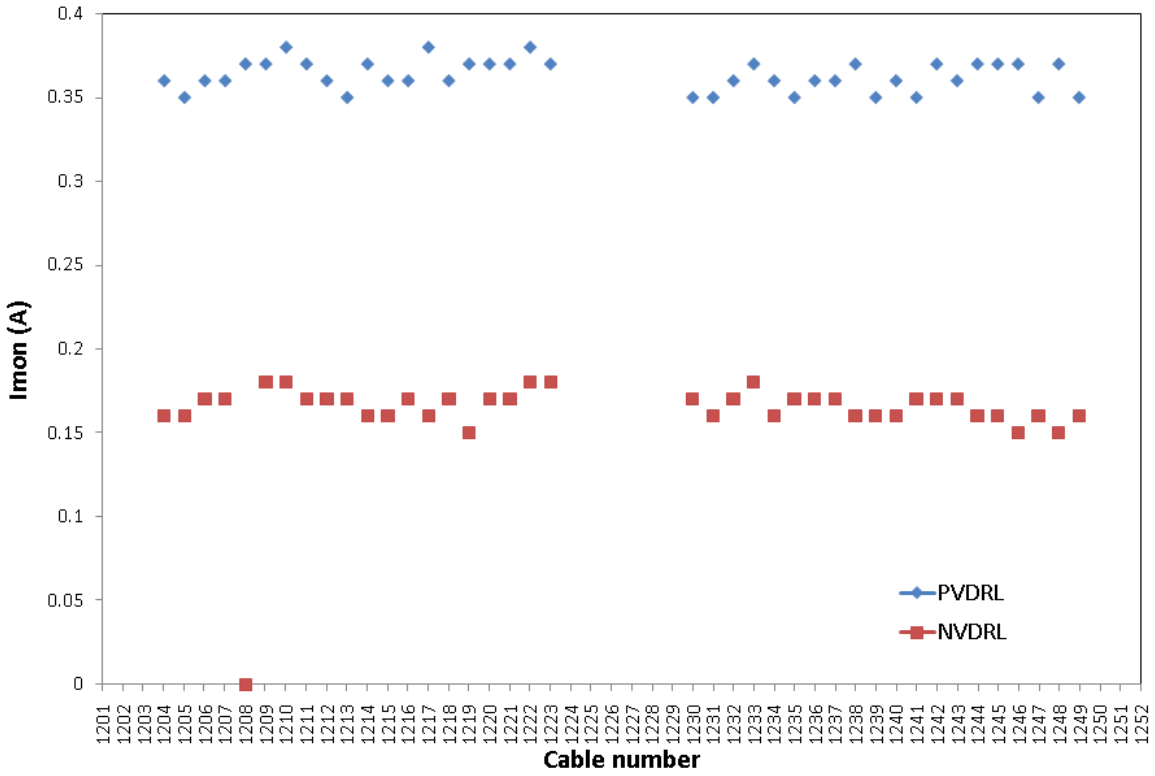

Figure 20 The current measured on the repeater channels of the dummy load as a function of cable number with the load connected to the long cables.

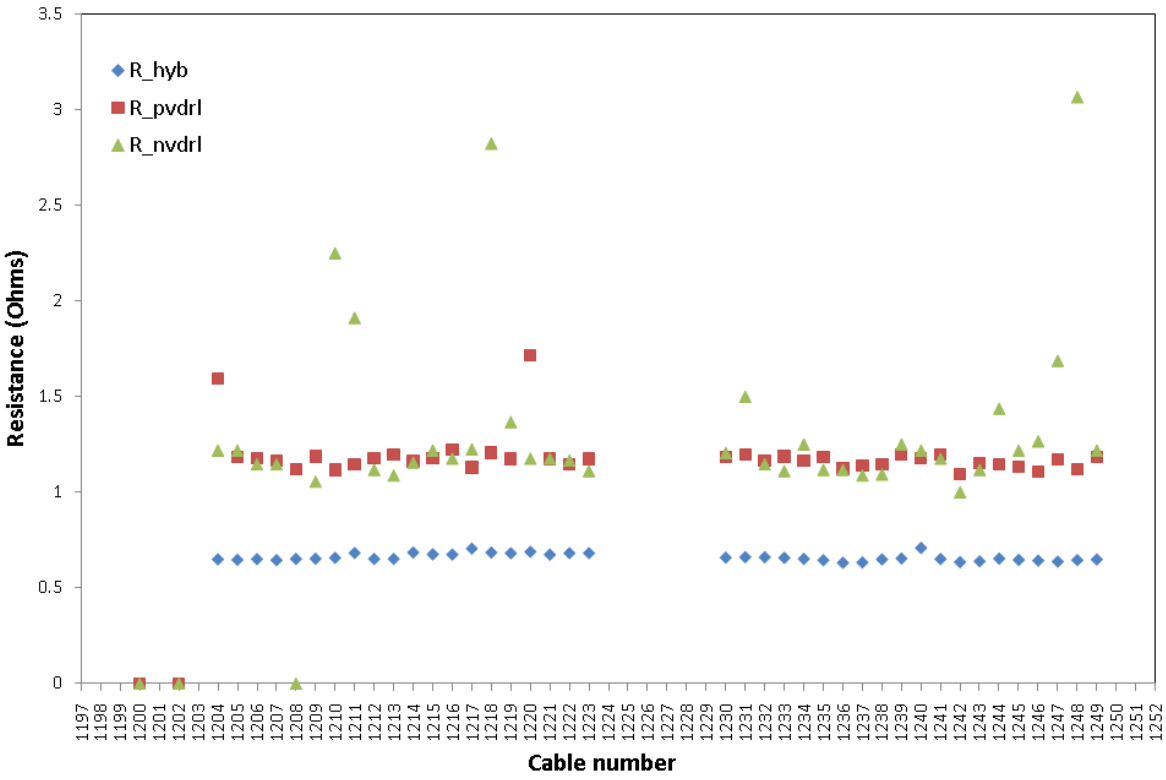

Figure 21 The resistance of the cables/connectors as a function of cable number measured with the dummy load connected to the long cables.

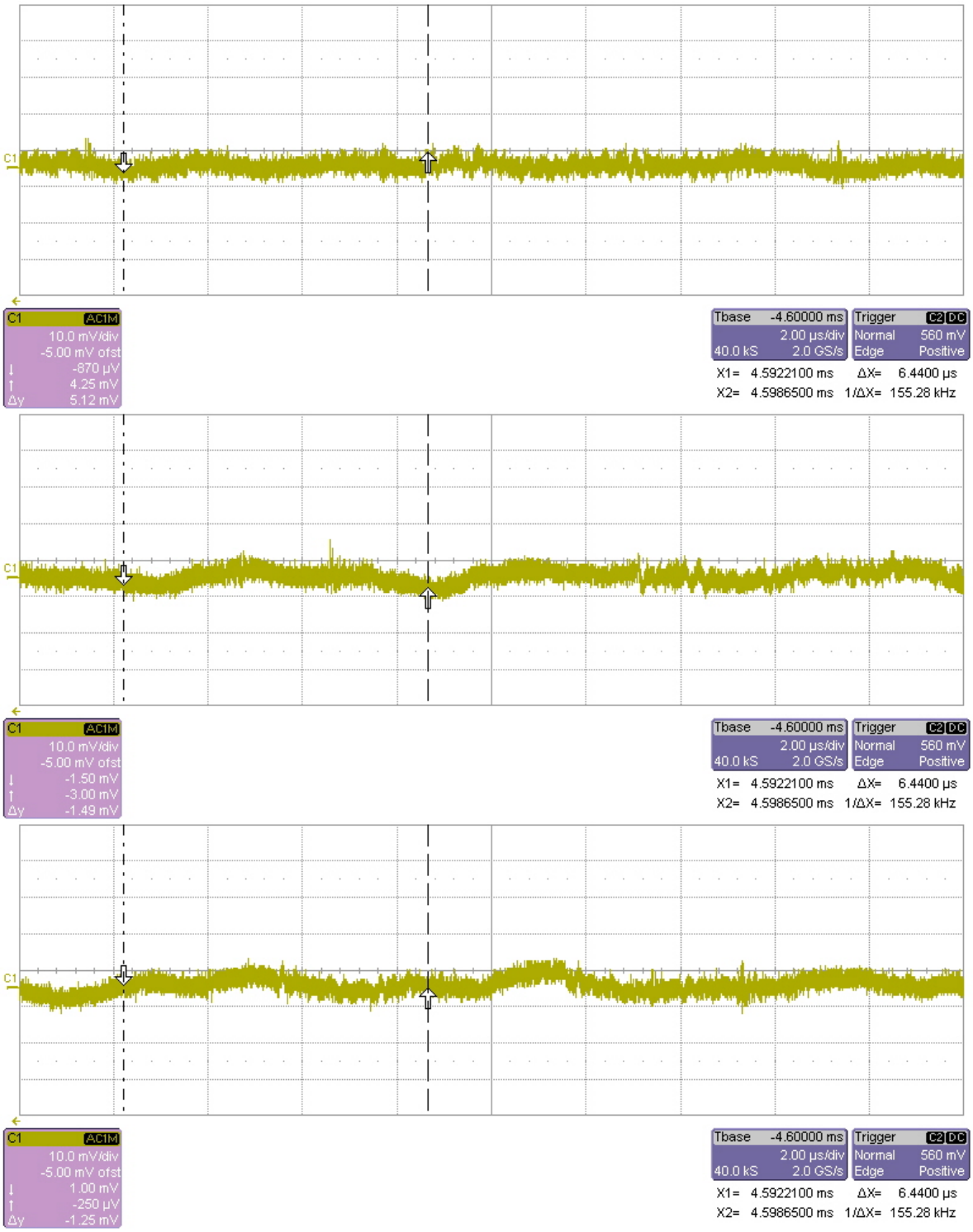

Figure 22 Typical noise measured on channels corresponding to the hybrid (top), positive driver (middle) and negative driver (bottom) voltages with the load connected to the long cables.

5.2 Testing the Long Cables with a Dummy Hybrid

Each long cables was connected to a dummy hybrid and repeater board. The temperature cable from the corresponding to the same module was also connected. A single control cable was connected to the dummy repeater card and the LV was turned on. The chips on the dummy hybrid were powered and the values of Vmon, Imon and Vcon were measured. The resistance of the cables was measured as before and a large

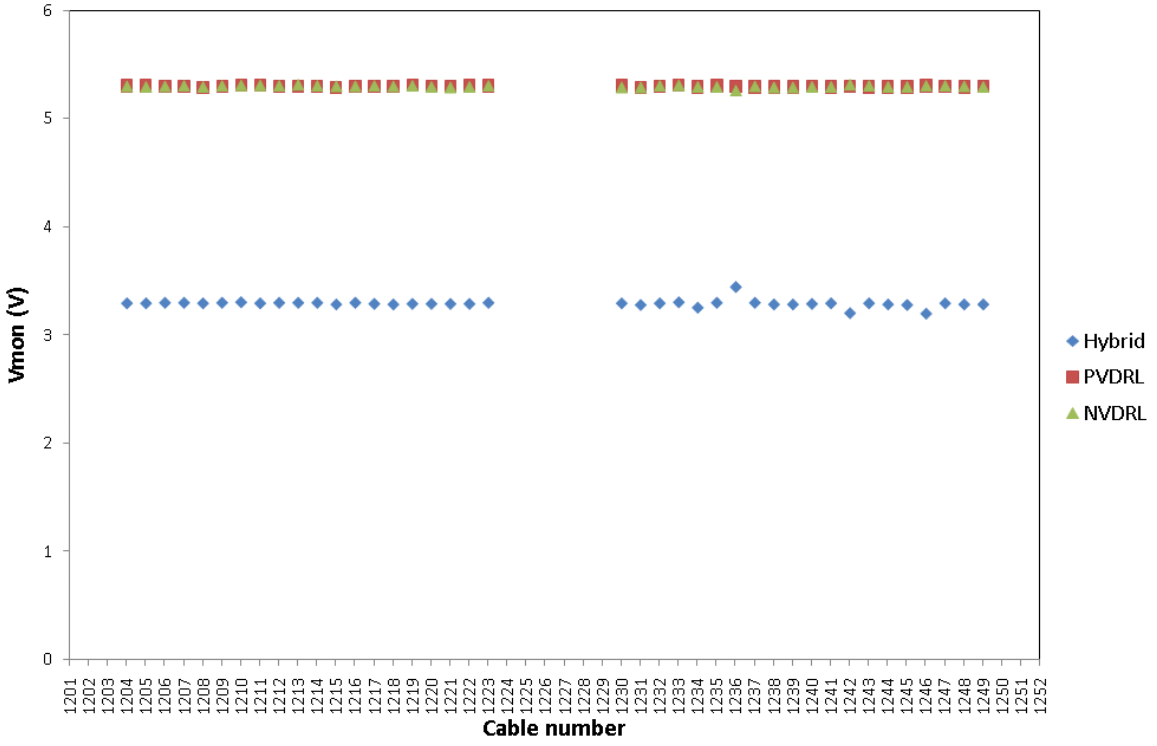

Figure 23 The voltage measured at the module (Vmon) as a function of cable number with the supply connected to the dummy module at the end of the long cables.

The temperatures of the NTCs on the hybrid and repeater board were monitored until the interlock was fired with a "Too Warm" signal. The temperature of the NTC which triggered the interlock is shown in figure 27. This was repeated for every module position on the C side of the VELO.

6 Conclusion

The VELO Low Voltage and cables have been extensively tested and the system is ready for operation. Additional protection is required in front of the supplies in the racks in D3 to ensure that they cables do not move.

7 References

[1] CAEN Technical Information Manual, MOD. A3009/A3009B 12 CH 8V/9A/45W Power Supply Board, http://www.caen.it

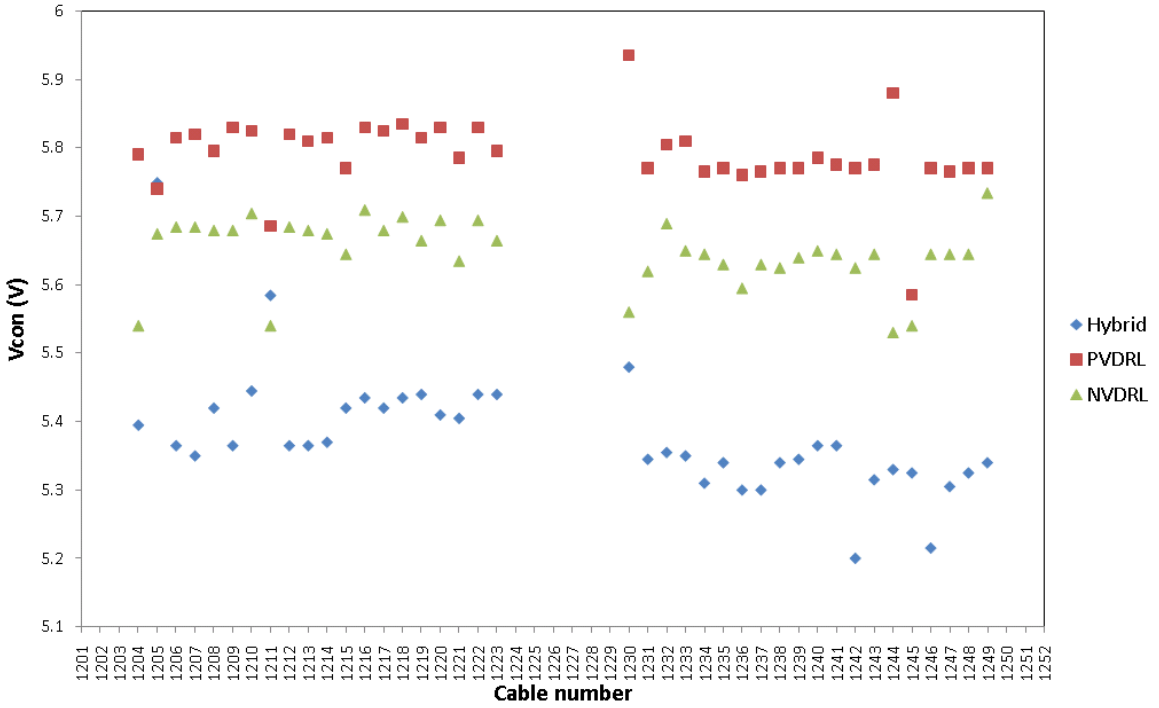

Figure 24 The voltage measured at supply (Vcon) as a function of cable number with the dummy module connected to the long cables.

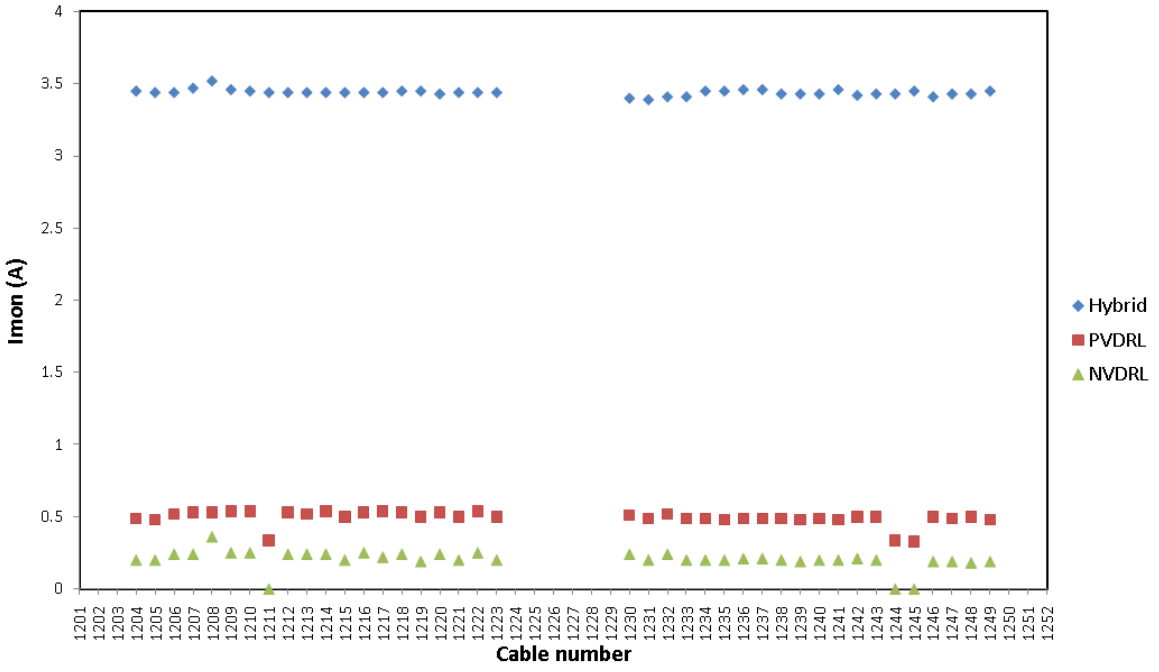

Figure 25 The current measured on the hybrid channel of the dummy module as a function of cable number with the module connected to the long cables.

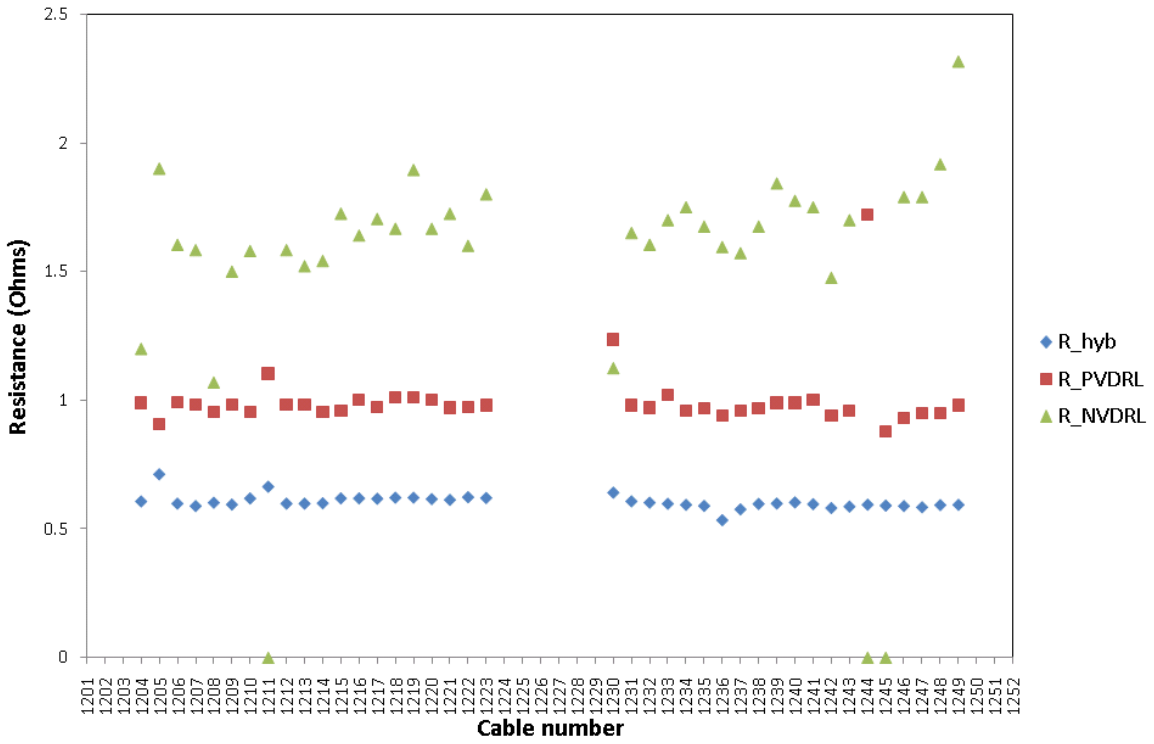

Figure 26 The resistance of the cables/connectors as a function of cable number measured with the dummy module connected to the long cables.

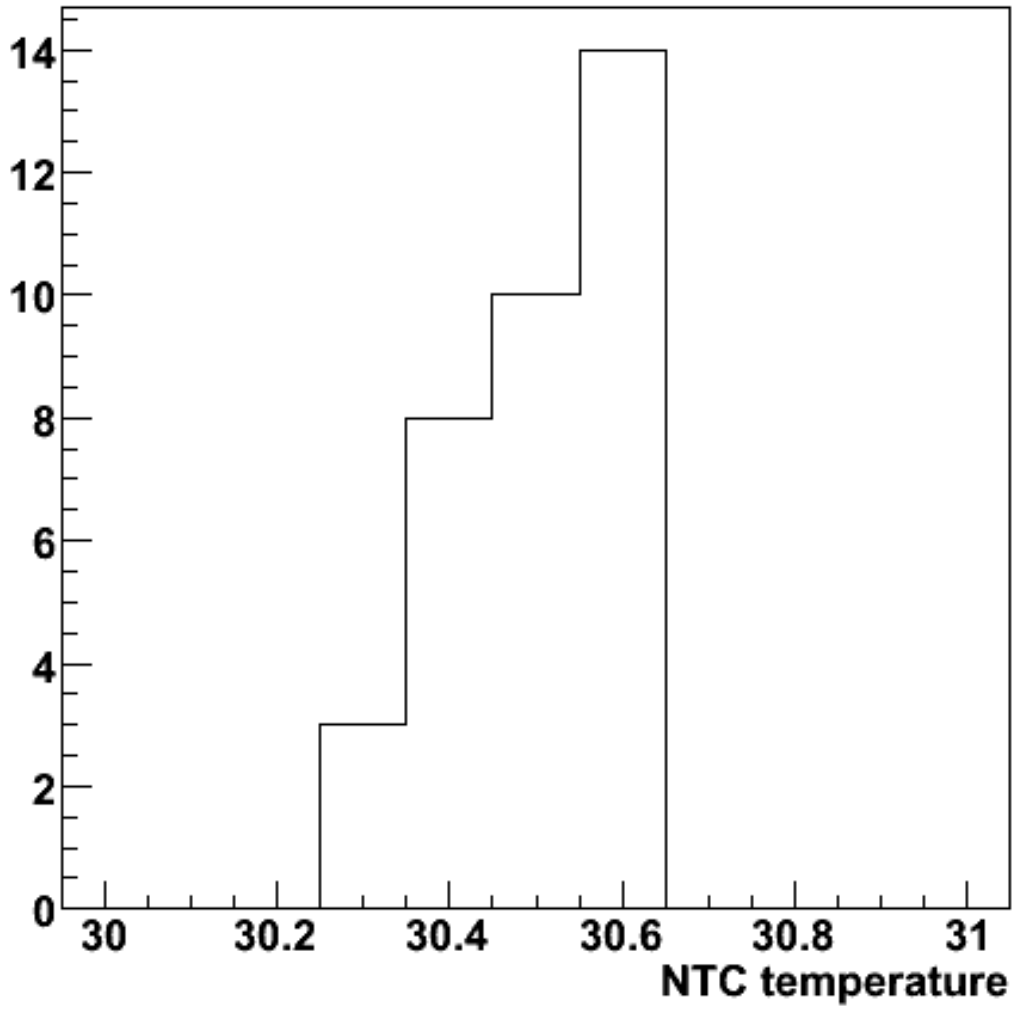

Figure 27 The temperature measured by the NTC on the hybrid when the interlock was triggered.

A Raw data from ramping tests

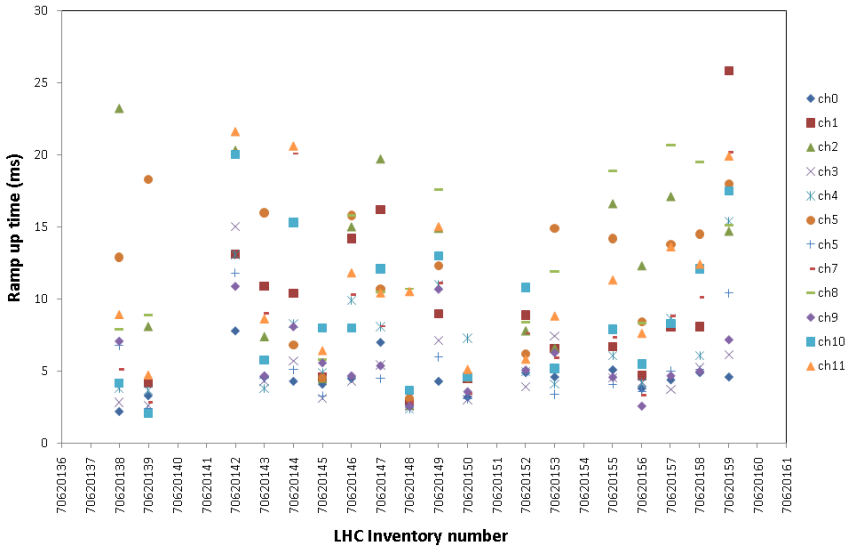

Figure 28 Time taken to ramp up.

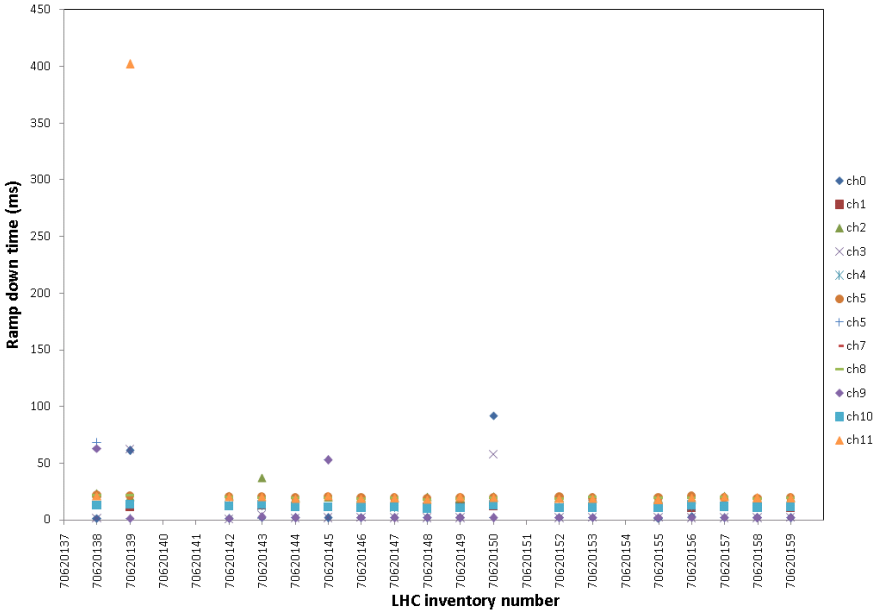

Figure 29 Time taken to ramp down.

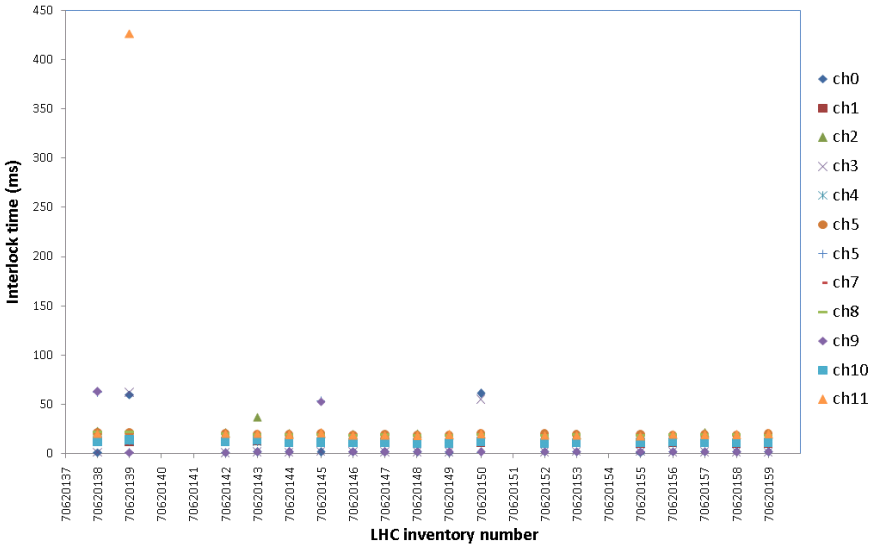

Figure 30 Time taken to ramp down after an interlock