SiLC:

Confronting the 06-09 R&D challenges

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LPNHE, Université Pierre et Marie Curie-Paris6/CNRS-IN2P3

Third SiLC Collaboration Meeting, Liverpool, June 13-14, 2006

SiLC R&D collaboration objectives & EUDET

Europe

IMB-CNM Barcelona, Sp
HIP, Uni of Helsinki, Fi
IEKP, Karlsruhe U., Ge
Uni of Liverpool, UK
Moscow State Uni, Ru
Obnisnk State Uni. Ru
LPNHE, CNRS-IN2P3, Fr
Charles Uni, Prague, Cz
IFCA U. of Cantabria, Sp
University of Torino, It
IFIC-CSIC, Valencia, Sp
IHEP, Ac Sc. Vienna, Au

USA

U. Of Michigan, Ann Arbor
SCIPP & UCSC Santa Cruz

Asia

Kyungpook U. Taegu, Ko
Yonsei U., Seoul, Ko
Korea U. Seoul, Ko
Seoul Nat. U., Seoul, Ko
SungKyunKwan U. Seoul
Tokyo U. (Japan)
HAMAMATSU (Japan)

Close contacts with:
FNAL Si Lab team
SLAC SiD Team
CERN LHC & Microelectronics teams

Industrial firms (in progress)

R&D Objectives:

- R&D on sensors
- R&D on associated electronics
- R&D on Mechanics

and developing the needed tools:

- Laboratory test benches
- Alignment and position monitoring
- Simulations
- Cooling and other related integration tools

Synergy with the LHC present construction and future upgrades

EUDET test beam ILC E.U. space
SiTRA participation

- Instituto de Microelectronica, Centro Nacional de Microelectronica CSIC, Barcelona, Spain (associate)
- HIP, University of Helsinki, Finland
- University of Liverpool, United Kingdom (associate)
- State University of Obninsk, Russia (associate)
- State University of Moscow, Russia (associate)
- LPNHE, Université Pierre et Marie Curie/IN2P3-CNRS, Paris, France
- Charles University in Prague, Prague, Czech Republic
- Instituto de Fisica de Cantabria, CSIC-Universidad de Cantabria, Santander, Spain
- Instituto de Fisica Corpuscular, CSIC-Universitat de Valencia, Valencia, Spain (associate)

The Korean team is asking to join as associate

Representing: 30 Physicists, 30 Engineers & Technical staff,
3 EUDET postdocs and ~ 12 PhDs or non EU postdocs

Indeed participating to all related EUDET activities:
the SiLC R&D International collaboration

GOOOOOOOOAL!!!!!!!!!!!!!!

To build the next generation of Si trackers for the ILC:
Next generation meaning:
Higher precision on momentum (x10 better/LEP)
Higher precision on spatial measurements
(average 7-8 μm, 4μm in some case)
Low material budget
Robustness
Easy to build and
to work with
Low cost

R&D on sensors

IEKP-Karlsruhe, HIP Helsinki & VTT, IMB-CNM/CSIC, SiLAB-Moscow State U. Korean team+ETRI, IHEP-Vienna, Hamamatsu Japan, LPNHE Liverpool (see this meeting) & Italy ?

SENSOR TECHNOLOGIES:

Silicon strips are the baseline with:

Larger size wafers, single sided, thinner/thinning

New technos in some regions (pixelization)

New Hybrid Pixels, DEPFET, MAPS/FAPS, SOI,??

STRATEGY:

The research Labs develop & test new ideas

Transfer to small Fabs for reduced production

Large production, high quality and reliability:

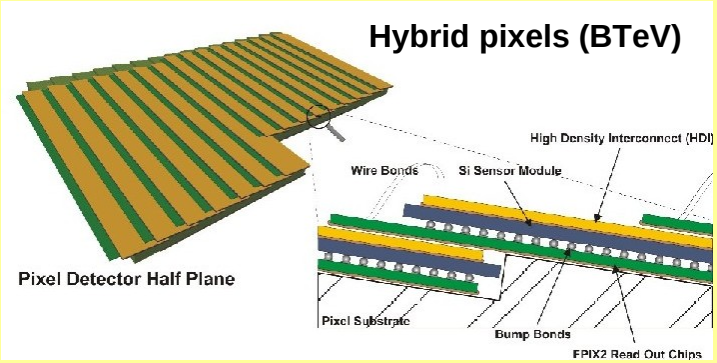
HAMAMATSU Monopoly

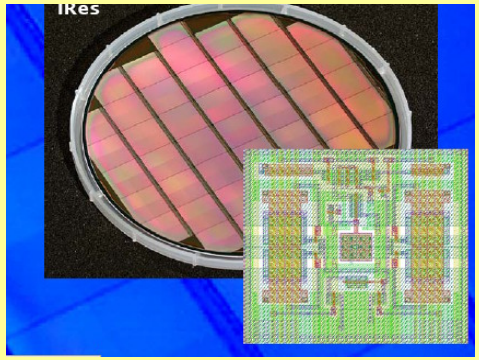
But attempt to create alternative

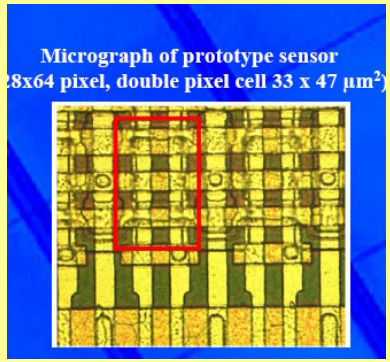
Upcoming test beam will make use as much as possible of the new sensors for constructing the Si tracking prototypes

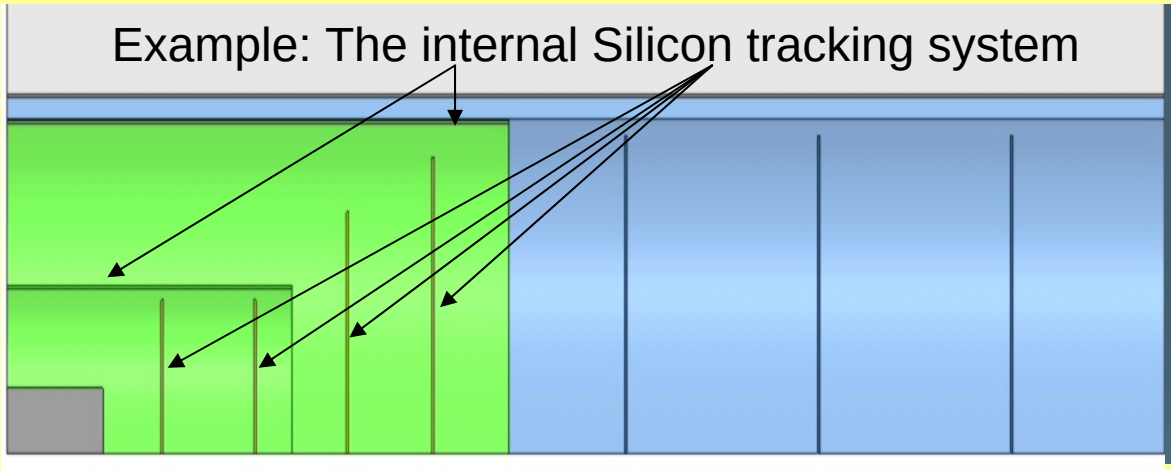
USE of PIXELS

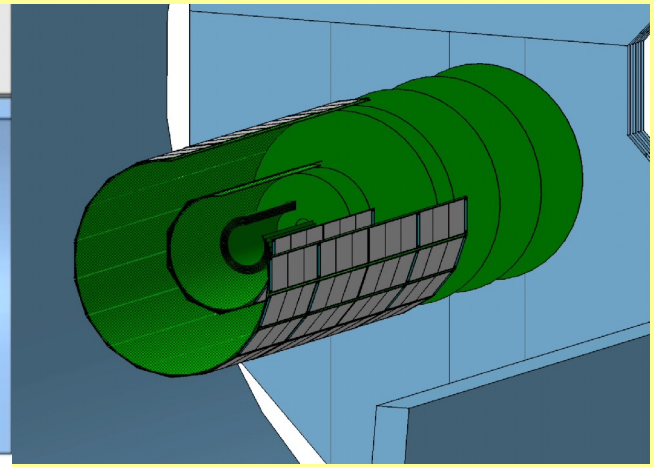
IFIC-Valencia, HIP Helsinki, Liverpool, MPI Munich, & others in SiLC

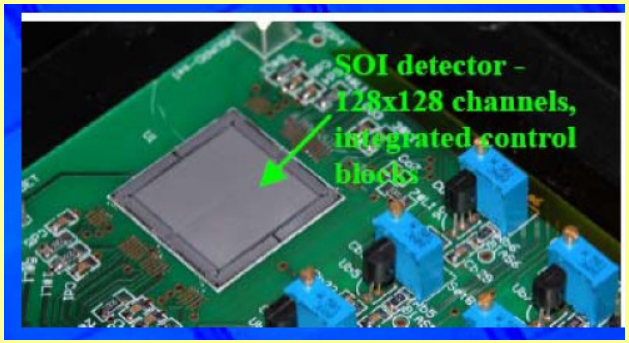








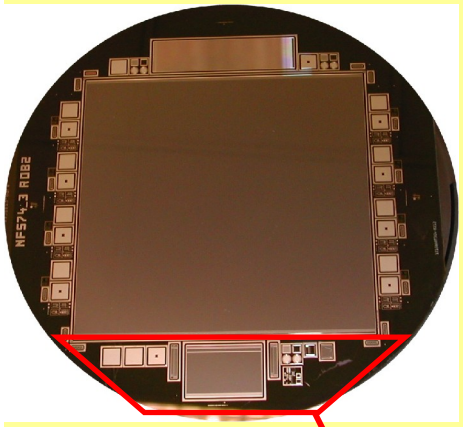


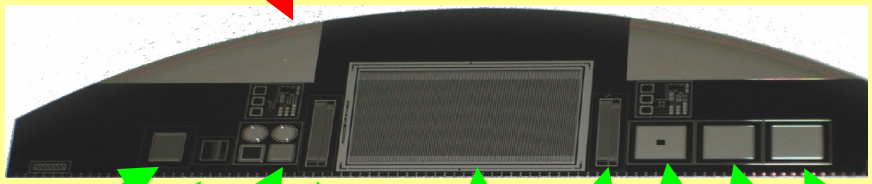


Small prototypes with different pixel technologies will be tested for the EUDET project

R&D on sensors cont'd

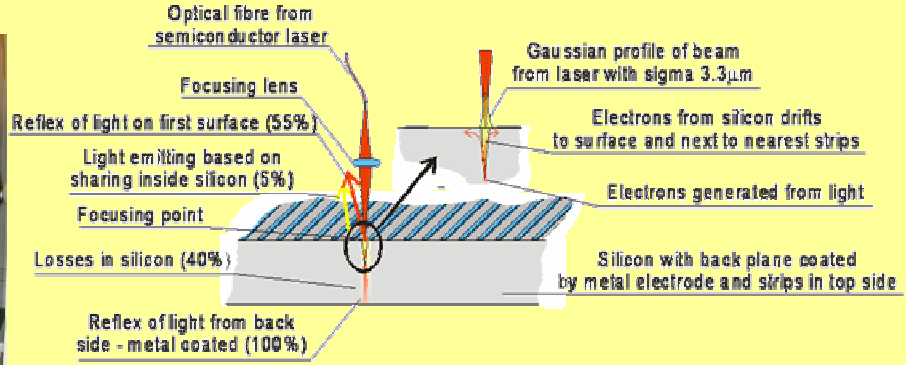
- **Test Quality Control of fab. Line**
  (IEKP Karlsruhe, IHEP Vienna + others)



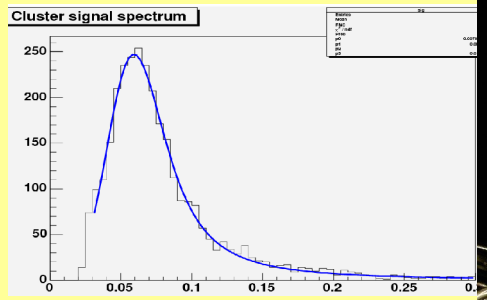


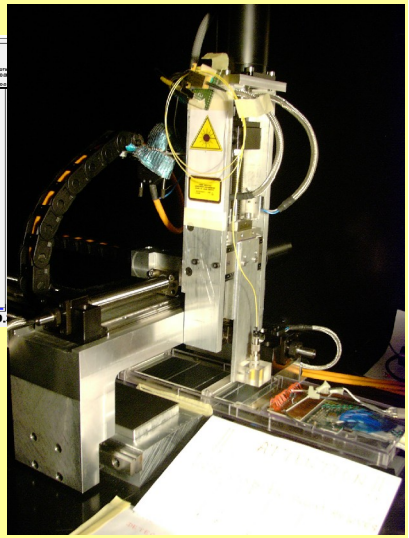
Detailed test structures allowing full characterization & quality test of the production line.

- **Sensor characterization with LD**
  (Prague, Paris, HIP & many others)



- **Sensor characterization with radioactive sources** *(Prague, Paris, HIP & many others)*



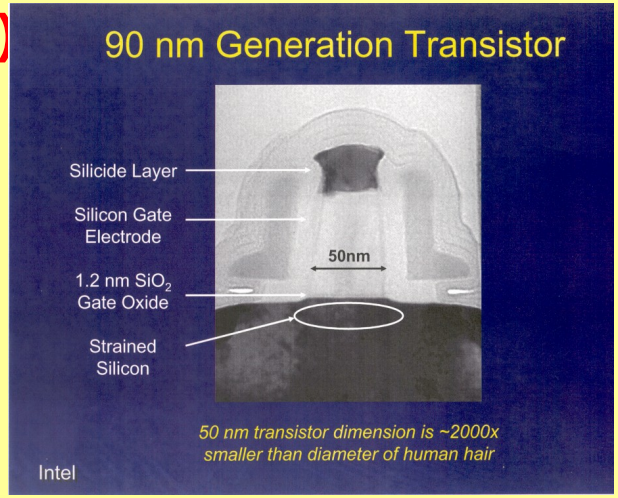


All these test facilities will be used and further improved to test new wafers (not only strips) that will be used in EUDET project

On-detector System-On-Chip electronics using (Very) Deep Sub-Micron CMOS technologies

(see Alessandro's & Jean François's talks)

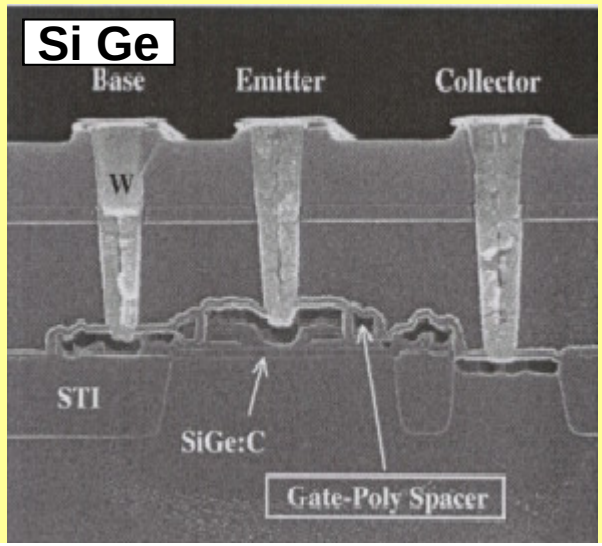
- On detector low-noise amplifiers mandatory
- Radiation tolerance & hardness
- Less on-detector material: Silicon, wiring, packaging, cables, kaptons, connectors ...



90 nm Intel transistor

- Processing: A/D conversion, zero suppression, calibration, realtime data processing & filtering; thus reduced output dataflow
- Less power dissipation
- Speed: SiGe faster than CMOS for same power dissipation and CMOS compatible
- Excellent reliability

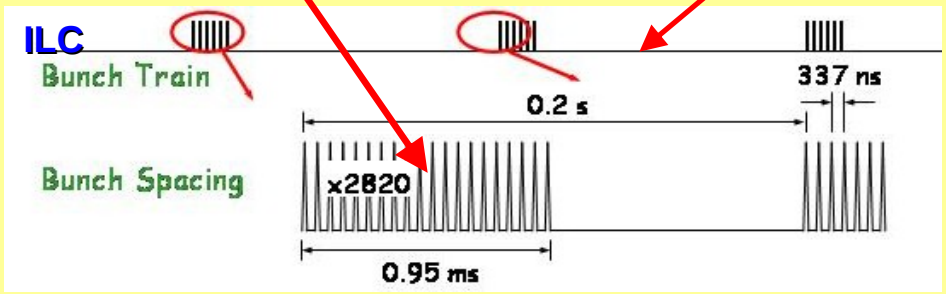
There is no other way !

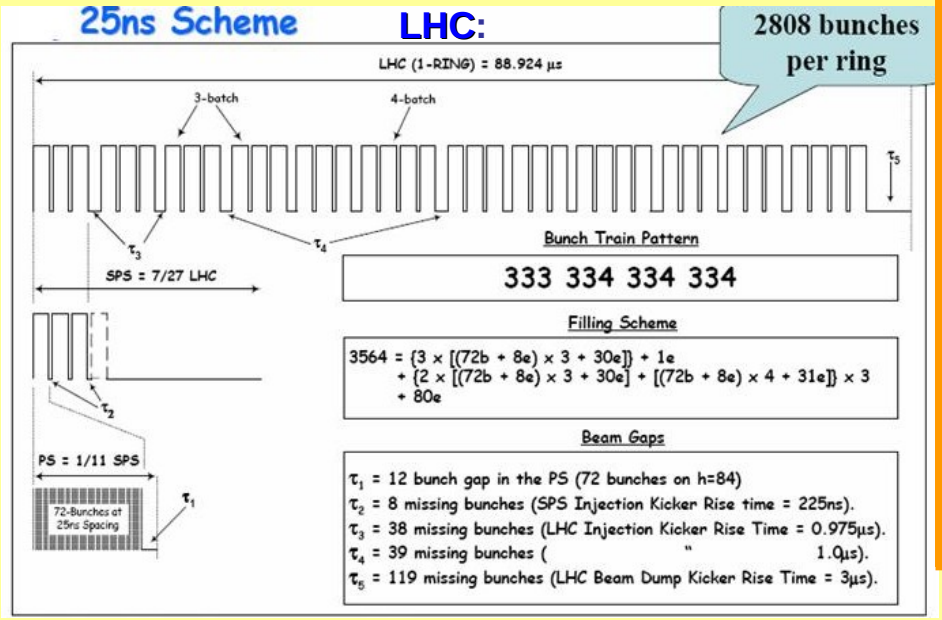


R&D on Electronics

LPNHE-Paris, LAPP, IMB-CNM/CSIC,...

FE chip to read out the Si tracking prototypes for the EUDET project will be:
VDSM, with:
Bunch (BCO) tagged electronics & power cycling





Pulse sampling: *5-10 samples over 2 possible shaping times*

Buffering: *8-deep 2D analog buffer (8*5-10 samples cells)/channel*

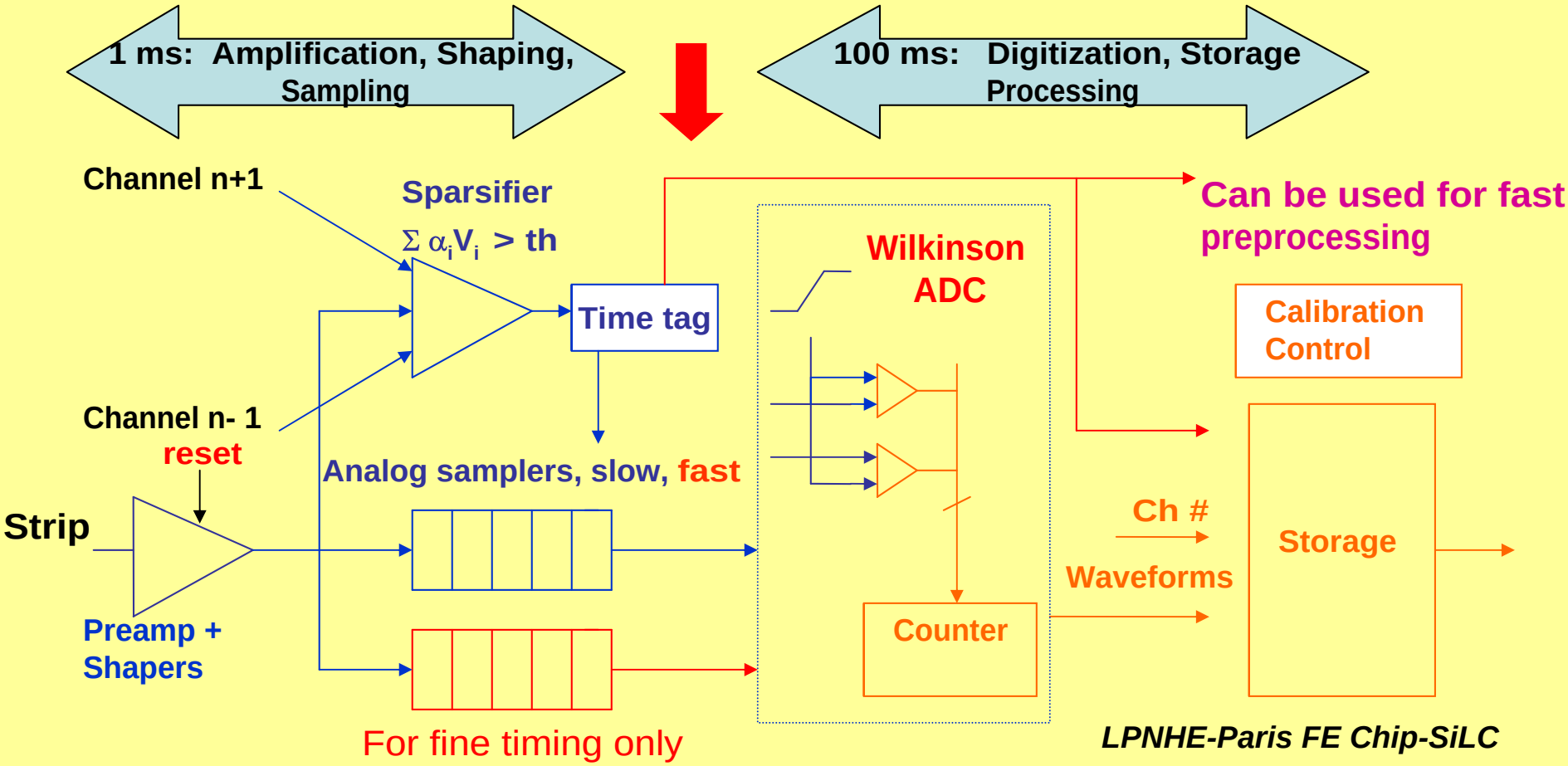
Analog-Digital conversion: *Wilkinson optimum (SVX architecture)*

Sparsification/calibration : *Integrated on detector FE chip*

Digital processing:
Amplitude and time estimation + charge cluster algorithm

Power:
1/100 ILC duty cycle: *FE Power cycling*

Front-end architecture



Charge 1- 40 MIP, S/N~ 15- 20, Time resolution: BC tagging, fine: ~ 2ns (?)

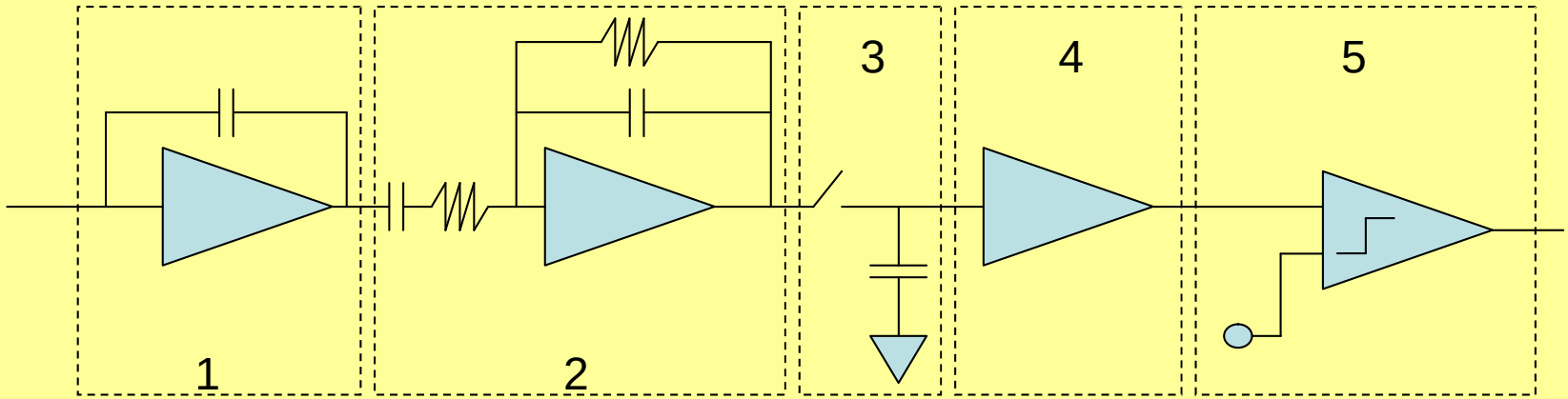
Present technologies - Deep Sub-Micron CMOS
UMC 0.18 μm, 0.13 μm

Fine timing:
SiGe & deeper DSM

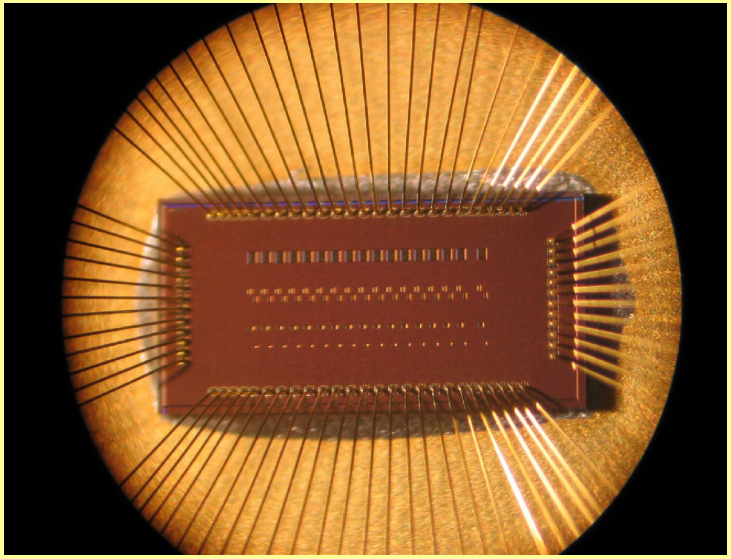
Time-stamping on all layers and fine time resolution on some layers

First prototype (Sept 06 test in DESY)

Front-end Prototype chip in 180nm technology

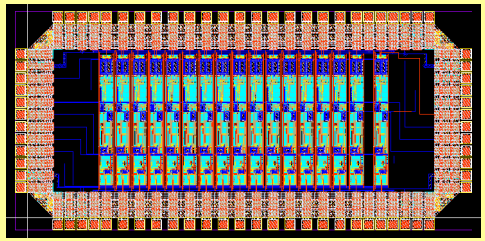


LPNHE-Paris Chip



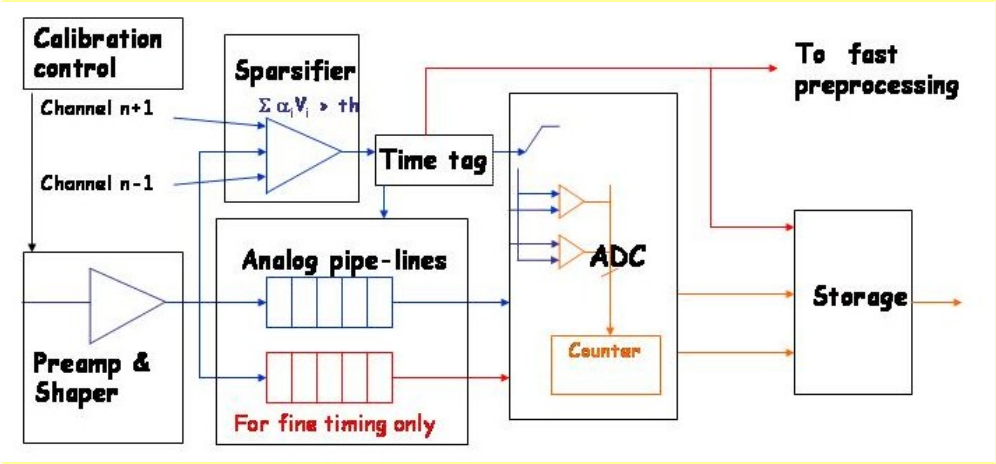
3mm

17 channels (one test Channel)



1. Low noise amplification
2. Pulse shaper
3. Sample and Hold
4. Buffer
5. Comparator

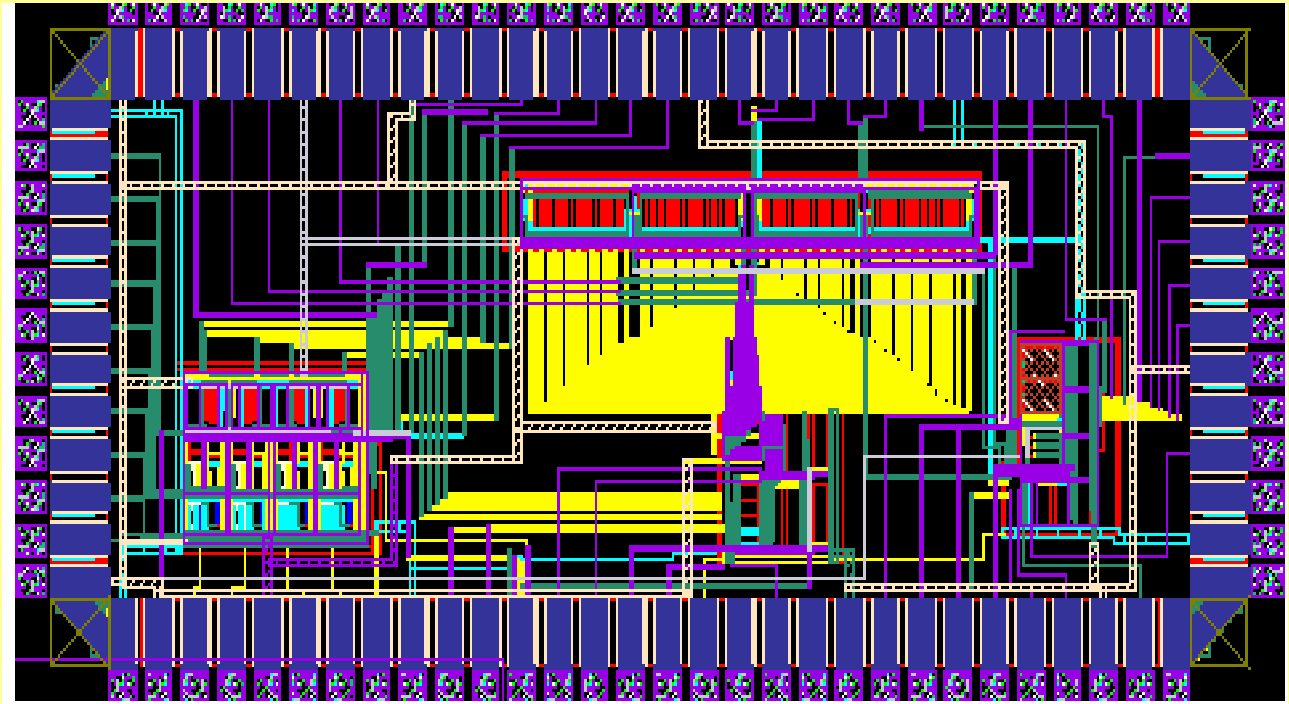
130nm new chip



Sent to foundry April 19th
Get back: end of July

(today news from Jean François)

LPNHE-Chip130-SiLC



FE Electronics Plan for EUDET project:

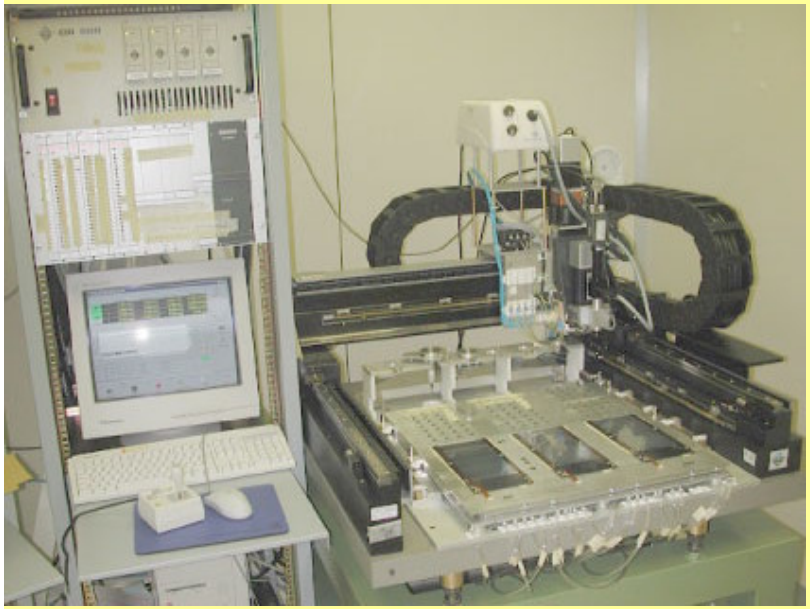
- Chips on 130 nm first version sent by April 19th 2006,
- Second 130 nm foundry to be sent in August.
- 180nm chips tested at DESY test beam September 2006.
- 128 channels per chip submitted Fall 2006, will equip the prototypes for 2007 fall test beam
- First 130nm chips tested at beam test in DESY end 2006.
- Development of a VFE SiGe version (fast shaping) in VDSM for the time measurement if proven to be feasible.
- New version with larger number of channels, 90 nm techno if available, plus bump bonding onto detector development for the final test beam in 2009

R&D on Mechanics and EUDET

- Developing the elementary module
- CAD design studies of the various components (light & large mechanical structure) and,
- Prototype design and construction
- Cooling thermo mechanical studies
- Related positioning, alignment and
- integration issues (with other subdetectors for combined test beams)

The elementary module: tile of the overall architecture

Based on present experience (LHC) must be light, precise, robust, easy to build & assemble:

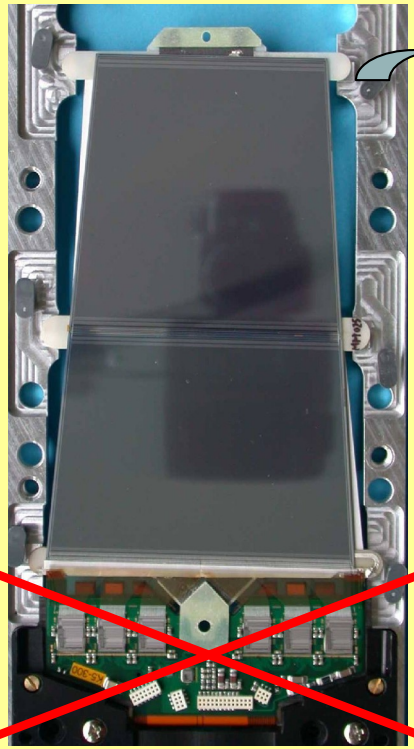


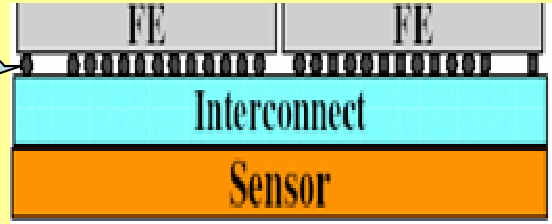
Robotic assembly (CMS)

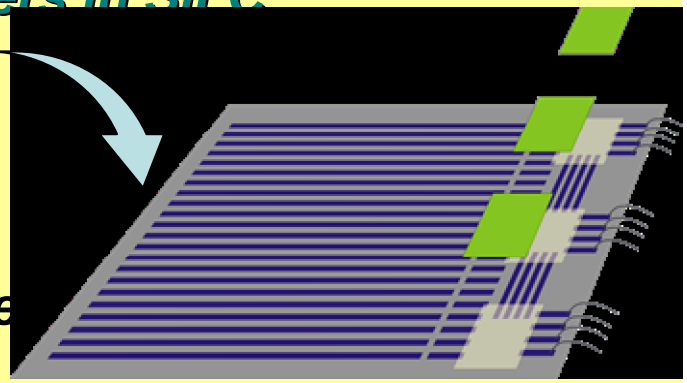
- **New sensors (next generation)**
- **Support: new material &design**
- **VDSM FE electronics & wiring**
- **Precise positioning on the module & the support structure**
- **Easy to build (robotisation ?)**
- **Industry transfer: big number**
- **Favouring a ‘’universal tile’’ (instead of different shapes)**

R&D on the new elementary module concept

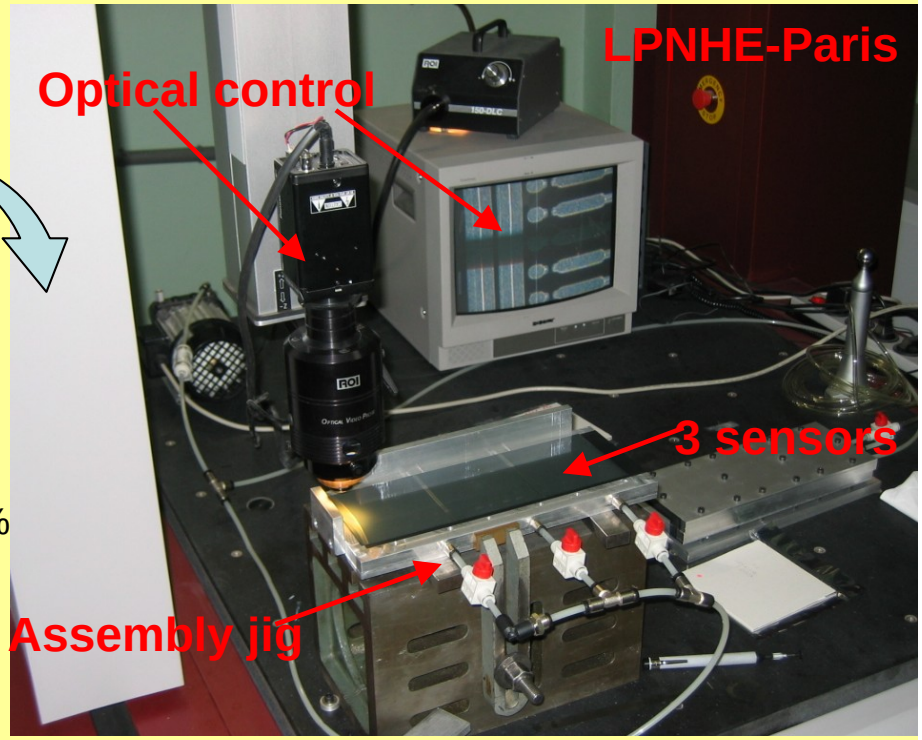
LPNHE-Paris, IMB-CSIC, and others in SiLC





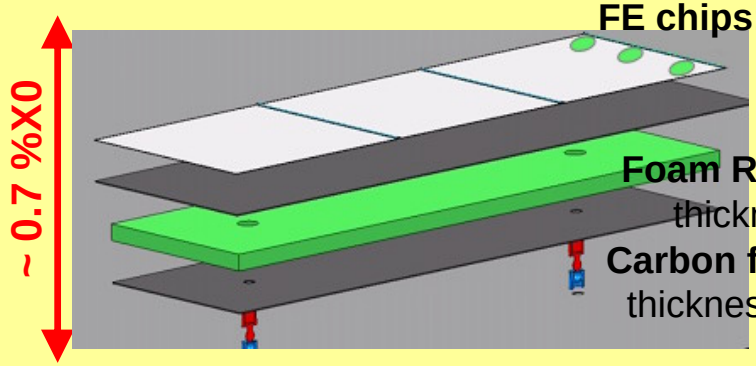


New wiring of FE chips onto the detector: under investigation



Si sensors: 0.3%X0

FE chips: ~0.1%X0+?

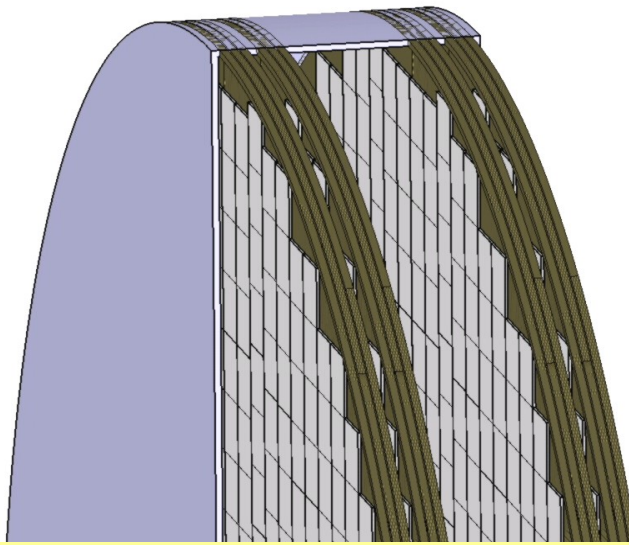


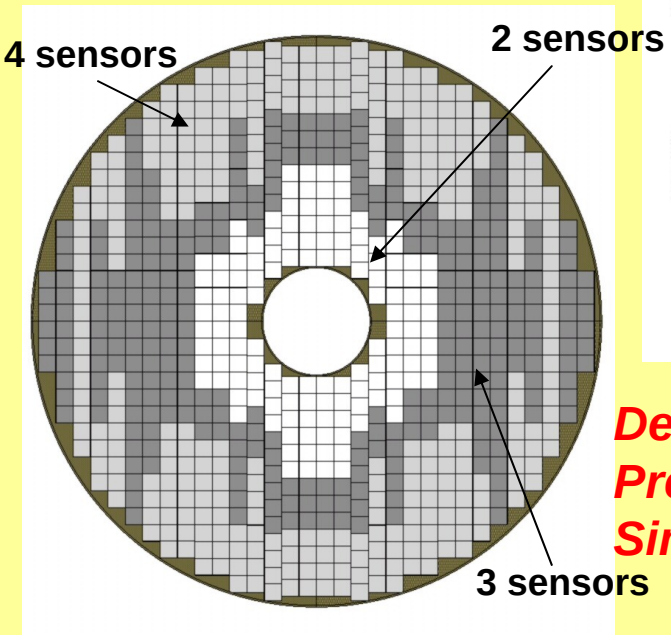
Foam Rohacell 0.05%
thickness ~ 4mm

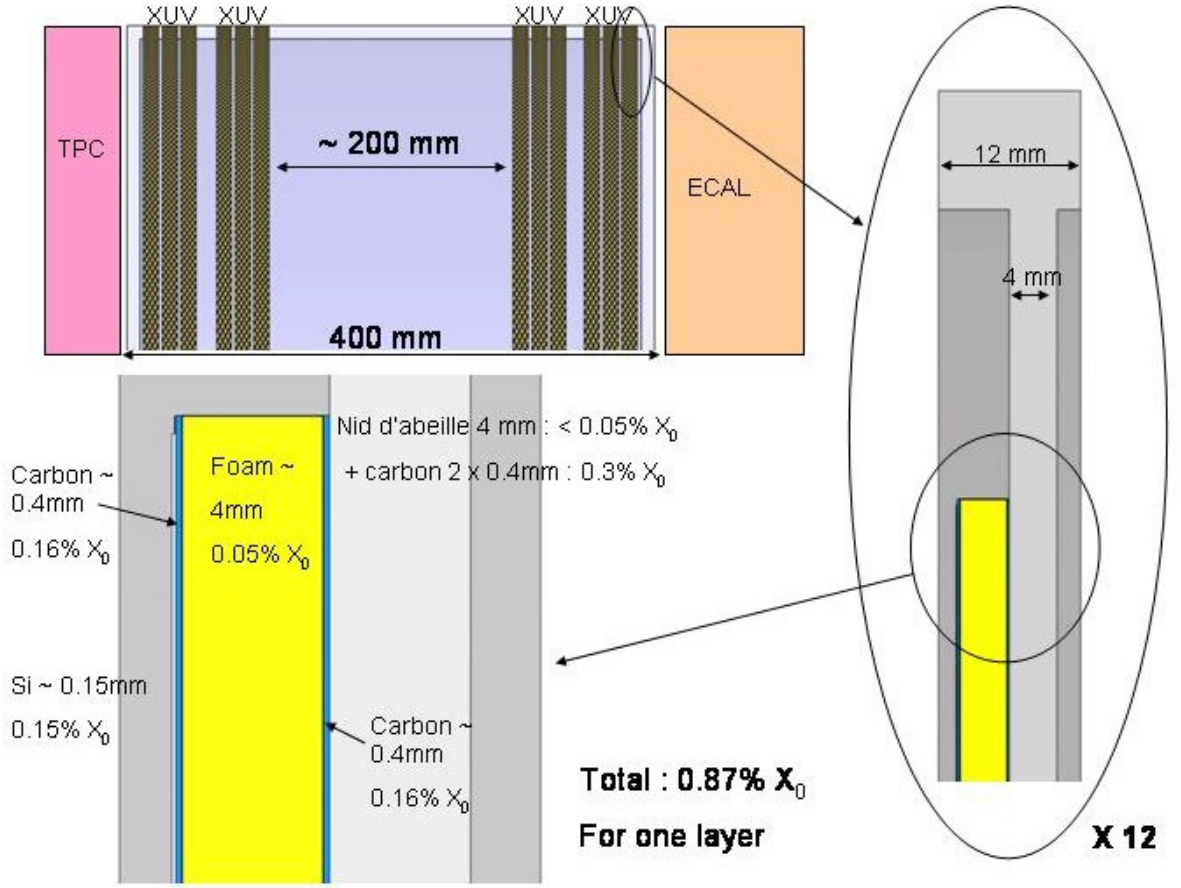
Carbon f. 0.15% X0
thickness ~ 0.4mm

R&D on Mechanics: CAD of Si components/protos

LPNHE-Paris, IFIC-Valencia and others in SiLC







Detailed CAD design of the End Cap External Tracker;
Preferred XUV to projective geometry chosen at LHC;
Simpler with a universal sensor (idem for central barrel)

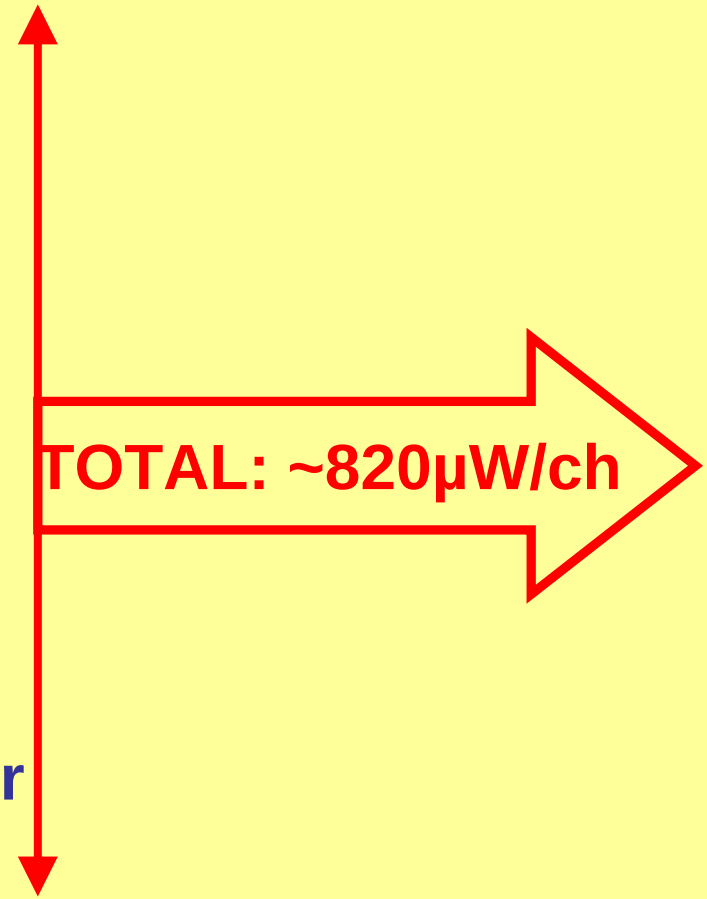
COOLING:
Expected power dissipation in 180 nm

Analog:

Preamplifier:	**70 µW**
Shaper:	**210 µW**
Sparsifier:	**50µW**
Sampling:	**100-200 µW**
ADC:	**120µW**
Total analog:	**670 µW**

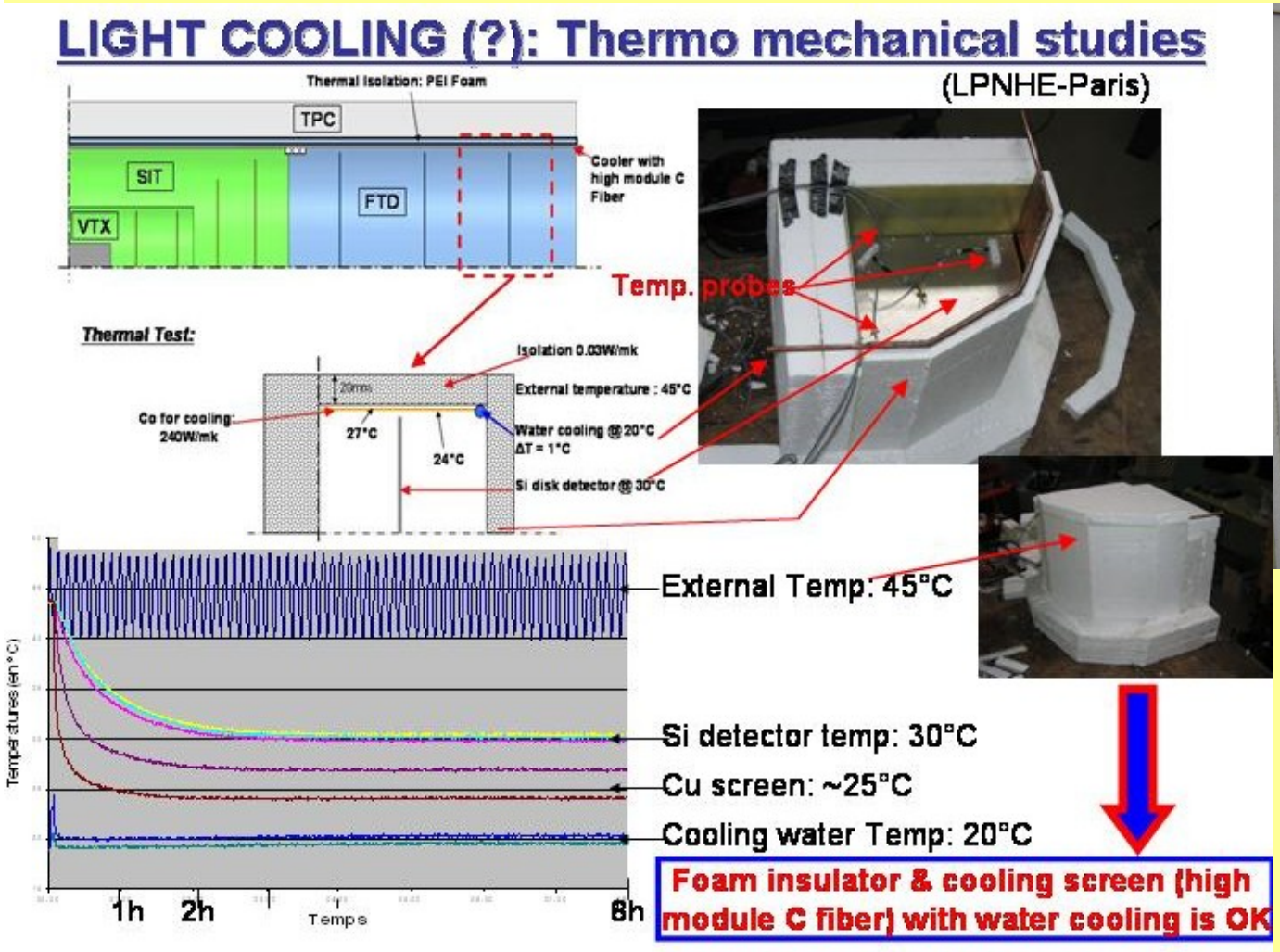
Digital:

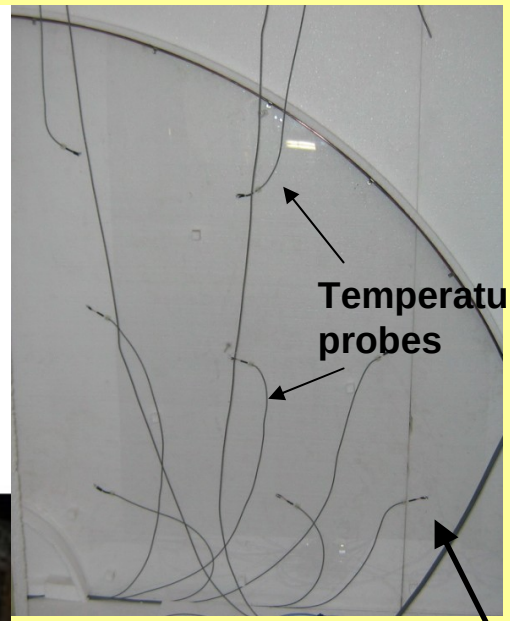
Take benefit of DSM digital low power
Clocking + buffering: 150 µW



R&D on Mechanics: Thermo mechanical studies

LPNHE-Paris, IFIC-Valencia and others in SiLC





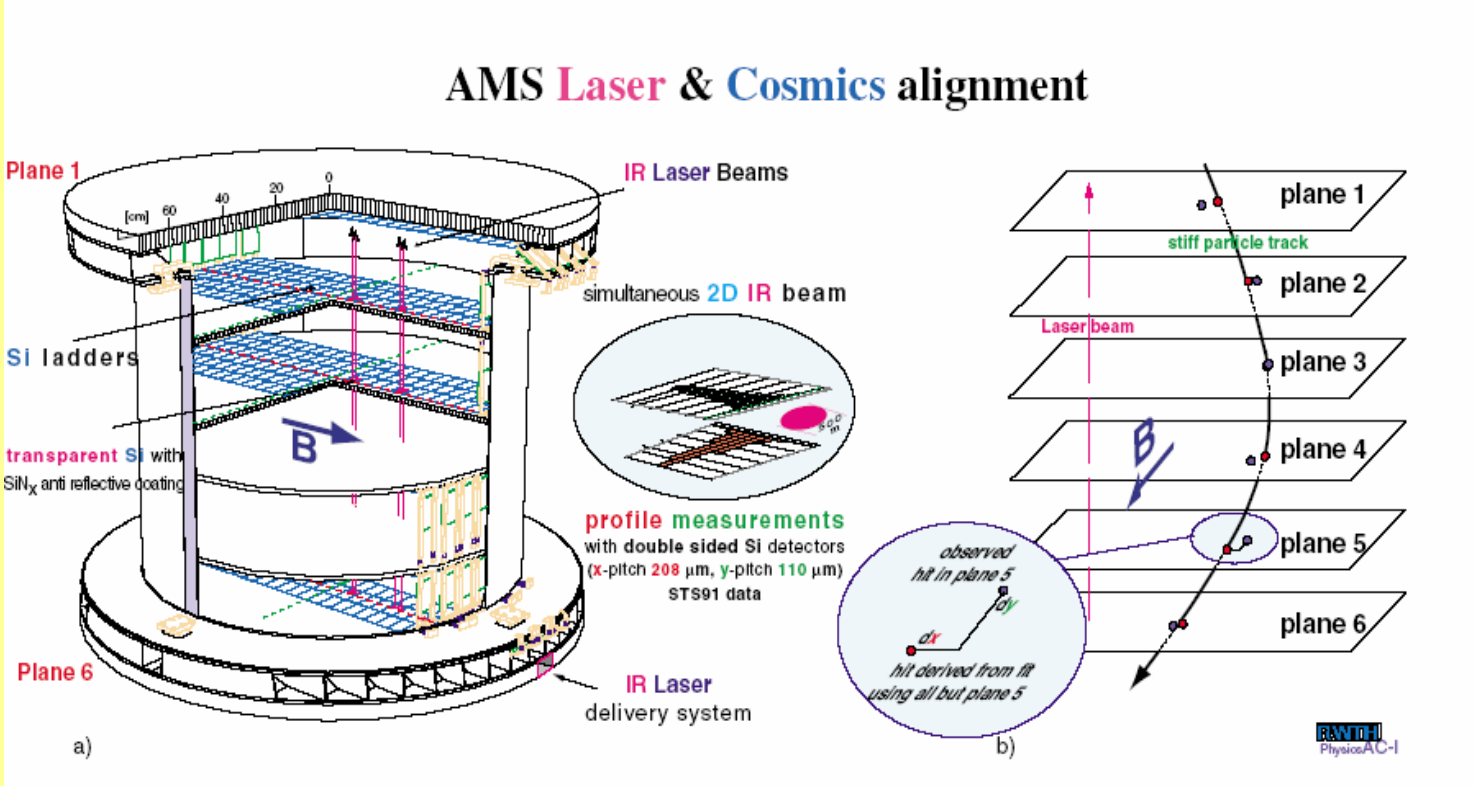
Now under preparation testing cooling on a large surface:
End Cap External layer Prototype, in real scale:
1.6m diameter.
Also simulation modeling (SAMCEF package)

All this developed expertise + savoir-faire of LHC builders and work will be used for the design of the EUDET cooling system

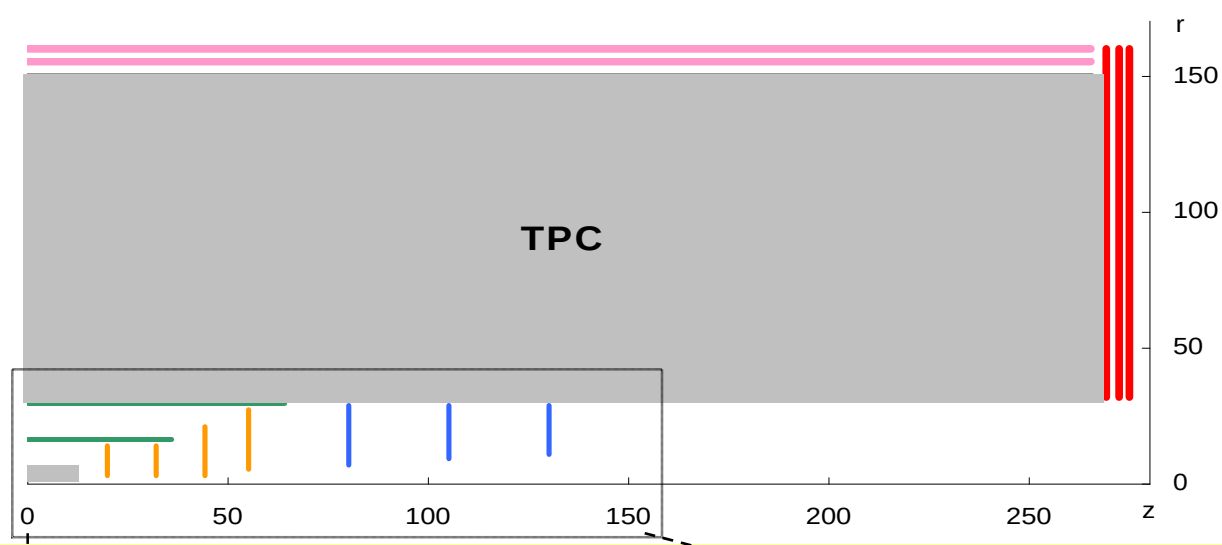
Alignment for Si sensors

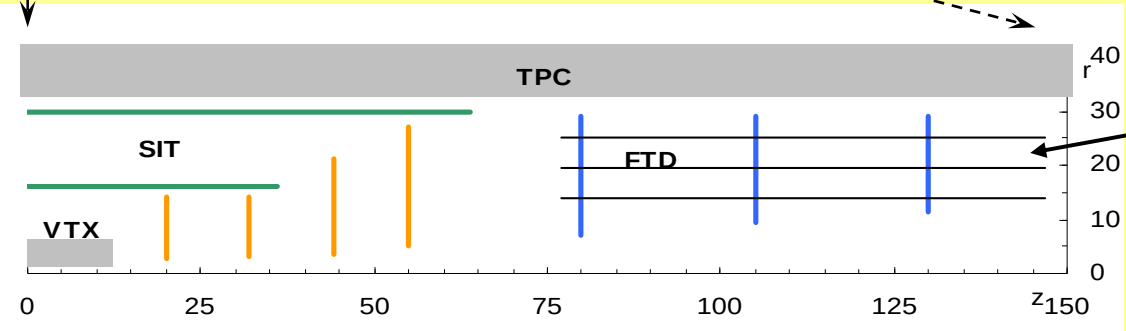
IFCA-Santander

- Usage of collimated laser beams (IR spectrum) going through silicon detector modules. The laser beams would be detected directly in the Si-modules.
- Based on previous AMS-1 experience we can project that few microns (<2 um) resolutions would be achieved.



- ***Main advantages:***
  - Particle tracks and laser beam share the same sensors removing the need of any mechanical transfer.
  - Minimum interference with Silicon support structures
- ***Start up plan:*** feasilibilty study (optical treatment of the Si wafer, test stand to determine achievable position resolution).





Proposal:
Connecting other sub-detector units (barrel –forward) using steering optics
Angular tilts using inclinometers.

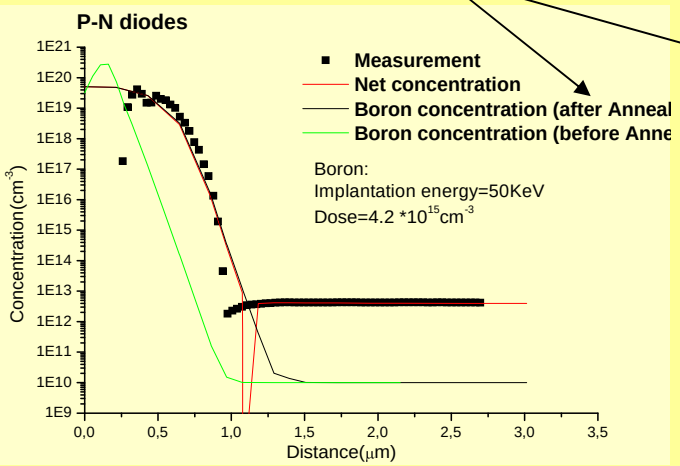
Laser lines

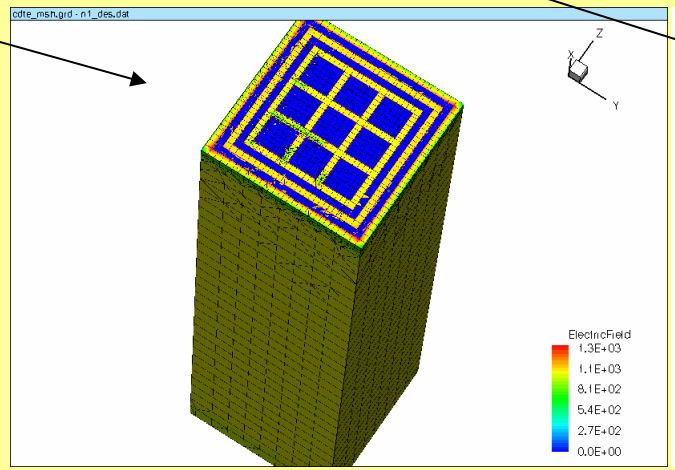
Alignment system for combined tracking tests Si-tracking+TPC will be applied for EUDET

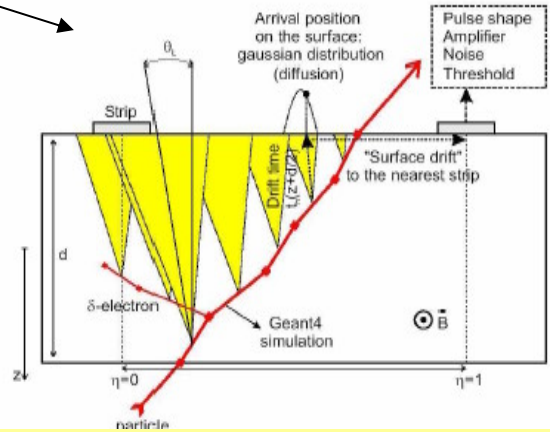
SIMULATIONS

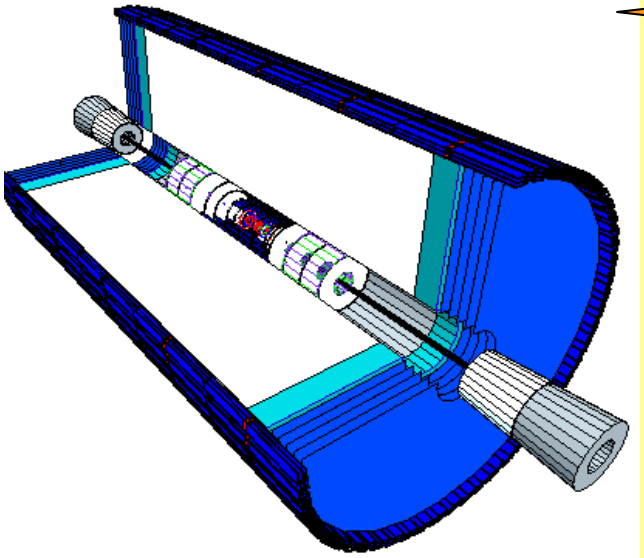
Obninsk St Uni., IHEP-Vienna, LPNHE-Paris, CU Prague, and others in SiLC plus joint EUDET effort

Technology simulation, GEANT4 detailed sensor simulations are available



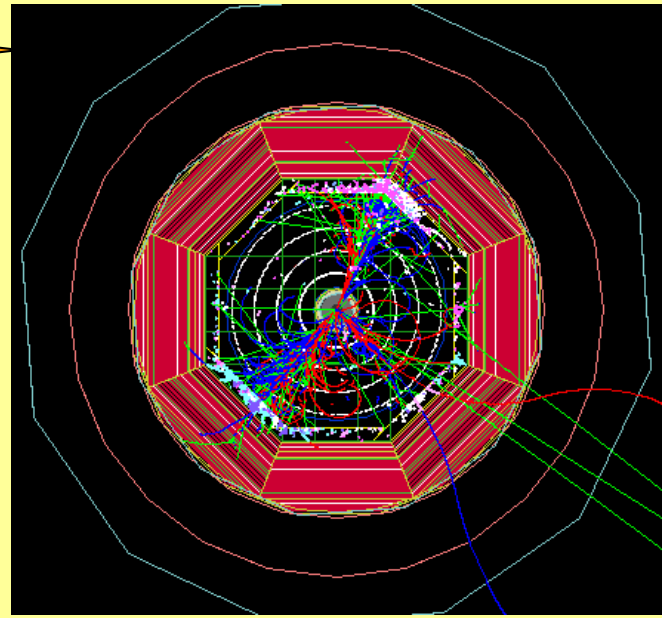




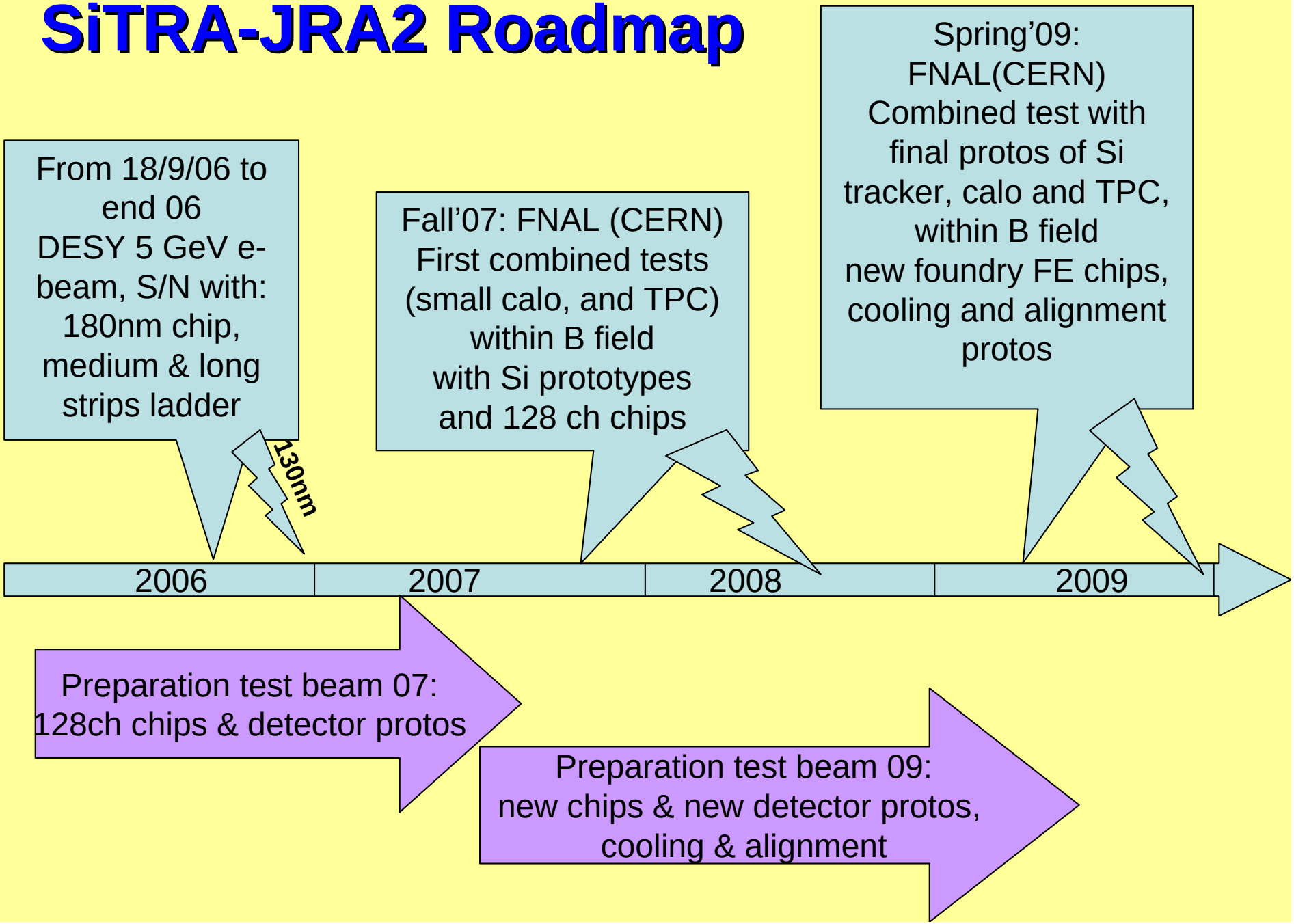


But still lacking: pattern recognition & reconstruction prog.

Proposal: Standalone Si tracking reconstruction inclu-ding the μvertex



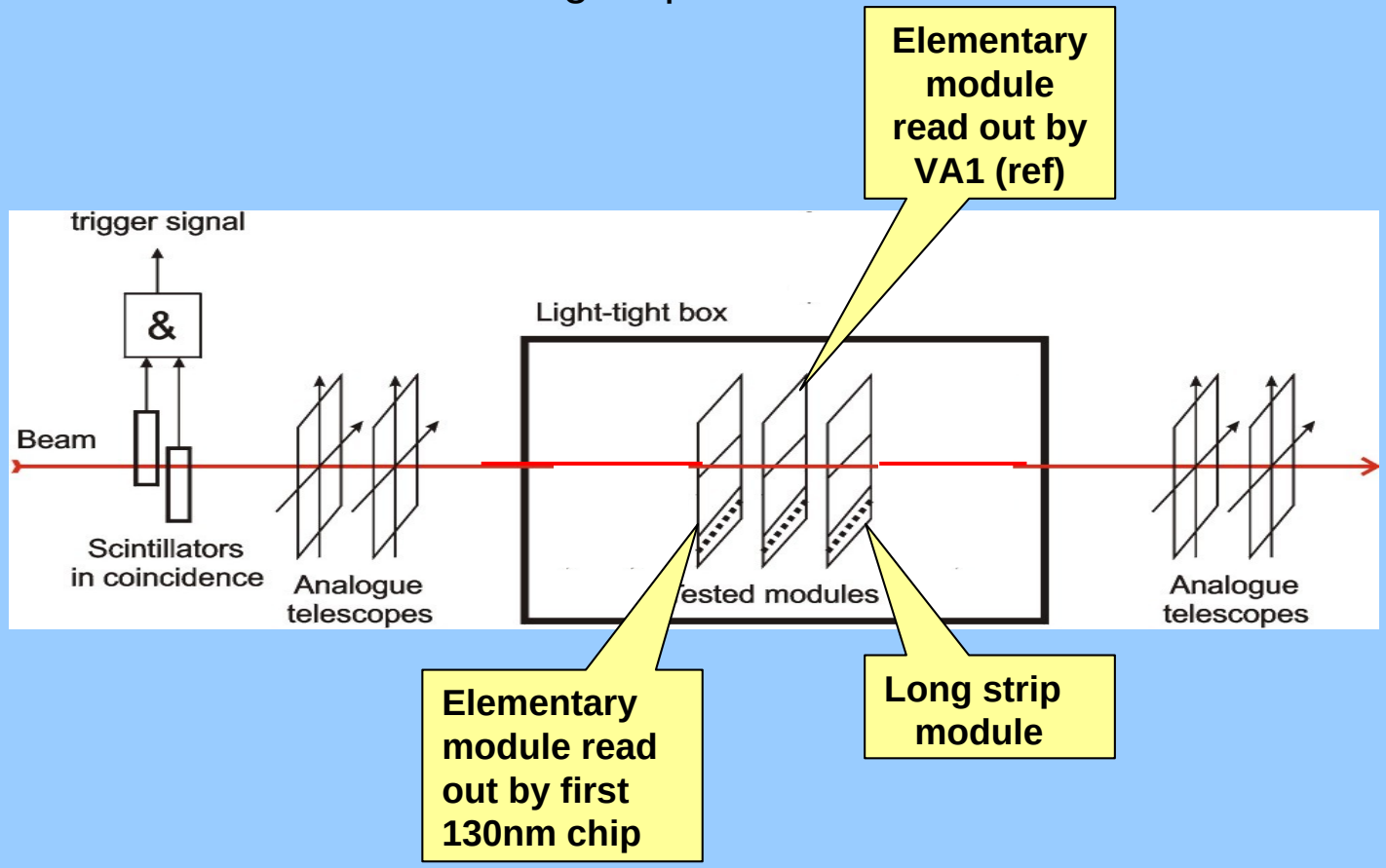
SiTRA-JRA2 Roadmap



EUDET Test beams with Silicon tracking

First series of tests in September 2006 at DESY electron test beam, no magnetic field:

- Test new FE chip prototype (first 180 and 130 nm prototypes)
- Measure S/N on the long strips

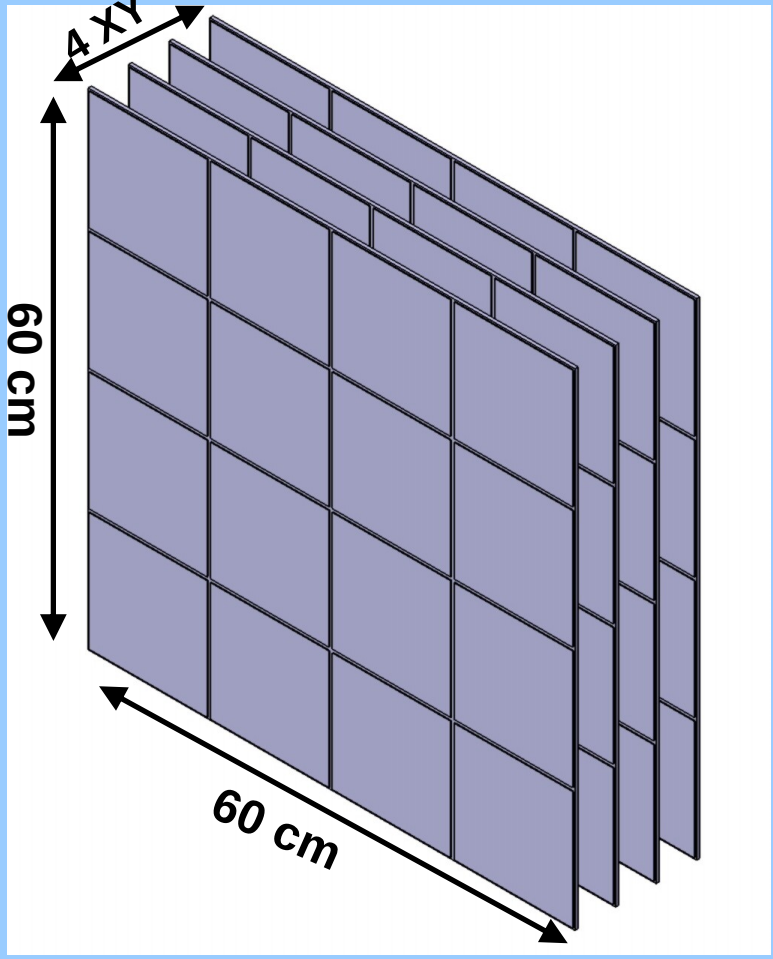


Coordinated by CU Prague team(Zdenek's talk), with the participation of all SiLC to this activity

EUDET test beams with Silicon tracking(cont'd)

Series of tests frpm 2007 to 2009, combined test beams with other subdetectors and high magnetic field:

- Test new FE chip prototype (130 nm prototype-128)
- Various detector prototypes with new sensors and new FE chips



Example:
4 '' telescope layers '' made of 15 x15 cm sensors (≥ 8''), false double sided, thinned, equipped with new chips.

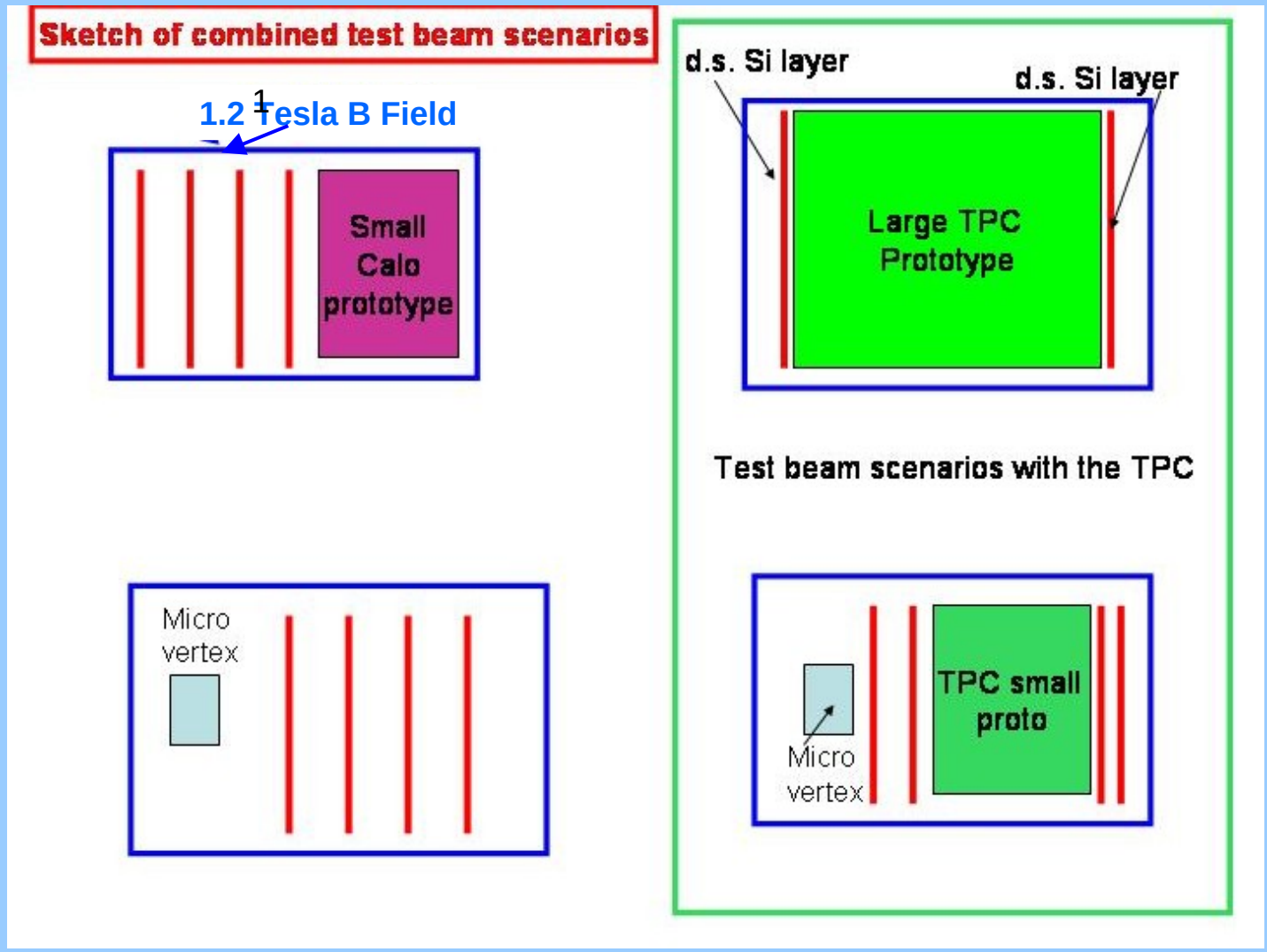
Total: 128 sensors
60000 channels
(~150µm r.o.pitch)
About 250 FE chips

EUDET test beam scenarios (cont'd)

- Test beams with larger telescopes, FWD and barrel prototypes, combined with other subdetectors:
- Calorimeter prototype
- Microvertex prototype
- TPC (field cage proto etc..)

Included in the B magnetic field,various scenarios are foreseen sketched in the next slide

EUDET test beams with Silicon tracking(cont'd)



Deliverables for EUDET from SiTRA

- **Front-end chips to equip the SiTRA prototypes (partially funded by EUDET: CUPrague, HIP, LPNHE)**
  - Order of 60 K channels to be equipped
  - Two foundries foreseen in VDSM (at least…)
    128 ch/chip in 130nm CMOS techno
    ≥ 512ch/chip in 90nm (?) CMOS techno
- **Detector Prototypes (No EUDET funds)**
  (Large & light mechanical support for Si trackers)
  - Telescopes with microstrips and various pixel technolgies
  - Forward prototype
  - Barrel prototype
- **Alignment prototype (No EUDET funds)**
  IFCA-CSIC is in charge
- **Cooling prototype (partially funded by EUDET)**
  LPNHE-CNRS/P6 is in charge

Related items to deliver these workpages

F.E. Chips

Electronics module linking the FE chips to the EUDET DAQ system

Standalone & Transportable DAQ system

(to set-up and test the SiTRA system in the test beam set-up before introducing it in the overall DAQ and also for Lab test bench purposes; The intention is to equip SiTRA & further on SiLC partners with this common tool for cross-checks at Lab test benches)

Wiring and cabling FE electronics onto the detector (new techs)

Detector Prototypes

Sensors are crucial items: the detector prototypes will be made experiencing new sensors technologies, namely:

New microstrip sensors (larger size, thinning)

New pixel technologies (New hybrid pixels, DEPFET, MAPS, SOI …)

Exploiting new Fab lines plus sensor simulations and Test Quality set-ups

➢ Detector Prototypes (cont'd)

Mechanical issues:

- Design and construction of basic element prototypes: (closely related to wiring the FE chip on the detector), thus mechanical & electronics are closedly related)
- Design & contruction of Telescopes, End Cap and Barrel trackers (adressing issues on new material, lightness and robustness etc…)

➢ Alignment:

To be defined by IFCA, team in charge, with some focus on:

Precision (resolution & accuracy), technologies (?), integrated to the overall Si tracker design, minimizing material budget, position monitoring, different scenarios (with or without TPC), dependant of the Si trackers components, integration issues

Cooling prototype

To be developed by the team in charge (LPNHE), inspired by the valuable experience of SiLC LHC colleagues.

Will study a light cooling system (based on ongoing studies on prototypes at the Lab) Plus an e.m compatible frame (Faraday cage); Closely linked to the Mechanics.

Outer thermal Enclosure for SCT-ATLAS by IFIC

Concluding remarks

- All the topics of the SiLC R&D are used for the SiTRA-JRA2 EUDET Project
- All the SiLC partners including the non E.U. ones, will be contributing to EUDET, and
- will have access to the EUDET facilities.
- EUDET will be a fantastic asset to achieve the R&D objectives of SiLC and vis & versa.
- The prepacontributiration of this large scale test bench facility will need a huge effort and the contibutions
- **EUDET: unique opportunity for tests & for progress in this tracking technology and the related topics; it will also allow further development and reinforcement of collaborative contacts with high tech firms**

LET'S START NOW!!!