Readout of Silicon strips detectors using Deep Sub-Micron technologies

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on behalf of

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3d SiLC Workshop
Liverpool UK

June 13 14th 2006

Outline

- Context of the Silicon strips for the ILC
- Front-End Electronics design
- Integrated electronics
- 180nm CMOS chip
- Design in 130nm and future plans
- Detector integration
- Evaluation, Beam tests

Silicon strips for the ILC

Silicon strips tracker at the ILC

- a few 10^6 Silicon strips
- 10 - 60 cm long
- Thickness: 200-500μm
- Strip pitch 50-200 μm
- Single sided, AC coupled,

Experience from CMS:
DC 10-20% cheaper, more reliable

Detector data

SN = 25000 e-/1000e- ~ 25

- Pulse height: Cluster centroid to get position resolution to a few μm

  Detector pulse sampling

- Time: Two scales:

  ¤ Coarse 150-300ns BCO tagging

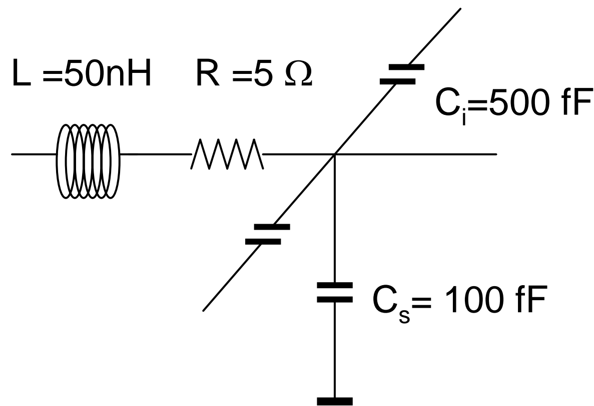
  Two shaping time ranges 500 ns and 2 μs

  ¤ Nanosecond timing for the coordinate along the strip
  Not to replace another layer or double sided
  Spatial estimation to a few cm

  Shaping times: 20-100ns

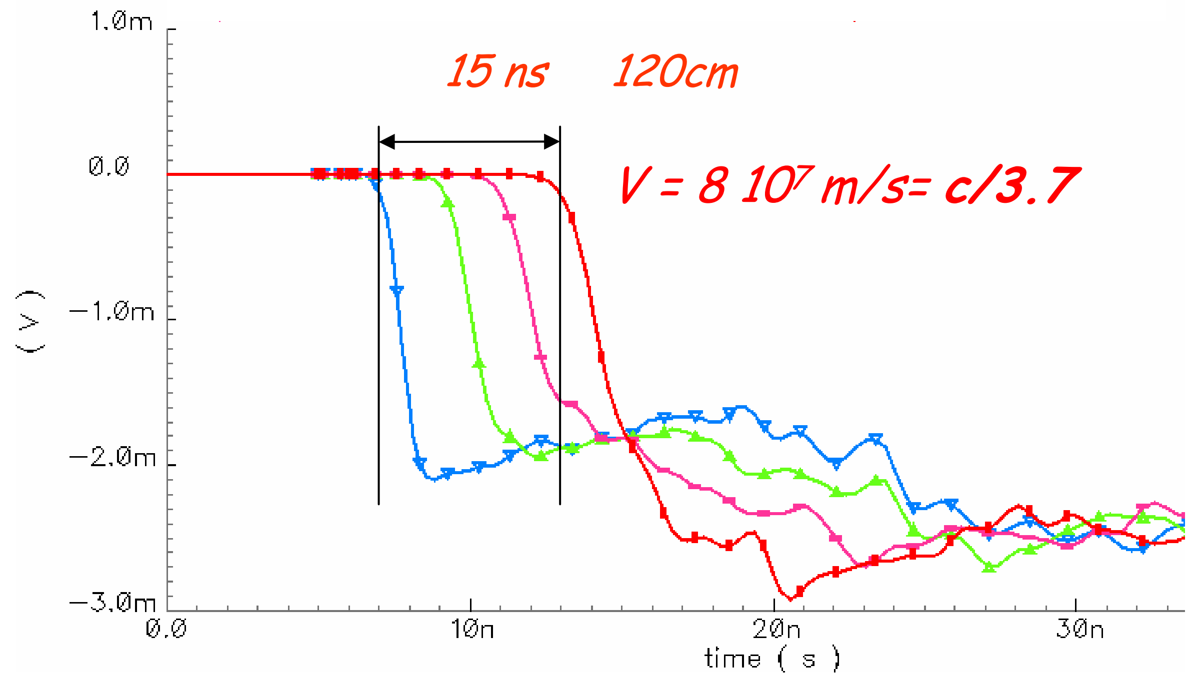
Coordinate along the strip

SPICE



$$V = 1/\sqrt{LC}$$

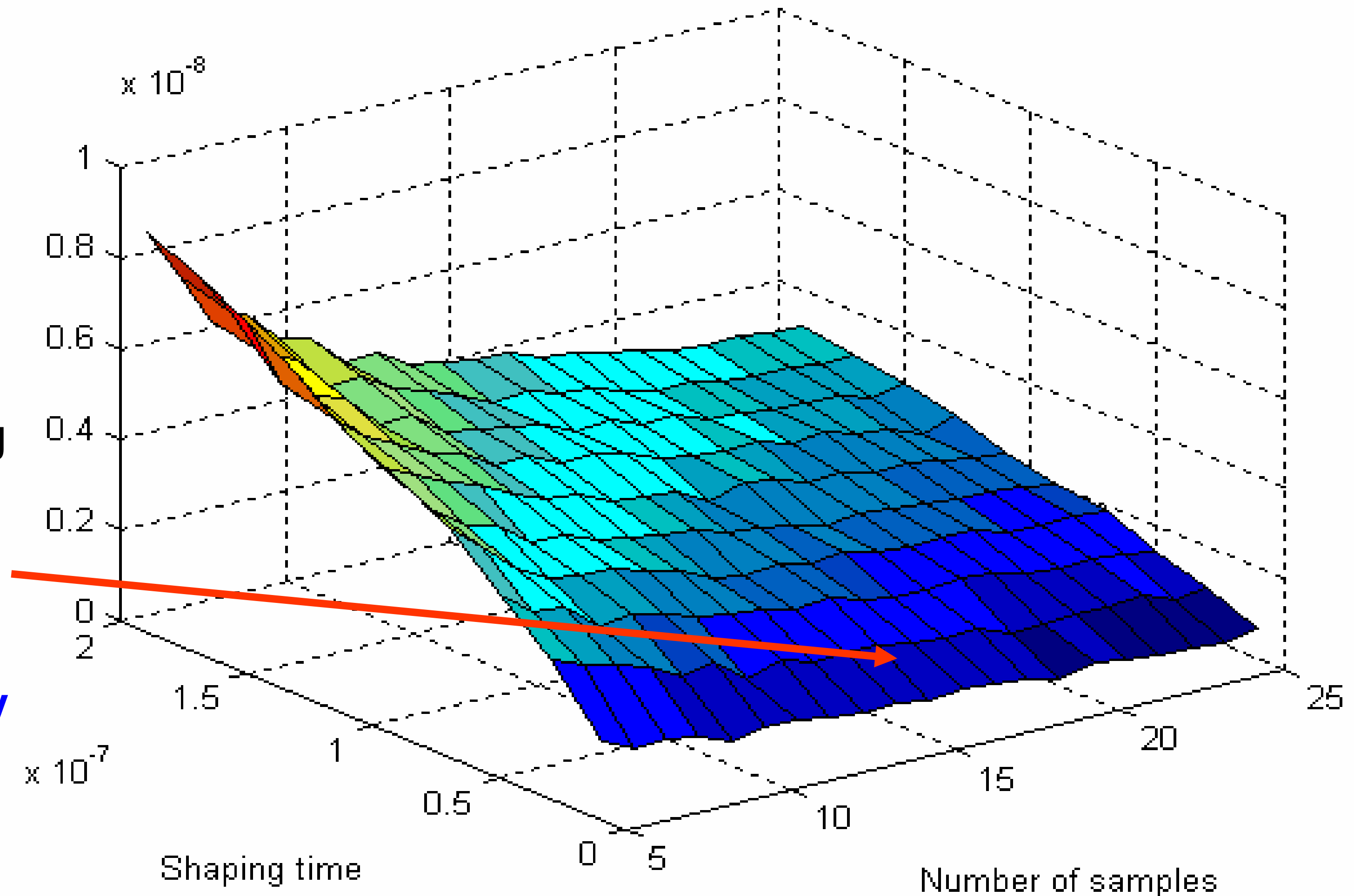
$V = 6.3e7\ 10^7\ m/s$ = ***c/4.7***



1 ns time resolution is 8 cm
Confirmed by measurements

Expected time resolution

Simulated time resolution using multiple sampling and a least square fit of the shaper pulse algorithm (Bill Cleland)



- S/N =25
- 16 samples
- 40 ns shaping

→ 1 ns time resolution

SiGe technology

Front-End Electronics Design

Silicon strips Electronics design

Guidelines

As compact as possible i.e. integrate whenever possible:

- Transparency
- Less passive parasitics: better S/N
- More reliable
- In principle simpler

Readout parameters

- Interstrip capacitance ~ 1 pF/cm
  Strip to substrate capacitance ~ 0.1 pF/cm
- Occupancy defined as % channels hit per BC:

  Outer barrel and end caps layers: < 1 %
  Inner barrel and end caps layers: < a few %
- ILC timing: 1 ms: ~ 3-6000 trains @150-300ns / BC
  100ms in between

Integrated Electronics

Front-End Electronics Chip

Front-end Analog:

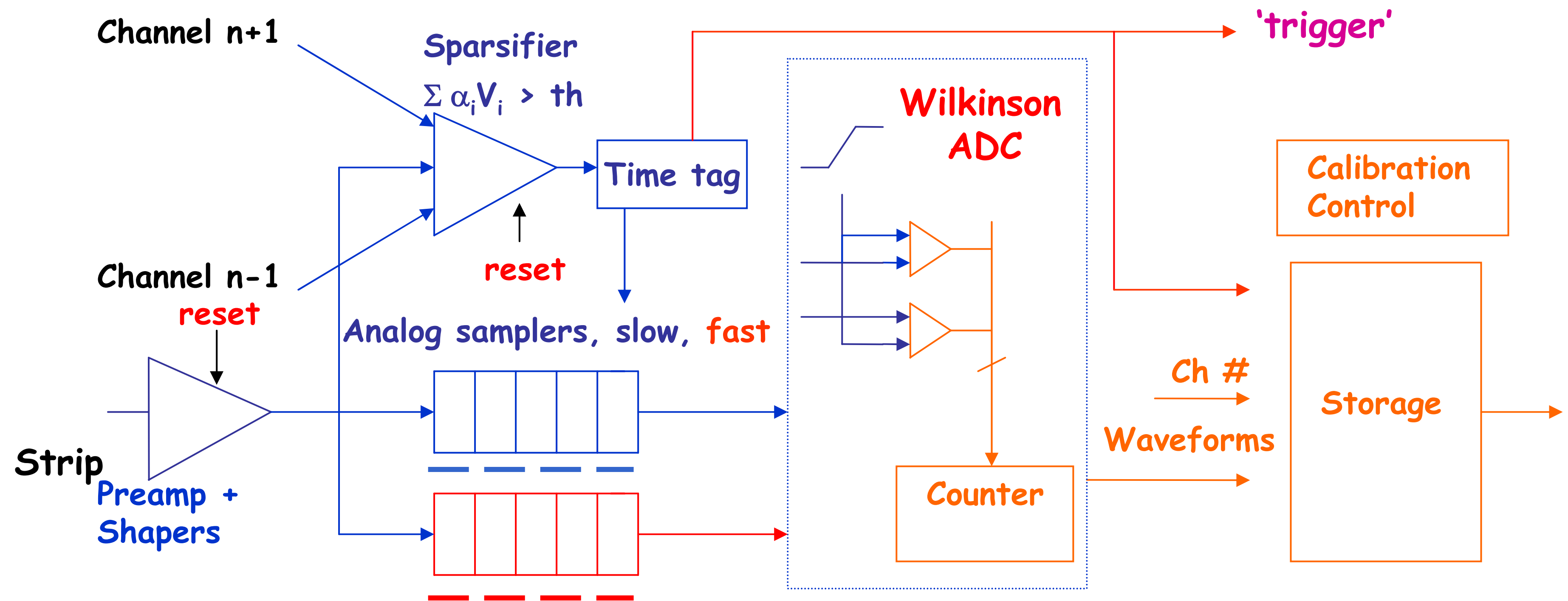
- Integrate 512-1024 channels in 130-90nm CMOS:

amplifiers	
shapers	two time scales wrt strip length
sparsification	
samplers	8 samples over two peaking times
ADC	Wilkinson optimum
Power switching	1/100

- Presently measured in 180nm CMOS

amplifiers:	500 + 16 e-/pF
shapers:	375 + 10.5 e-/pF

Foreseen Front-end architecture



Charge 1-40 MIP, S/N~ 15-20, Time resolution: BC tagging, fine: ~ 2ns

Technologies: Deep Sub-Micron CMOS 180-130nm
Future: SiGe &/or deeper DSM

Charge measurements

- Preamp + Shaper
  Gain: 20mV/MIP over 1-30 MIP
  S/N = 30 750 e- ENC at 3 µs peaking time
  Reset transistor

  → Presently AC coupled
  DC feedback to accommodate DC coupled detectors

- Analog sampler and event buffer
  2D: 16-deep sampling, a few 10-deep events

- Sparsifier
  Threshold an analog sum of 3 adjacent channels
  after pulse shaping. Auto-zeroed.

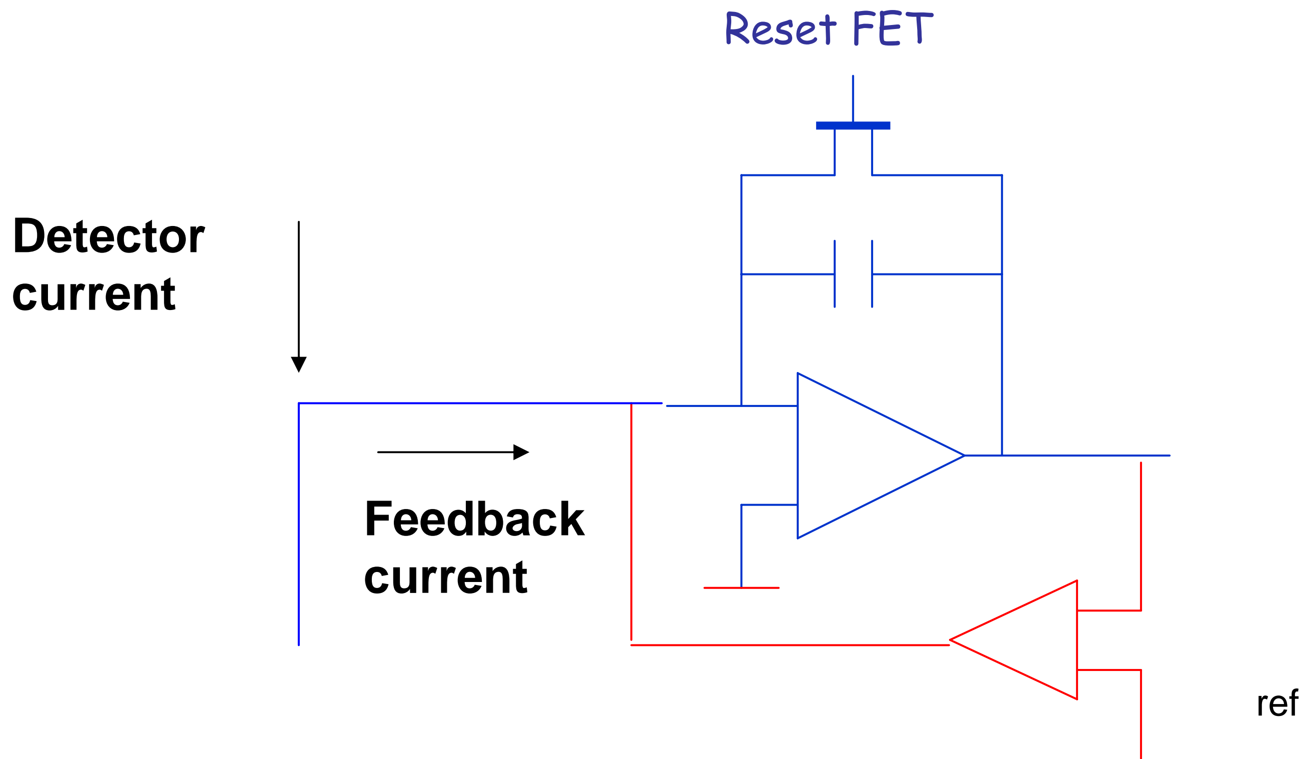
- ADC
  8-10 bits
  Clocked at 12 MHz, time interpolated if needed

DC feedback

PREAMPLIFIER

PROs: Cheaper detector
No oxide pinholes

CONs: Room (silicon area)
and power



Time measurements

- Time stamping

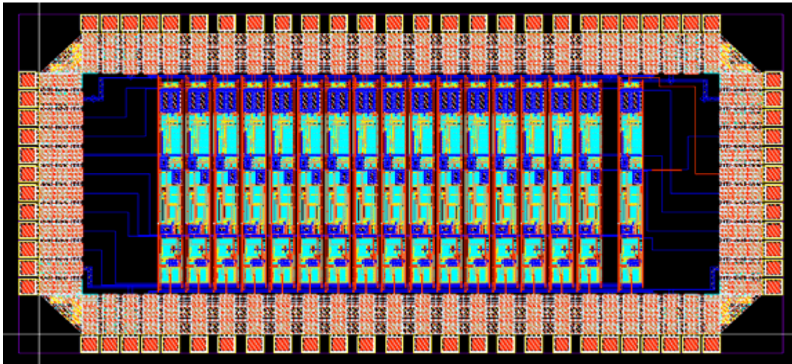
  BC tagging: resolution of 30 to 50 ns
  Time-stamp the sparsifier output at 4 * BCO clock (83 ns)

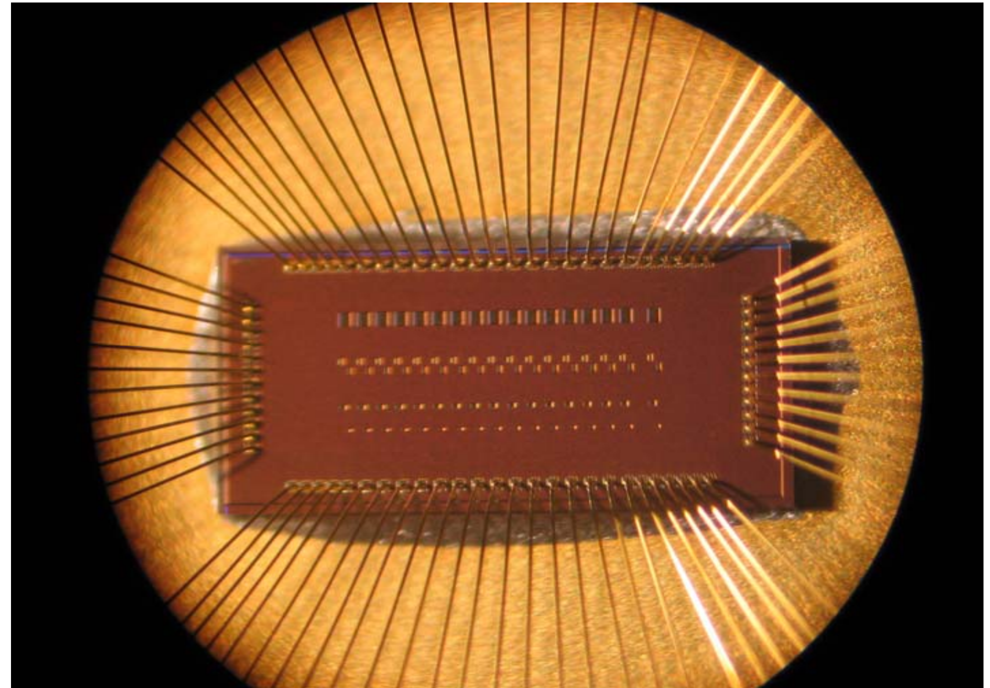
- Fine time measurement

  Order of 1 ns
  32 * BCO clock (12ns on-chip vernier sampling clock)
  Use digital signal processing over 16 digitized samples

CMOS 180nm Chip

Silicon

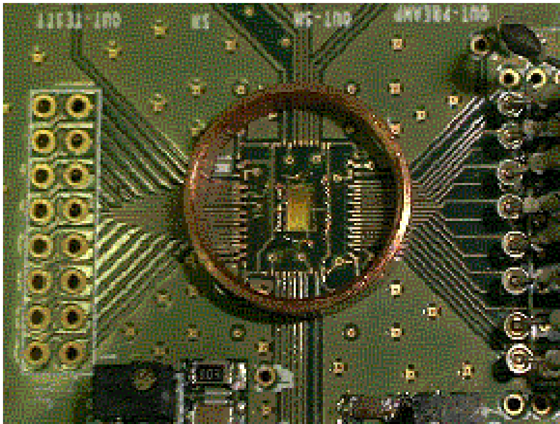




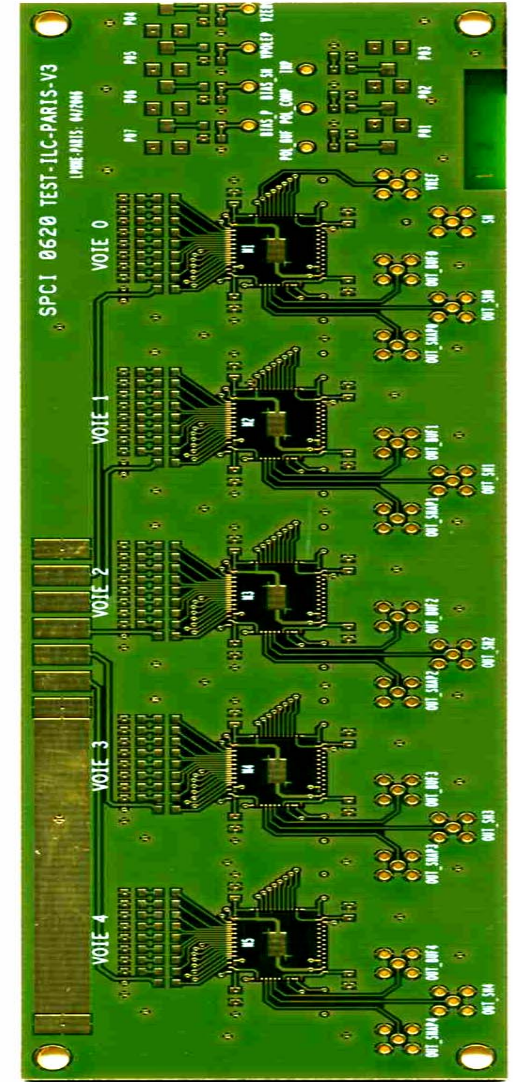
3mm

16 + 1 channel UMC 0.18 um chip (layout and picture)

Test Cards

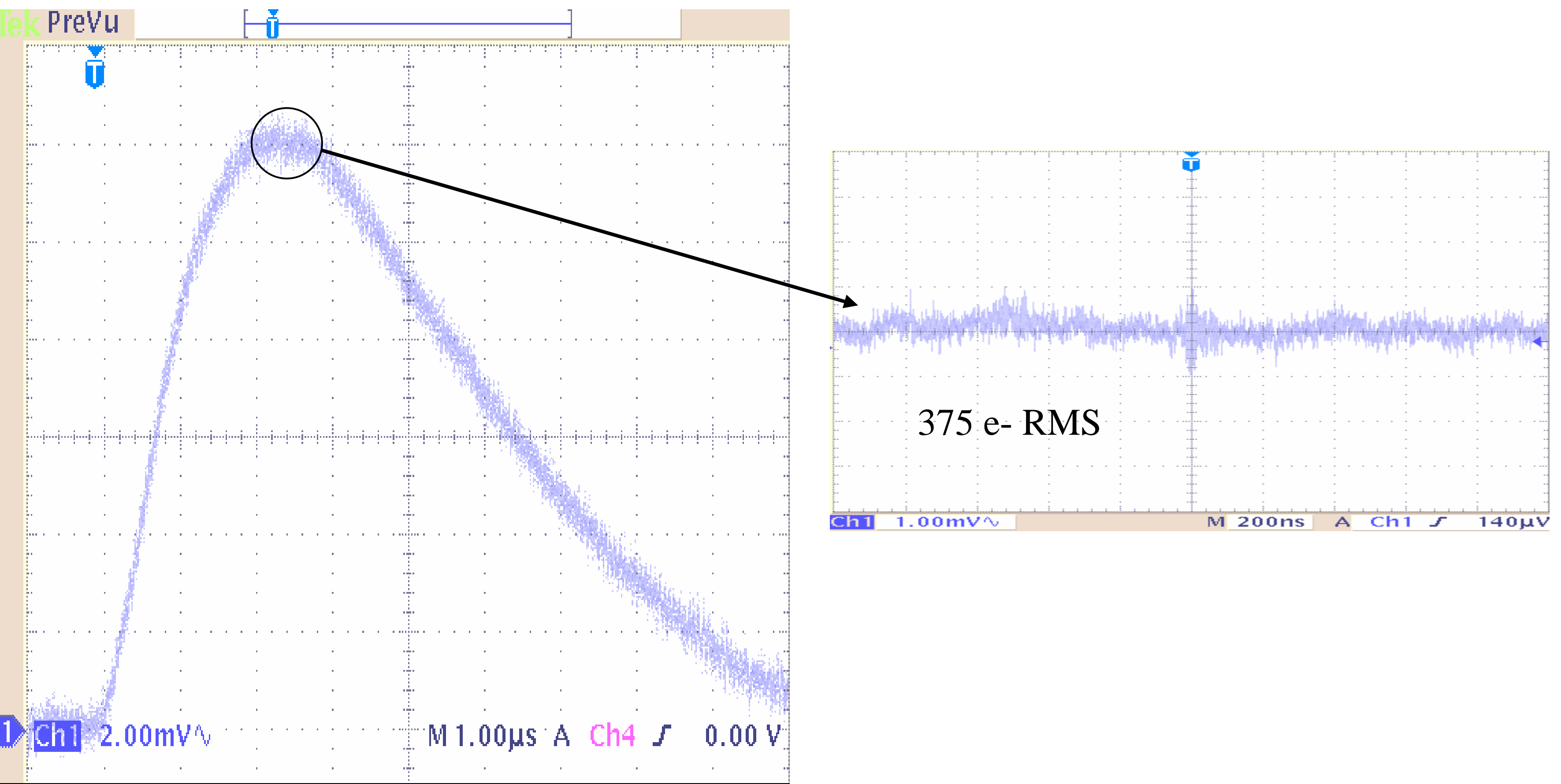


Chip on Board versions (wire bonded)



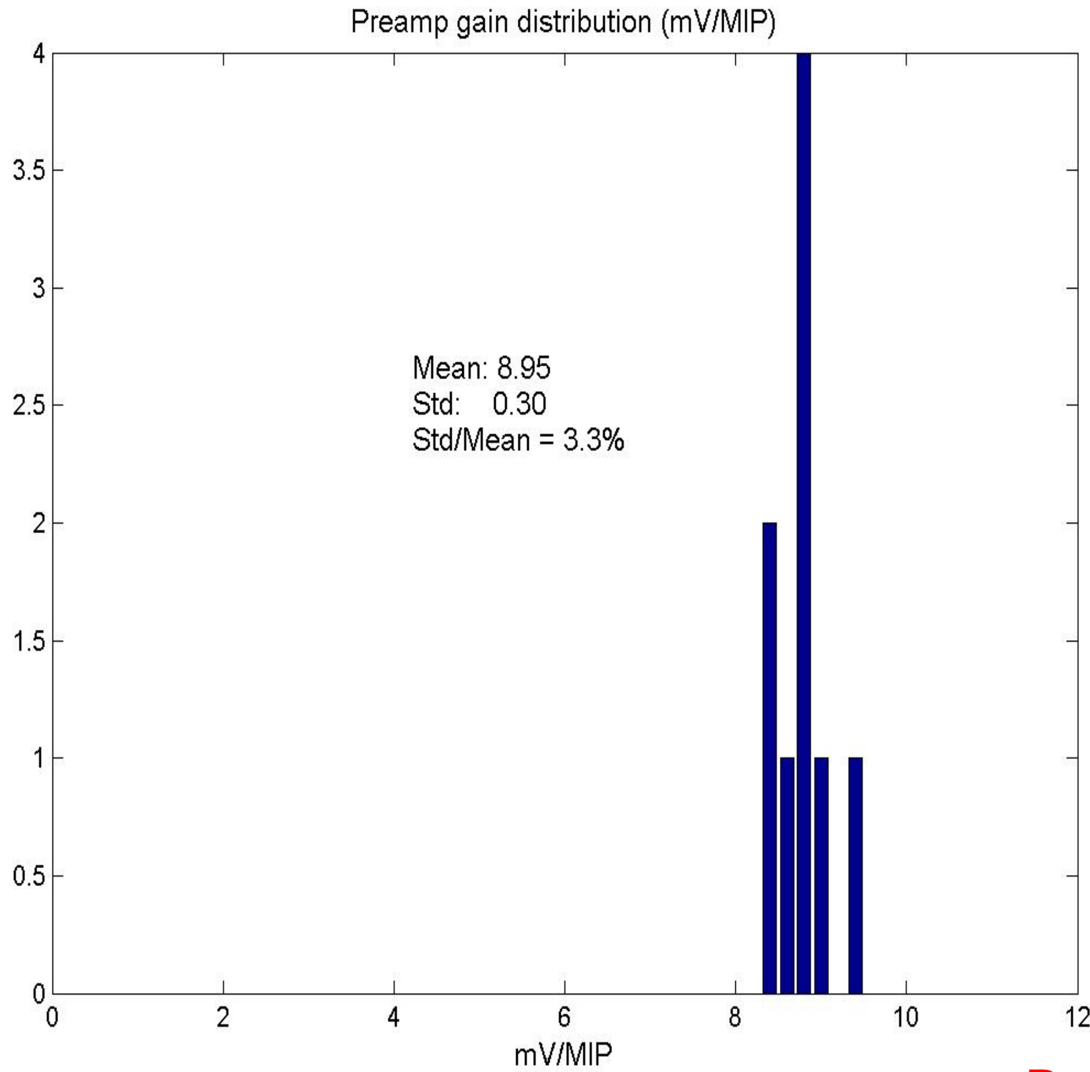
Beam tests card

Shaper Noise



375 e- input noise with chip-on-board wiring (against 280 simulated)

Process spreads



Preamp gains statistics

Process spreads: 3.3 %

Chip tests results

- Peaking time:

  1.5 - 6 µs tunable peaking time 1-10 targeted

  Linearity: +/- 6% +/- 1% targeted

- Noise @ 3 us shaping time and 140µW power:

  375 + 10.4 e-/pF 274 + 8.9 e-/pF expected

Sample & Hold Comparator

- Sample and hold: OK
- Comparator:

Vt spreads of the order of 5 mV due to transistors size

- Increase from 10/0.5 to 200/10 to reduce spreads
- Increase Preamp + Shaper voltage gain from 8 to 25 mV/MIP

Tests Conclusions

12 chips tested (Sept '05)

The UMC CMOS 180nm process is mature and reliable:

- Models mainly OK
- Only one transistor failure over 12 chips
- Process spreads of a few %

Chip to be checked in beam tests in Sept '06

Encouraging results regarding CMOS DSM

→ go to 130nm

CMOS 130nm chip design

Front-end in CMOS 130nm

130nm CMOS:

- Smaller
- Faster
- More radiation tolerant
- Lower power
- Will be (is) dominant in industry

Drawbacks:

- Reduced voltage swing (Electric field constant)
- Leaks (gate/subthreshold channel)
- Models more complex, not always up to date
- Crosstalk (digital)

Technology parameters

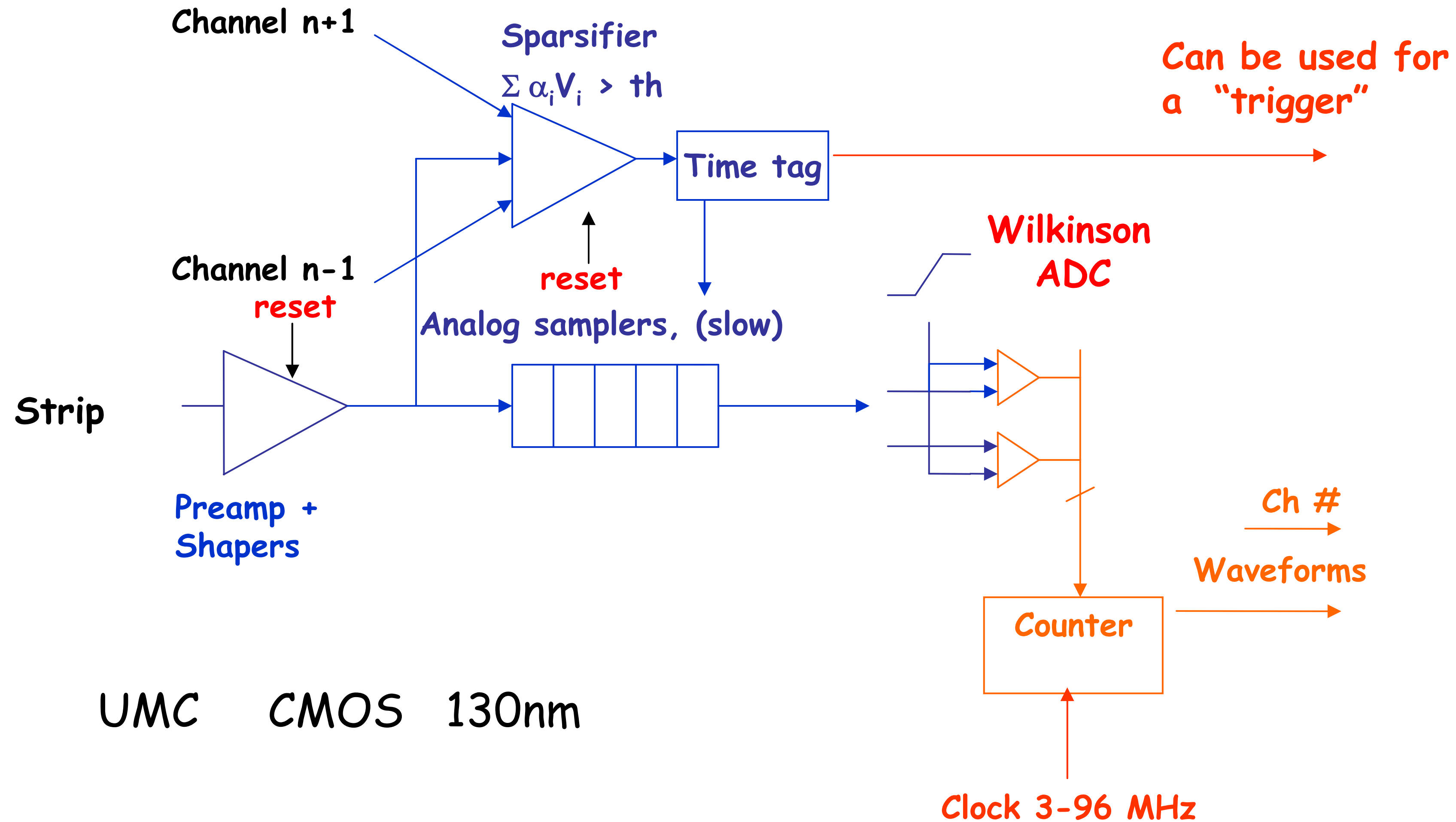
180 nm

- 3.3V transistors
- 1.8V logic supply
- 6 metals layers (Al)
- MIM capacitors = 1fF/μm^2
- Three Vt options

130nm

- 3.3V transistors
- 1.2V logic supply
- 8 metals layers (Copper)
- MIM capacitors =1.5fF/μm^2
- Three Vt options +
- Low leakage transistors option

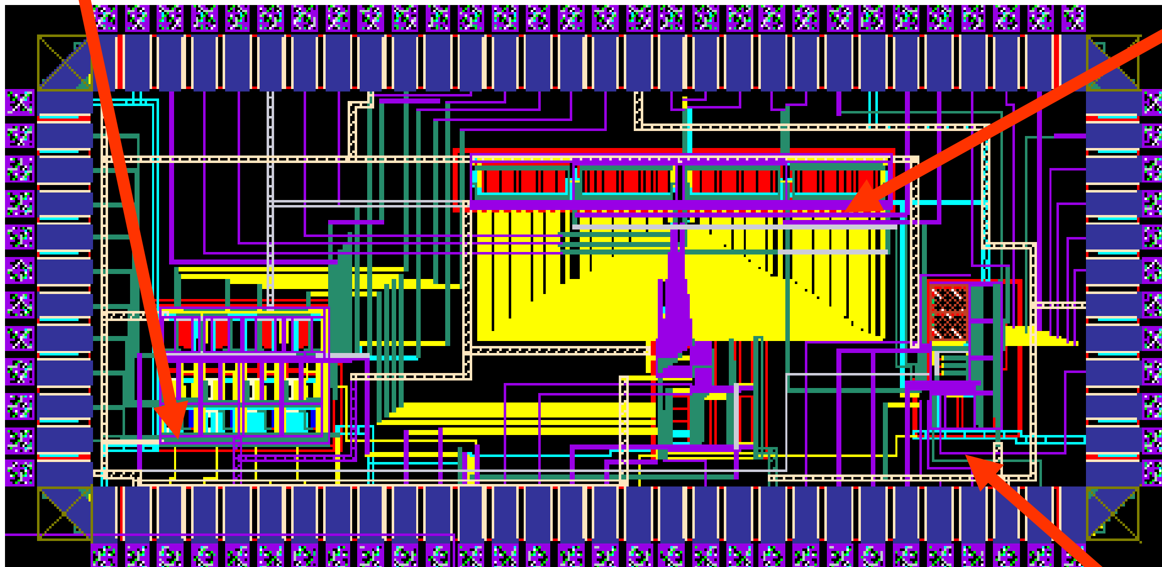
4-channel test chip



130nm CMOS chip

Amplifier, Shaper, Sparsifier 90*350 μm2

Analog sampler 250*100 μm



Layout of the 130nm chip including sampling and A/D conversion

A/D 90*200 μm

Submitted April 19th '06
Reception July

Test card under design

Some issues with 130nm design

- Noise not properly modeled:

  1/f noise out of belief… (both coefficient and exponent)

- Design rules more constraining
- Lower power supplies voltages

  Low Vt transistors leaky

- Some (via densities) not available under Cadence (Mentor)

Possible issues: Transistors leaks

Two situations:

- **Gate-channel due to tunnel effect (can affect noise performances)**
- **Through channel when transistor switched-off (only affects large digital designs)**

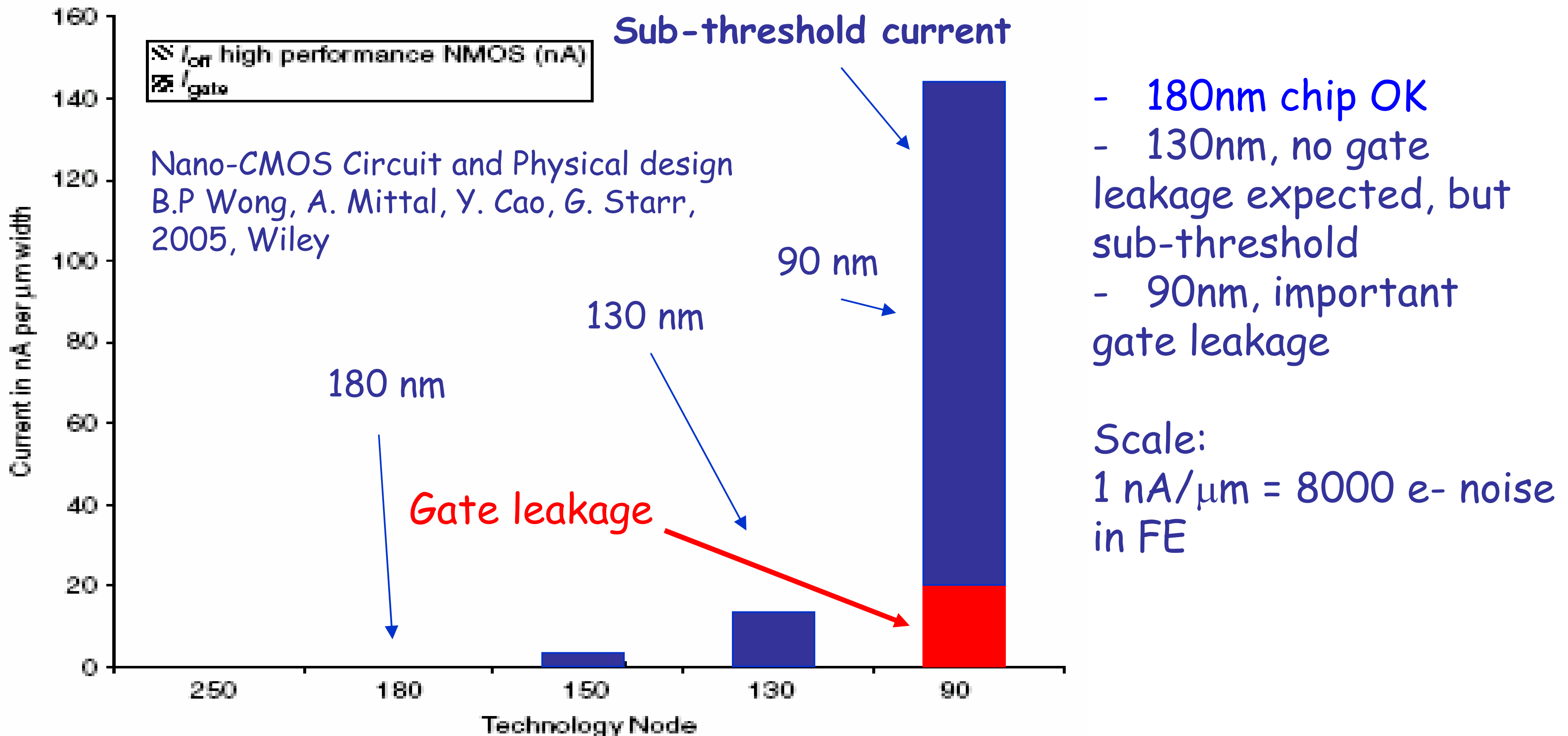


Figure 1.2 I_{gate} and subthreshold leakage versus technology.

- 180nm chip OK
- 130nm, no gate leakage expected, but sub-threshold
- 90nm, important gate leakage

Scale:
1 nA/μm = 8000 e- noise in FE

Future plans

- Improve sampler (130nm August)
  DC coupling, Calibration, Power cycling

- Implement the fast (20-100ns shaping) version with Silicon-Germanium / CMOS including:

  - AC or DC coupling
  - Preamp + Shaper (20-100ns)
  - Fast sampling
  - Power cycling

- Submit a full 128 channel version in 130nm including slow analog processing, power cycling, digital

Future Digital

- Chip control
- Buffer memory
- Processing for
  - Calibrations
  - Amplitude and time least squares estimation, centroids
  - Raw data after zero suppression lossless compression
- Tools
  - Digital libraries in 130nm CMOS available
  - Synthesis from VHDL/Verilog
  - SRAM memory
  - PLLs

Detector integration

Grounding & Shielding

- Signal is referred to the backplane

  AC stick preamp input reference to this voltage
  On-FE chip decoupling as much as possible

- Shield all detector from external interferences using a thin aluminum foil wrapped around the carbon fiber support structure

- Digital I/Os

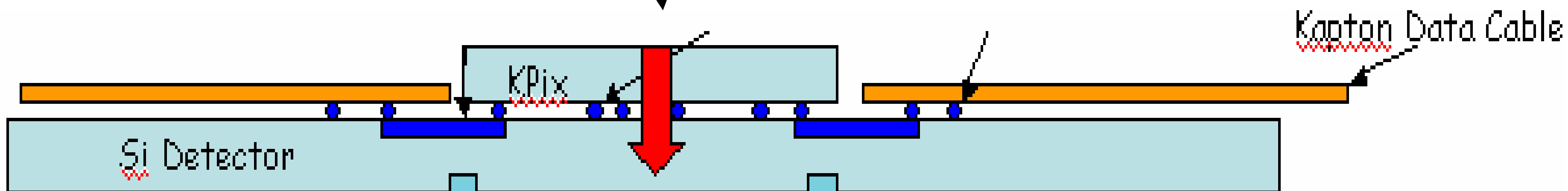
  Use fiber optics:

  - Trains stage: 3-6 MHz BCO synchronous controls
  - Digitization stage: 100 MHz ADC clock
  - Transfer stage: >1 GHz fiber serial clock

Wiring Detector to FE Chips

~~Wire bonding~~

Flip Chip Technology



Courtesy: Marty Breidenbach (Cal SiD)

OR (later)

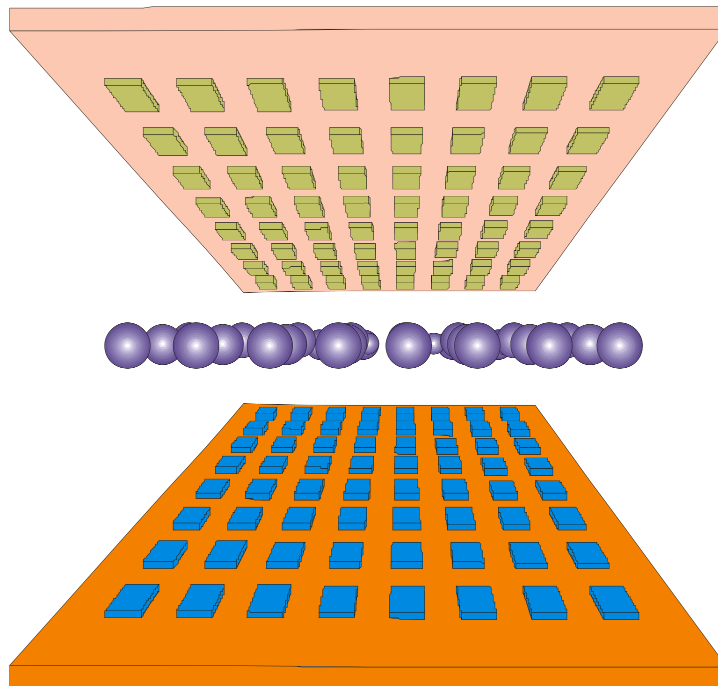
Bump bonding flip chip technology

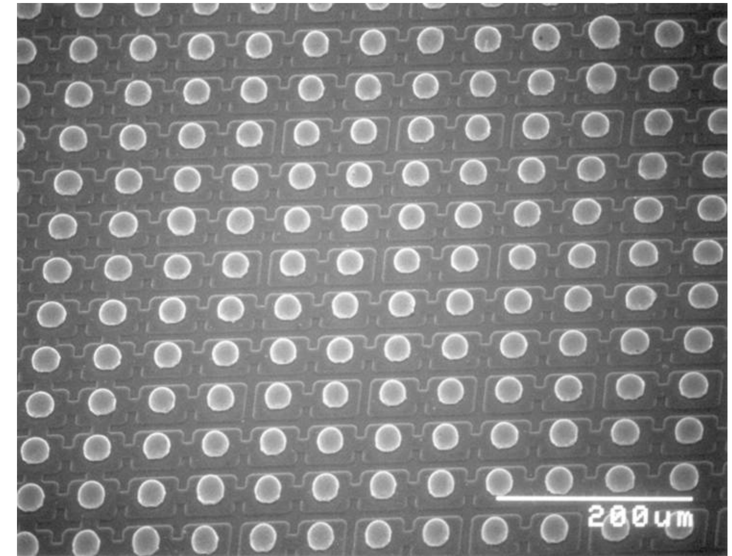
- Electrical connection of chip to substrate or chip to chip face to face

  flip chip

- Use of small metal bumps

  bump bonding





CNM

- Process steps:
  - Pad metal conditioning: Under Bump Metallisation (UBM)
  - Bump growing in one or two of the elements
  - Flip chip and alignment
  - Reflow
  - Optionally underfilling

Wiring Detector to FE Chips

Thinned Wafers

Thinned wafer mounted on Quartz handle wafer (MIT Lincoln Labs)

Wafer thinned to 50 microns (leti)

May 2006 FEE 2006

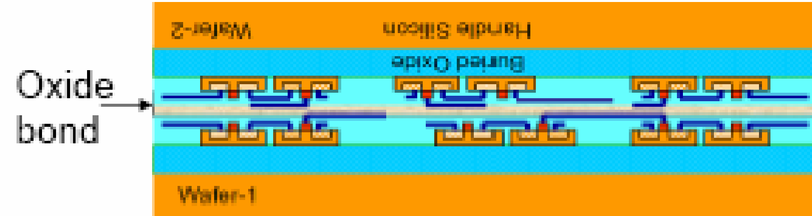
Courtesy: Ray Yarema, FEE 2006, Perugia

3D Wiring

Process flow for 3D Chip

- 3 tier chip (tier 1 may be CMOS)
  - 0.18 um (all layers)
  - SOI simplifies via formation
- Single vendor processing

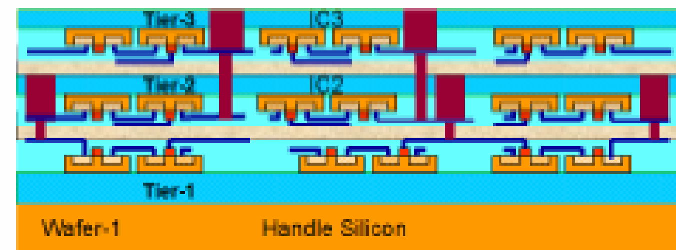
2) Invert, align, and bond wafer 2 to wafer 1



3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten

1) Fabricate individual tiers

4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



May 2006 FEE 2006 36

Courtesy: Ray Yarema, FEE 2006, Perugia

Beam Tests

Beam-tests at DESY

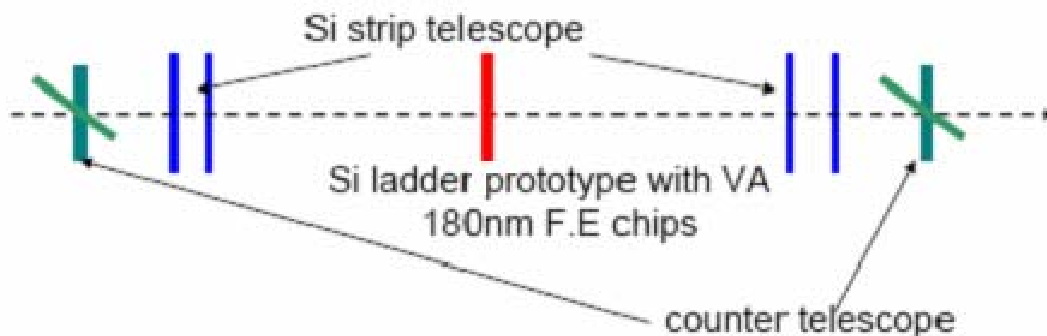
At 5 Gev e- beam in DESY

Very simple telescope set-up in Silicon strips ladders of CMS read out with VA1 FE and a few channels with present version of new FE chip together with a reference telescope

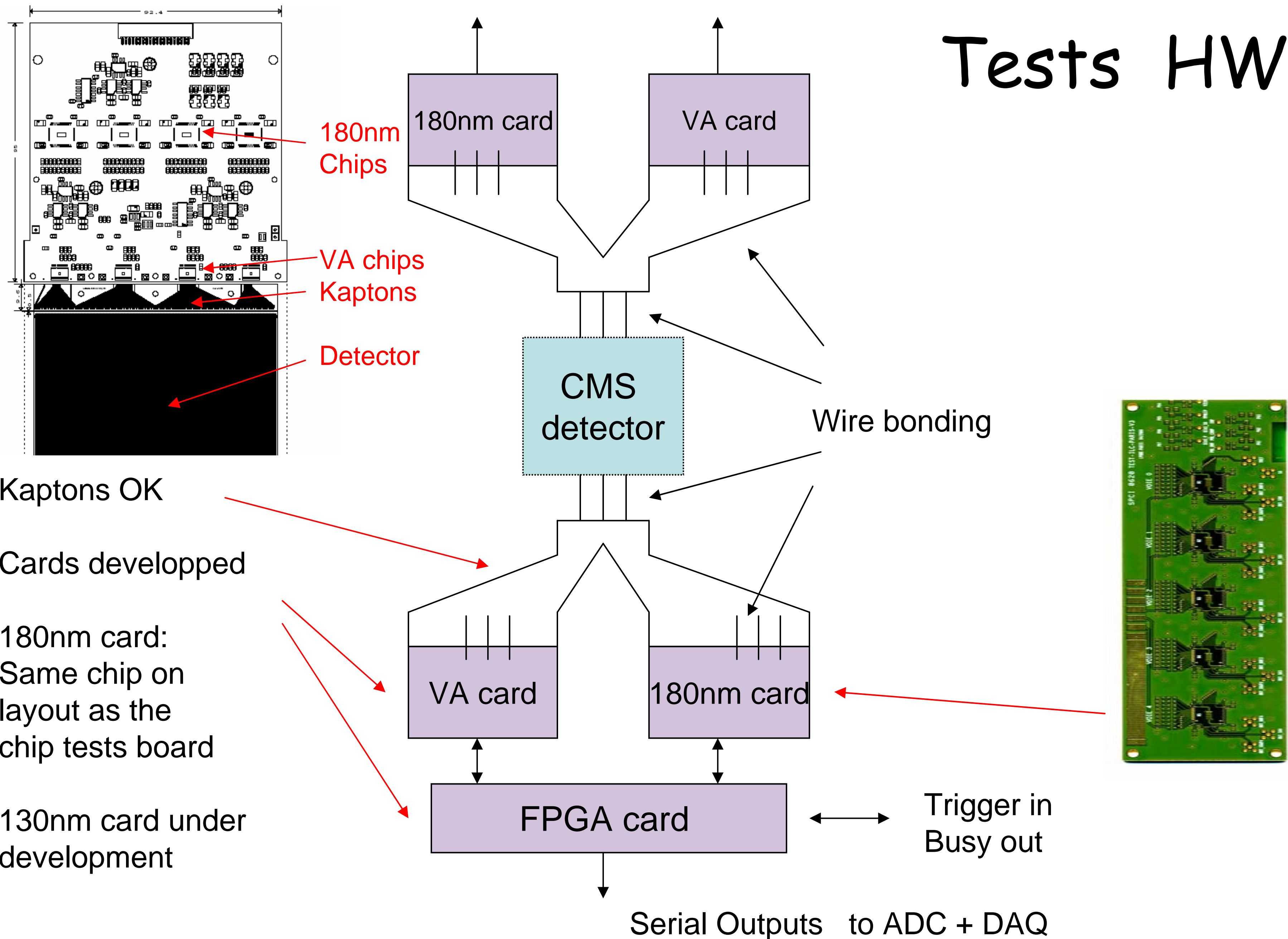
Purposes:

Check S/N for the first proto measured at Lab test bench

Characterize performance of the new FE chip in realistic conditions after Lab test bench and comparing with ref FE electronics (VA1)

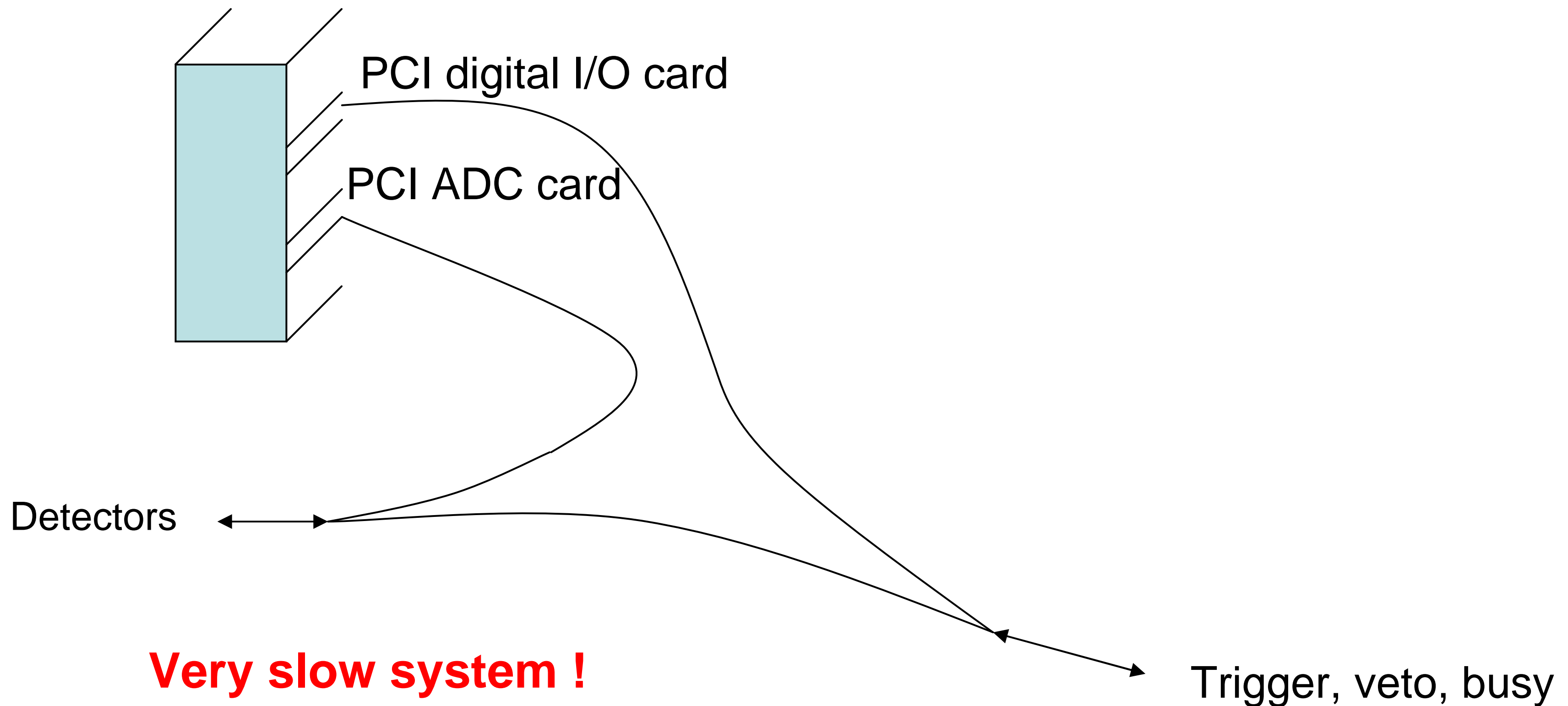


Beam timing: 1μs e- 30μs readout


Tests HW
180nm Chips
VA chips
Kaptons
Detector
180nm card
VA card
CMS detector
Wire bonding
VA card
180nm card
FPGA card
Trigger in
Busy out
Serial Outputs to ADC + DAQ
Kaptons OK
Cards developped
180nm card:
Same chip on layout as the chip tests board
130nm card under development

Tests DAQ September

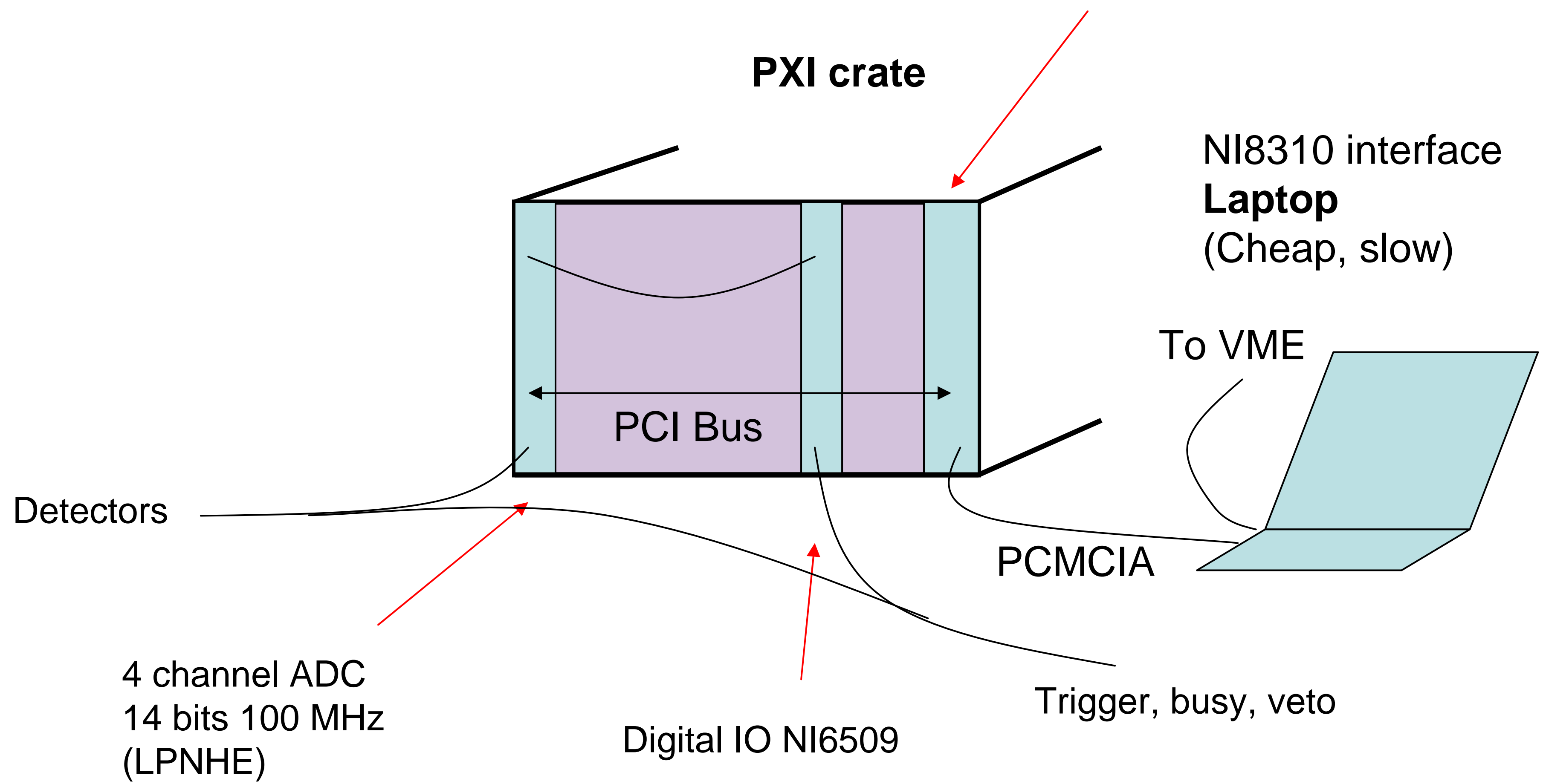
Paris present setup



Very slow system !

Tests DAQ December

PXI under development

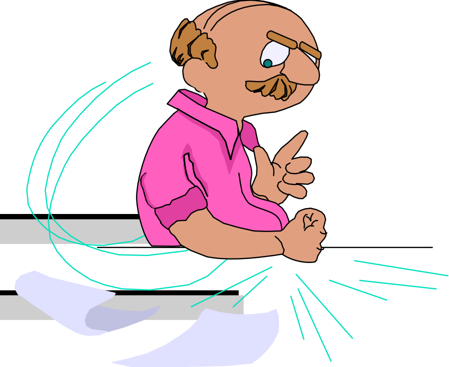


The End …

Backup

Foreseen on-detector FE chip

- Pulse sampling: *16 samples over 2 shaping times (inc pedestal)*
  16-deep sampling analog buffer
- Buffering: *a few 10 events buffer*
  *2D structure: (a few 10)*16 caps/channel*
- Sparsification/calibration : *On FE chip*
- Analog-Digital conversion: *Wilkinson optimum (power)*
- Digital processing: *Amplitude and time estimation + charge cluster algorithm, lossless data compression*
- Power: 1/100 ILC duty cycle: *FE Power cycling*



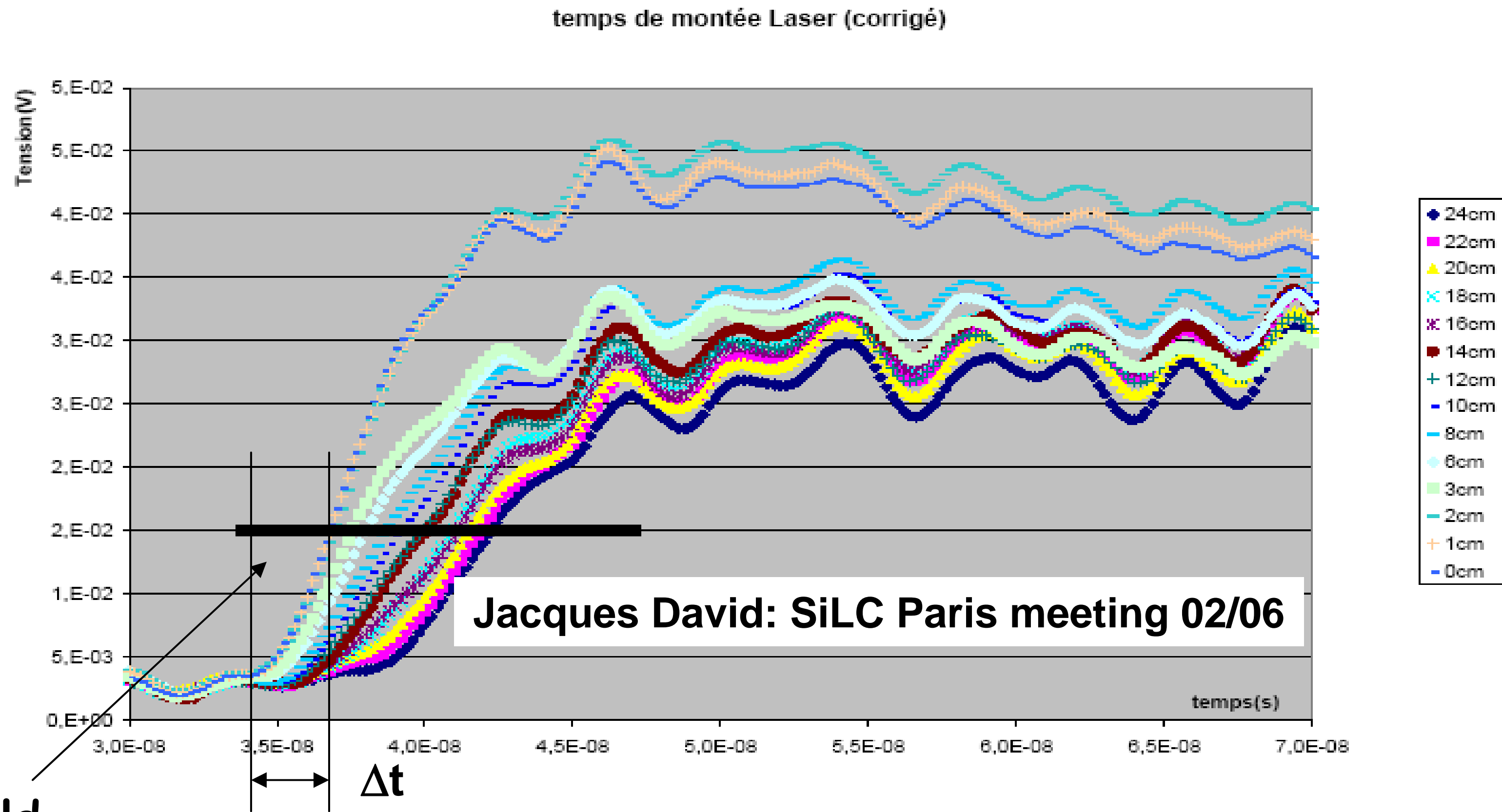
Patrick Le Du (Saclay): Summary of current thinking

The ILC environment poses new challenges & opportunities which will need new technical advances in Data Collection

→ NOT LEP/SLD, NOT LHC !

- The FEE integrates everything
  - →From signal processing & digitizer to the RO BUFFER …
- Very large number of channels to manage (Trackers & ECal)
- Interface and feedback between detector and machine is fundamental
  - →optimize the luminosity → consequence on the DAQ architecture
- Classical boundaries are moving : Slow control, On/Off line …

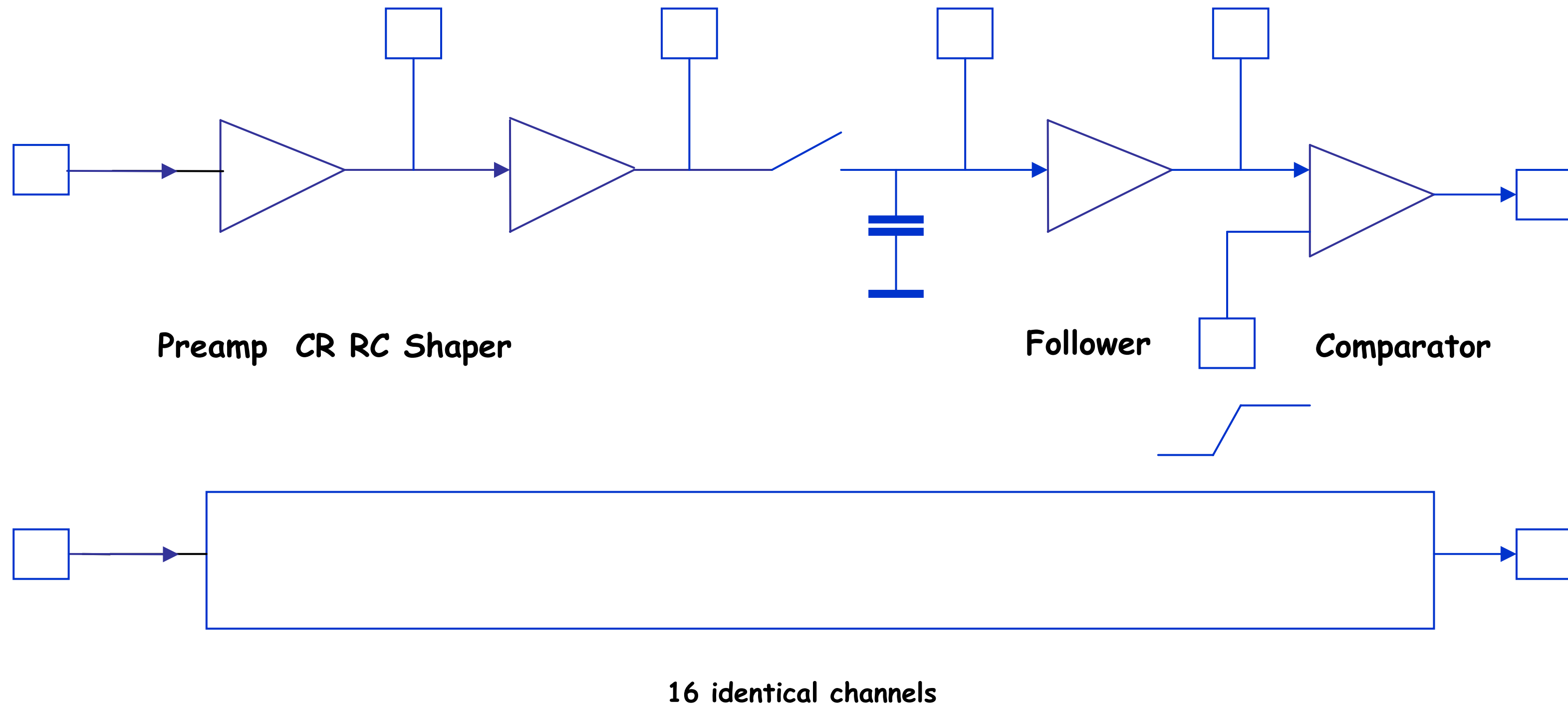
Measured Pulse Velocity



Threshold

Moving a laser diode along the Silicon strip detector

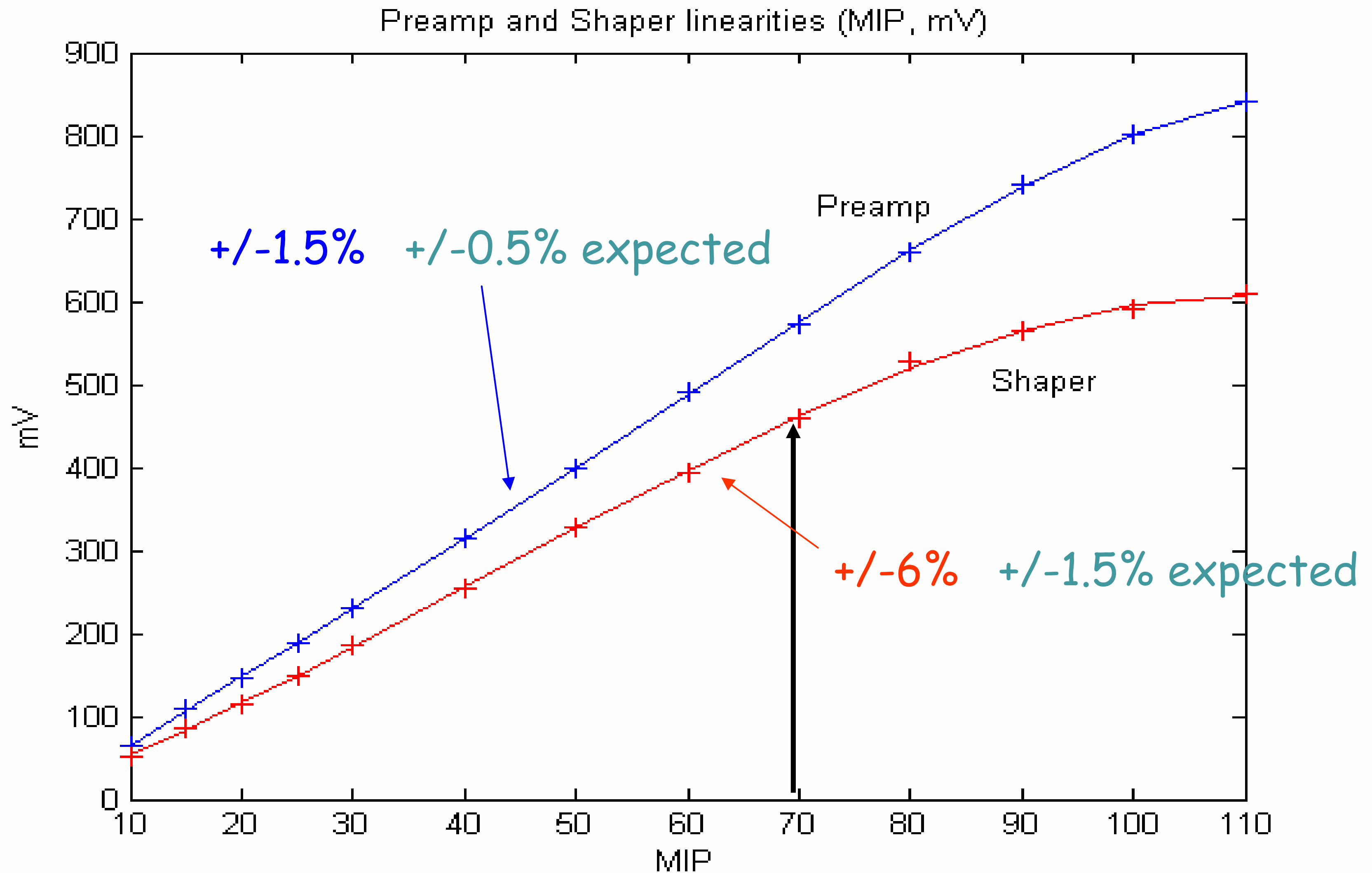
Front-end test chip in CMOS 180nm



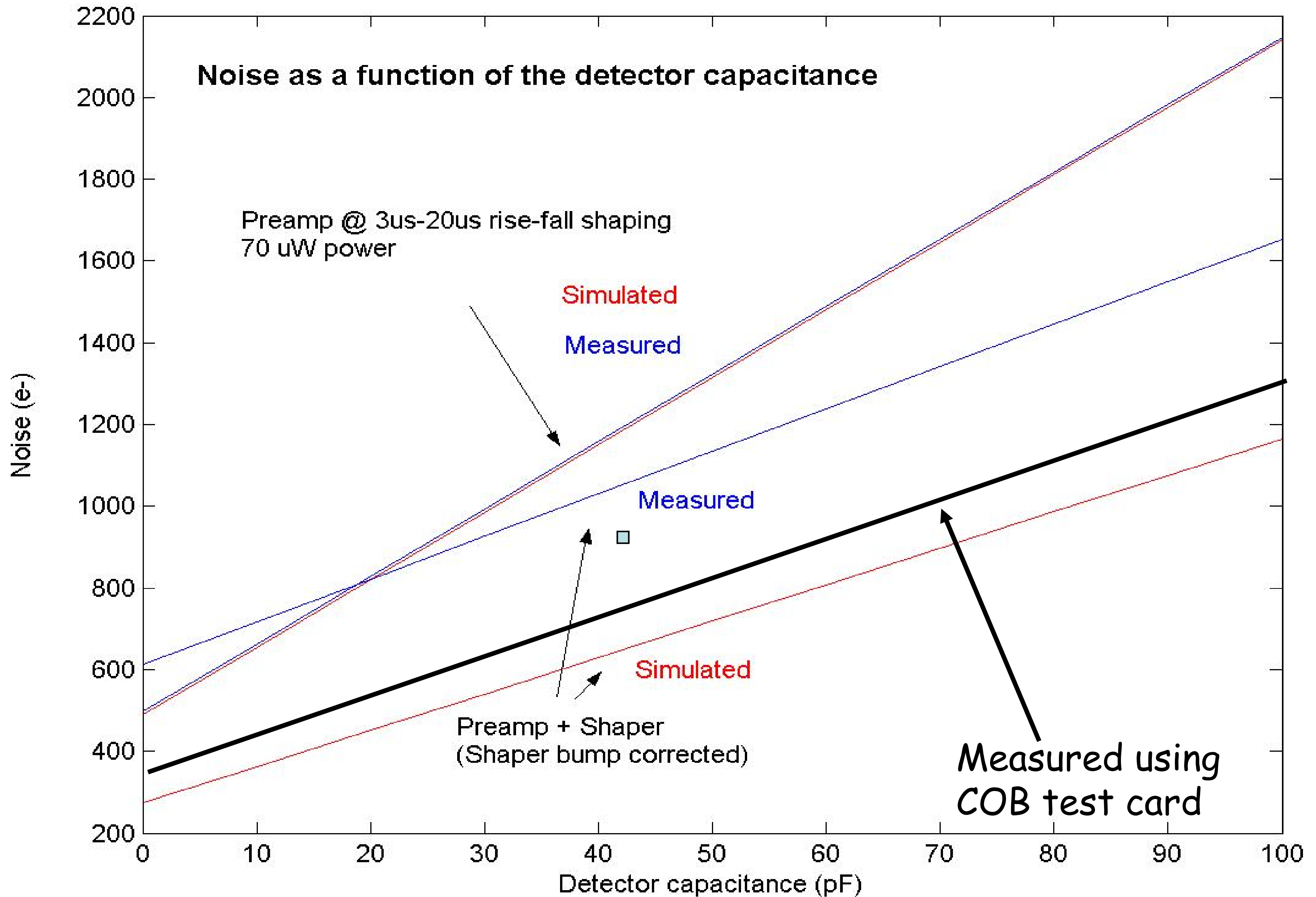
- Low noise amplification + pulse shaping
- Sample & hold
- Comparator

Submitted end '04

Linearities

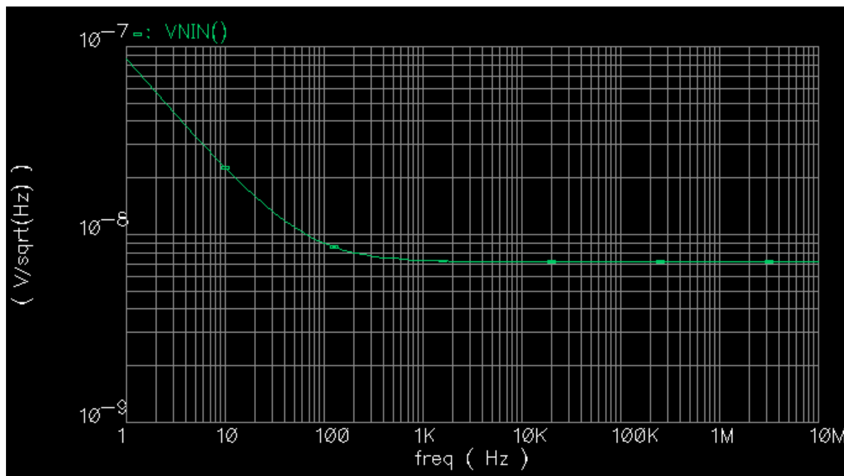


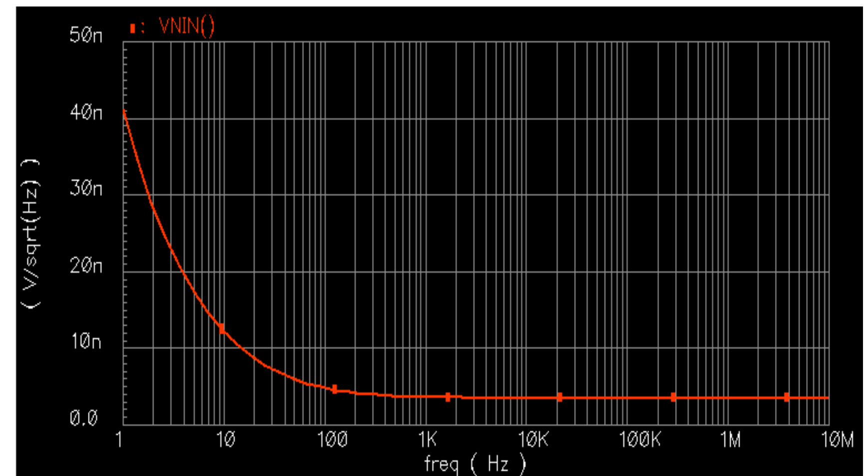
Noise summary



Possible issues: noise: 130nm vs 180nm (simulation)

- **PMOS:**





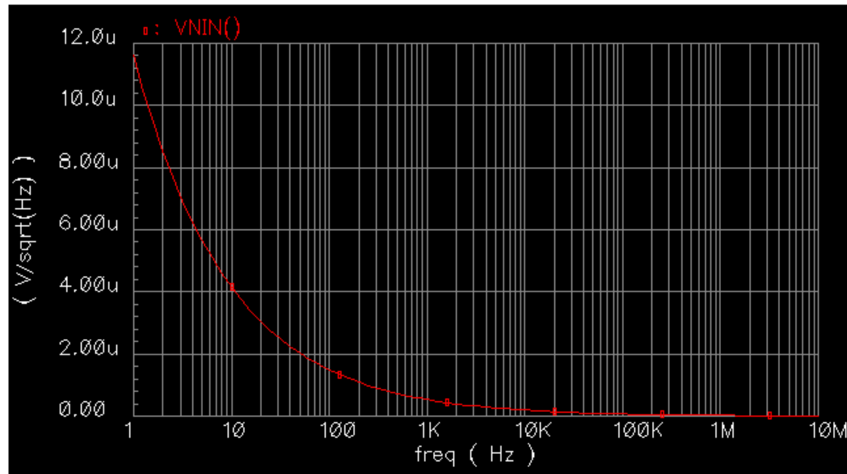
130nm
W/L = 2mm/0.5u
Ids = 38.79u,Vgs=-190mV,Vds=-600mV
gm=815.245u,gms=354.118u
1MHz → 7.16nV/sqrt(Hz)
Thermal noise hand calculation = 3.68nV/sqrt(Hz)

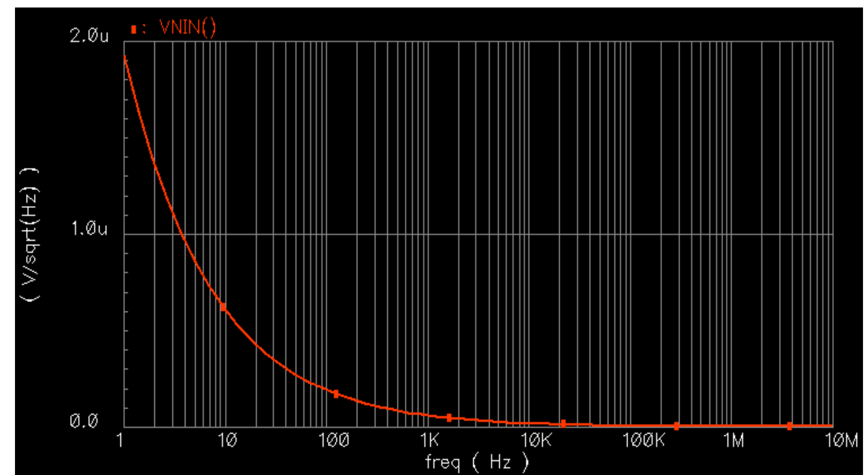
180nm

gm=944.4uS,gms=203.1uS
1MHz → 3.508nV/sqrt(Hz)
Thermal noise hand calculation = 3.42nV/sqrt(Hz)

Noise: 130nm vs 180nm (simulation)

NMOS :



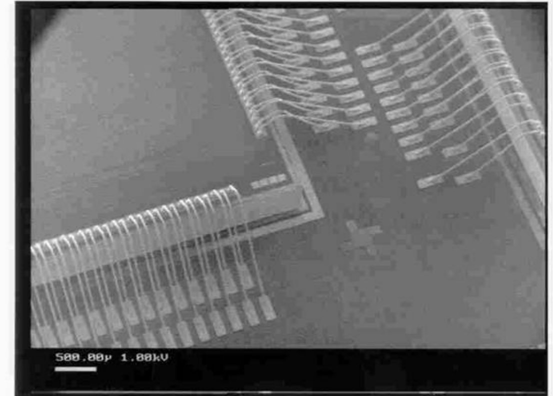


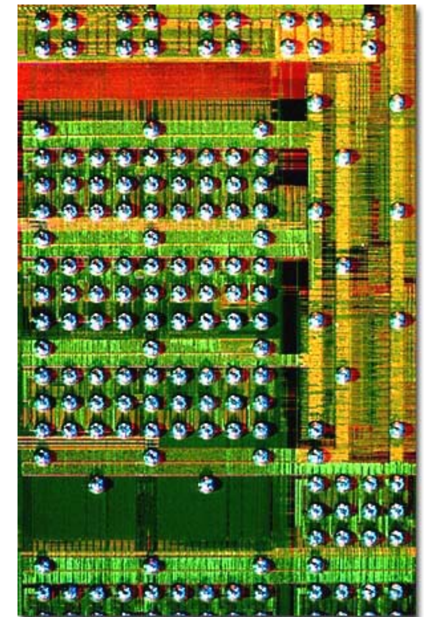
130nm
W/L = 50u/0.5u
Ids=48.0505u,Vgs=260mV,Vds=1.2V
gm=772.031uS,gms=245.341uS,gds=6.3575uS
1MHz --> 24.65nV/sqrt(Hz)
100MHz --> 5nV/sqrt(Hz)
Thermal noise hand calculation = 3.78nV/sqrt(Hz)

180nm
W/L=50u/0.5u
Ids=47uA,Vgs=300mV,Vds=1.2V
gm=842.8uS,gms=141.2uS,gds=16.05uS
1MHz --> 4nV/sqrt(Hz)
10MHz --> 3.49nV/sqrt(Hz)
Thermal noise hand calculation = 3.62nV/sqrt(Hz)

Manuel Lozano (CNM Barcelona)

Chip connection





- Wire bonding
  - Only periphery of chip available for IO connections
  - Mechanical bonding of one pin at a time (sequential)
  - Cooling from back of chip
  - High inductance (~1nH)
  - Mechanical breakage risk (i.e. CMS, CDF)
- Flip-chip
  - Whole chip area available for IO connections
  - Automatic alignment
  - One step process (parallel)
  - Cooling via balls (front) and back if required
  - Thermal matching between chip and substrate required
  - Low inductance (~0.1nH)

Manuel Lozano (CNM Barcelona)

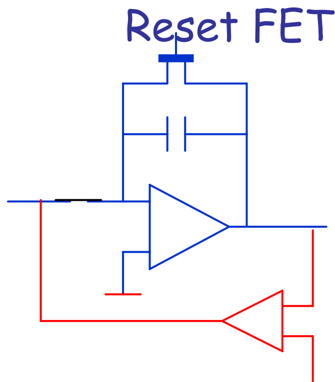
Bump bonding flip chip technology

- Expensive technology
  - Especially for small quantities (as in HEP)
  - Big overhead of NRE costs
- Minimal pitch reported: 18 μm but ...
- Few commercial companies for fine pitch applications (< 75 μm)

- Bumping technologies
  - Evaporation through metallic mask
  - Evaporation with thick photoresist
  - Screen printing
  - Stud bumping (SBB)
  - Electroplating
  - Electroless plating
  - Conductive Polymer Bumps
  - Indium evaporation

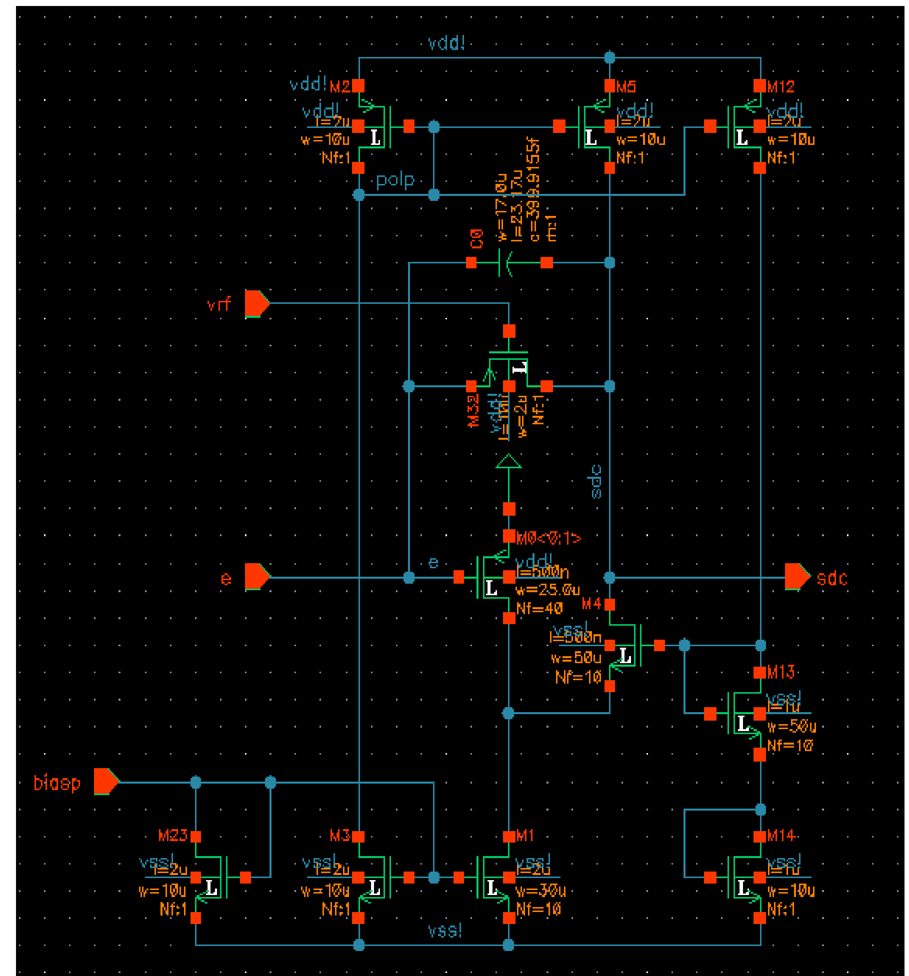
0.18 µm chip

PREAMPLIFIER



ref

Gain: 8mV/MIP
3.3V input trans
2000/0.5
gm = 0.69 mS
40 µA (Weak inversion
IC ~= 0.01)



Tests results :

Gain OK

Linearity : +/-1.5% +/-0.5% expected

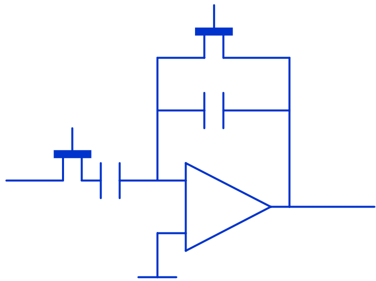
Noise 3µs-20µs rise-fall,

40 µA : 498 + 16.5 e-/pF OK

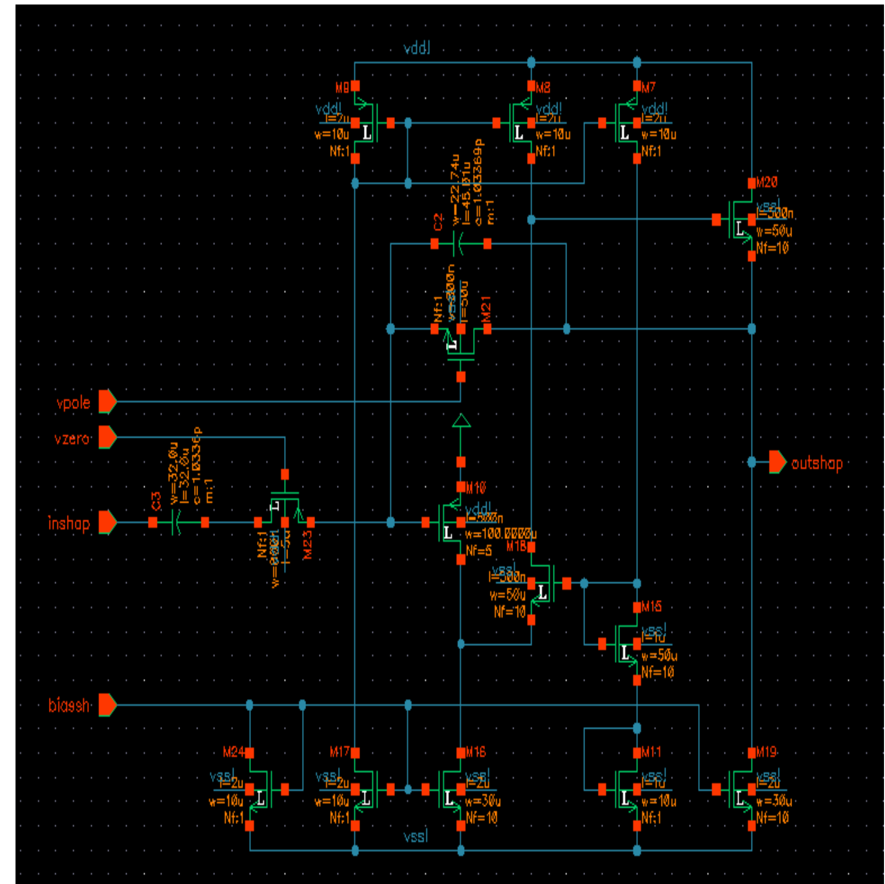
Dynamic range : 60 MIPs OK

0.18 µm chip

SHAPER



RC-CR
Peaking time
ajustable :1µs -> 5µs



Tests:

1.5 - 6 µs rise/fall

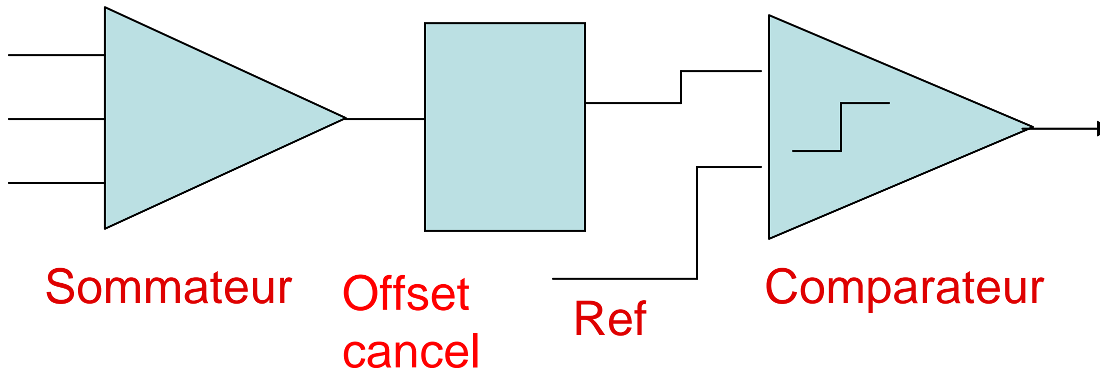
Linearity: +/- 6% +/- 1% expected

Noise @ 3 µs 140µW power :

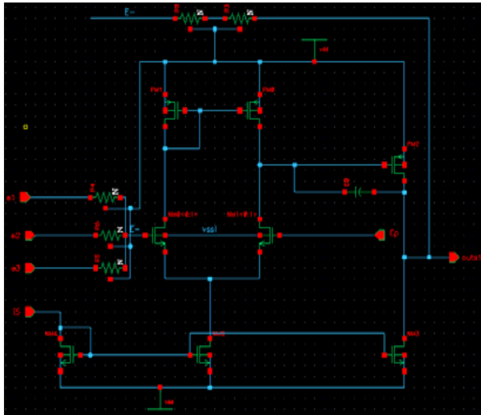
375 + 10.4 e-/pF 274 + 8.9 e-/pF expected

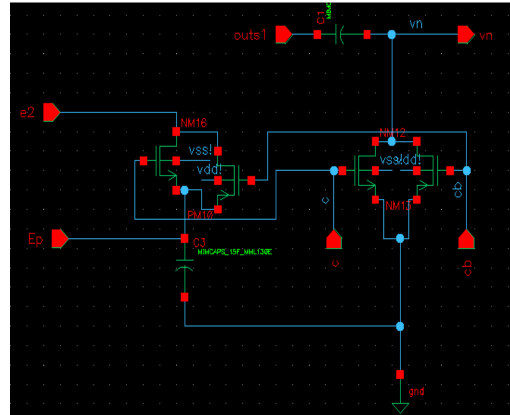
0.13 μm Chip Sparsifier

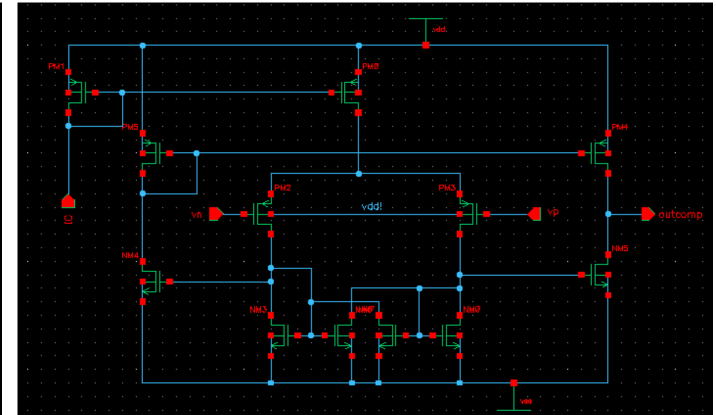
SPARSIFICATION



+ Sum of3 adjacent channels
+ Résolution ~ 0.1mV
+ Response time = 186ns

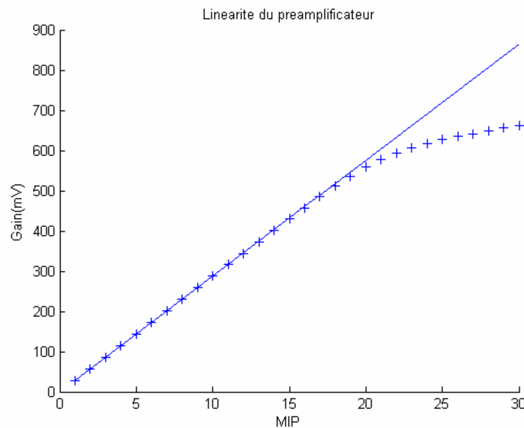




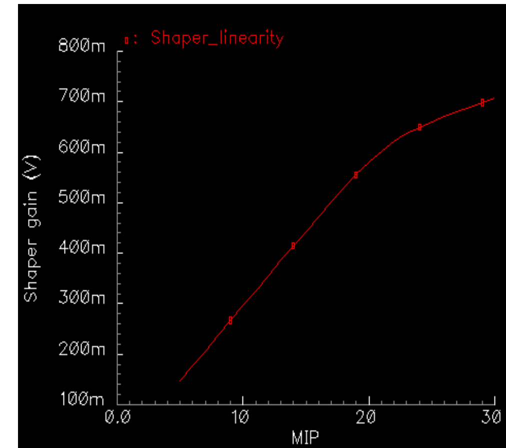


0.13 µm Chip Simulations

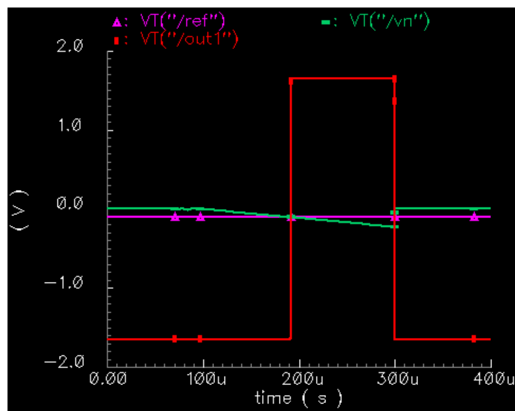
SIMULATIONS :



Preamps linearity



Shaper linearity



Sparsifier response

Possible issues: Transistors leaks

Two situations:

- Gate-channel due to tunnel effect (can affect noise performances)
- Through channel when transistor switched-off (only affects large digital designs)

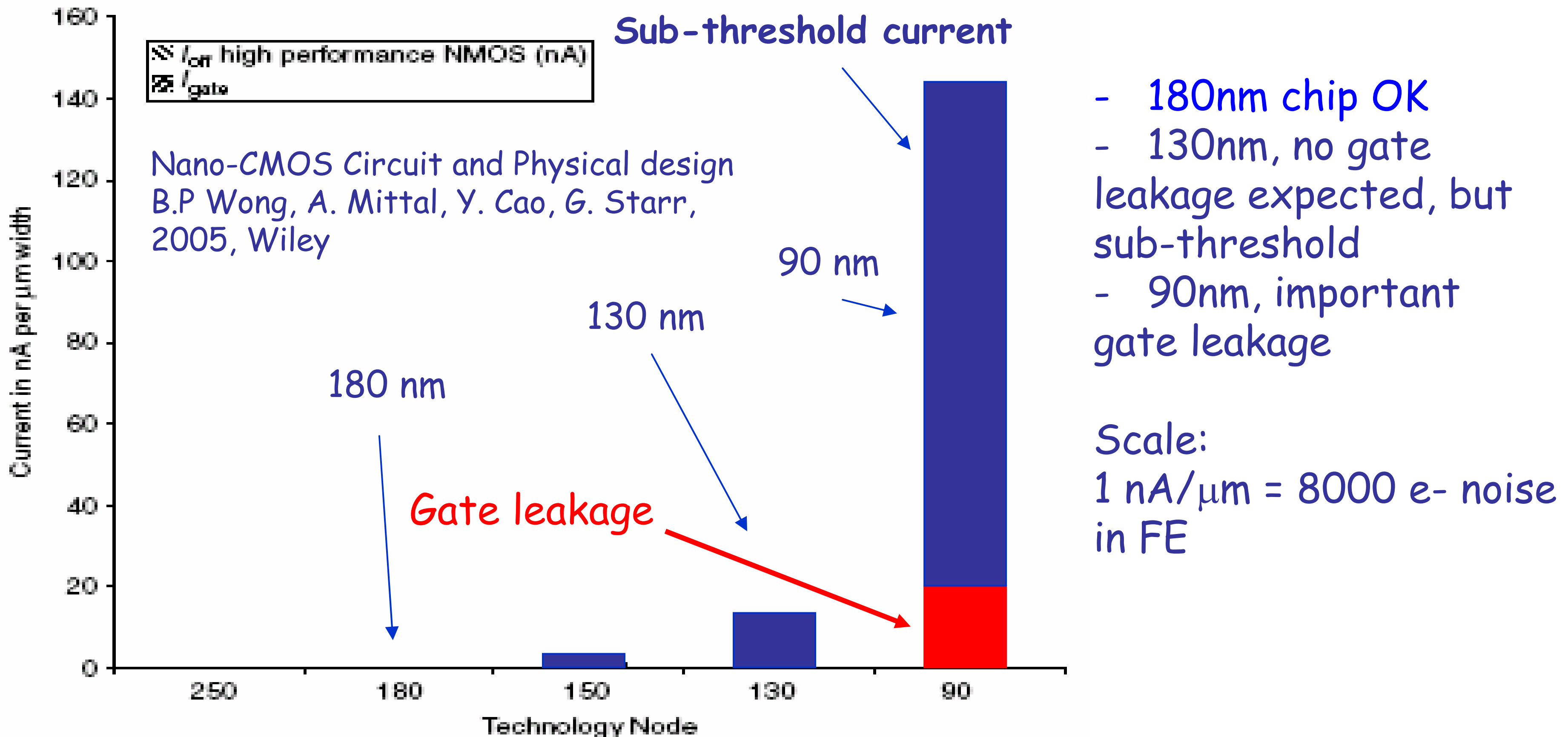
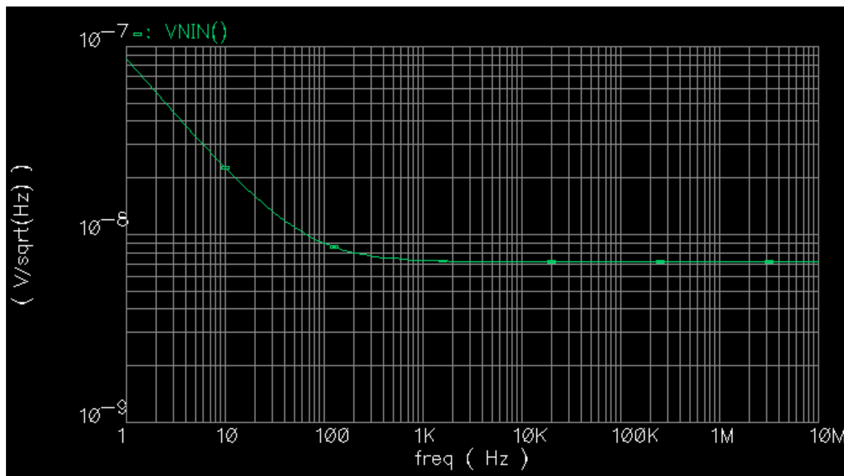


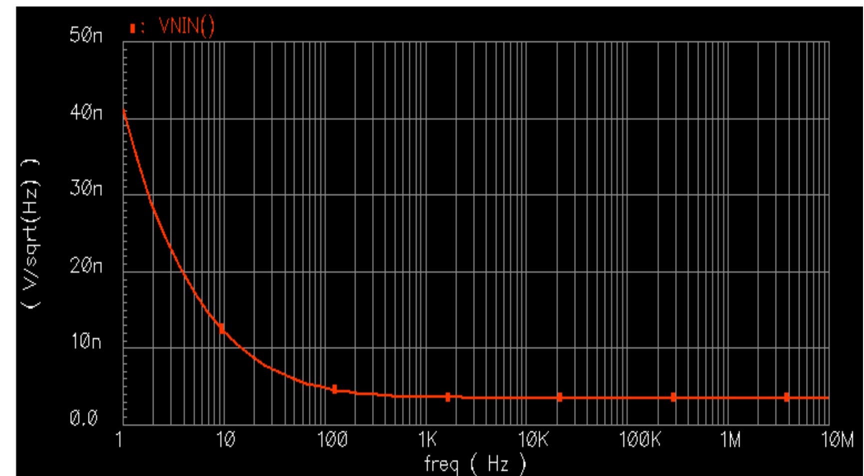
Figure 1.2 I_{gate} and subthreshold leakage versus technology.

Possible issues: noise: 130nm vs 180nm (simulation)

- **PMOS:**



130nm
W/L = 2mm/0.5u
Ids = 38.79u,Vgs=-190mV,Vds=-600mV
gm=815.245u,gms=354.118u
1MHz → 7.16nV/sqrt(Hz)
Thermal noise hand calculation = 3.68nV/sqrt(Hz)

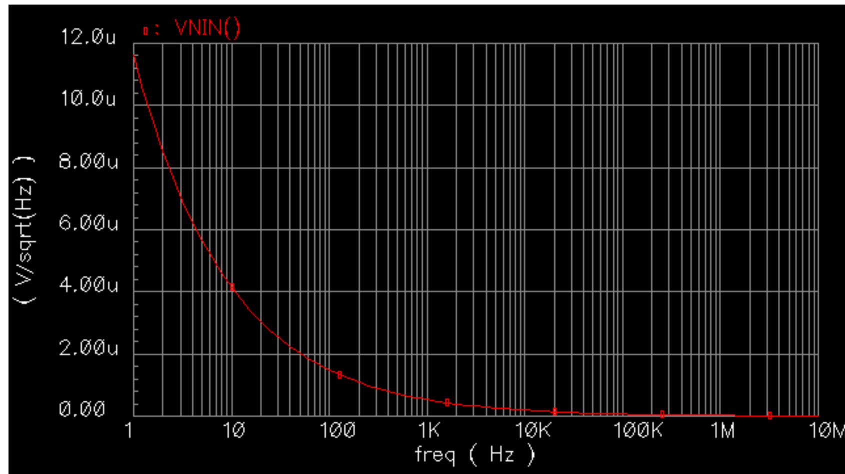


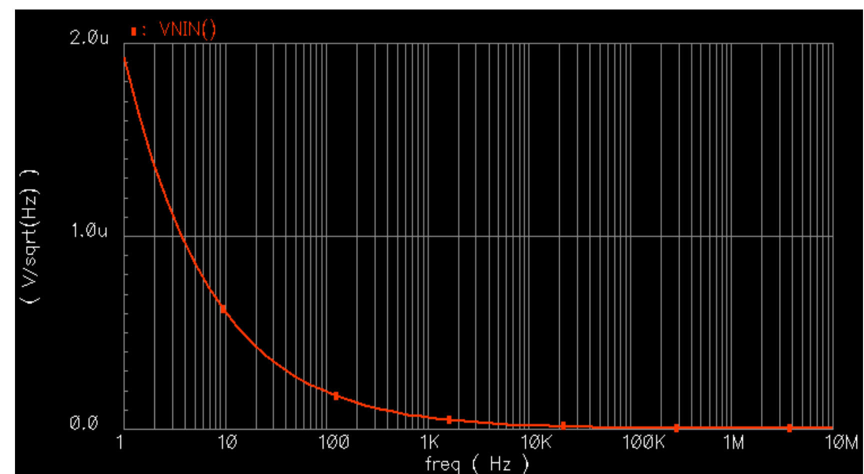
180nm

gm=944.4uS,gms=203.1uS
1MHz → 3.508nV/sqrt(Hz)
Thermal noise hand calculation = 3.42nV/sqrt(Hz)

Noise: 130nm vs 180nm (simulation)

NMOS :





130nm
W/L = 50u/0.5u
Ids=48.0505u,Vgs=260mV,Vds=1.2V
gm=772.031uS,gms=245.341uS,gds=6.3575uS
1MHz --> 24.65nV/sqrt(Hz)
100MHz --> 5nV/sqrt(Hz)
Thermal noise hand calculation = 3.78nV/sqrt(Hz)

180nm
W/L=50u/0.5u
Ids=47uA,Vgs=300mV,Vds=1.2V
gm=842.8uS,gms=141.2uS,gds=16.05uS
1MHz --> 4nV/sqrt(Hz)
10MHz --> 3.49nV/sqrt(Hz)
Thermal noise hand calculation = 3.62nV/sqrt(Hz)