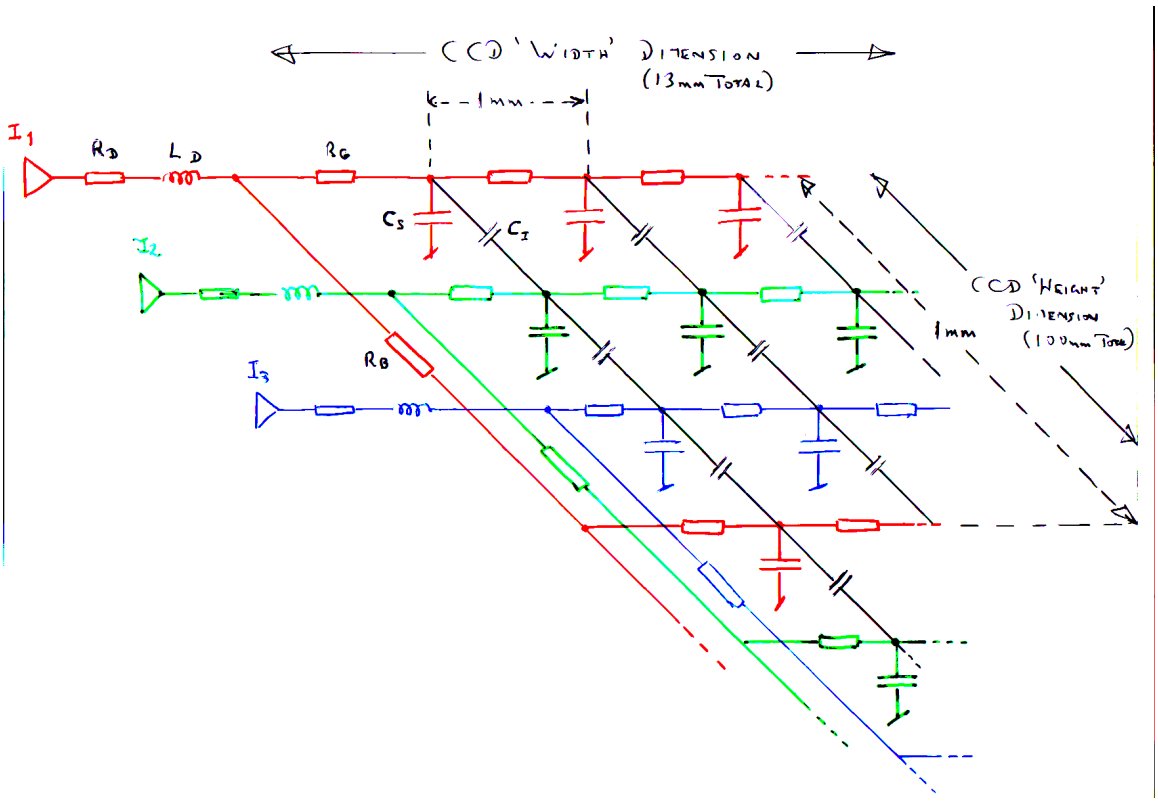
PSpice simulation of CCD array.

The determination of the maximum clocking speed for a given CCD, driver and interconnect is required for the development of the column parallel architecture.

The performance of a CCD has been modeled using an equivalent RC circuit with the PSpice software. This allows a good approximation of the voltage waveform at any of the gates within the CCD array to be obtained.

The example in this report is of a TESLA layer-1 CCD. In this case, there are eight CCD devices arranged in an octagonal barrel. Each CCD has dimensions of 100 mm by 13 mm. The CCD has a three phase architecture, i.e. three I clocks and the drives are connected at each of the four corners. The ground connection is assumed to be solid at the back of the CCD.

The CCD is modeled as 1300 pads of 1 mm by 1 mm as shown in the following figure:



The parameters for the model are as follows.

Rd: Resistance of the drivers assumed to be zero.
Ld: Inductance initially assumed to be zero.
Rb: Resistance/mm of on-CCD busline. In the first instance, this is assumed to be zero. Later simulations have this value set at a realistic level.

Rg: Resistance/mm "width" of I gates
Cs: Capacitance to substrate.
Ci: Inter-phase capacitance.

Determination of values

Rg: The gate resistance per mm "width" of CCD. Optimised polysilicon can have as low a resistance as 20 Ohms/sq. It may be possible to reduce this value to 1 Ohm/sq by stripping of dielectric in regions of say 3 um wide on each gate and depositing aluminium.

For the present use 20 Ohms/sq x 1000 um / 6.7 um /50 (50 of each phase running in parallel over 1mm in height of the CCD.)

60 Ohms for 1300 1mm x 1mm pads

Cs: Capacitance to substrate: Assuming that the buried channel and channel stop regions are depleted (as would be the case with a positive gate bias throughout the clock swing), a value of 1 nF per cm^2 has been suggested. A 1 mm by 1 mm pixel would have a total capacitance of 10 pF between the three phases. The value of Cs for a 1 mm by 1 mm pixel is 3.3 pF.

Ci: Inter-phase capacitance: With Marconi technology, the best inter-phase capacitance is 1pF/cm length. (One phase to both neighbours). For 1 mm by 1 mm pixel. Ci = 0.1pF x 50/2 = 2.5 pF

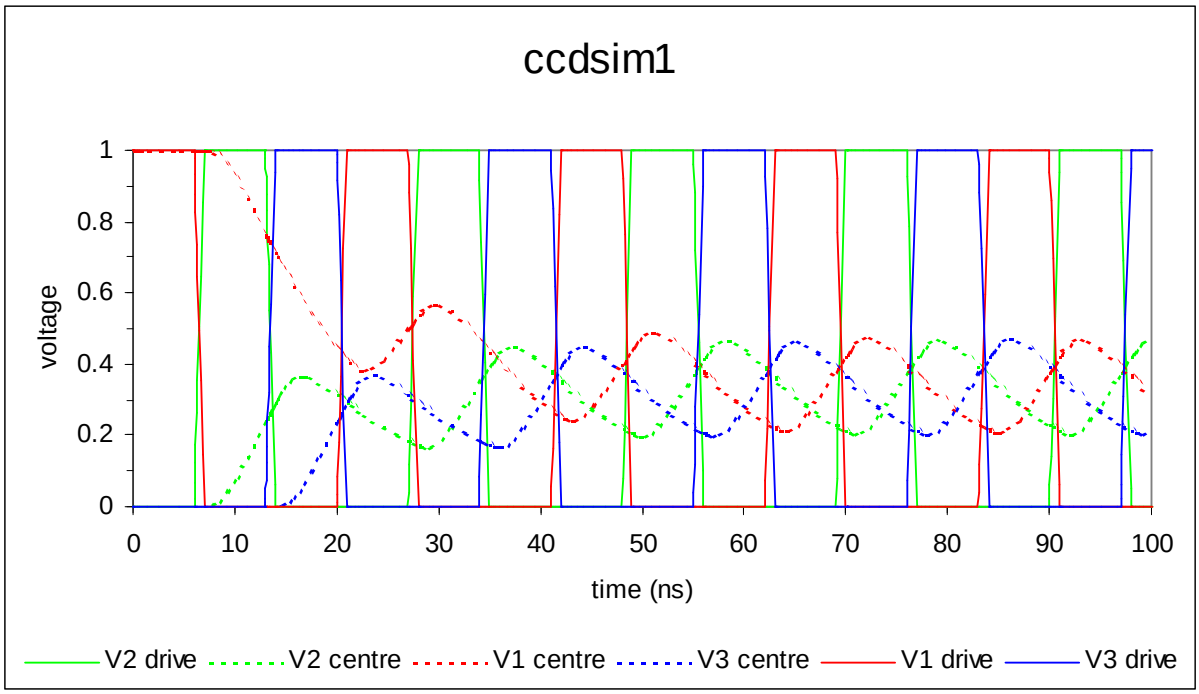
Simple 1-d model

In this model, the bus line resistance running "vertically" along the sides of the CCD is assumed to be zero. Thus, the voltage profile is not dependent upon the y (vertical) dimension but only upon the x (horizontal). The CCD can be modeled using just 13 elements each representing an area 1 mm by 100 mm of the CCD surface. The parameter values must be changed as each element represents 100 square mm of CCD surface.

Rg: The gate resistance is 60 Ohms/100 = 0.6 Ohms
Cs: The capacitace to substrate is 3.3pF x 100 = 330 pF
Ci: The inter-phase capacitance is 2.5pF x 100 = 250 pF

We are concerned with the rise time of a drive pulse in the centre element of the string. A piecewise linear waveform is used as the stimulus and is connected directly to the 1st and 13th elements. The waveform consists of a Square wave with a rise time of 1ns, a peak time of 6ns, a fall time of 1ns and a period of 20ns. (This equates to a clock speed of 50 MHz)

Results: CCDsim1.xls

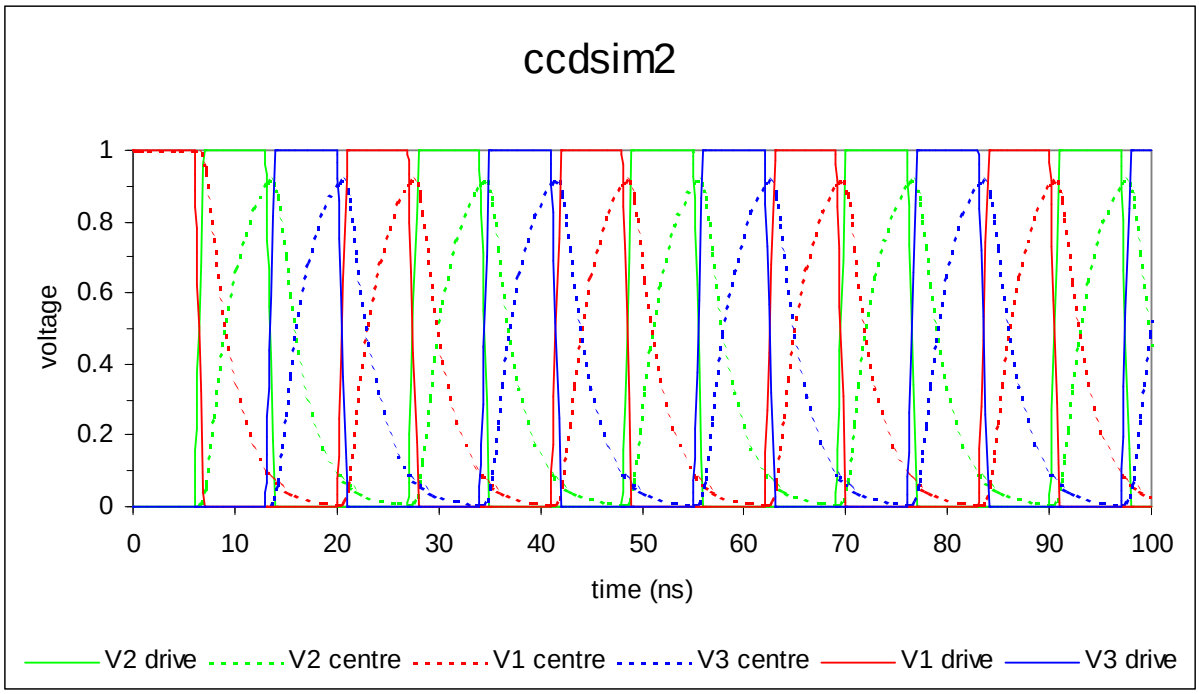


These results show that the CCD would not operate in the centre of the device at that particular frequency as the crossovers between the individual phases are not sufficiently defined.

If the gate resistance can be improved (say by stripping of dielectric in regions of say 3 um wide on each gate and depositing aluminium) so that the resistance for the 1mm pixel is 12 Ohms instead of 60 Ohms, the voltage waveform in the centre of the 1 dimensional array is more defined as shown below.

For this simulation the value of Rg is changed from 0.6 Ohms to 0.12 Ohms.

Results: CCDsim2.xls



In this case, the voltage crossovers between the individual phases is sufficiently defined for the CCD to operate properly.

Realistic value of Rb.

So far, we have only considered the case where Rb is zero. Thus, the 13 mm by 100 mm pixel array has been modeled using a 1 dimensional equivalent circuit. If a realistic value of Rb is introduced, the model must be changed. The CCD array is divided into ten sections each of 13 mm width and 10 mm height. Each section is modeled as a 1 dimensional array, but is linked to the adjacent section both at the bus lines at the edges and at in the centre through the inter phase capacitance. The voltage signal is fed at each corner.

The parameters used in the simulation need to be changed as each element within the model refers to a 1 mm by 100 mm slither of CCD rather than a 1 mm by 100 mm slither as in the previous two examples.

Rg: 0.8 Ohms. This is based upon a further improvement of the gate resistance to 8 Ohms for a 1 mm by 1 mm pixel. In our slither, ten such gate resistances are running in parallel.

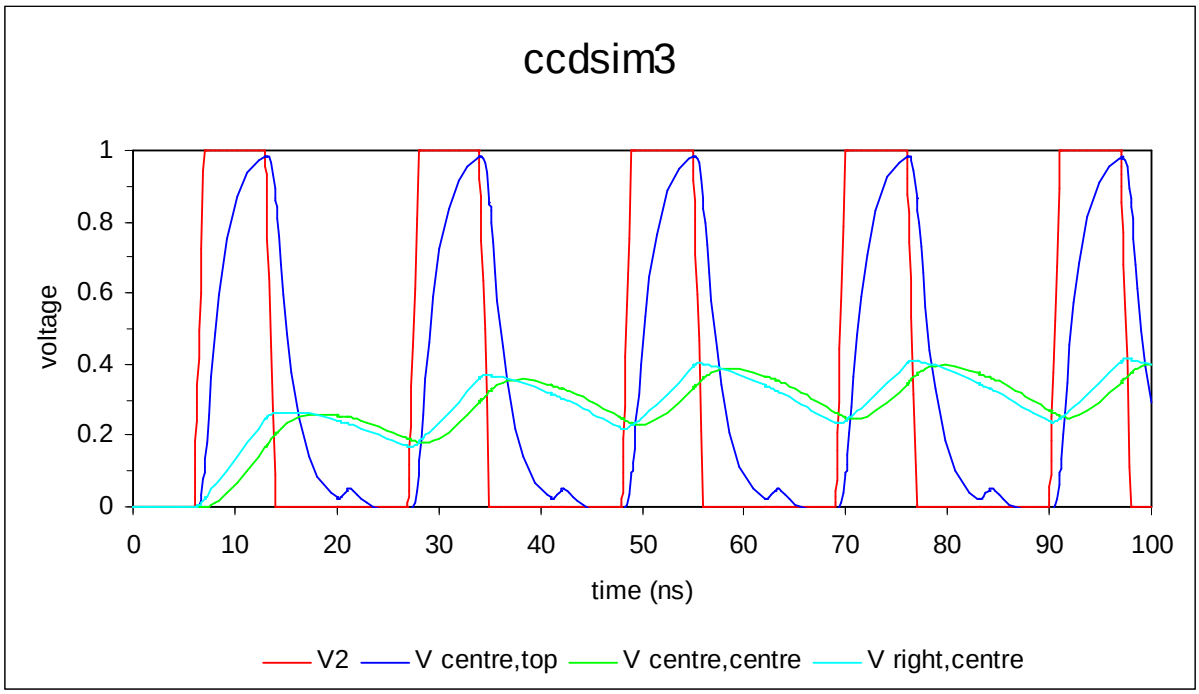
Cs: 33 pF: As in the previous example except that a 1 mm by 10 mm slither is being modeled.

Ci: 25 pF: As in the previous example except that a 1 mm by 10 mm slither is being modeled.

Rb: The bus line resistance. If the bus lines consist of a 100 um wide aluminium track, 1 um thick, the resistance along a 10 mm length would by 2.7 Ohms at room temperature.

The performance of the CCD under these conditions is shown below. Four cases are shown, referring to the right-top, centre-top, right-centre and centre-centre points on the CCD.

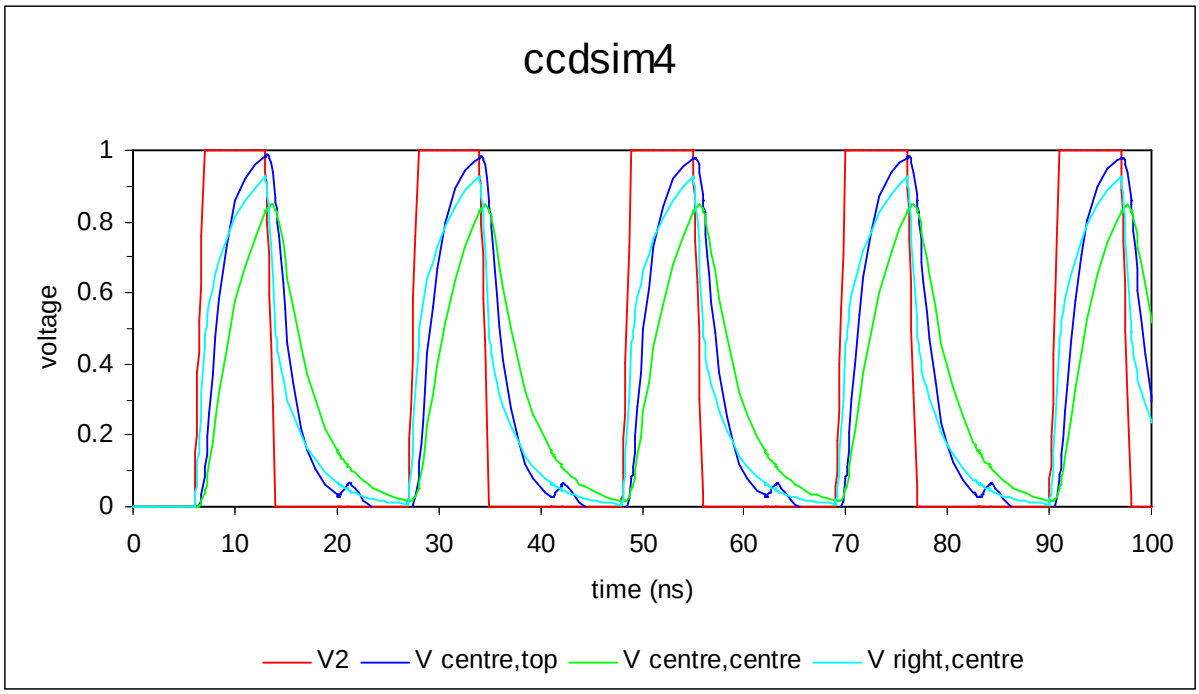
Results: CCDsim3.xls



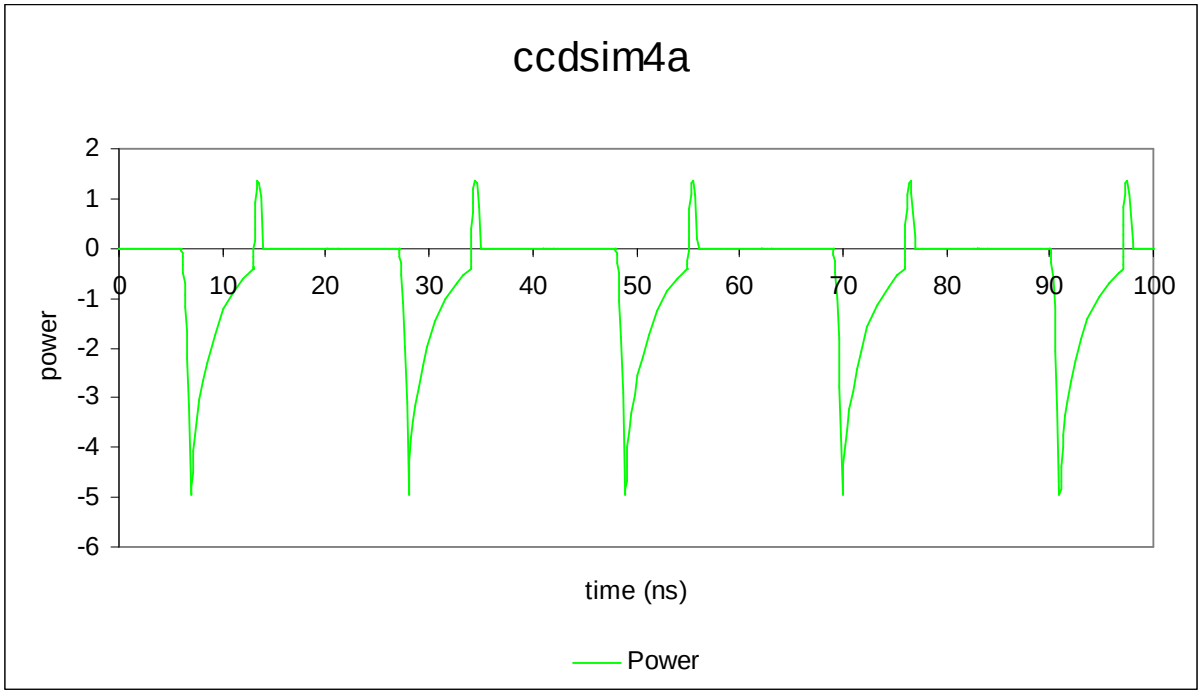
It is seen from these results that the voltage waveforms at the right-centre and centre-centre points are not distinct enough for the correct operation of the CCD.

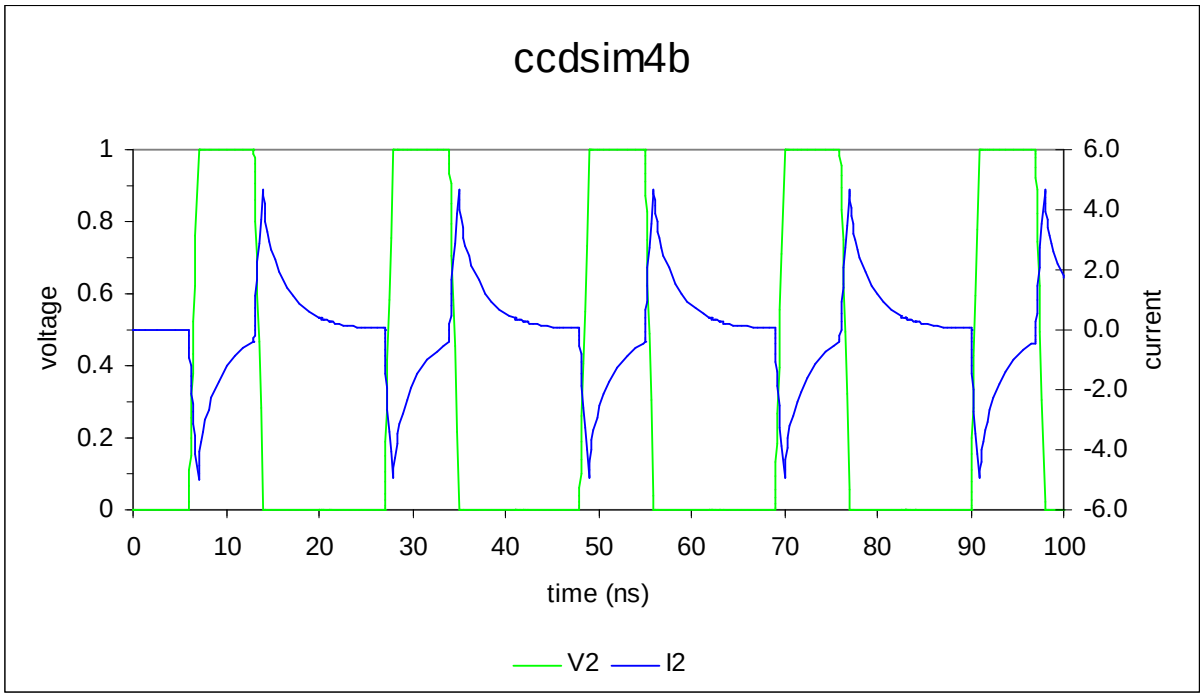
By increasing the thickness of the bus line from 1 um to 10 um, the value of Rb may be reduced to 0.27 Ohms at room temperature. In which case, the voltage waveform at the various points in the CCD are as shown below.

Results: CCDsim4.xls



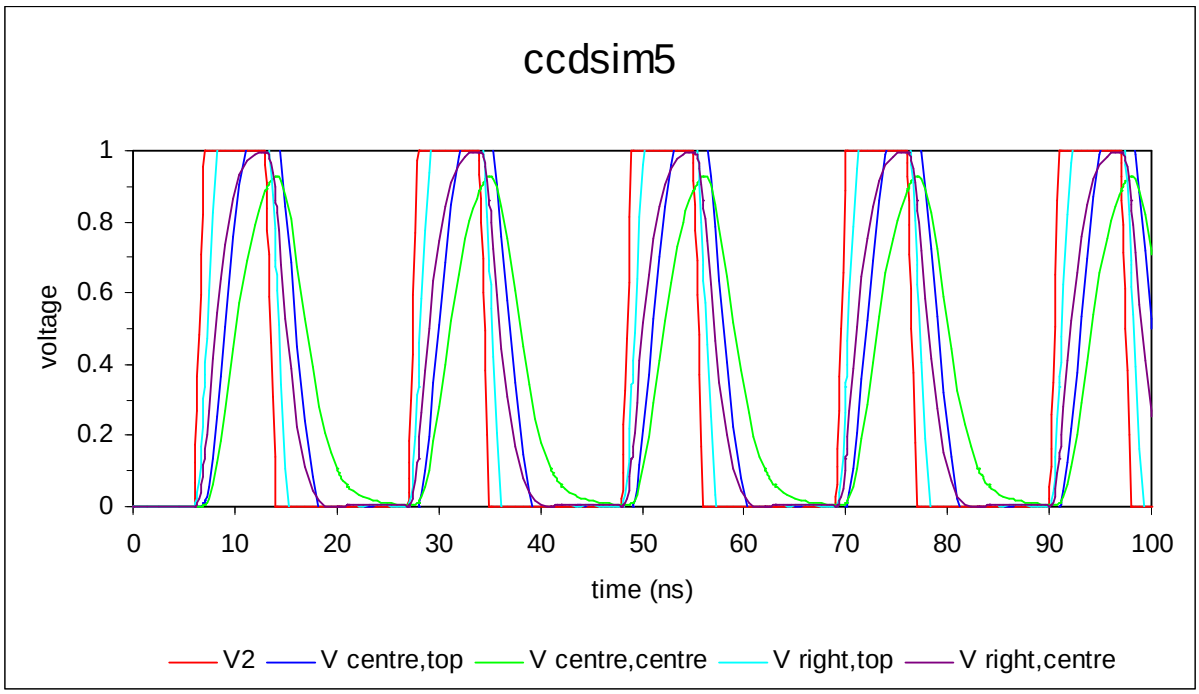
The current drawn by the supply to one of the phases is shown and the power delivered by that one supply is shown in the following graphs.

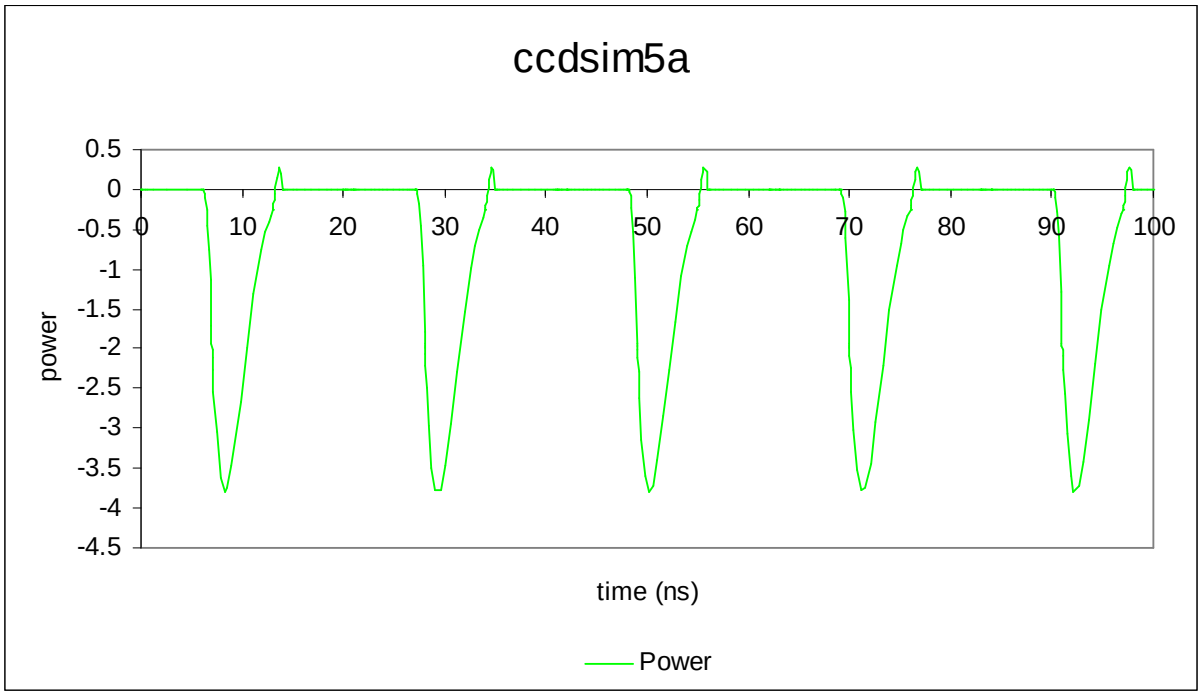


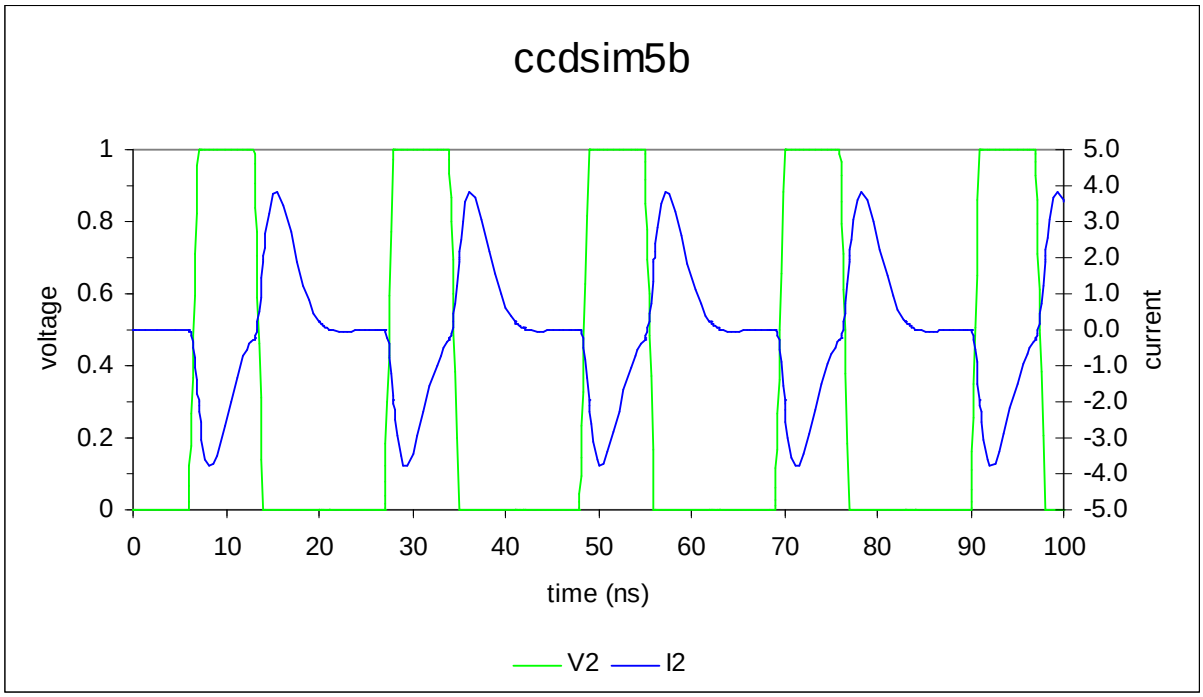


In the next example, the effect of adding some line inductance to the supplies to the CCD is modeled. A 200 pH inductance is placed in each phase between the voltage source and the feed to the corners of the CCD. The effect of the inductance upon the voltage waveform in each point of the CCD and upon the current drawn is shown below.

Results: CCDsim5.xls




ccdsim5a
0.5
0
-0.5
-1
-1.5
-2
-2.5
-3
-3.5
-4
-4.5
power
0
10
20
30
40
50
60
70
80
90
100
time (ns)
Power


ccdsim5b
1
0.8
0.6
0.4
0.2
0
voltage
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
-2.0
-3.0
-4.0
-5.0
current
0
10
20
30
40
50
60
70
80
90
100
time (ns)
V2
I2

Skin effect

The conductivity of the various lines and gates is limited by the skin effect. This can be significant at the frequencies of interest. The skin effect is dependent upon the frequency, relative permeability and the conductivity of the medium. The skin depth can be taken as the effective practical thickness of any conductor carrying ac power.

The skin depth for various metals under various conditions is given below.

Frequency (MHz)	*Temperature (ºC)*	*Skin Depth (um)*			
		Al	Cu	Ag	Au
50	0	11	8.8	8.6	11.2
50	-100	8	6.6	6.7	7.9
100	0	7.8	6.3	6.1	7.2
100	-100	5.7	4.7	4.7	5.6

In the case of the Al bus lines, the use of 10 um thick appears to be exceeding the skin depth for Aluminium at -100 ºC. However, the resistivity at such low temperatures is less by a greater amount, so the value of 0.27 Ohms for Rb is conservative. (In fact, the skin depth varies inversely with square root of the resistivity).

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