CCD-Based Vertex Detector (Past and Future)

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Workshop at Bad Honnef
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For the SLD and LCFI (Linear Collider Flavour ID) collaborations.

URL:

- Operating principles

- The SLD vertex detector

- R&D towards a future LC detector

  - Mechanical design
  - Readout electronics
  - [Radiation tolerance]

- Conclusions

  - Comparison with other vertex detector technologies
  - [Relevance to other fields]

Charge Coupled Semiconductor Devices

By W. S. BOYLE and G. E. SMITH

In this paper we describe a new semiconductor device concept. Basically, it consists of storing charge in potential wells created at the surface of a semiconductor and moving the charge (representing information) over the surface by moving the potential minima. We discuss schemes for creating, transferring, and detecting the presence or absence of the charge.

In particular, we consider minority carrier charge storage at the Si-SiO₂ interface of a MOS capacitor. This charge may be transferred to a closely adjacent capacitor on the same substrate by appropriate manipulation of electrode potentials. Examples of possible applications are as a shift register, as an imaging device, as a display device, and in performing logic.

A new semiconductor device concept has been devised which shows promise of having wide application. The essence of the scheme is to

Pixel detectors for particle tracking:

unambiguous space points
tolerant of high track density and background
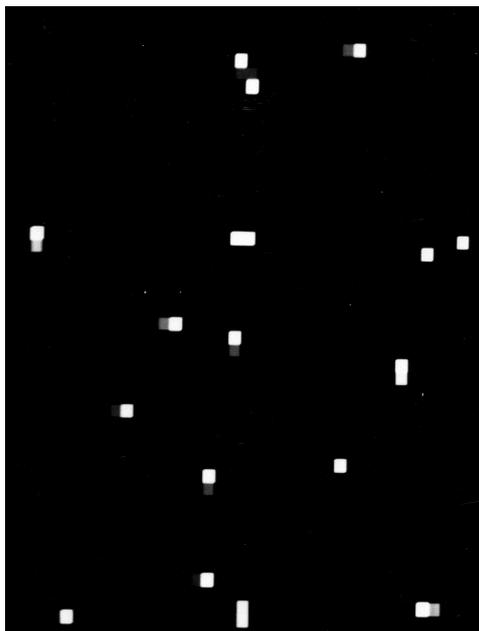
t6 – 1980
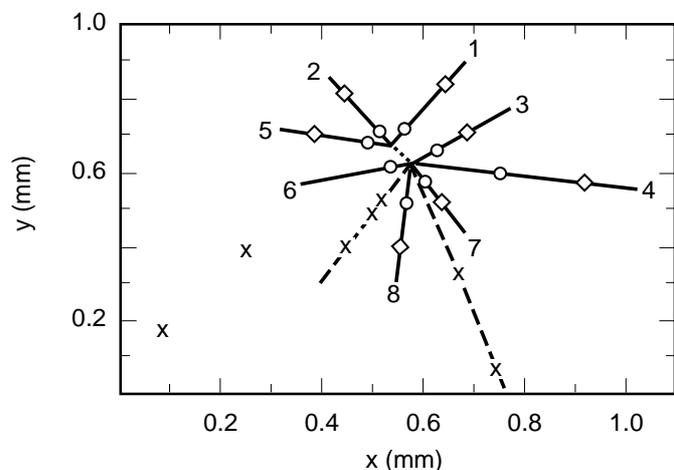
NA32 1985

e^+e^- linear collider will inevitably have high background at small radii

Run 33544,   EVENT   6476
27-APR-1996 06:05
Source: Run Data   Pol: R
Trigger: Energy CDC Hadron
Beam Crossing   1215252296
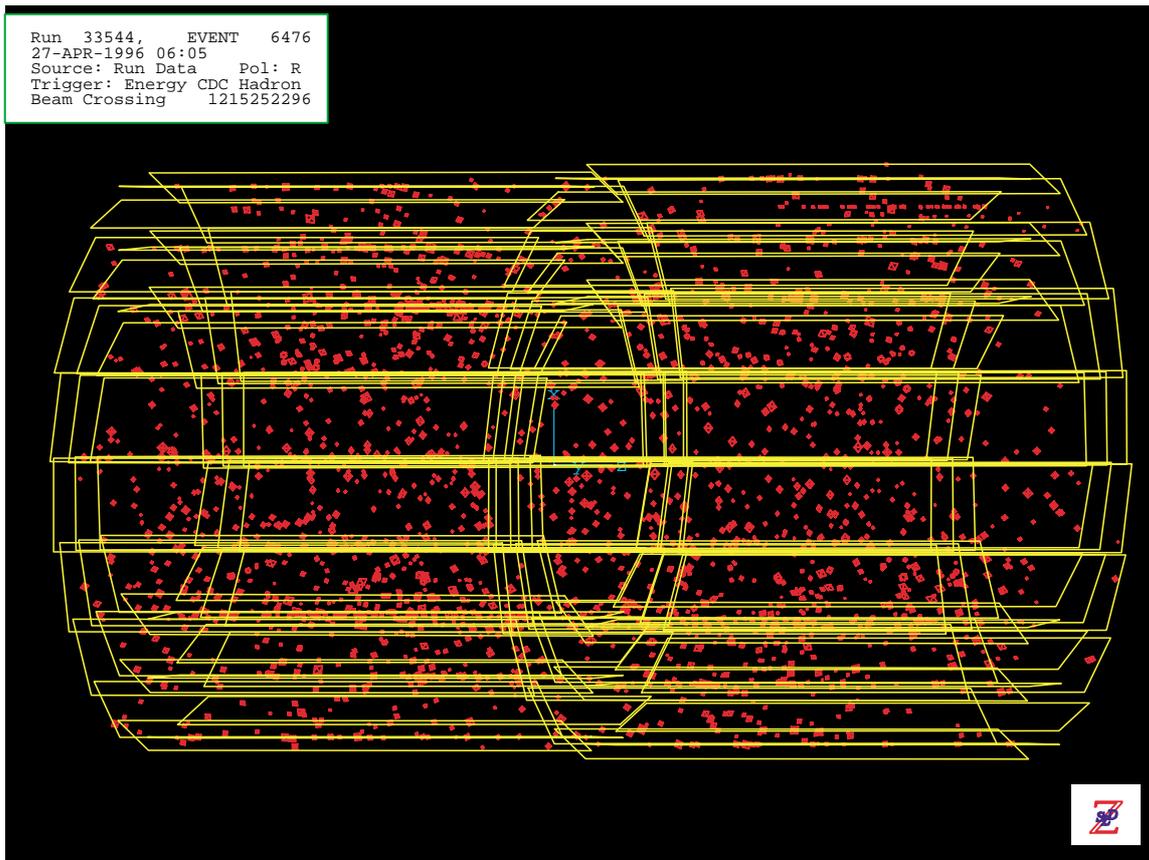
A pixel detector is extremely tolerant of this background

Run 33544,   EVENT   6476
27-APR-1996 06:05
Source: Run Data   Pol: R
Trigger: Energy CDC Hadron
Beam Crossing   1215252296

Track Properties
0.167 < P <   50.000 GeV

y

x

centimeters
0   4.000   8.000

CCD operating principles

(a) Potential well containing charge

(b) Well just created

(c)

(d) Well collapsing

(e)

(f)
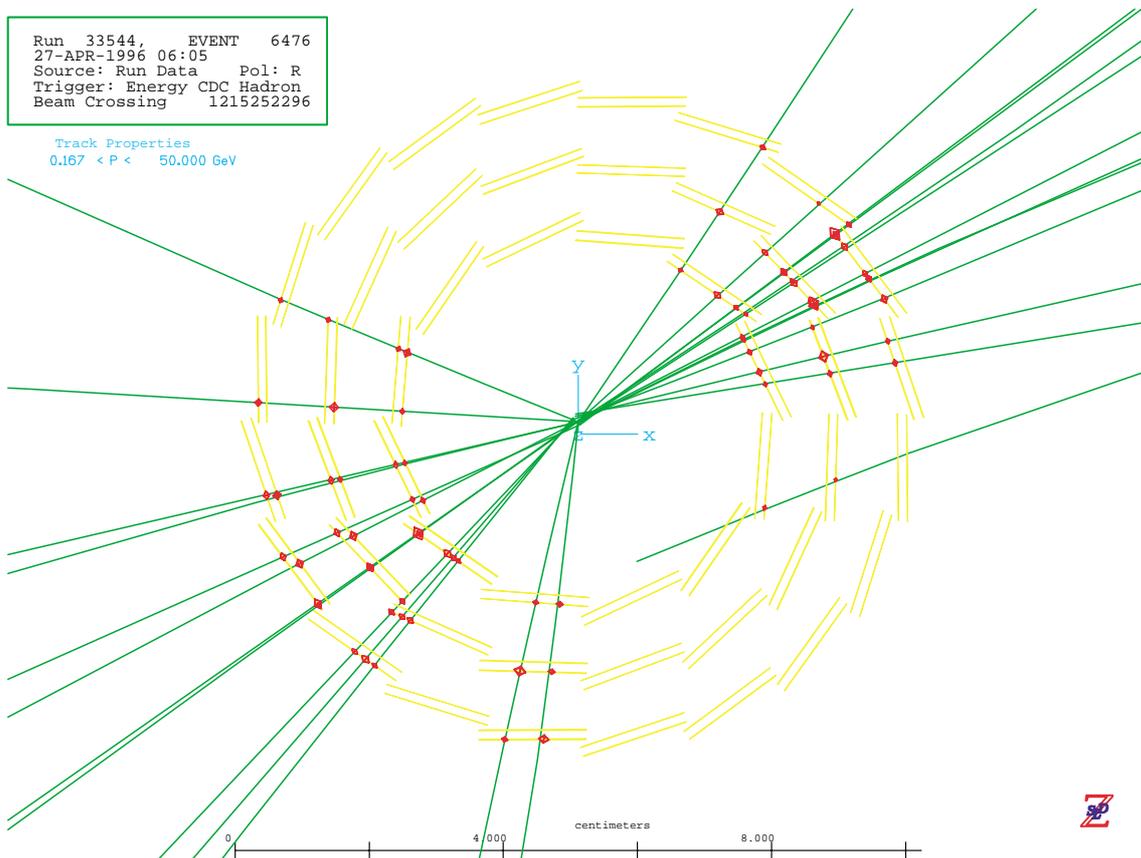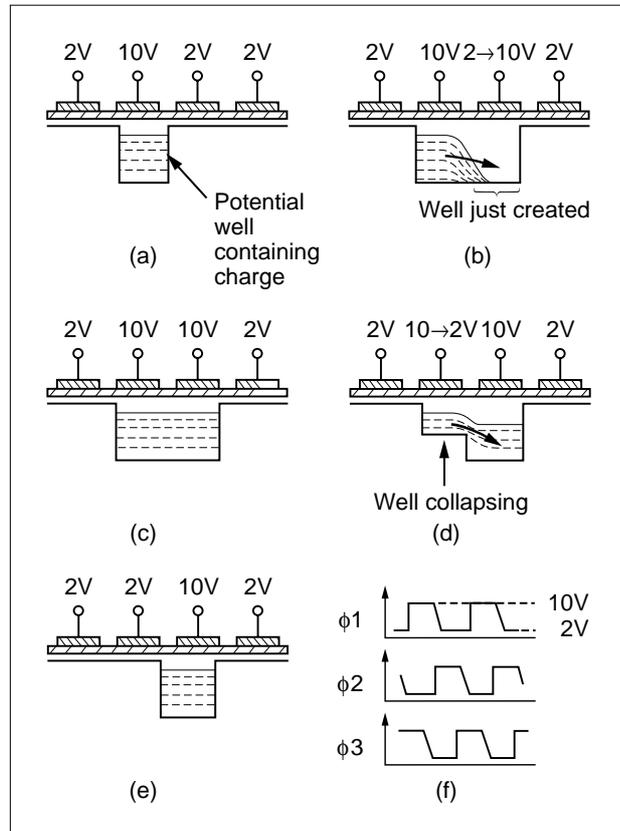
Simplest particle detector architecture

I φ gates
Buried n channel (~1μm)
p(~20μm)
p+
1 pixel (20x20x20 μm³)
p+ channel stop
polysilicon gates
V$_{OD}$
OG
C$_n$
R φ gates
Remote preamp
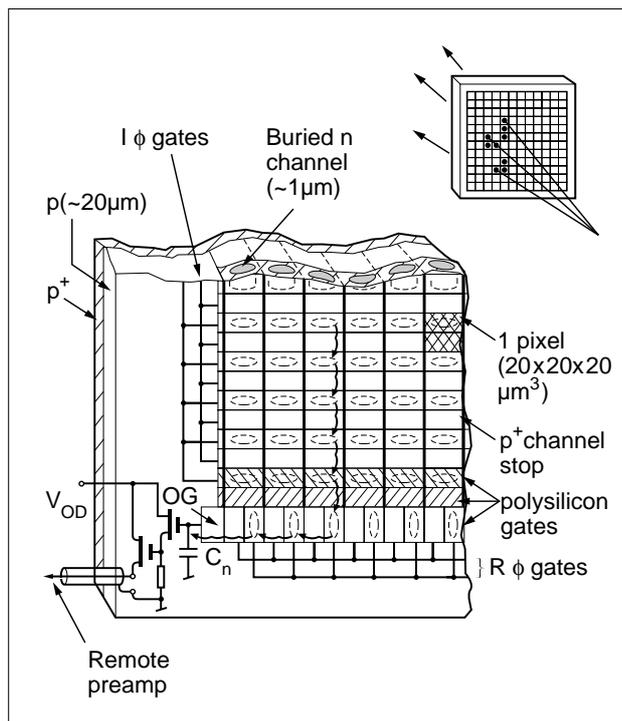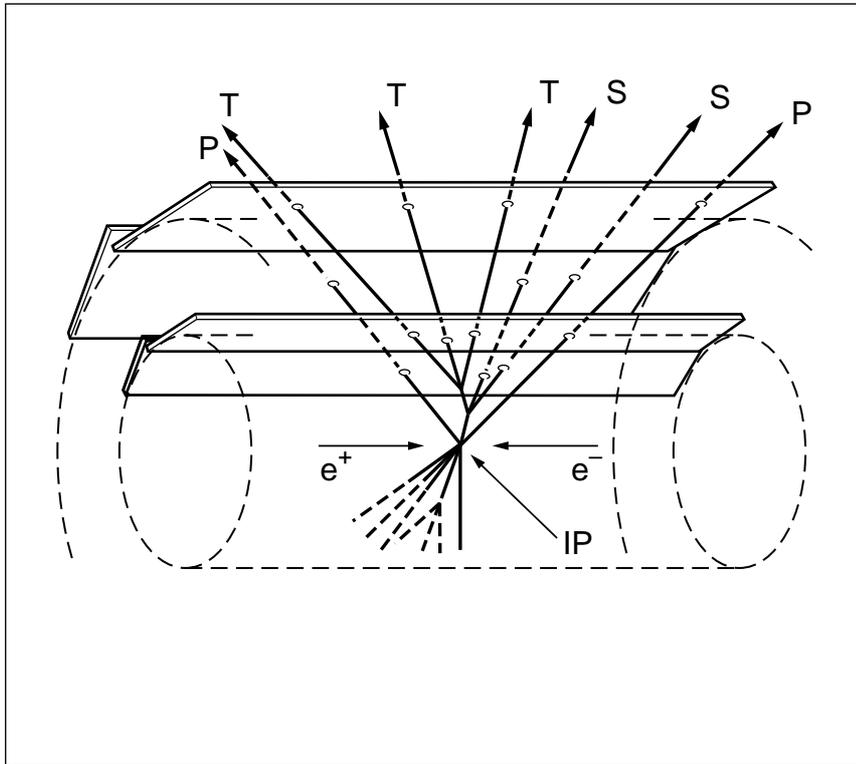
- Due to effects of

    - multiple scattering

    - photon conversions

   - loss of precision for oblique angles

    we need thinnest possible layers for a collider vertex
    detector

- Here the CCD technology is (so far) unsurpassed

Principles of signal charge collection for min-I particles
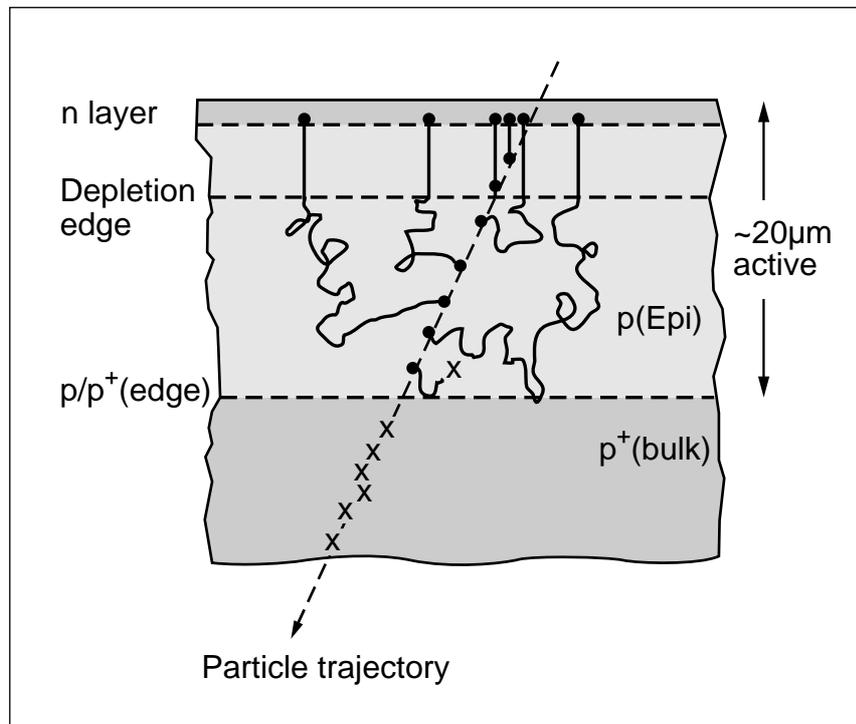
- Highly doped p^+ bulk : impurity gettering

- Signals from well-defined thickness of silicon (epitaxial layer) by diffusion and drift

- 80 e-h pairs/μm
    - ~ 1600 e^- in 3-6 pixel cluster

- Efficiency $\geq$ 99.8% and spatial precision ~ 3.5 μm if read with ~ 50 e^- rms noise

Look in a little detail at the charge-generation process

- 3.2 M-shell plasmons per μm (17 eV)

- 0.6 L-shell ionization per μm (120 eV)

- 10^{-2} K-shell ionization per μm (1.5 keV)

- $\Rightarrow$ ~ 4 primary collisions per μm with widely fluctuating energy loss

- final thermalization yields one e-h pair per 3.6 eV deposited (approx)

390 eV

37 eV
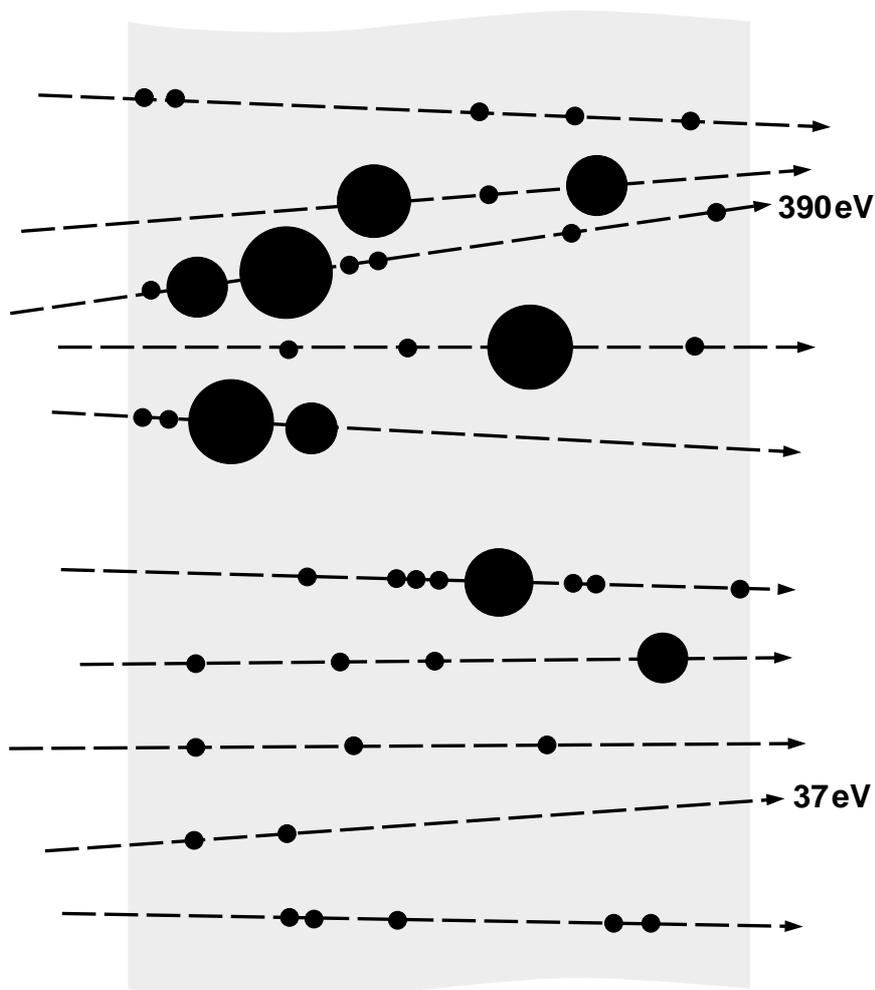
Implication: need low threshold for efficient min-I detection
from a thin detector

(a)

1.0μm

Probability of energy loss E

E/E_p

(b)

10μm

Probability of energy loss E

E/E_p

(c)

150μm

Probability of energy loss E

E/E_p

(d)

300μm

Probability of energy loss E

E/E_p
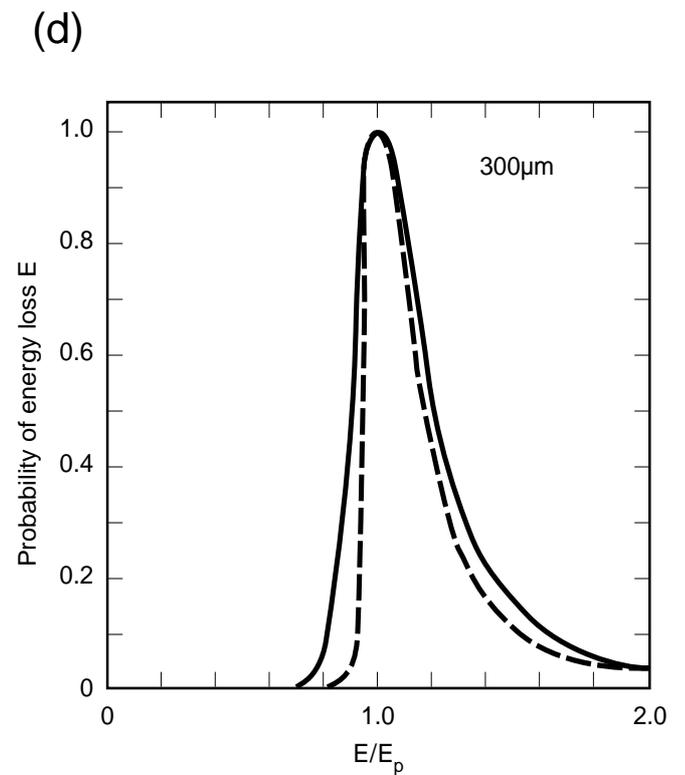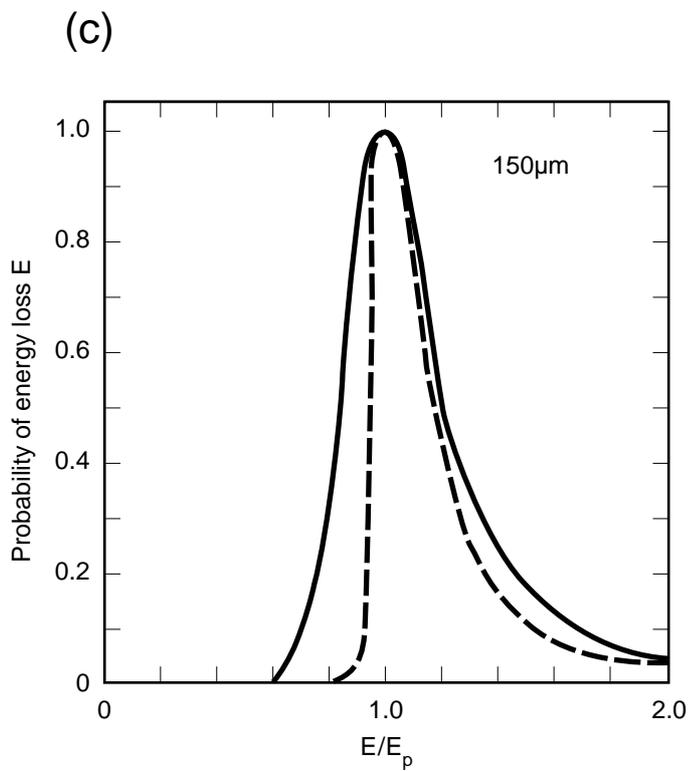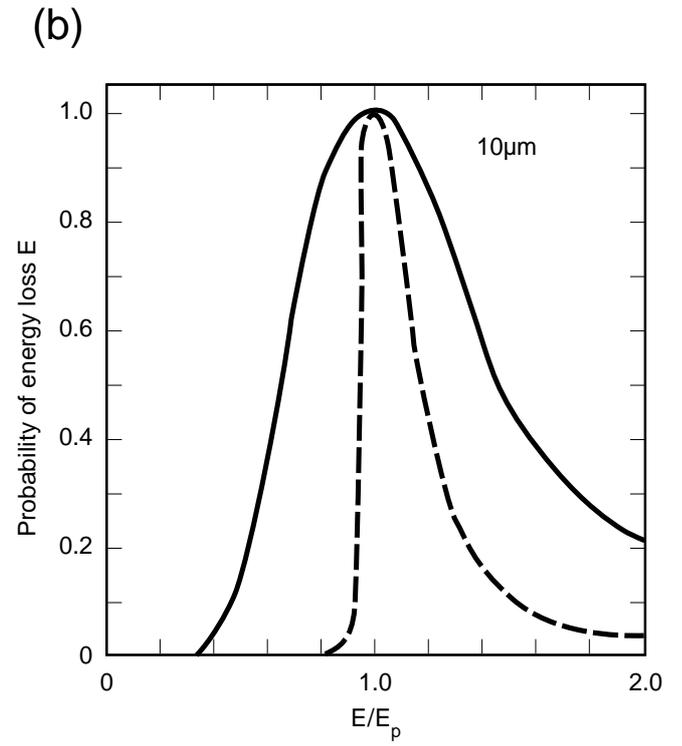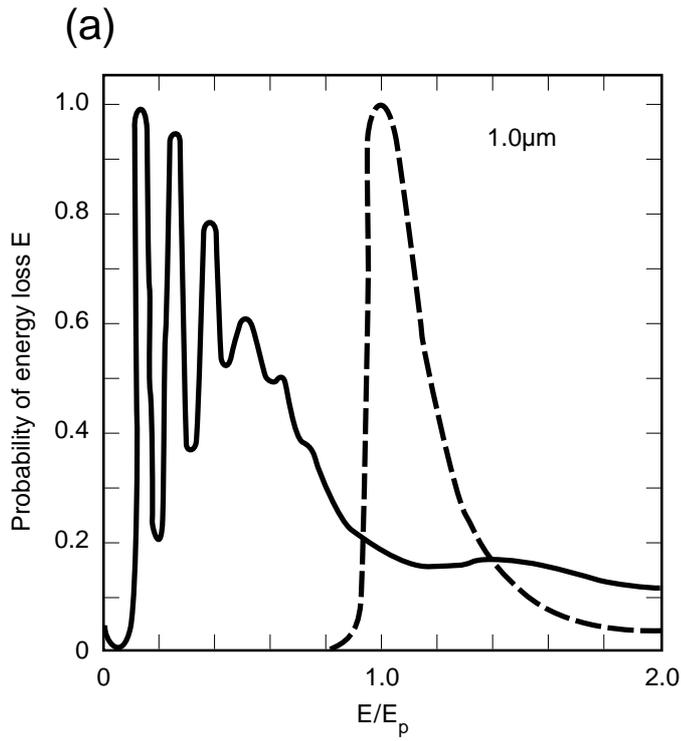
The SLD Vertex Detector

VXD2 Proc 26th Int Conf on HEP, Dallas TX (1992)
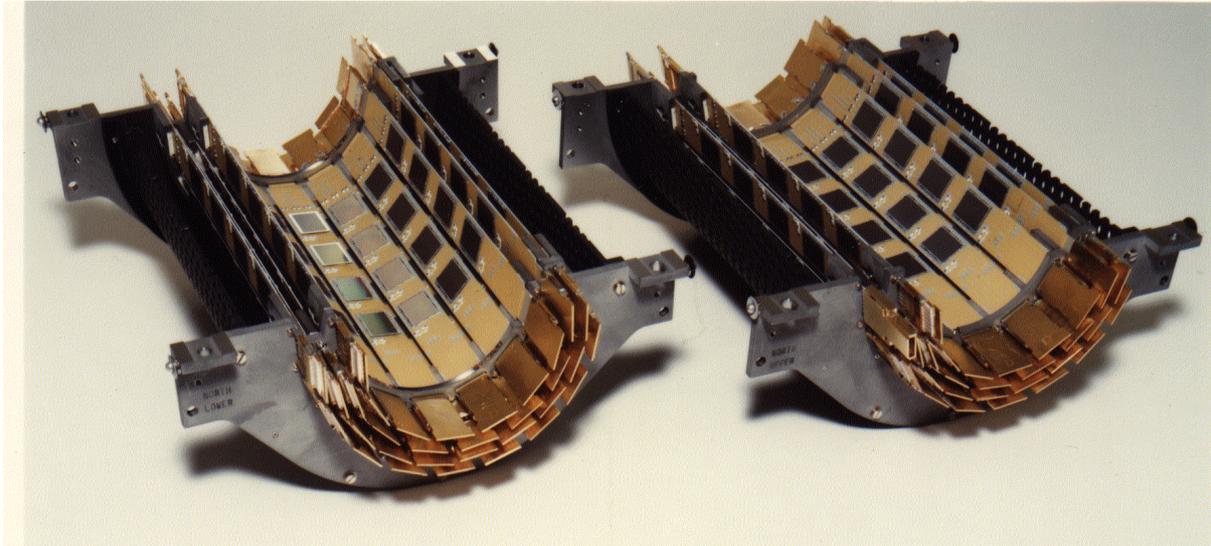
VXD3 NIM A400 (1997) 287
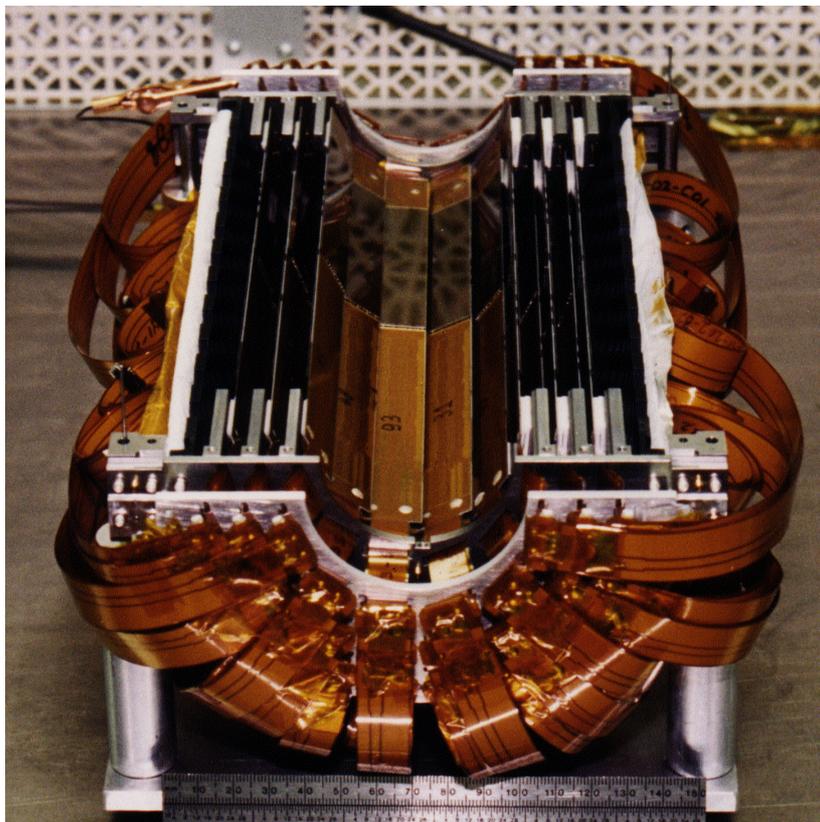
SLD Vertex Detector Properties

Detector	VXD2	VXD3
Installed	January 1992	January 1996
CCDs	480	96
CCD active area	9×13 mm^2	16×80 mm^2
Pixel size	22 μm square	20 μm square
Number of pixels	120×10^6	307×10^6
Effective number of layers	2	3
Average layer radii R_{max} / R_{min}	32, 40 mm 1.25	28, 38, 48 mm 1.71
CCD thickness	200 μm	$180 \pm 20 \mu$m
Average layer thickness	1.1% X_0	0.40% X_0
$\left(\cos\theta_p \right)_{max}$ (2-hit)	0.75	0.90
Impact parameter resolution		
$\sigma_{r\phi}$	$11 \oplus 70 / p\sin^{3/2}\theta$	$9 \oplus 33 / p\sin^{3/2}\theta$
σ_{rz}	$38 \oplus 70 / p\sin^{3/2}\theta$	$17 \oplus 33 / p\sin^{3/2}\theta$

Reliability after three years operation:

VXD2

- 2 micro-connector fingers (out of 1380) lost contact due to an 'incident' on installation. A few others gave intermittent poor contact (increased noise)

- No degradation of any CCDs or inaccessible and completely burned-in inner electronics

VXD3

- Inner layer suffered radiation damage due to non-standard SLC running prior to detector commissioning. Fixed by reducing operating temperature from 200 to 170 K

- Commercial micro-connectors now available. One hundred percent reliable

- No degradation of any CCDs

- Inner electronics was accessible, less completely burned-in, and subject to occasional minor repairs

R&D towards a future LC vertex detector

Status report from the Linear Collider Flavour ID collaboration (LCFI)

- Design concept stable since Snowmass '96

    - concentric cylinders
    - maximum polar angle coverage
    - 5 layers for redundant standalone tracking

- Current status of the design concept

    - 4 Tesla solenoid
    - R_{bp} in range 10 to 14 mm
    - L1 active length 100 mm
    - 3-hit coverage including L1 to

 $$\cos\theta \geq 0.955$$

**Suggested layout of Vertex Detector for future e⁺ e⁻ Linear Collider** *(Updated October 1999)*

Scale:
Barrel: 1 L = 100mm
         R = 12mm

Cos θ = 0.9

Ladders

Barrel 1
L = 100mm

Barrel 2 - 5
L = 250mm

Gasket seal

CCDs (fitted to inner surfaces of Ladders)

Stripline

Beam-Pipe

Foam Cryostat and Faraday Cage

Chris Damerell
Rutherford Appleton Laboratory
October 1999
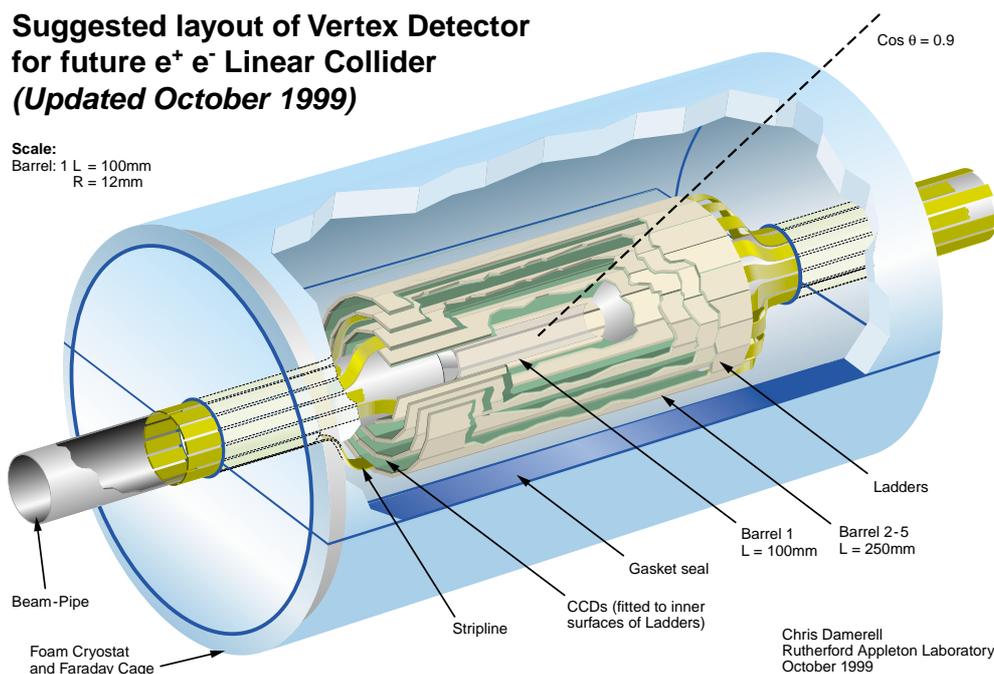
- **Layer thickness**

    - official goal 0.12% X_0

    - may reduce to $\leq$ 0.06% X_0

    - ideas for a similarly thin inner beam-pipe

- **Fast readout**

    - conventional clocking at 50 MHz will suffice for NLC

    - TESLA bunch structure is more challenging
        $\rightarrow$ column-parallel CCD

    - this development resonates with requirements in several other areas of science

- **Radiation resistance**

    - Tooling up for R&D

- **Technology choice**

    - Physics goals:

        - high efficiency/purity for charm jet ID

        - measurement of vertex charge (for separating b from $\bar{b}$ and c from $\bar{c}$)

        - measurement of charge dipole (for separating b from $\bar{b}$ in jets with neutral Bs)

$$\delta_{ch} = \frac{Q_D - Q_B}{|Q_D - Q_B|} \cdot \delta$$

Charge Dipole δ_{ch} (cm)

- Data
- MC
- b quark
- b-bar quark

Q_B (-ve or 0)

δ D

IP

$\bar{B}^0$

Q_D (+ve or 0)

ZVTOP/NN charm tagging performance, $\cos\theta < 0.9$

c-tagging purity (only b background)

- ● mass tag, 2.0cm APS
- ○ NN tag, 2.0cm APS
- ■ mass tag, 2.0cm CCD
- □ NN tag, 2.0cm CCD
- ▲ mass tag, 1.5cm CCD
- △ NN tag, 1.5cm CCD
- ▼ mass tag, 1.0cm CCD
- ◇ NN tag, 1.0cm CCD
- ○ mass tag, 1.0cm CCD (int)
- ✛ NN tag, 1.0cm CCD (int)

c-tagging efficiency

c-tag performance
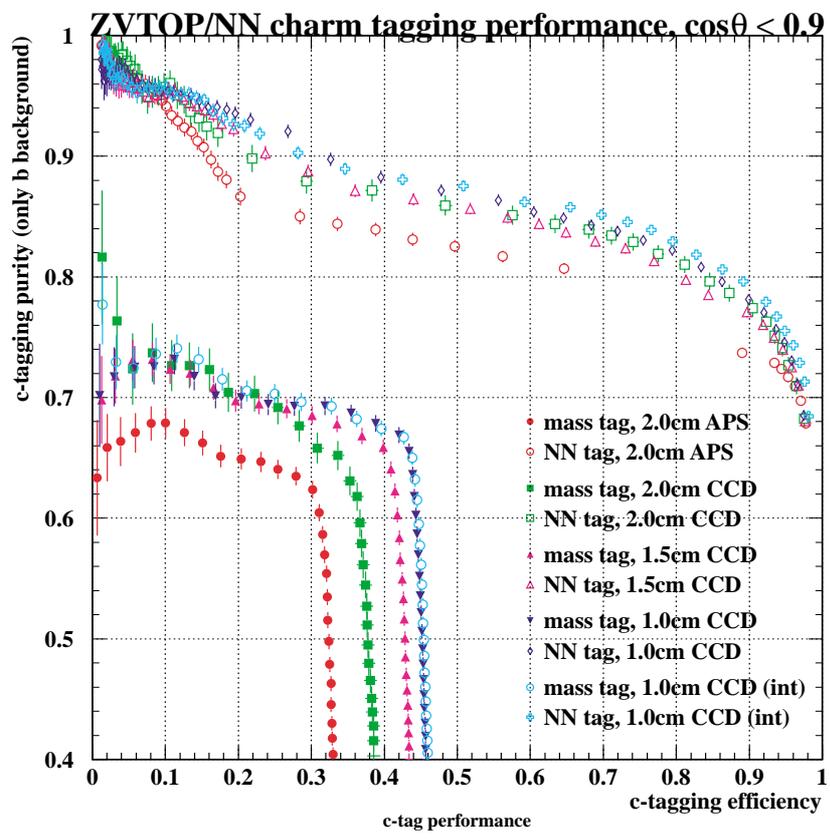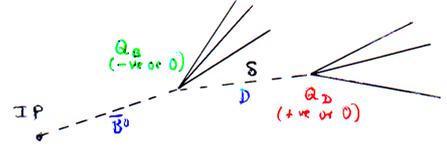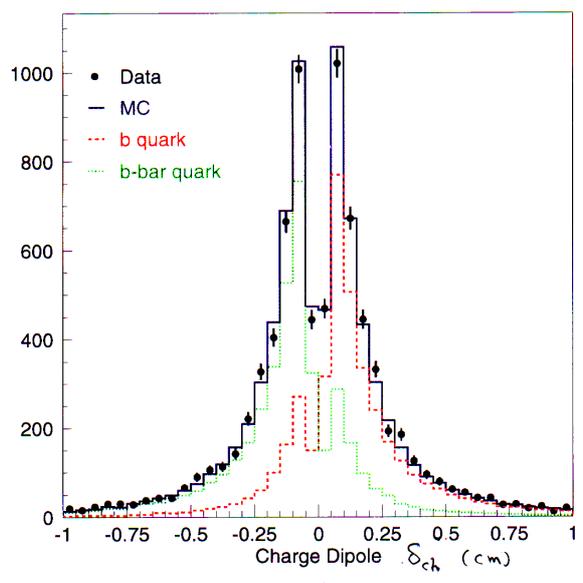
Low-mass detector

- Our official goal is 0.12% X_0 per layer

  (30 μm silicon bonded to 250 μm beryllium substrate in form of omega or vee beam)

- Unsupported-silicon option (under tension) could reduce this by a factor two, to 0.06% X_0, assuming 60 μm die thickness

- Assisted by the strong technology evolving for paper-thin packages (PTP)

- R&D programme consists of

  - tests with unprocessed silicon

  - tests with thinned CCDs

- Supports will consist of annulus block/ladder block assemblies as used in SLD, with an additional tensioning spring

- If successful, this approach will put pressure to reduce beam-pipe thickness to 0.25 mm (0.07% X_0) or lower. This may be feasible if VXD support shell is used for strain relief, particularly important during installation/removal of inner detector assembly

Fast Readout

- Column-parallel readout with a single row of staggered bump bonds on 60 μm pitch follows standard industrial practices (unlike large area bump bonding)

- Minimising electronics suggests a no-reset output with resistive load

- Feasible clocking rate depends on many parameters:

  - clock voltages (1-3 V)

  - I gate capacitance (function of CCD operating conditions)

  - cooling power at ends of ladders beyond vertexing aperture

  - developments in driver IC design

- Signal processing looks like a project well matched to 0.25 μm CMOS technology. Power dissipation?

Layout of ladder end

Data fibre

Readout IC

Bump bonds

CCDs
1 2

Ladder
inner
face

DC power

Active area

Clock fibre

Driver IC

Ladder
outer
face

Coolant flow

DC power

Cooling
block

2 of 3-point
mech-support

Readout IC

Pixel

CCD

Beryllium
substrate

Bond pad

Solder bump
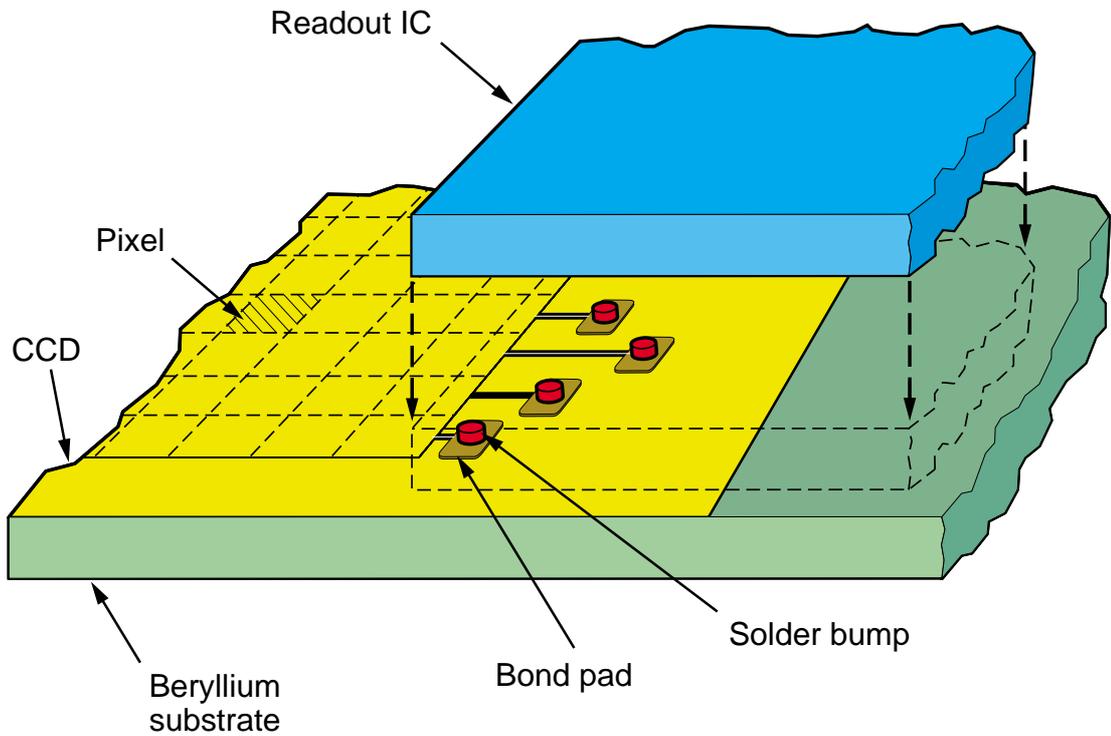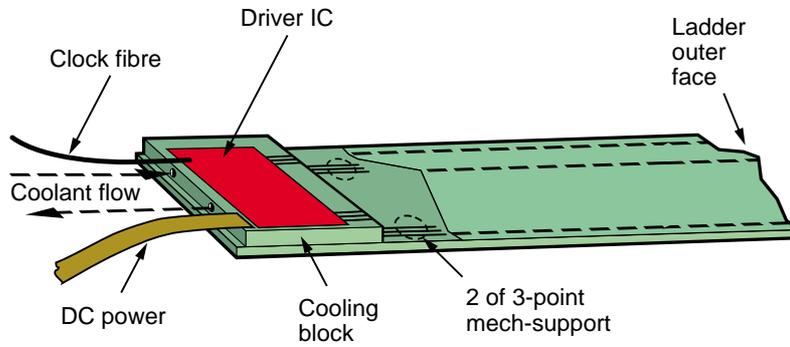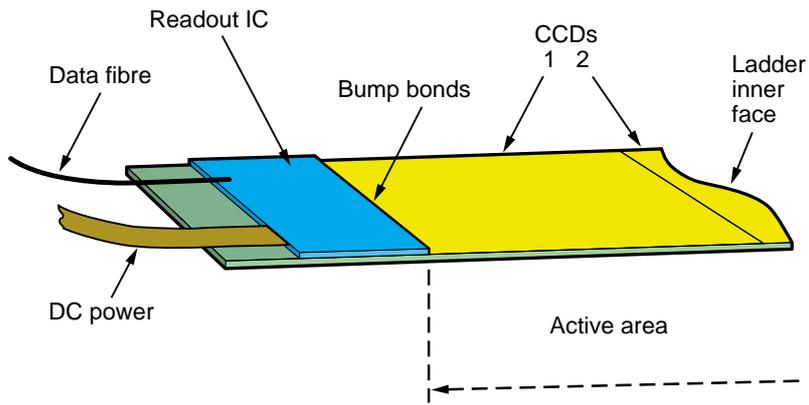
Technology choice between CCD and monolithic APS

- Similar charge collection process from equally thin layers is possible

- Issue is whether to transport signal charge to readout beyond the active volume, or to sense the charge where it is generated

- Numerous associated advantages and disadvantages. Examples:

  - Charge transfer to serial output is slow

  - Charge transfer is sensitive to (bulk) radiation damage from hadron irradiation (notably neutrons at future LC)

  - Serial output gives excellent inter-pixel uniformity of response (0.1 μm centroid precision possible)

  - Output at edge permits unrestricted area for processing

  - Reduced feature sizes permit more complex in-pixel logic

  - Power dissipation due to parallel clocking is undesirable

  - Power dissipation due to in-pixel logic is undesirable

  - In-pixel logic with min-I hit trigger would permit very fast readout of sparse data

  - CCD clock drive voltages can be reduced from 10 V to 3 V, I V, …

- CCD gate capacitances can be reduced by non-standard operating voltages, deep depletion, etc

- Numerous features where both designs are similar

  - Tolerance of ionizing radiation (both OK)

  - Layer thickness (probably will be limited by other considerations)

- Hybrid APS (as required for LHC detectors) look less competitive, but could be an important fallback option.

Conclusions

- We probably have 5 years of R&D before technology choices need to be made

- For all options, important to push hard since there is much scope for development and the physics prizes could be immense

- As usual, the technological developments for vertex detectors are likely to continue to make brisk progress into the distant future (improved pixel detectors are in demand for numerous imaging applications)

- Therefore, vital to ensure convenient access to the inner detector, in order to permit ongoing vertex detector upgrades every few years

- The preferred technology may well change during the life of the collider

- We hope that some of these developments may be of value for other areas of science where fast image capture is important (space-based earth observation, X-ray telescopes, SR applications, …)