A Fast CCD Vertex Detector for the Future Linear Collider: Some Recent Developments

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Abstract

Experiments at a future e^+e^- linear collider will require a high-performance vertex detector to identify heavy quarks in multi-jet final states. The SLD experiment at SLAC has successfully demonstrated that charge-coupled devices (CCDs) are ideal candidates for this role, offering excellent two-dimensional spatial resolution with extremely low mass.

This paper discusses recent R&D studies aimed at further reducing the vertex detector material budget and significantly increasing the CCD readout speed, in order to extend the physics reach of the future linear collider.

A radical new CCD architecture is described, which would enable a CCD-based vertex detector to be used in the extremely challenging environment of the superconducting TESLA collider.

1. Introduction

Charge-coupled devices (CCDs) have been used for over 15 years as vertex detectors in high energy physics experiments. They were initially used in a fixed-target charm-production experiment (NA32) [1], and then very successfully in two generations of vertex detector in the SLD experiment at the SLAC Linear Collider (SLC) [2], [3]. They are ideal candidates for a high-precision vertex detector in the linear collider environment, having already demonstrated (with 1990s technology) excellent two-dimensional space-point resolution (~3.5 μm), a very small layer thickness (0.4% X_0) and negligible cable plant owing to the very high level of signal multiplexing (>10^5). Furthermore, silicon processing technology is still advancing rapidly, enabling larger area devices to be realised with faster clocking capability and improved signal/noise performance.

A vertex detector for use at the at the Future Linear Collider (FLC) must satisfy several demanding conditions, all of which stem from the requirement for the best possible measurement of impact parameter. The two generations of CCD-based vertex detectors in SLD, VXD2 and VXD3, achieved impact parameter resolutions in the r-ϕ (r-z) plane of $\sigma_{r\phi}$ (σ_{rz}) ~ $11\oplus 70/p\sin^{3/2}\theta$ μm ($38\oplus 70/p\sin^{3/2}\theta$ μm) and $9\oplus 33/p\sin^{3/2}\theta$ μm ($17\oplus 33/p\sin^{3/2}\theta$ μm) respectively. The challenge for the FLC vertex detector is to improve on these figures to enable clean and efficient separation of multiple vertices in events with complex topologies.

With typical particle momenta of ~1 GeV/c, multiple scattering from the material in the beam-pipe and detector layers is the most significant factor in limiting the impact parameter resolution. By minimising the material budget, and decreasing the beam-pipe radius to bring the inner detector layer closer to the interaction point, the effect of multiple scattering could be significantly reduced. In the FLC it is expected that the beam-pipe radius could be made as small as 10 mm, (*c.f.* 24 mm in SLD), and by using the vertex detector support shell for strain relief it may be possible to fabricate it from beryllium of wall thickness 250 μm, which would contribute only 0.07% X_0. Furthermore, some radical ideas for minimising the material in the detector layers (Section 3.1) could dramatically reduce the contribution per layer down to as little as 0.06% X_0 (*c.f.* 1.1% X_0 in VXD2 and 0.4% X_0 in VXD3).

If these challenging goals can be met, simulation studies show that for the FLC vertex detector it should be possible to achieve impact parameter resolutions in both the r-ϕ and r-z planes of $\sigma_{r\phi}$ and $\sigma_{rz} \sim 4.2\oplus 4.0/p\sin^{3/2}\theta$ μm, which would enable pure and efficient tagging of b and c jets, and make accessible physics processes in the TeV range characterised by heavy-flavour jets.

2. A CCD-based vertex detector for the FLC

A series of design studies of possible configurations of a CCD-based vertex detector for the FLC has evolved into the conceptual layout shown in Fig. 1 and Fig. 2.

The vertex detector is a 5-barrel construction designed to provide stand-alone tracking with redundancy. The innermost layer, B1, has a radius of 15 mm, and consists of eight ladders each formed from single CCDs of 100 mm in length. The four outer layers, B2 – B5, consist of 8, 12, 16 and 20 ladders

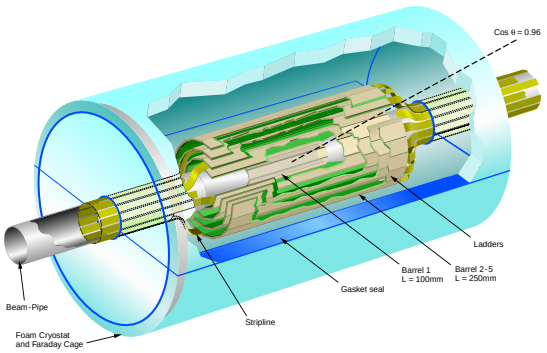

Figure 1. Conceptual layout of a CCD-based vertex detector for the FLC

respectively, where each ladder is formed from pairs of butt-jointed CCDs, each of length 125 mm.

Only two sizes of CCD are required: 100 mm × 13 mm in B1 and 125 mm × 22 mm in B2

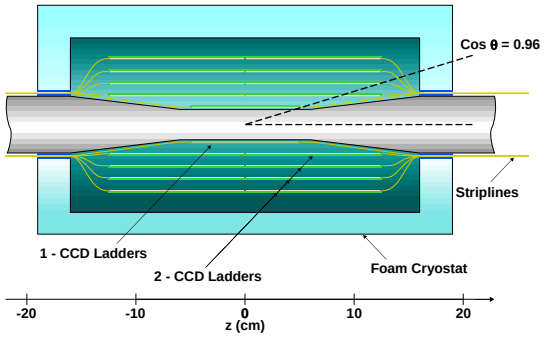

Figure 2. Cross-section of 5-barrel FLC vertex detector

to B5. Assuming pixel dimensions of 20 μm × 20 μm, the vertex detector will be a ~800 Mpixel device, and will provide a 3-hit acceptance (including B1) out to $|\cos\theta| = 0.96$. The final ladder tiling geometry will provide for sufficient overlap of CCD active areas to ensure that each layer is fully hermetic in ϕ.

3. Current R&D studies

At present, there are two main technology contenders for the design of the FLC. The Next Linear Collider (NLC) from SLAC and the Japanese Linear Collider (JLC) are both room-temperature designs utilising copper accelerating cavities in the X-band (11.4 GHz) or C-band (5.7 GHz), whereas the TESLA design from DESY [4] will use superconducting cavities in the L-band (1.3 GHz). R&D studies for a CCD-based vertex detector have so far focussed on its operation in the more benign environment of the NLC/JLC, where the repetition rate of the bunch trains will be 120 Hz. This will allow the CCDs to integrate the tracks resulting from the collisions of up to 190 bunches before being read out in the 8.3 msec inter-bunch train period.

The main background in the vertex detector will come from incoherent e^+e^- pair production, where most, but not all, of the particles are confined to a very small radius by the solenoidal magnetic field of the detector. Simulation studies estimate that inner layer CCDs on a radius of 15 mm will each integrate ~5 hits per mm^2 through the entire bunch train. Experience suggests that to avoid significant confusion of tracks, the pixel occupancy level should not exceed ~1%, implying a tolerable upper limit of ~10 background hits. To maintain this occupation level, each inner layer CCD must be completely read out between the bunch trains. This can be achieved by providing a multi-port output register at both ends of the CCD, as was the case for VXD3 in SLD (2-port registers clocked at 5 MHz), and increasing the readout rate. With 4-port output registers clocked at ~50 MHz, the inner layer CCDs could be fully read out in ~8.1 msec, or in ~5.5 msec if the output registers were subdivided into 6 ports.

One of the main goals of the current R&D programme [5] of the LCFI collaboration, therefore, is to study the performance of current imaging CCDs in this speed regime, which is an order of magnitude higher than that experienced in VXD3. This represents a significant challenge for the clock drive system, which for 3-phase CCDs must deliver fast rise-time

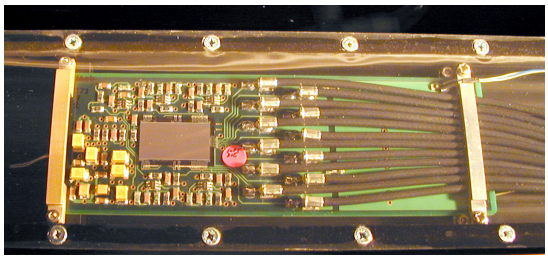

Figure 3. Test CCD mounted on preamplifier mother-board, with low-z clock drive feeds

pulses of width <6 nsec into highly capacitative loads (output register gate structure), while producing minimal feedthrough on the CCD output signal node.

Fig. 3 shows a test CCD wire-bonded to a mother-board assembly containing surface-mounted preamplifiers. To ensure fast rise-times, the clock drive pulses are fed to the mother-board via a 17 Ω cable system.

Further R&D studies will explore real-time signal processing, using fast FPGA-based algorithms for efficient dead-time free cluster-finding of minimum-ionising particle hits.

In conjunction with CCD designers, emphasis will be placed on a systems approach to the instrumentation, with careful consideration being given to the interface from the CCD to the fast clock drivers and low-noise analogue signal processing electronics.

3.1 Mechanical studies

As discussed in Section 1, for the vertex detector to achieve good impact parameter resolution, one of the most important goals is to minimise multiple scattering by reducing the materials budget, in particular for the beam-pipe and detector layers. The two generations of vertex detector in SLD achieved layer thicknesses of 1.1% X_0 and 0.4% X_0 respectively, and a further evolution for the FLC vertex detector could reduce this down to 0.12% X_0. This would be achieved using lapping and etching techniques to thin the CCDs down to the edge of the epitaxial layer (~30 μm). They would then be mounted on one side only of a thin beryllium substrate, strengthened by bonding to a thin beryllium beam of Ω or Λ cross-section.

However, as even this thin beryllium substrate structure itself contributes ~0.09% X_0 of the layer thickness, it is tempting to consider how it may be

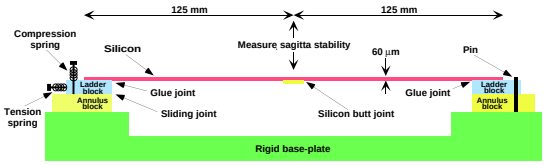

Figure 4. Test-rig to measure mechanical stability of a stretched silicon assembly

eliminated entirely. Studies have been conducted to investigate a support system whereby CCDs thinned down to 60 μm would be held only at their ends, achieving mechanical stability by placing them under tension. For the inner vertex detector layer, each ladder would consist of a single CCD of length 100 mm, whereas ladders in each of the outer four layers would require that pairs of CCDs be mechanically joined at their inner ends, using thin overlaid silicon strips.

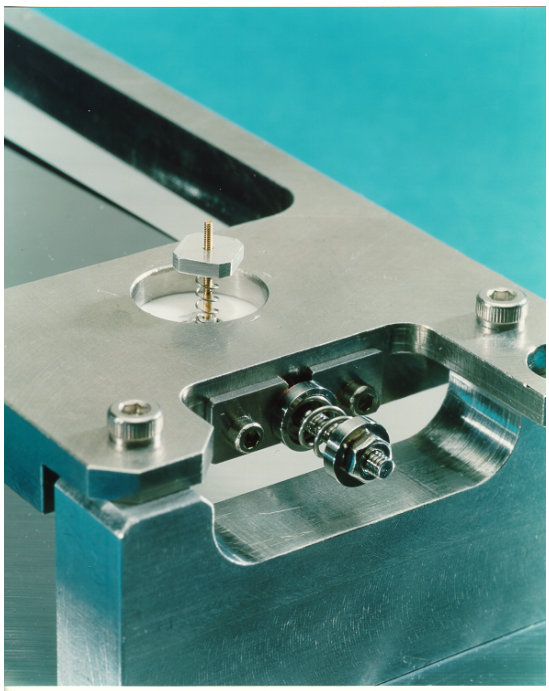

Figure 5. Photograph of stretched silicon test-rig, showing compression and tensioning spring system

Using the well-proven SLD vertex detector technique of sliding V and flat pairs of ceramic blocks, a test-rig was constructed (Fig. 4 and Fig. 5) to measure the stability of a representative assembly. This consisted of a pair of silicon strips, each 60 μm thick and 125 mm in length, bonded together as described above to represent a vertex detector outer layer.

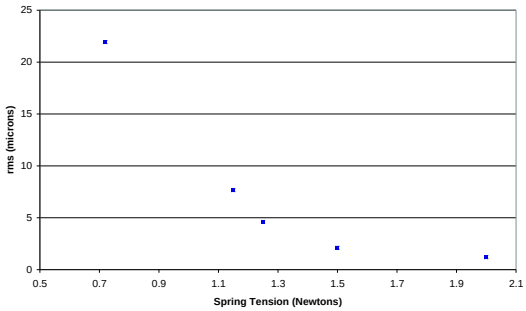

Figure 6. Sagitta stability as a function of spring tension applied to the unsupported silicon

Having determined a suitable compressive force to hold the sliding ladder and annulus blocks together (observed to be non-critical), a series of measurements of the sagitta of the silicon assembly was made as a function of tension. The procedure was to measure the sagitta, disturb the system and re-measure. Fig. 6 shows that with a modest tension of ~1.5 N the assembly remains remarkably stable at the level of ~2 μm, which is already much better than required.

Further studies will measure the stability of the full ladder profile following cycling between room temperature and operating temperature (~180K).

4. The TESLA challenge

In contrast to the NLC/JLC machine, the superconducting TESLA design will have a much lower bunch train repetition rate of only a few Hz, but the luminosity per bunch train will be correspondingly very much higher. This would result in unacceptably high integrated backgrounds in the CCDs, particularly for those in the inner layer. In order to accommodate this time structure, which would appear ill-matched to conventional CCD operation, a radical new CCD architecture is proposed.

4.1 Column-parallel CCD architecture

Conventional CCD architecture operates in a raster-scan mode, whereby the charge pattern in the imaging area is transferred one row at a time into the output

register, which then shifts it out sequentially to the output node capacitance and sensing circuit. As described above, the effective readout time can be reduced by segmenting this register into multiple output ports, but there remains a high level of multiplexing of many columns to each output port. This inevitably implies a long readout time.

We believe that by eliminating the serial output register entirely, providing each column with its own output port and clocking the imaging region at 50 MHz, it should be possible to increase the effective CCD readout rate by two orders of magnitude. For the inner layer CCDs, where the output ports would be situated at both ends of the imaging area, this would imply an overall data transfer rate from the CCD of ~65 Gpixels per second, and a readout time of ~50 μsec.

An alternative way of considering this architecture is to regard it as a parallel array of linear CCDs (650 for the inner layer devices) reading out synchronously at 50 MHz.

Column-parallel CCDs of this nature could be read

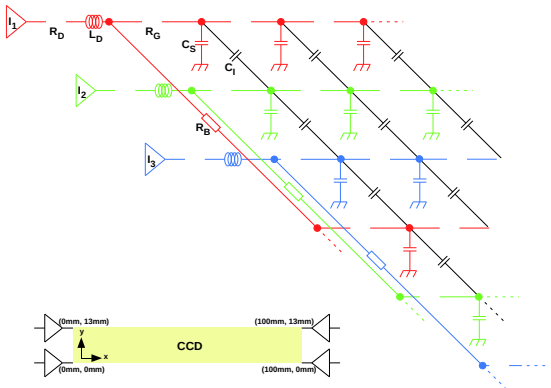

Figure 7. SPICE model of an inner-barrel CCD

out continuously during the TESLA bunch trains, so the vulnerable inner layer of the vertex detector would now accumulate only a modest level of background hits in the 50 μsec effective integration time.

4.2 SPICE simulations of clocking

As discussed above, a column-parallel CCD would require to be read out in 50 μsec to ensure an acceptable background hit density. This implies a clocking rate of 50 MHz, which is extremely demanding. To study the performance limitations of such a speed regime a SPICE model of an inner-barrel CCD was created (Fig. 7).

A 3-phase CCD of length $\Delta x = 100$ mm and width $\Delta y = 13$ mm was modelled in sections of 1 mm^2, initially using the following nominal parameter values:

- Gate-substrate capacitance $C_S = 3.3$ pF/mm^2
  (achievable if the buried-channel and channel stop regions are both depleted)
- Inter-gate capacitance $C_I = 2.5$ pF/mm^2
- Polysilicon gate electrode resistance $R_G = 3$ kΩ/mm
- Aluminium clock bus-line resistance $R_B = 0.5$ Ω/mm
- Driver output impedance, R_D, and interconnect inductance, L_D, both assumed negligible

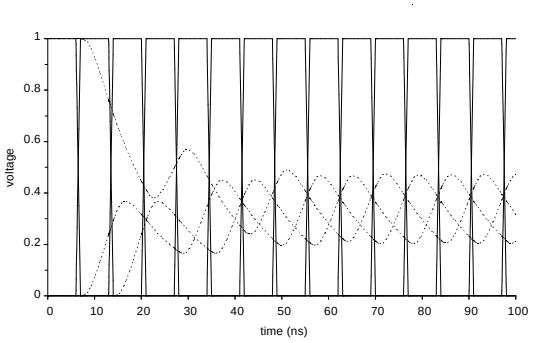

Figure 8. 3-phase clock waveforms (x = 0 mm): y = 0 mm *(solid lines)* and y = 6.5 mm *(dotted lines)*

- Each corner of the CCD fed with square clock pulses of amplitude 1 volt at 50 MHz

With the above nominal parameters, SPICE was used to examine the quality of the resultant clock

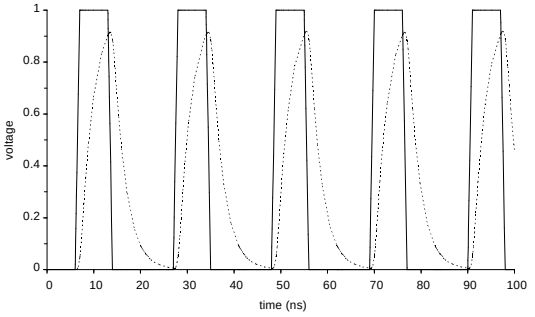

Figure 9. 1 phase of 3-phase clock waveforms with 3 μm wide aluminium overlay of gate electrodes (x = 0 mm): y = 0 mm *(solid line)* and y = 6.5 mm *(dotted line)*

pulses at extreme positions across the CCD.

Fig. 8 shows the severe degradation of the waveforms in the central region of the CCD at y = 6.5 mm and at x = 50 mm, effectively preventing charge transfer. It is caused by the highly resistive polysilicon gate structure, and can be dramatically reduced by overlaying the polysilicon gates with 1 μm thick, 3 μm wide aluminium strips to lower their resistance.

Fig. 9 shows the clock pulses at the same two positions on the CCD as before, but now the waveforms at the centre of the gate structure (y = 6.5 mm) are

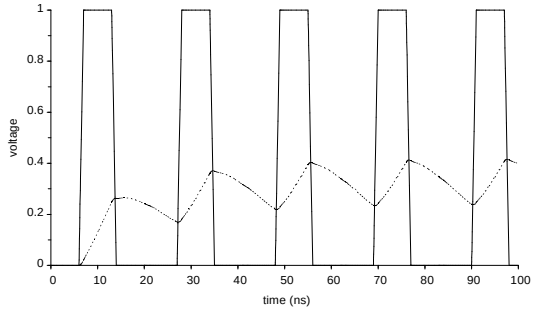

Figure 10. 1 phase of 3-phase clock waveforms (y = 0 mm):

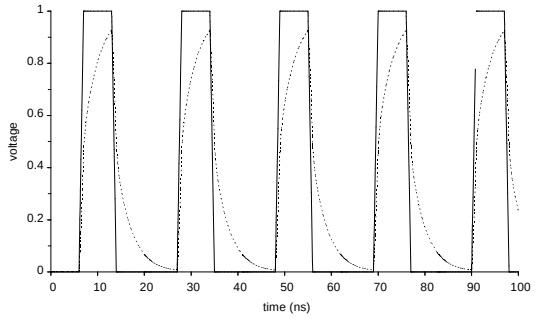

Figure 11. 1 phase of 3-phase clock waveforms with 10 μm thick aluminium bus lines (y = 0 mm): x = 0 mm *(solid line)* and x = 50 mm *(dotted line)*

completely adequate for good charge transfer efficiency.

Fig. 10 shows how the clock waveforms also collapse at the mid-point of the CCD (x = 50 mm), due to the resistance of the long aluminium bus lines.

By thickening these traces from 1 μm to 10 μm, acceptable waveforms can be maintained across the full length of the CCD (Fig. 11). Assuming six 100 μm wide bus lines along a 13 mm wide inner-layer CCD, the resultant area-averaged increase in the material budget is completely negligible (<0.0005% X_0).

The addition of a finite (realistic) value of clock driver interconnect inductance L_D = 200 pH produces

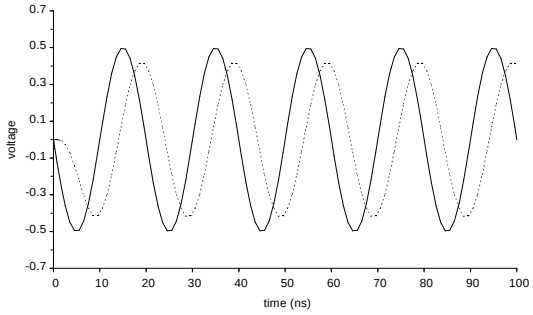

Figure 12. 1 phase of 2-phase clock waveforms at x = 0 mm, y = 0 mm *(solid line)* and at x = 50 mm, y = 6.5 mm *(dotted line)*

negligible changes to any of the above simulation results.

Retaining the previously optimised parameters and including L_D = 200 pH, the SPICE model was then modified to simulate a 2-phase CCD structure, in order that the clock waveforms could be changed from square pulses to anti-phase sinusoidal waveforms. A clock system of this nature offers the potential benefits of the lowest possible frequency spectrum and reduced peak current demands on the clock drivers, both of which minimise clock pickup. The balanced nature of the antiphase drive waveforms should also produce minimal crosstalk to the CCD output signals.

Fig. 12 compares one of the two clock phases at two extreme positions across the CCD, and shows that excellent amplitude uniformity can be achieved.

Finally, in order to estimate the necessary cooling requirements of the vertex detector, the power dissipation in the entire CCD due to clocking was simulated. Assuming 2-phase clock amplitudes of 1 volt, Fig. 13 compares the instantaneous power dissipation in the two resistive regions of the device. Although the total average power dissipation per CCD is ~3.6 W, in the TESLA environment the clocks could be stopped in the inter-bunch train period, thereby reducing the effective power dissipation by a factor of ~200. The inner barrel of the vertex detector would then dissipate <150 mW. With much smaller background hit densities, the outer layers could be clocked at lower rates, giving an estimated cooling requirement for the entire vertex detector of only a few watts. As in SLD, this could be met by a cold gas system with very modest flow rates.

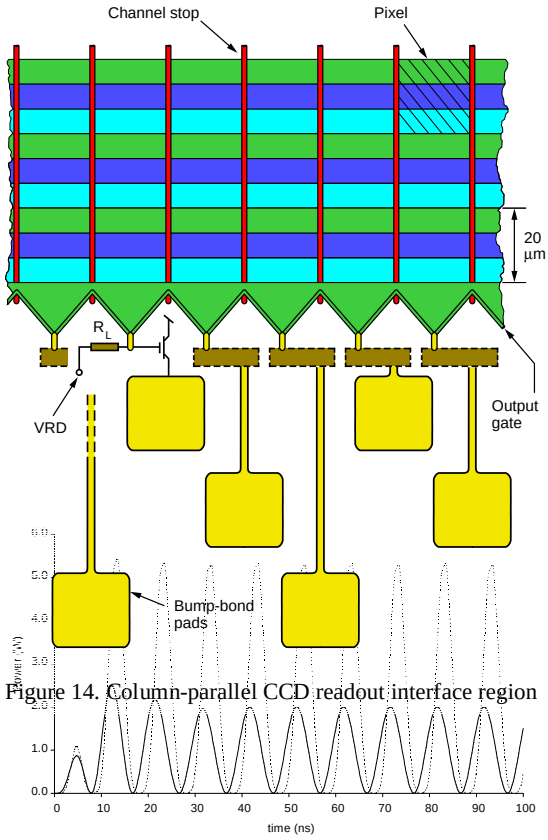

Figure 14. Column-parallel CCD readout interface region

Figure 13. Clock power dissipation in CCD gate structure *(solid line)* and in the clock bus traces *(dotted line)*

4.3 Signal processing

Another challenge associated with the column-parallel architecture is handling the very high density of signals emerging from the device. Assuming $20\ \mu m \times 20\ \mu m$ square pixels, the on-chip CCD output circuits must be on a 20 µm pitch, which would imply minimal active circuitry. For example, in our sparse-data application it is assumed that the reset transistor could be replaced by a simple resistive load, R_L.

The readout chip would be an Application Specific Integrated Circuit (ASIC) to perform all the necessary signal processing functions. It would be connected locally to the edge of the CCD via a one-dimensional row of staggered bump bonds, for example on a pitch of 60 µm, as shown conceptually in Fig. 14.

Following preamplification, the readout chips could utilise modern CMOS digital signal processing techniques to perform digitisation (4-bit precision is probably adequate), real-time cluster-finding and data sparsification. The resultant data could be stored in on-chip memory during the bunch-train and transported out of the vertex detector with optical links during the long inter-bunch train gap. Fig. 15 shows a possible signal processing chain up to the memory.

Located at the ends of the CCDs, the readout and clock driver chips would lie outside the acceptance of the FLC vertex detector and would therefore not have such critical material limits, so if power dissipation were to prove a problem, more robust cooling techniques could be used specifically in this region.

Fig. 16 shows conceptually how these chips might be arranged at the ends of the CCD assemblies.

4.4 Data volumes

Some estimates have been made of the data volumes which would need to be stored locally until the inter-bunch train gaps. Using current estimates for the background rates in TESLA, the total number of hits

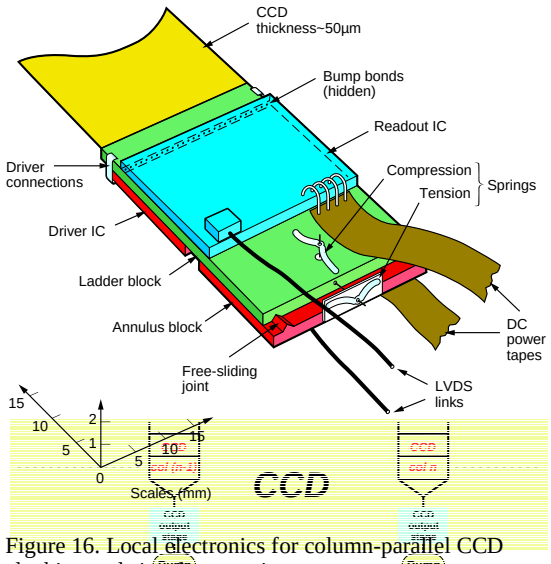

Figure 16. Local electronics for column-parallel CCD clocking and signal processing

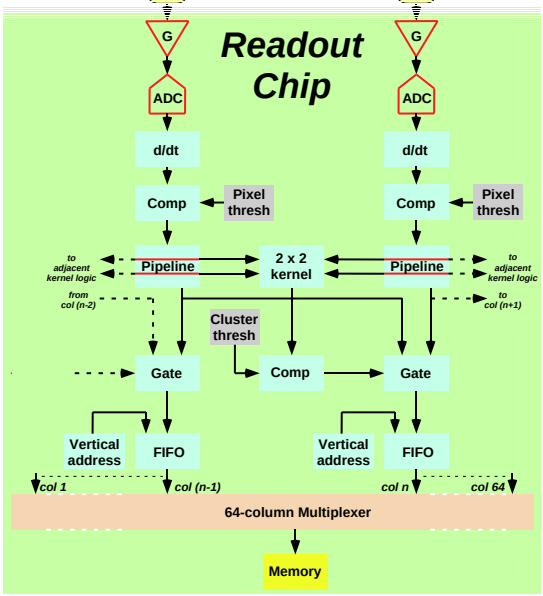

Figure 15. Column-parallel CCD processing chain

expected in the entire vertex detector during a single bunch train ~1.3×10^6, almost half of which are from the inner layer CCDs. Each hit can span up to four pixels, so with the addition of some form of address tagging the total data volume to store during the bunch train ~8 Mbytes.

Running in an untriggered mode, all these data must be exported from the vertex detector before the next bunch train, which corresponds to a very modest rate of ~40 Mbytes per second for the full detector. A single optical link would therefore provide more than adequate bandwidth.

5. Summary

Design studies have already indicated that a CCD-based vertex detector would be a very powerful tool at the Future Linear Collider. The advantages of CCD technology have already been successfully demonstrated in the SLD experiment, and subsequent developments will further enhance performance.

A programme of R&D studies is therefore under way to investigate solutions to some of the technical challenges imposed by operation at the FLC.

Increasing the readout frequency of CCDs by a factor of ten beyond the SLD rates, to 50 MHz, is an important goal for their use in NLC/JLC.

Very promising results have already been achieved with the technique of tensioning unsupported silicon in order to reduce the vertex detector material to as low as 0.06% X_0. Mechanical stability of ~2 μm has been observed with very modest values of tension.

To meet the stringent demands of operating CCDs in the environment of TESLA, the novel column-parallel architecture has been proposed. Preliminary simulations have already demonstrated the feasibility of clocking such a structure at rates ~50 MHz, with power dissipation well within the capability of conventional gas cooling. With powerful local processing electronics in a customised ASIC, only a very modest optical link bandwidth would be required to export the sparsified data from the vertex detector.

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