Linear Collider Flavour Identification (LCFI) Collaboration

P306 – Status Report and Proposed Future Programme

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Abstract

The LCFI collaboration started work in October 1998, after PPESP approval for an exploratory R&D programme. In March 2001, the PPESP approved the start-up of a more ambitious R&D programme, with the 7-year goal of proving the design concept for a CCD-based vertex detector for the future e^+e^- linear collider. This means polar angle coverage to $|\cos\theta| = 0.96$, a readout time of 50 μs for the inner layer, and sufficiently thin layers ($<0.1\%\ X_0$) to preserve ~5 μm impact parameter precision down to ~1 GeV/c. This last requirement implies sufficiently low power dissipation in the active volume to permit gaseous cooling. Furthermore, the CCDs need to satisfy new levels of radiation tolerance. An outline of the overall scientific programme and required funding was submitted to the Science Committee in January 2002. Based on their recommendation that the project 'go forward for full peer review as soon as possible', this document provides a comprehensive revision of the proposal of 2001, tailored to the financial constraints suggested by the SCP4 Panel.

1. Introduction

LEP, SLC and the Tevatron have established the importance of vertex detectors in understanding the physics accessible at high energy colliders. At the future linear collider (LC), both precision measurements and particle searches set stringent requirements on the efficiency and purity of the flavour identification of hadronic jets, since final states including short-lived *b* and *c*-quarks and τ-leptons are expected to be the main signatures. The vertex detector must provide highly accurate reconstruction of the charged particle trajectories close to their production point, in order to reconstruct the topology of secondary vertices in the decay chain of short-lived heavy flavour particles in a complex environment. High tagging efficiency is essential due to the small event samples in individual processes, and high purity is required because of the large backgrounds to many processes of interest.

Experience at LEP and SLD shows the way forward. Jet flavour identification can be based primarily on the topological vertex structure in the jet, since this in principle allows most *B* and *D* decay modes to be detected. By aiming for good sensitivity down to decay times short compared with the mean lifetimes, high efficiencies may be realised. Distinguishing clearly between *b* and *c* jets requires additional information. This comes from the secondary and tertiary vertex topology, the charged decay multiplicity and the vertex mass, after applying corrections for missing neutrals [1].

As well as tagging *b* and *c* jets, the vertex charge (if non-zero) can distinguish *b* from $\overline{b}$ and *c* from $\overline{c}$. This requires sufficient precision to distinguish between all the decay tracks and those coming from the primary vertex. Even the case of neutral *B* decays can often be handled by measuring the charge dipole between the secondary and tertiary vertices, as demonstrated in SLD.

Cases where leptons (and hence neutrinos) are absent from jets are particularly valuable for precise jet energy measurement. However, the absence of a single electron in a jet is not easily established. Due to the prevalence of gamma conversions, it is important to track detected electrons inwards through the thin layers of the vertex detector to establish if they were really produced in semileptonic *B* or *D* decays. As well as providing a clean sample of jets free of missing neutrinos, this procedure in principle allows corrections to be applied to jets with charged leptons (hence also neutrinos). In these cases, the jet energy measurement may be improved substantially by extending the procedure used for the p_T-corrected mass, allowing a correction for the transverse momentum of the missing neutrino.

The optimised flavour ID, vertex charge determination and enhanced jet energy measurement, will provide valuable physics tools. What precise discovery potential is associated with these tools is emerging as they become more widely used (in simulation) by the international physics study groups. In the meantime, we are guided by the excellent SLD experience.

Extensive studies of the machine-detector interface have shown that by careful control of backgrounds, the LC interaction region can be made particularly favourable for the operation of a vertex detector of unprecedented performance, well-matched to the physics goals of the TeV regime.

Since the formation of the LCFI collaboration and approval by the PPESP in October 1998 for an exploratory R&D programme, we have played an active part in the ongoing international physics and detector studies related to flavour identification and vertex detectors. Of the 4 detector options currently being studied (all of them silicon pixel-based) it is our opinion that a CCD-based design, building on the 307 Mpixel SLD vertex detector, is the most promising. This opinion was shared by the DESY PRC in their review of May 2001, which states: 'Compared to alternative vertex detector technologies, the proposed approach exhibits the highest potential for reaching ultimate performance'.

This document describes the R&D programme proposed in order to prove the design concept for the detector. This means polar angle coverage to $|\cos\theta| = 0.96$, a readout time of 50 μs for the inner layer, and sufficiently thin layers ($<0.1\%\ X_0$) to preserve ~5 μm impact parameter precision down to ~1 GeV/*c*. This last requirement implies sufficiently low power dissipation in the active volume to permit gaseous cooling.

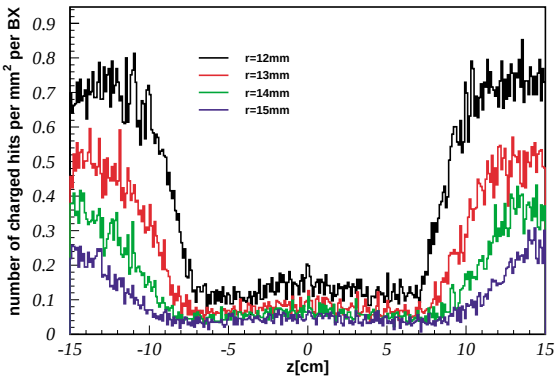


Figure 1: Pair background in the TESLA interaction region as function of position for various detector radii and a solenoid field of 4 T.

Furthermore, the CCDs need to satisfy new levels of radiation tolerance. Some of these requirements represent a modest extension of the SLD performance. However, two of them are a major challenge, notably the layer thickness ($0.4\%\ X_0$ achieved in SLD) and the readout time (100 ms in SLD). Our funding request is compatible with achieving the goals for the LC detector within the next 6 years.

An outline of this proposal document is as follows. In Section 2, the current vertex detector conceptual design (which is now reasonably stable) is discussed. In Section 3, we discuss the R&D programme for the advanced CCDs and associated electronics needed for this detector. Here, the injection of seedcorn funding from the PPESP in 2001 has enabled the work to move forward in high gear. As important as the CCD development, is the R&D to minimise the detector thickness while still providing excellent mechanical stability. Fortunately, this is much less expensive, and steady progress continues, as discussed in Section 4. There are important new ideas in the area of radiation effects, as discussed in Section 5. In the conclusions (Section 6) we mention the status of the global detector R&D coordination, and the 'no-lose' scenario which will ensure a strong place for the LCFI collaboration in the future project, whichever technology is eventually selected for the vertex detector system.

The LCFI web page [2] provides access to all collaboration publications and talks listed in Appendices A and B. Financial and managerial aspects of the project, in accordance with the new guidelines, are included as Appendices C to J.

2. Vertex detector conceptual design and performance

2.1 Machine-related issues

The most important machine-related parameter which directly impacts on the physics potential of the vertex detector system is the beam-pipe radius. This was already much better at SLC than at LEP (24 mm as opposed to 50 mm). The lessons learned at SLC have since led to far more advanced beam delivery and synchrotron radiation (SR) masking, with the result that both NLC and TESLA will permit beam-pipe radii below 15 mm with negligible SR background. What can not be avoided is the e^+e^- pair background from the beam-beam interaction, but its effects can be limited by the use of a high field detector solenoid (4 T is envisaged). For TESLA, a vertex detector inner layer at a radius of 15 mm can have an active length of ± 5 cm without encountering serious pair background as shown in Figure 1; the average background hit density is 0.03 hits/mm^2 per bunch crossing. Results for NLC are similar.

In the case of NLC, the integrated background during the fast train of 190 bunches at 1.4 ns interval is modest, and it is sufficient to read the data out in the 8.3 ms between bunch trains. For TESLA, the long train of 2820/4500 bunches at 500/800 GeV would produce excessive background in a static detector, so multiple readout during the 950 μs bunch train is required. The proposed solution gives a readout time of 50 μs, which is sufficient to limit the pair background on layer 1 to the comfortable level of 4 hits/mm^2. One has also to consider the question of radiation damage. The LC background conditions are expected to be sufficiently benign that modest developments in radiation resistant CCD technology will deliver an adequately robust detector, as discussed in Section 5. This is one of the advantages of the e^+e^- collider with respect to LHC, where the environmental conditions severely limit the potential vertex detector performance.

2.2 Detector conceptual design

While the background levels require a reasonably fine-grained pixel detector at small radii, the hit densities within the core of high

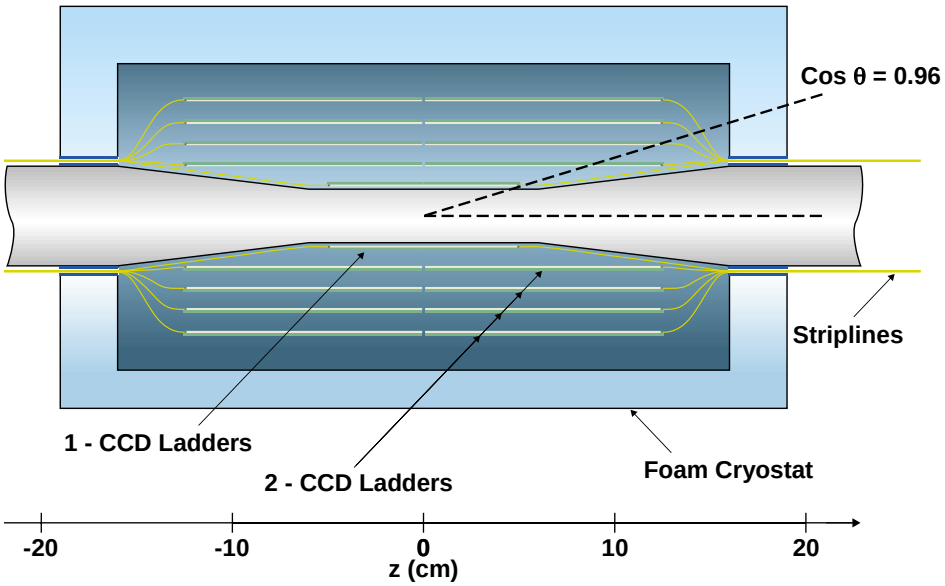


Figure 2: Cross-section of vertex detector. Cylindrical support shell is not shown.

energy jets provide an even stronger constraint. On a 10-15 mm inner layer radius, it has been demonstrated [3] that pixels of size well below 50×50 μm^2 are required to avoid serious cluster merging within the cores of jets. The proposed CCD detector design, based on 20×20 μm^2 pixels, is sketched in Figures 2 and 3, and provides full 5-layer coverage to $|\cos\theta| = 0.9$. The outer 4 layers are used for stand-alone track reconstruction. The advantages of stand-alone reconstruction in tracking sub-detectors are well-established; they include internal alignment optimisation, efficiency monitoring of the outer tracking systems and vice versa, optimal identification of γ conversions within the vertex detector and optimal rejection of 'bad' hits due for example to cluster merging between closely spaced hits.

Having found the tracks in layers 2-5, the layer 1 hits are used solely to refine the track extrapolation to the IP, which is particularly important for low momentum particles.

When used in conjunction with a well-tuned outer tracker, the vertex detector will provide high quality impact parameter measurements over the angular region covered by layers 1-3, giving excellent coverage all the way to $|\cos\theta|$=0.96.

As discussed in Section 5, radiation damage considerations lead to an optimum operating temperature of around 180 K. Figure 3 shows the detector inside its low-mass foam cryostat, as well as the extremely stable support structure (a closed pair of beryllium half-cylinders) which is mounted onto the beam-pipe inside the cryostat. Being outside the volume used for the precision measurement of tracks and their extrapolation to the IP, this shell can be relatively robust (1-2 mm wall thickness). It serves the additional purpose of clamping the two outer sections of beam-pipe rigidly together (clamps located at z approximately $\pm$ 15 cm). This allows the critical inner section of beam-pipe of length 12 cm and radius 14 mm to be made extremely thin: 0.25 mm wall thickness beryllium is considered possible.

The barrel staves or 'ladders' which comprise the detector elements as shown in Figure 3, are made as thin as possible over their active lengths. This design has the great advantage that the thin active regions of layers 1-3 comprise all the material in the fiducial volume needed for the highest precision tracking and vertex reconstruction. The low power dissipated in the CCDs means that they can be cooled by a gentle flow of nitrogen gas, making a negligible contribution to the material in the fiducial volume. This gives unprecedented quality of impact parameter measurement over the greatest possible polar angle range. However it does require that the signal charge packets be transferred out of the fiducial volume before they can be sensed. The innermost layer consists of single-CCD ladders, read out from both ends, while layers 2-5 are made of 2-CCD assemblies butted together and read out from the outer ends only, as indicated in Figure 2. Thus in some cases signals of only about 1000 electrons have to be transferred faithfully over a distance of up to 12.5 cm (~ 6000 pixels) en route to the CCD output. While this is a standard procedure for

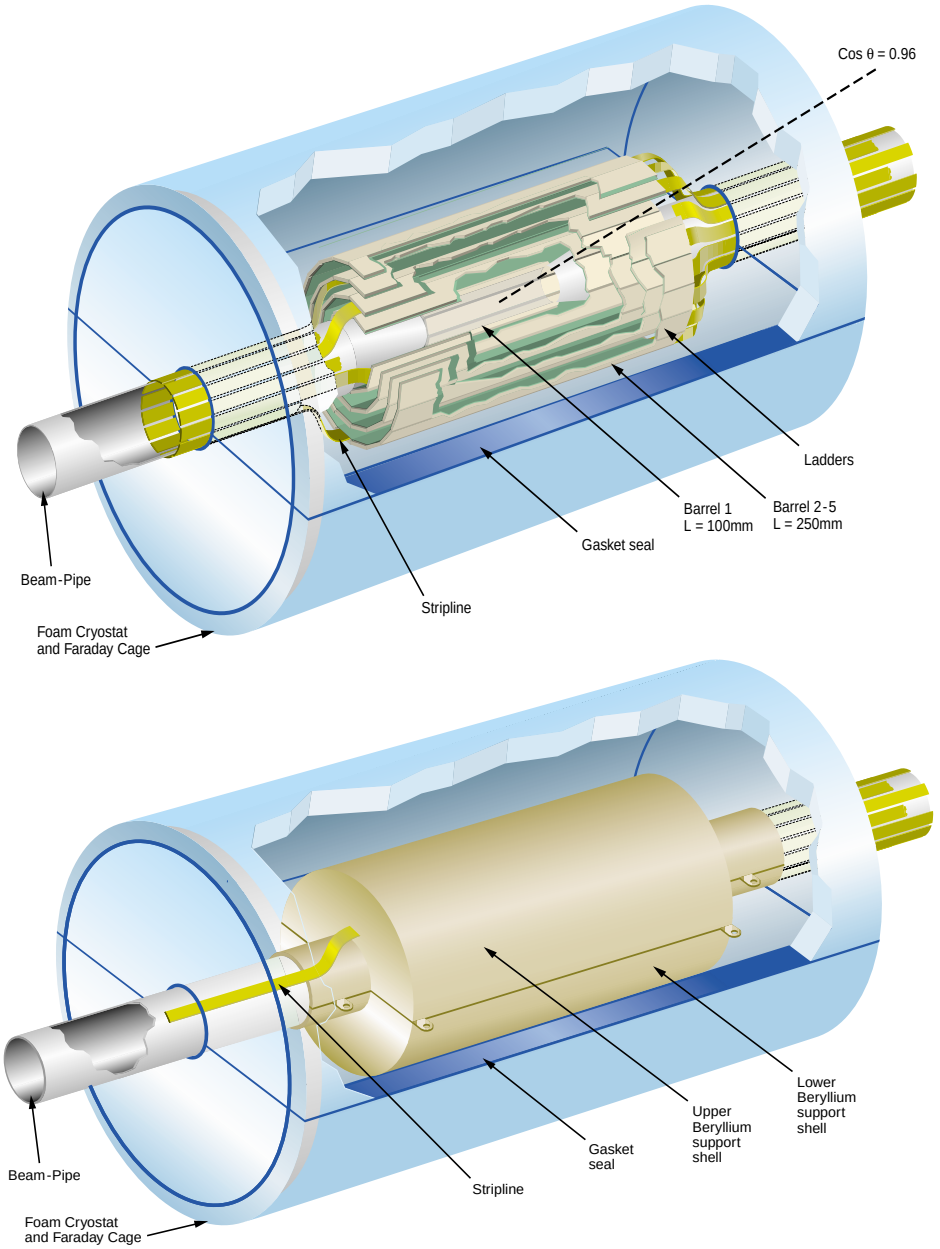


Figure 3: Top: Isometric view of the 5-layer vertex detector.
Bottom: Beryllium shell which supports the 5 detector layers and provides stress relief to the delicate inner section of beam-pipe.

scientific grade devices, achieving this at high speed and in the LC environment is challenging.

All the thin ladders are stabilised mechanically beyond the fiducial volume by being bonded to 'ladder blocks' at each end. These are attached to rigidly supported 'annulus blocks'; see Figure 4. The ladder block at one end is pinned to its annulus block, the other can slide in the *z* direction and is held under tension. The tension adds stability to the thin ladder. The sliding allows the tension to be maintained despite differential contraction as the system is cooled down to its operating temperature. This support system extends the principles pioneered in the SLD vertex detectors [4,5], and is discussed in detail in Section 4. As well as providing the mechanical support for the CCD, each ladder block carries the local electronics components in the form of two or three integrated circuits; these are discussed in Section 3.

The power dissipation in these components will considerably exceed the capability of gas cooling. At the ends of the ladders, the material budget is less critical and one can employ a more robust cooling system. A likely candidate is evaporative nitrogen cooling as used successfully in the CCD vertex detector of the CERN NA32 experiment [6], the first particle physics experiment in which a pixel-based vertex detector was used.

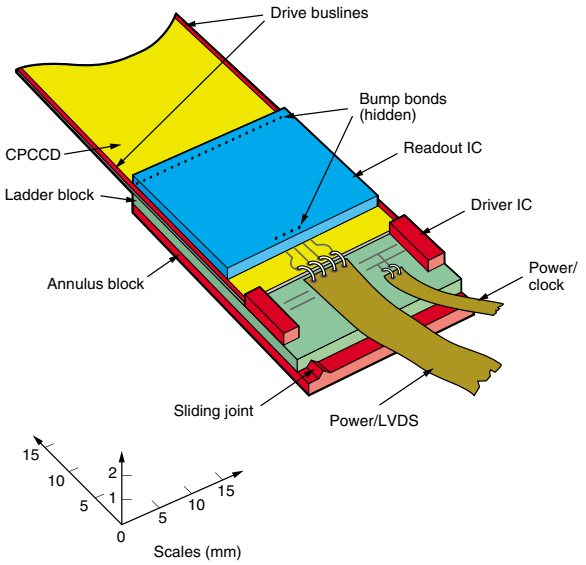


Figure 4: Layout of components at end of ladder. A compression spring establishes correct engagement of the sliding joint between the blocks, while a tensioning spring helps stabilise the shape of the ladder.

The local electronics on the ladders is powered, controlled and read out via striplines and optical fibres routed along the beam-pipe below the polar angle range used for tracking, connecting to inner electronics mounted in the form of a thin shell on the surface of the SR mask assembly.

Given that TESLA provides the more challenging operating conditions, this option has been used for the detailed design study. The NLC situation is similar, but with more relaxed readout requirements. Parameters of the proposed vertex detector for TESLA (799 Mpixels) are listed in Table 1. Processed data stored in the readout ICs during the bunch train, amounting to ~ 8 Mbytes, are read out between trains for online event reconstruction.

Taking account of all these components, the estimated material budget for the entire

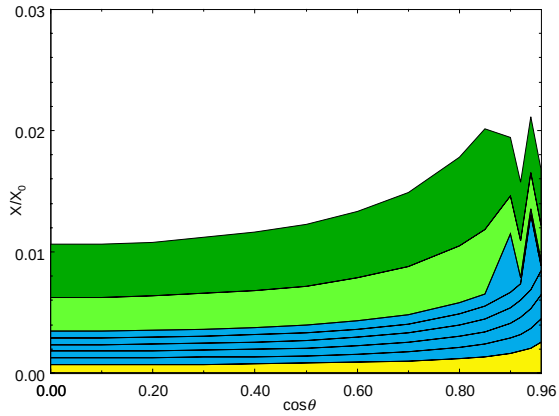


Figure 5: Material budget as a function of polar angle (beam-pipe, each of 5 layers, support shell and cryostat)

vertex detector system, assuming a successful outcome to the thin ladder development programme, is shown in Figure 5. The beam-pipe and critical first 3 layers amount to 0.25% X_0 at $\cos\theta = 0$ and rise to only 0.8% X_0 at $|\cos\theta| = 0.96$. The ends of layers 4 and 5, the support shell and cryostat are all beyond the region of high precision tracking; by the time the particles encounter this material, their impact parameters are well measured.

2.3 Generic detector performance

In this section, we discuss simulations based on the complete TESLA tracking system, namely the vertex detector, intermediate tracking detector (ITC) and main tracking detector (TPC) operating in a 4 T solenoid field. Details of these studies are reported in [7].

The most important figure of merit for any pixel-based vertex detector can be expressed by the precision with which the track impact parameter to the interaction point is measured, separately in the $r\phi$ and rz projections. For a set of cylindrical detectors, this resolution can

Layer	Radius	CCD L×W	CCD size	Ladders and CCDs/lddr	Row clock fcy and Readout time	Bgd occupancy	Integrated bgd
	mm	mm^2	Mpix			Hits/mm^2	kHits/ Train
1	15	100×13	3.3	8/1	50 MHz/50 μs	4.3	761
2	26	125×22	6.9	8/2	25 MHz/250 μs	2.4	367
3	37	125×22	6.9	12/2	25 MHz/250 μs	0.6	141
4	48	125×22	6.9	16/2	25 MHz/250 μs	0.1	28
5	60	125×22	6.9	20/2	25 MHz/250 μs	0.1	28

Table 1: Key parameters of the TESLA vertex detector design. Background occupancy is based on calculated density per bunch crossing multiplied by number of bunch crossings during readout of that layer.

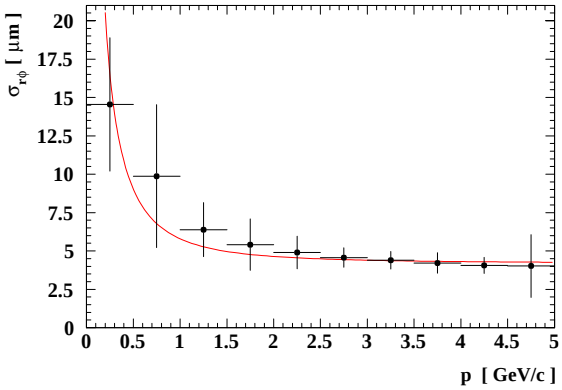


Figure 6: Track impact parameter resolution in $r\phi$ vs momentum for $\theta = 90^{o}$, for 4 T solenoid field

be expressed as

$$\sigma = \sqrt{a^2 + \left(\frac{b}{p \sin^{\frac{3}{2}} \theta} \right)^2}$$

The constant a depends on the point resolution, layout and geometrical stability of the detectors and b represents the resolution degradation due to multiple scattering, which varies with track momentum p in GeV/c and polar angle θ. For the present detector design, the values of a and b are similar for both projections, and take the values 4.2 μm and 4.0 μm respectively. An example is plotted in Figure 6. These calculations are based on a full GEANT description of the TESLA detector, and use the BRAHMS detector simulation program. It is assumed that the goals of the mechanical R&D programme discussed in Section 4 can be met, and that the point resolution of 3.5 μm achieved with earlier generations of CCD detectors can be maintained.

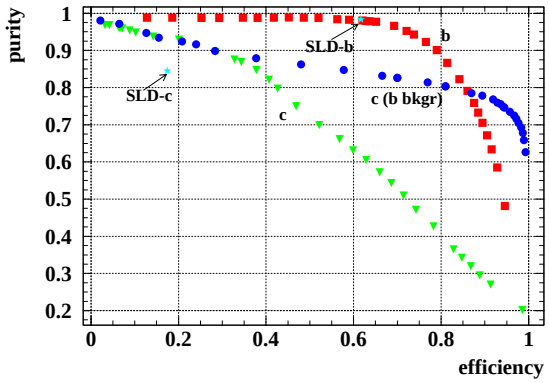


Figure 7: b and charm tagging efficiency/purity performance compared with the best existing detector.

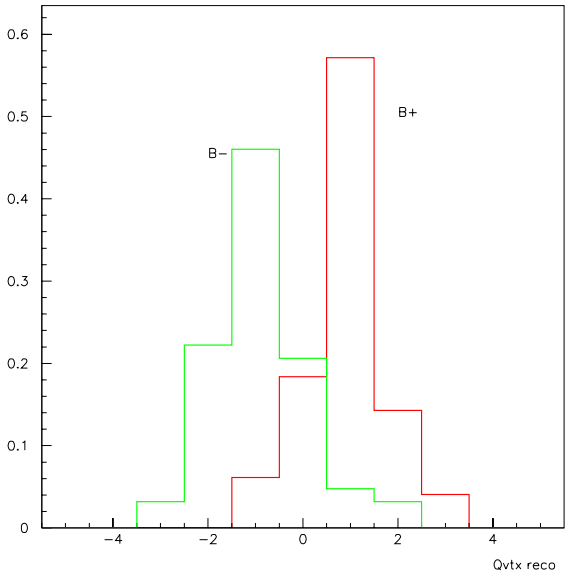


Figure 8: Vertex charge determination for $Z \to b\bar{b}$ events.

The other important performance parameter is the 2-track resolution, which is particularly relevant to the core of high energy jets where the particles traverse the inner layer of the vertex detector. With a clean 2-track spatial resolution of about 40 μm, CCDs are extremely robust. However, some B hadrons decay close to or beyond layer 1, giving merged or single-hit data in this layer. Experience from NA32 shows that these long-lived particles will form a particularly clean category, given unambiguous information from the outer layers. However, these questions need detailed study.

Studies of the physics performance of such a detector system are just beginning. First results are reported in [7]. As an example, the capability for b and charm tagging for $e^+e^- \to Z \to q\bar{q}$ is shown in Figure 7. Such events are a widely used benchmark for vertex detectors, and the 45 GeV jets are typical of the high multiplicity events in the TeV regime. The result for b tagging is similar to that achieved with the SLD vertex detector, which was already close to optimal. However, the new design delivers a dramatic improvement in the charm tagging performance. The figure also shows the excellent charm tagging performance in the case of predominantly b background, which is relevant to the important physics example of measuring Higgs branching ratios.

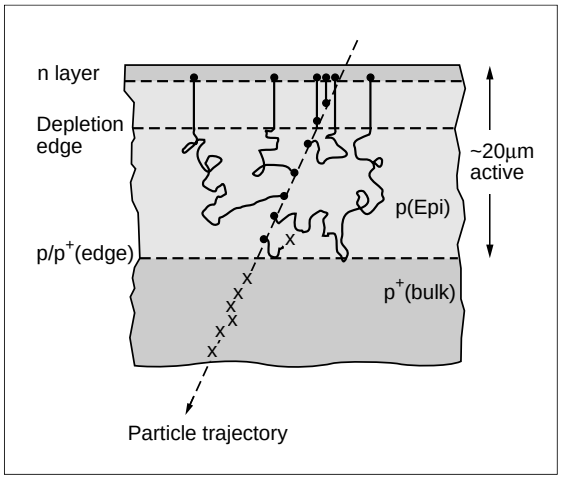


Figure 9: Charge collection within a buried-channel CCD structure.

The performance for more delicate physics requirements such as vertex charge and charge dipole determination is currently being evaluated. The vertex charge measurement is important for distinguishing between b jets and $\bar{b}$ jets; a first indication is shown in Figure 8. This work is only beginning, and one can expect a neural net approach to lead to an optimised assignment of tracks to vertices, considerably enhancing what would already be extremely valuable information for physics. This measurement depends on the correct vertex assignment of all tracks in the angular region of the jet. The lowest momentum B decay track is typically around 1 GeV/c, so the multiple scattering term in the impact parameter resolution is important. This term scales linearly with the radius of the beam-pipe and detector inner layer, so it is clear that minimising this radius is important for physics. While this statement needs to be supported by a quantitative simulation, it provides the basis for pushing this radius to the minimal level with which the accelerator physicists are comfortable.

It should be noted that since making a strong contribution to the flavour tagging performance published in the TESLA TDR, members of the LCFI collaboration have continued to take a lead in developing general purpose tools for future studies. These are about to be released to the ECFA/DESY community, and will surely enhance the interaction between the simulation and detector physicists working in this field.

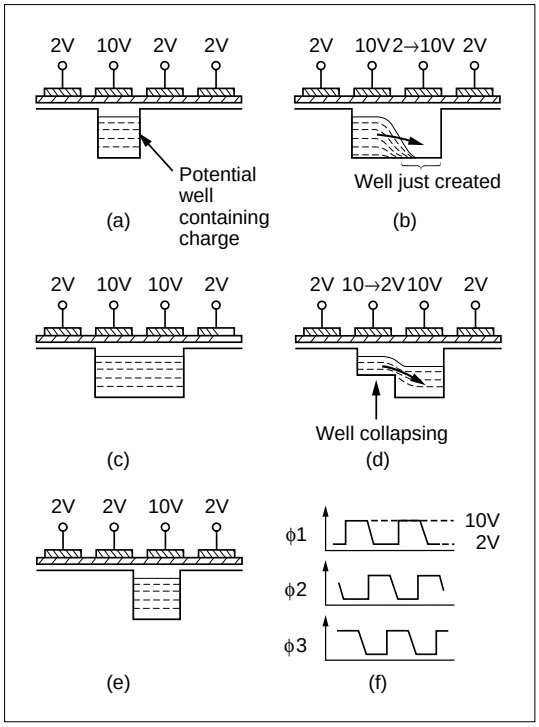


Figure 10: (a)-(e) Movements of potential well and associated charge packet by clocking of gate electrode voltages. (f) Clocking waveforms for a 3-phase CCD.

3. Advanced CCDs and electronics

3.1 Introduction and results so far

In CCD detectors used for particle tracking, the signal electrons are generally collected by a combination of drift and diffusion. The imaging area of a CCD consists of a reverse-biased structure (n^+ on a p-type substrate for an n-channel device), on which an MOS gate structure is superimposed. Figure 9 illustrates the charge collection in a typical device, consisting of a lightly doped epitaxial p layer on a heavily doped p^+ substrate, the top ~1 μm being n^+. The partial depletion of the n^+/p region creates a potential minimum for electron storage just above the n^+/p edge. Signal electrons generated within the depletion region of thickness ~5 μm drift rapidly into these storage wells. However, electrons generated in the undepleted epitaxial material diffuse till they reach the depletion edge, at which point they are rapidly collected. Those which diffuse to the p^+/p edge are reflected by the intrinsic potential barrier. The heavily doped and oxygenated p^+ bulk has a very short minority carrier lifetime, so is effectively inert. The signal is thus collected from a well-defined layer of thickness typically 20 μm .

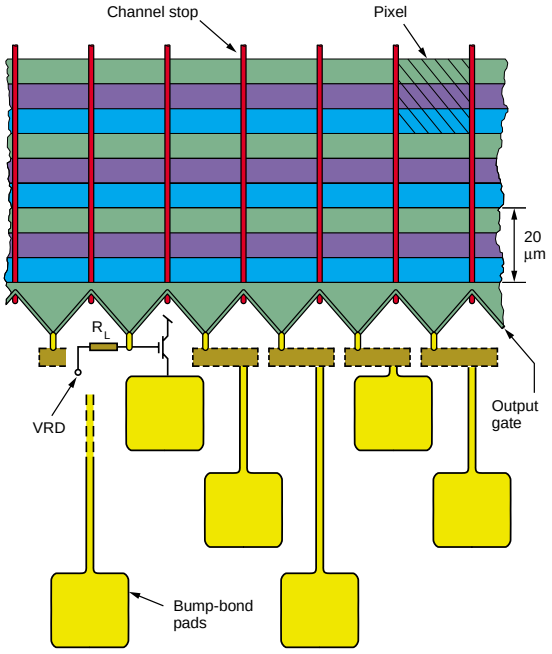


Figure 11: Edge of CPCCD in region of interface to readout chips. For one channel, the on-chip front-end circuit schematic is indicated.

The CCD surface is divided into rows and columns which define the pixel structure. Viewed face on, the 'vertical' columns consist of implanted channel stops which constrain the electrons to move in potential trenches extending over the full height of the imaging area. The rows are defined by the potential on the surface electrodes (gates) which run 'horizontally' across the width of the CCD. Figure 10 shows the movement of potential wells down the device by 1/3 pixel, in response to the changing potential of two of the gates of a 3-phase CCD.

In an alternative architecture (2-phase) the pixels are defined by only two instead of three gates, with additional 'barrier implants' to bias the stored charge to the downstream half of each gate. 2-phase devices can be driven by a pair of sinusoidal clocks running in anti-phase, which enhances the speed capability and greatly reduces the unwanted 'clock feedthrough' to the sensitive low-capacitance output nodes on which the signal charge is sensed.

In conventional CCDs, the signals from the imaging area are transferred row by row into a serial register, which typically transports the charges to readout circuits in the corners of the device. This would be far too slow for the LC application. The LCFI design concept is based on the column parallel CCD (CPCCD) in which the serial register is omitted, and

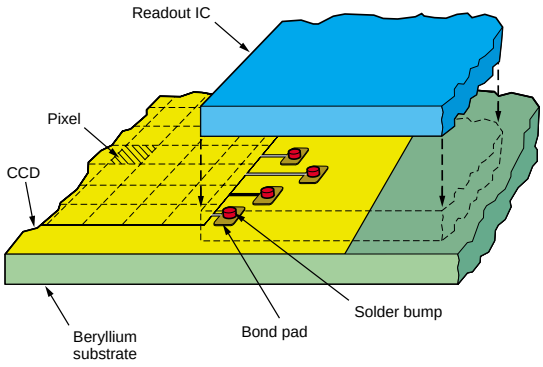


Figure 12: Exploded isometric view of the interconnect region between CPCCD and readout chip.

every column of the parallel register is connected by bump bonding to the readout IC (see Figures 4, 11 and 12). For TESLA, this multi-chip module (MCM) needs to be clocked at 50 MHz in order to achieve the necessary readout time for layer 1, as indicated in Table 1. The CPCCD architecture has other advantages which also make it our preferred design choice for NLC.

For TESLA, the fast readout will necessitate fast collection of the signal charge. The CCD must therefore be constructed using relatively high resistivity epitaxial material which can be fully depleted.

The driver chips (see Figure 4) generate the waveforms which shift the stored signals row by row down the device. The readout chip receives the analogue signals from all columns in parallel as they are shifted out of the active area to buffer amplifiers. This chip incorporates analogue-to-digital conversion, correlated double sampling to suppress reset noise in the charge-sensing circuit, data sparsification by a sequence of pixel- followed by cluster-comparators, and data storage.

The first step in the lengthy R&D programme was to establish 50 MHz clocking for a conventional CCD readout register, which already goes beyond the SLD capability by a factor of 10. The design, construction and commissioning of the custom-built specialised electronics were completed in November 2001, and within a week the test CCD (a Marconi device, model CCD 58) was running smoothly at 50 MHz, with excellent noise performance.

This 3-phase CCD was initially driven conventionally with 10 V clocks. One of the essential requirements of the LCFI R&D programme is to achieve much reduced clock voltages, ideally in the region 1-2 V. It was

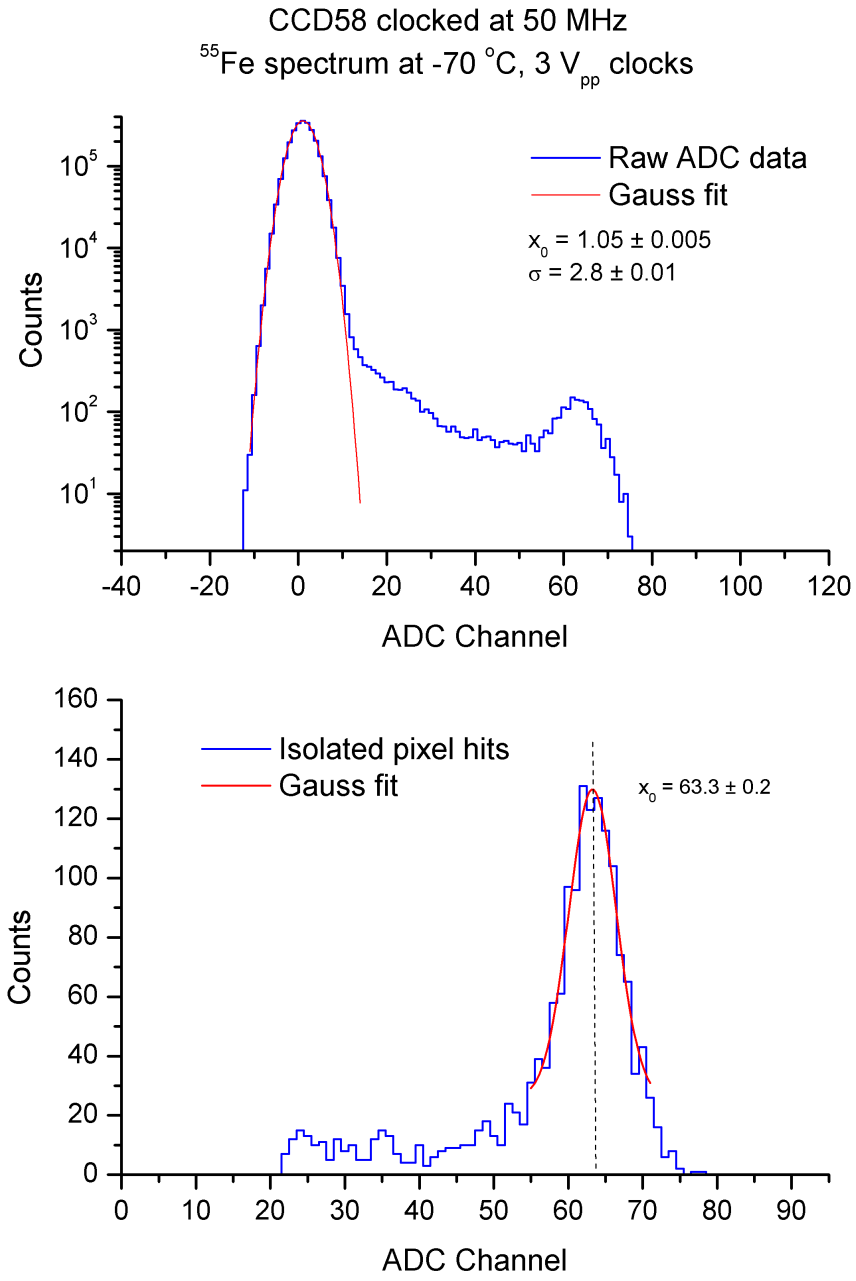


Figure 13: Spectra of 5.9 keV X-rays from ^{55}Fe source. Top plot: raw data; bottom plot: single-pixel clusters. CCD 58 at 50 MHz and 3 V clocks.

found possible to retain excellent performance (charge transfer efficiency) of the CCD 58 with 3 V clocks. ^{55}Fe data taken under these conditions are shown in Figure 13. Since the 5.9 keV X-ray signals are measured with excellent signal/noise, and are similar to the mean minimum ionising signal from 20 μm of silicon, these results establish that this detector would deliver highly efficient tracking performance. While the conditions for driving a 2-phase CPCCD are different, these recent results augur extremely well for excellent performance from these devices, as the R&D programme proceeds.

These results, obtained using equipment developed with modest PPESP support and an off-the-shelf CCD, are about at the limit of what could be achieved before embarking on a more ambitious programme involving full-custom CCDs and readout chips.

3.2 CPCCD development

Designing a large area CPCCD for 50 MHz operation is a major challenge for many reasons, partly related to the fact that the

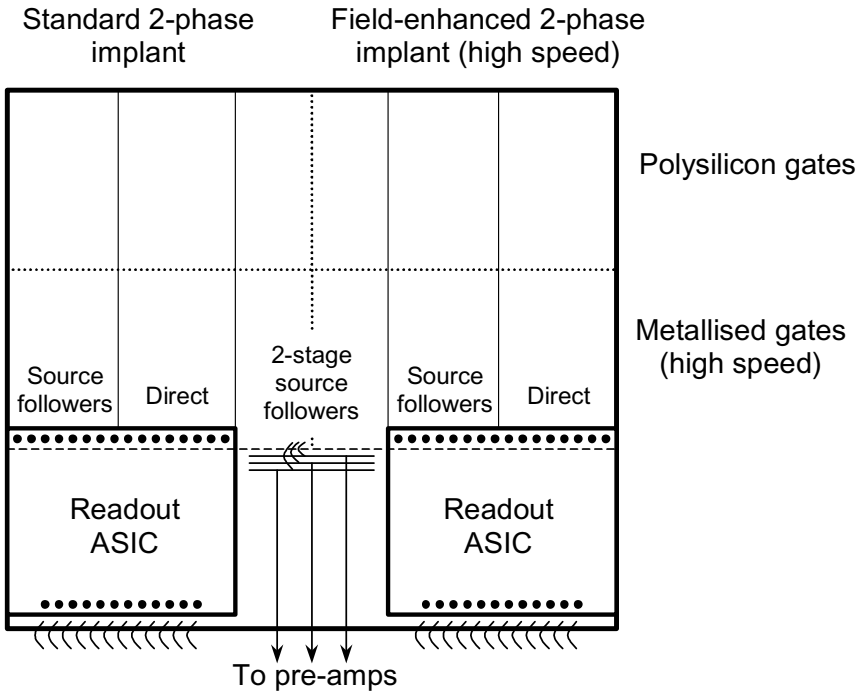


Figure 14: Layout of CPC-1 with its pair of on-board readout ICs. The matrix of regions used to explore different ideas is discussed in the text.

gate capacitances for the imaging area parallel register are orders of magnitude larger than for a serial register. Producing sufficiently uniform drive pulses over the full imaging area is itself complex. Adding the requirement of very low power dissipation (hence the need for much lower amplitude clocks) further increases the challenge.

The development of the CCDs and readout chips for this detector will require a multi-cycle R&D programme, comparable in scale and duration to that used for the LHC GPD vertex detectors. For example for CMS, their R&D programme will have spanned the period 1994 to approximately 2004, with 8 detector cycles and 12 readout chip cycles. For the LC, our estimate is 5 or 6 detector cycles and 8-12 readout chip cycles, over a 7 year period. During 2001, the PPESP made a generous allocation of 'seedcorn funding' to permit us, working with Marconi Applied Technologies (MTech), to design CPC-1, the first CPCCD in our sequence of prototypes. The design is now complete, process variations are being planned and we will be ready to go into production in April 2002.

With CPC-1 we will test different aspects of high speed operation: optimisation of buried channel and barrier implants, fast clocking of a parallel register, bump bonding, various options for the CCD/readout chip charge sensing circuitry, and low power ADCs on a pitch of 20 μm .

CPC-1 will have dimensions 15×8 mm^2 (horizontally × vertically, where the columns are considered to run in the vertical direction), hence 400 rows and 750 columns. This permits a *matrix* of regions in which different ideas can be explored, as shown in Figure 14. The following design variations have been incorporated:

Vertically, the imaging area is subdivided into a region with conventional polysilicon gates, and a second region with metal-buttressed gates designed for 50 MHz clocking. Setting this goal so early in the R&D programme may be too adventurous, in which case the standard-gate region will provide backup.

Horizontally, CPC-1 is divided into three regions. The centre region (3 mm) will allow triplets of adjacent columns to be read via wire bonding using the same design of on- and off-CCD electronics as the CCD 58. A 3-column stripe allows isolated X-ray hits in the centre column to be identified. This will provide the safest path to probe the intrinsic performance of the CP concept, even if the high density circuitry to the left or right does not operate perfectly in the first prototype.

The left-hand region (6 mm) uses a conventional barrier implant structure and

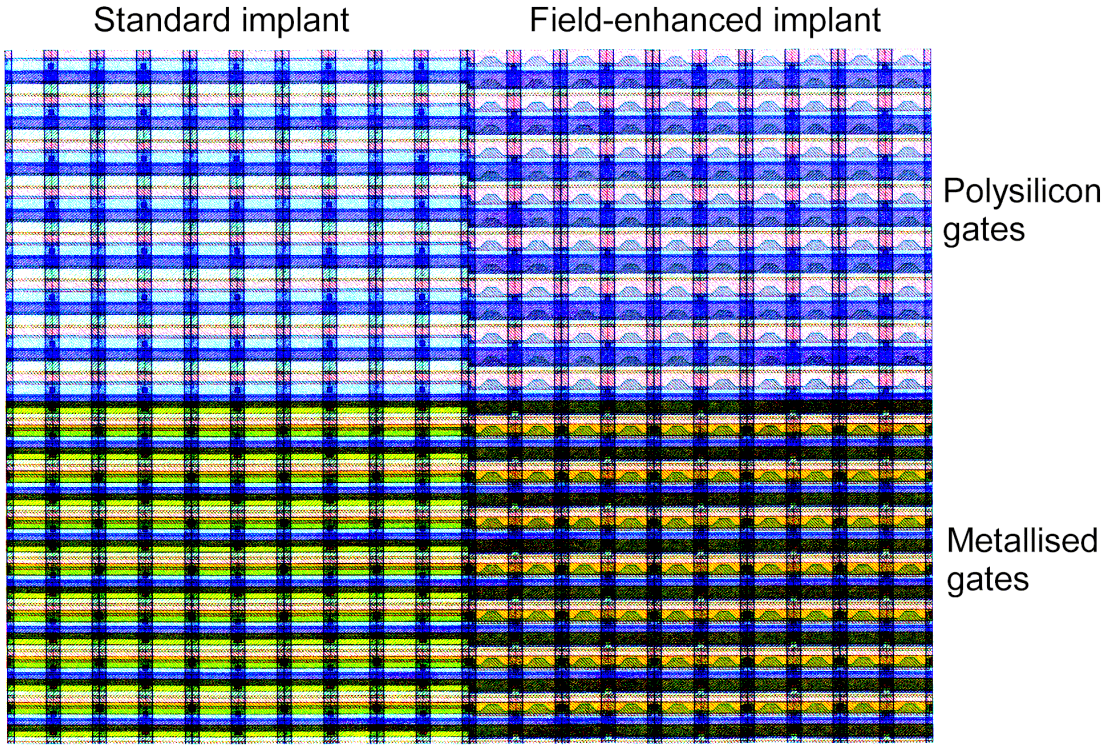


Figure 15: CPC-1: Centre of imaging area. Thick vertical bands indicate the channel stops, i.e. the column boundaries on 20 μm pitch.

bump-bond connections to the readout chip, to test the CP plus bump bond configuration, as well as the performance of the readout chip. Even this region is subdivided into two, one of which has a conventional single-stage source follower on the CCD, while the other has a more daring direct connection. If the direct connection can be made to work (which may be possible with a novel design of readout chip front-end circuit), this will be further developed in CPC-2, the second generation prototype. If it fails, we will have eliminated this idea at the earliest possible stage in the R&D programme.

The right-hand region of CPC-1 uses a 'field-enhanced' barrier implant structure designed to support very fast clocking. Beyond the imaging area, it is similar to the left-hand region, and has its own readout chip attached.

CPC-1 will thus incorporate numerous ideas for achieving enhanced performance. The ambitious goal of 50 MHz CP clocking may be possible over part of the device. Figure 15 shows the centre of the imaging area, in which four regions can be distinguished. The layout of the CCD output circuits (source followers and their active loads on a pitch of 20 μm) are shown in Figure 16 for a 4-column test structure.

A number of LCFI collaborators have worked hard along with the world-leading MTech team to develop the CPC-1 design. MTech do not have access to sophisticated 2- and 3-dimensional semiconductor device modelling tools, such as ISE-TCAD, for which an affordable academic licence was purchased by our collaboration with PPESP support in 1999. During the past year, this software has been used intensively in order to model critical features of the CPCCD design. For example, the complex equivalent circuit of L, C and R elements that make up the load seen by the clock driver circuit has been carefully simulated. This was essential in order to arrive at a design which (by the use of multiple bond wires, optimised busline layout, metal buttressing of gate electrodes and other special procedures) is expected to operate at 50 MHz. Indeed, the current ISE-TCAD simulations indicate a variation of only 30% in the clock amplitudes over the entire area of the CCD, which is quite acceptable.

Equally importantly, the potential distribution in the 2-phase structure has been simulated, as seen in Figure 17. This study will be particularly important in deciding which process variations to implement when processing the CPC-1 batch. For as well as the design variations mentioned previously, the performance of the device will be

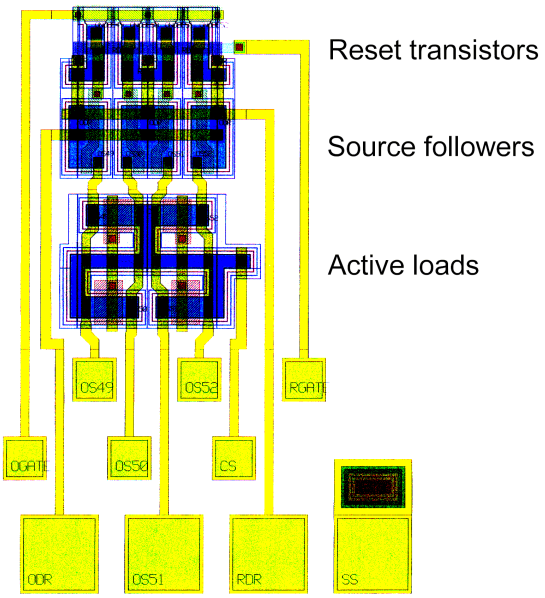


Figure 16: Test structure with 4 output circuits on 20 μm pitch. Output pads are OS49-52.

influenced by a number of critical process parameters. One of the most obvious ones is the physical depth of the buried channel (since a deeper channel will be less affected by potential pockets created by surface irregularities). Another is the dopant concentration in the barrier implant; lowering this may enable the CCD to be operated with reduced amplitude clocks.

3.3 Readout integrated circuit

While the CPCCD concept has advanced in an intensive 6-month design phase, the first prototype readout chip has also been a major challenge. Here the credit for the work goes primarily to the RAL Microelectronics Design Group.

The current thinking for the readout chip is indicated in the block diagram in Figure 18. The signals from each column of the CCD are amplified and digitised. The voltage on the CCD output node is returned to its nominal 'reset' value only at the end of a bunch train. During the train, each signal charge clocked onto the node causes a step in this voltage. In the readout chip, the digitised signals form an irregular staircase with steps at 20 ns intervals. By taking differences between successive signals and applying a threshold, pixel signals above the noise level are sensed. These signals trigger the evaluation of a cluster signal based on $N \times N$ pixels (usually 2×2 or 3×3) including the triggering pixel. Data from above-threshold clusters are stored along

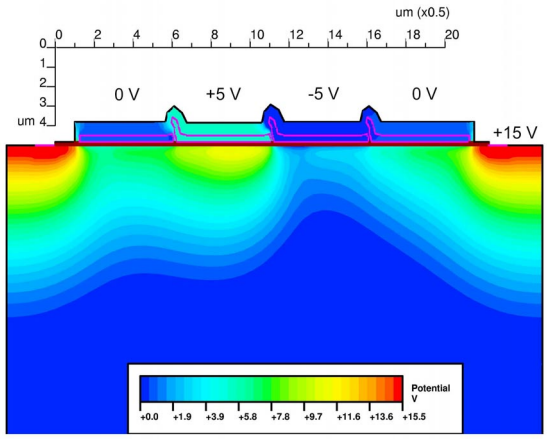


Figure 17: Potential distribution in a 2-phase test structure. With the gate potentials indicated, charge storage is under the second gate from the left.

with address information. The memories are read out at leisure during the period between bunch trains.

For testing CPC-1 we need a much simpler readout chip to be able to make thorough tests of the CCD and chip functionality. It will contain a front-end amplifier (gain about 10) and ADC followed by storage of raw data in memory. Data from individual frames will be read out and the further processing carried out offline, enabling any possible anomalies and malfunctions (saturation, crosstalk, timing jitter, overload recovery etc) to be studied all the way down to the noise floor of the system. The design of this initial readout chip, called CPR-1, is now nearing completion. Implemented in a 0.25 μm CMOS process, it is a mixture of a full-custom design followed by cell-based digital logic.

The challenge of detecting the very small signals from minimum ionising particles (~1 mV) is exacerbated by feedthrough to the output node from the CCD clocks. Elaborate precautions have been taken in the CCD design to minimise this. However, simulations of these effects are difficult, and results from testing the CPC-1/CPR-1 combination are eagerly awaited.

Beyond the front-end amplifier, the major challenge of the readout chip has been to devise an ADC system on 20 μm pitch having sufficient rate capability, yet operating with sufficiently low power. It has been possible to design 5-bit flash converters in which charge transfer amplifiers are used to achieve the required performance. As an example, the layout from the output of the front-end

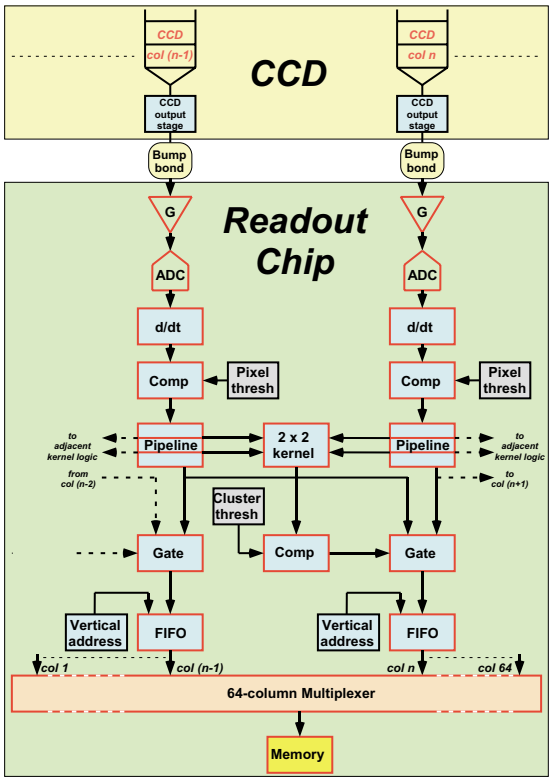


Figure 18: Preliminary logic of readout integrated circuit configured for 2 x 2 pixel cluster selection.

amplifier through one charge transfer amplifier, comparator and encoder element is shown in Figure 19. These structures are repeated 31 times for each channel, to produce the 5-bit ADC.

In CPR-1 the digitised signals are read synchronously into an on-chip memory. A frame deposited into this memory can then be read out to the VME by a conventional multiplexed architecture.

3.4 *Bump bonding*

There are two possible variants of the CCD-readout chip assembly. In the simpler of these, CPR-1 is mounted face up next to CPC-1, and connections are made by wire bonding to every third column (the minimal pitch for convenient wire bonding). In the second variant, shown in Figure 14, the CCD is diced 7 mm beyond the edge of the imaging area, and the readout chip is bump bonded face down on the CCD, this time contacting all bond-pads on the 20 μm column pitch.

As a result of extensive discussions with the bump-bonding company (VTT in Finland) is has become possible to devise a production plan which conforms precisely to their design rules and processing procedures. It seems

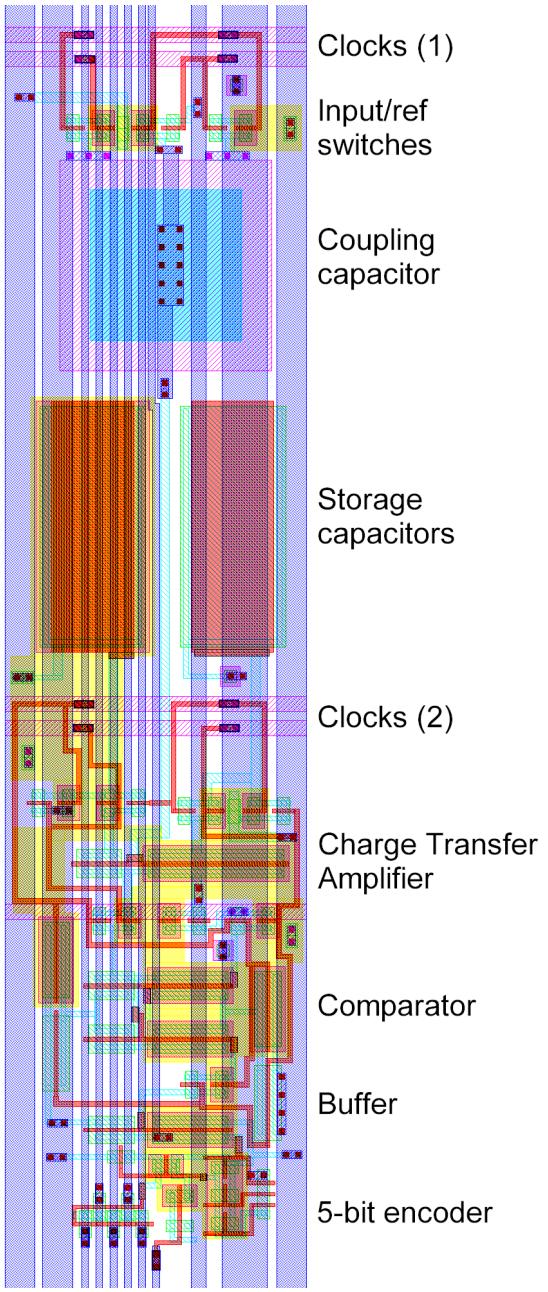


Figure 19: Section of one channel of readout circuit of width 20 μm and height 85 μm , showing the start of the digitiser. This section is repeated 31 times for each digit of 5 bits. Front-end analogue circuit is not shown.

probable that bad experience with bump bonding in some scientific applications is attributable to the use of non-standard procedures, so there is every reason to expect the MCMs produced for this vertex detector programme to be robust and reliable. The procedures to be followed will exactly match those used for industrial flip-chip processing.

The manufacturing procedure will be as follows. Processed CPC and CPR wafers will be sent directly from their production clean-rooms to those at VTT, who will apply the

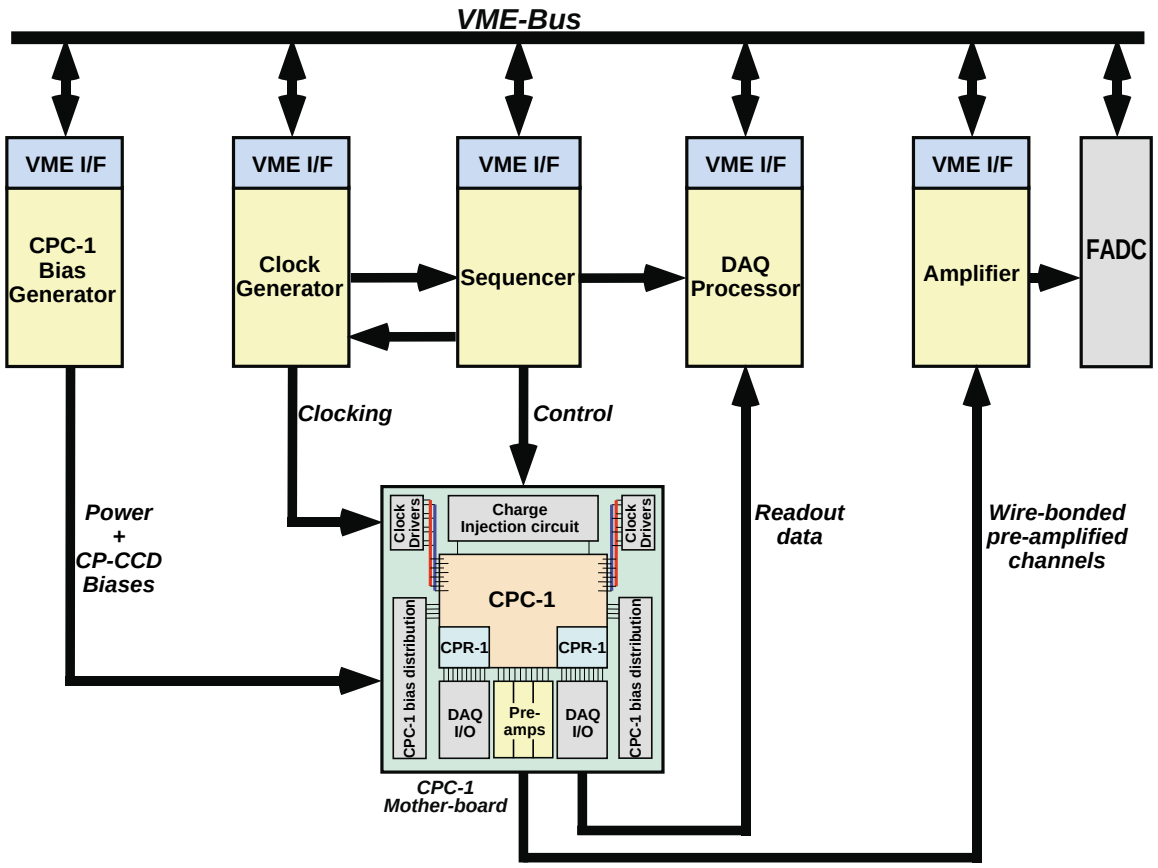


Figure 20: Electronics beyond the multi-chip module consisting of the CCD and readout IC, for evaluation of CPC-1 prototypes.

under-bump metallisation and solder bumps to both. VTT will then dice the wafers, and follow their standard procedures for bump bonding. Mechanical stabilisation and thermal contact will be enhanced by additional bump bonds at the back end of the readout chip. The resultant MCM consisting of one CCD and two readout chips can then be handled like any IC, attached to a chip carrier (in this case the CCD motherboard) and wire bonded. Given VTT's facilities, there will be no problem in eventually extending these procedures to full-sized ladder assemblies.

3.5 System electronics

The block diagram of the system electronics for the CPC-1 evaluation is shown in Figure 20. The motherboard contains a well of depth 0.6 mm in which the CCD is seated, having its surface flush with the motherboard. The bias connections are made by conventional wire bonds. The connections from the balanced 2-phase sinusoidal clock drivers on the motherboard to low-inductance buslines, and then to the corresponding buslines on the CCD, are made by multiple short (0.5 mm) wire bonds. These compact circuits have sufficiently low inductance that they will drive the CCD at 50 MHz, mirroring the layout envisaged eventually for the real ladders (Figure 4). A selected group of three adjacent columns from the central 3 mm of CPC-1 can be connected to preamps on the motherboard by wire bonding, providing a replica of the CCD-58 output circuit for the first level exploration of the system operation.

The two CPR-1 readout chips are shown in Figure 20 in the bump-bonded configuration. For the initial wire-bonded assemblies, the CCD is diced close to its output bond pads, and the readout chips are seated face up in the same well as the CCD. Wire bond connections are made between the CCD and the readout chips, and from the back-end of the readout chips to the motherboard.

In addition to the motherboard, the system electronics comprises 5 special purpose VME modules plus the commercial FADC unit used for the CCD 58 evaluation. All the special purpose electronics is being designed and manufactured by the Oxford University Physics Department Electronics Group. In

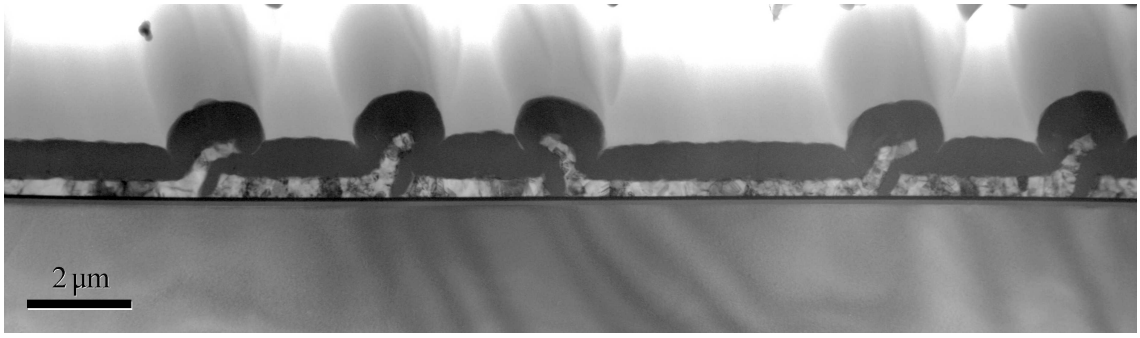


Figure 21: Scanning electron microscope photograph of cross-section of 3-phase CCD, indicating the considerable overlap in imaging gates. It may be possible to reduce these overlaps while retaining acceptable performance for particle tracking.

addition, they are simulating and making a model of CPC-1 (lumped array of capacitors, inductors and resistors) in order to investigate the integrity of the clock drive pulses over the full area of the device.

3.6 Test programme for electronics and detectors

The test structure for part of the readout chip will be submitted via CERN to an IBM multiproject run in April, and (if given PPRP approval) the full CPR-1 design will be submitted in August. These chips will initially be tested in the RAL Microelectronics Design Group. The system electronics will be commissioned at Oxford and RAL.

If approval is given for MTech to start work on the CPCCD production in April, the CPC-1 devices will be due for delivery in October. By that time, all the infrastructure and external electronics will have been thoroughly tested, including thermal issues such as power dissipation and temperature variation on the motherboard. The CCDs will therefore be installed in a well understood environment of cryogenic and electrical services, based on the powerful infrastructure built up to study the CCD 58 devices. Evaluating the assemblies of CPC-1 and CPR-1 in their various configurations will require an extensive test programme. We plan to borrow time on an existing picoprobe station owned by the RAL ATLAS group as well as using conventional test equipment in Oxford and RAL. We have recruited an excellent 1-year 'sandwich' student, and a graduate student may also join us in these pioneering studies. While one or two wafers are being bump bonded at VTT, wire-bonded assemblies will be under test in Oxford and RAL. Before the end of 2002, we hope to have first results from the bump-bonded assemblies.

3.7 R&D programme beyond CPC-1

As discussed previously, we anticipate 5 or 6 generations of prototype CCDs in order to establish the conceptual design for the linear collider detector. In this funding request, as in our submission to SCP4, we assume these cycles to proceed at 15 month intervals. If funds for the first three years are insufficient, we may be obliged to proceed more slowly, hoping to catch up later.

As in any complex R&D programme, the plans for each generation will depend on the outcome of the previous one. However, we already have a list of promising features to be considered for CPC-2. These include:

- reduced inter-gate capacitance via a more planar 2-phase gate structure. The present structure, optimised for extremely high charge transfer efficiency, is shown in Figure 21;
- reduced clock amplitudes, replacing the barrier implant by variable thickness dielectric or other new ideas;
- baseline restoration of the CCD node via a servo system feeding back from the readout chip to the reset FET, operating in the subthreshold regime;
- more adventurous open-phase shaped electrodes for reduced inter-gate capacitance (invented by SONY [8]), leading to lower power dissipation and relaxed driver design.

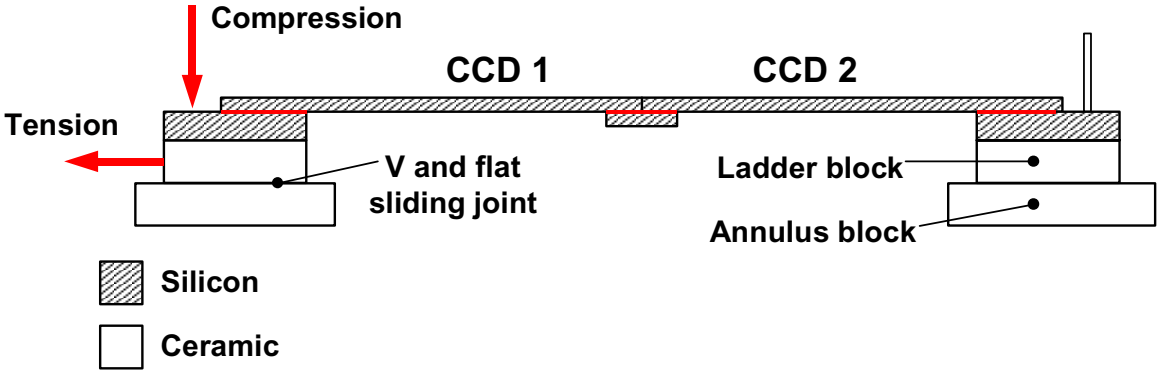


Figure 22: Unsupported 2-CCD assembly. The adhesive bonds from the membrane-like CCDs are all made to silicon, to minimise differential contraction effects.

All these ideas will be reviewed in the light of experience with CPC-1.

As with the CCDs, the readout chips will evolve over a number of generations. Since they are more affordable, and are available with a more rapid processing schedule, there will be more generations of these devices than of the CCDs. This also conforms to general experience (eg the ATLAS and CMS vertex detectors). For planning purposes, we have assumed that readout chip cycles move forward at twice the rate of CCD cycles.

It should also be noted that these developments will have a lot to offer other areas of science. We are maintaining a dialogue with the synchrotron radiation community, who may decide to prepare a proposal for funding. If they were successful, we would pool our ideas and thereby aim to slightly accelerate the R&D cycles. However, in first approximation they need to pursue a different optimisation path (larger signals, greater dynamic range, lower frequency). Their requirements for CCDs and readout chips would be significantly different from ours, so the potential for accelerating the LCFI programme would be modest.

4 Mechanics and Cryogenics

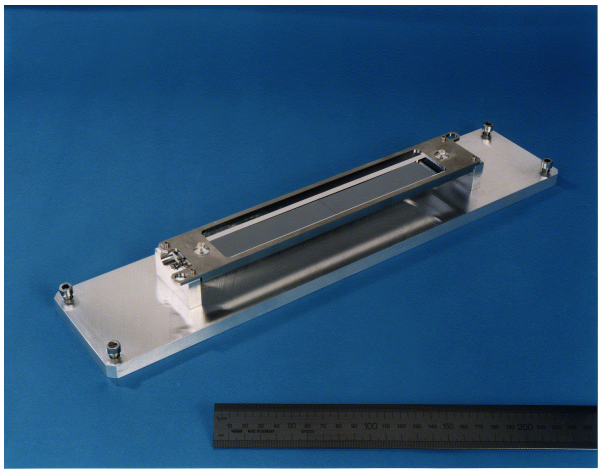
4.1 Introduction and results so far

It has been clear for several years that the physics requirements for the multi-jet TeV regime in general, and the measurement of vertex charge and dipole charge in particular, depend on reducing the layer thickness well below the figure of 0.4% X_0 achieved for the SLD detector (which was already a record). As well as thin layers in the fiducial volume, it is also important to minimise the material at the ends of the ladders beyond the region of precise tracking, in order to degrade as little as possible the tracking and calorimetric measurement of small angle jets. These goals for minimal material are complicated by the requirement of mechanical stability at the micron level.

Our current ideas for thinning the ladders fall into three categories, supported, semi-supported and unsupported silicon. In the supported option, the silicon is thinned as much as possible, typically to the edge of the epitaxial layer, hence removing all except the material used for the charge collection. The resultant fragile die (of thickness typically 20 μm) is adhesive bonded to a rigid substrate (eg a beryllium frame of shallow triangular cross-section). In the semi-supported option, the substrate is not thick enough to be completely self-supporting, but gains mechanical stability by being tensioned in the overall support shell of the vertex detector. In the unsupported option, the silicon is thinned less dramatically (say to 60 μm) and this flexible membrane is stabilised simply by being tensioned as shown in Figure 22.

Since the CCD-based vertex detector is operated at a temperature of around 180 K, differential contraction effects are very important for all three options.

Making these mechanical engineering models is fortunately relatively inexpensive, so it is possible to pursue numerous ideas. Furthermore, many suggestions are amenable to FEA simulations, and we have learned a good deal from the Oxford University Physics Department Mechanical Design Office, which has applied its expertise to the problem, and will continue with these studies in the future.



(a)

(b)

Figure 23: (a) Photograph of mechanical prototype of a 2-CCD silicon ladder of thickness 60 μm and length 25 cm, with (b) details of the spring tensioning system at one end.

These studies are also relevant to LC vertex detector technologies other than CCDs, provided that the in-detector power dissipation is small. High power dissipation would necessitate a robust and hence massive cooling system, as for example for hybrid pixel detectors of the type used for LHC. Such systems should be avoided if possible because they would degrade the measurement of low momentum tracks, and hence of physics performance.

The idea explored most thoroughly to date has been that of the unsupported silicon held under tension. For layer 1, the CCD is attached to ladder blocks at each end. For the outer layers, the two CCDs are joined end-to-end by a thin silicon bridge. The unsupported silicon option leads to a layer thickness of about $0.06\%\ X_0$, resulting in a very favourable multiple scattering term in the impact parameter formula.

In the first tests of this option, 2-CCD mechanical prototypes were assembled with unprocessed silicon sheets of dimensions 125×20 mm, and of thickness 60 μm, as seen in Figure 23. The assembly was clamped to a coordinate measuring machine (CMM) and the sagitta measured. This measurement was repeated 100 times, releasing the spring tension so the ladder sagged visibly between each measurement. The standard deviation on the sagitta plotted in Figure 24 indicates that for a spring tension above 150 g the mechanical stability at the centre of the ladder is better than 3 μm.

This result, while extremely encouraging, is only the first step. Tensioning is good for longitudinal stabilisation, but the processed CCDs tend to curl across their width, which is difficult to control. In short, a membrane is more complex than a wire, and achieving micron stability over the full surface may be challenging. Studies using CCD-processed silicon show complex behaviour. The SLD CCDs when thinned by mechanical grinding were concave, with curvature that increased rapidly as the thickness was reduced. However, devices from MTech thinned by chemical etching show relatively modest curvature and are convex. It is hypothesised that the dominant stress in the SLD devices was due to the crystal damage layer on the back face, while the shape of the etched CCDs is driven by front-surface processing. However, this all needs much more study.

4.2 Future R&D programme

Further studies of the unsupported option are needed:

- measurement of the transverse curling
- practicality of handling these delicate structure for bump bonding and detector assembly
- susceptibility to vibration, depending on the actual power dissipation and the gas flow rate needed for cooling.

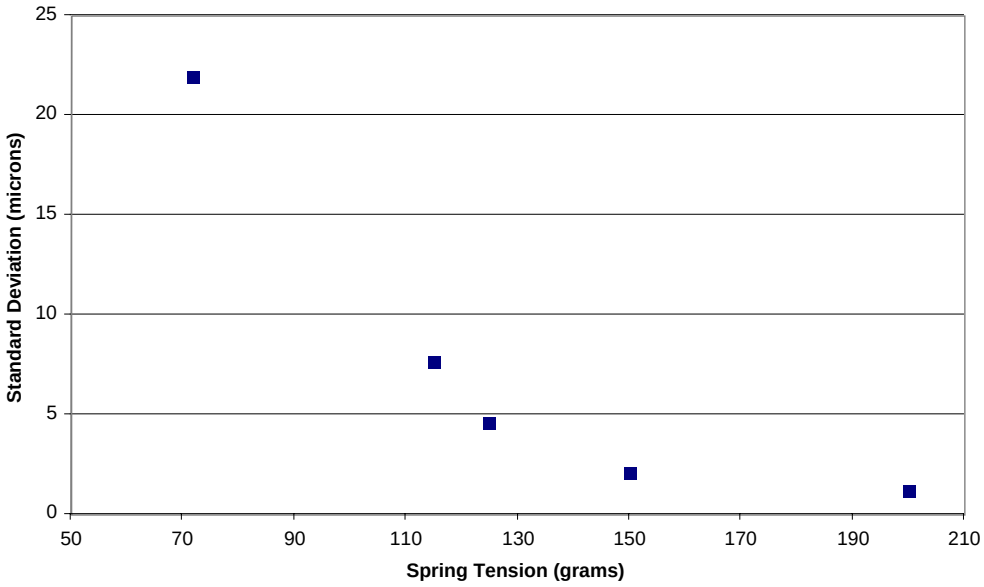


Figure 24: Sagitta stability as function of tension applied to the unsupported silicon.

The semi-supported option is also appealing for several reasons, despite being somewhat thicker in radiation lengths:

- As in SLD, an assembly of thin silicon attached to a strong substrate is a robust component that can be handled conventionally.
- The 2-CCD assemblies for layers 2-5 are as easily constructed as the 1-CCD assembly for layer 1. This is not the case for the unsupported option.
- These assemblies are compatible with the handling and processing procedures used in bump bonding. For the unsupported option, special procedures would be obligatory.
- Stability across the ladder width would be assured by the substrate. The only requirement of tensioning would be to provide longitudinal stability, for which it has already proved its effectiveness.

The main issues here are the selection of substrate material and adhesive, both areas in which MTech have wide experience and are offering valuable advice. The substrate preferred at first sight (due to its radiation length and stiffness) is beryllium. However, it has a significant expansion coefficient mismatch to silicon over the temperature range. For this reason, it may need to be thicker than one would like. MTech has recently suggested silicon carbide, the CVD form of which has a good thermal match to silicon and may therefore allow a lower thickness in radiation lengths.

This programme depends on considerations of numerous parameters, many of which need further investigation. Since time is on our side, there is every reason to expect eventually to surpass the SLD thickness of 0.4% X_0. However, this will necessarily be linked to the rest of the R&D programme, since the power dissipation in the fiducial volume and at the ladder ends are by no means known, and could have a decisive influence on the thermal and mechanical design of this detector.

5. Radiation effects

Due to the e^+e^- pair background, the vertex detector will see ~ 40 krads/year of ionising radiation on its innermost layer. The neutron background which leaks through the shielding from remote dumps is expected to be approximately $10^8 - 10^9$ 1 MeV-equivalent neutrons per year at the vertex detector.

The most serious effect of both these types of radiation on large area CCDs is loss of charge transfer efficiency (CTE). Signal is lost due to trapping in radiation-induced defects in the silicon. Early data on neutron irradiation were inconsistent, but recent careful studies by Stefanov [9] have shown qualitatively similar temperature dependence of the CTE for both neutrons and ionising radiation. The CTE improves dramatically as the temperature is reduced to ~ 180 K, due to the emission times for the relevant traps

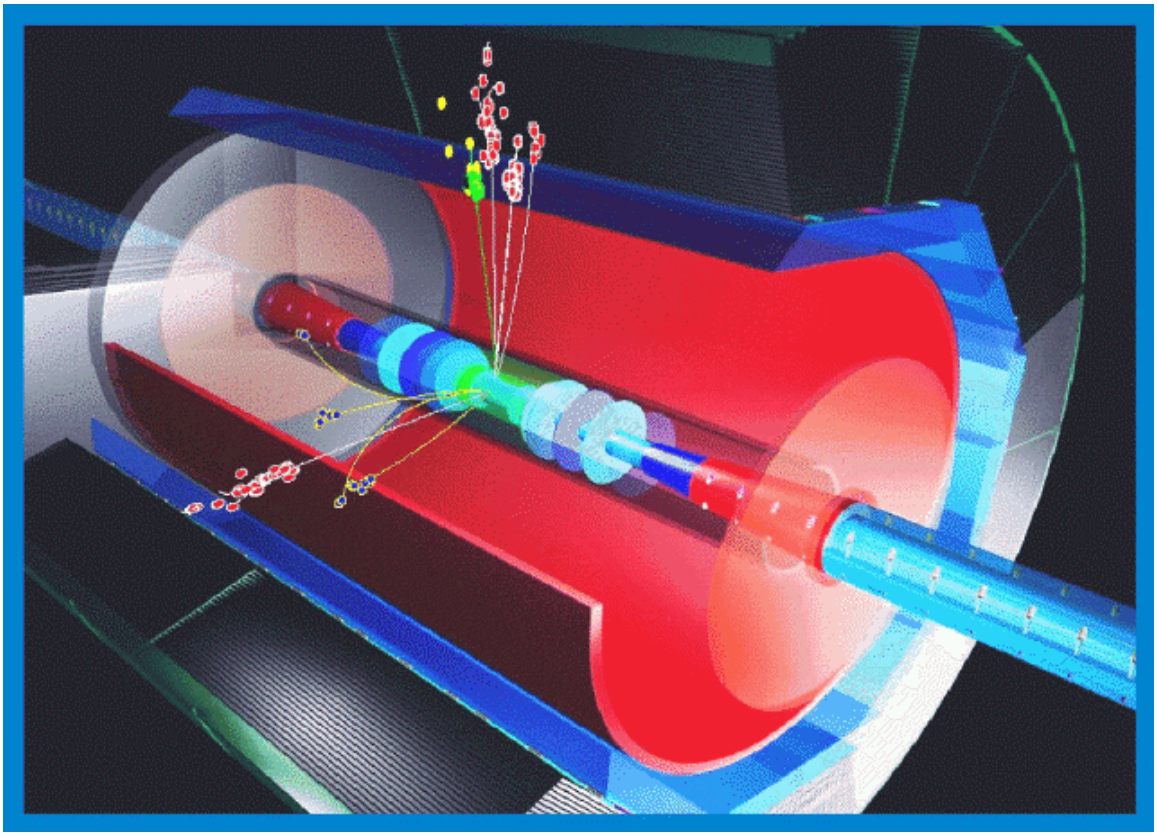


Figure 25: Heart of the TESLA TDR detector. Convenient access to the vertex detector, particularly for upgrades, is incorporated into the design.

becoming so long that they remain almost permanently filled. For this reason, a CCD-based vertex detector operated at approximately this temperature can be expected to be robust with respect to the fluences noted above.

However, there are many parameters involved, for example the particle hit density, the readout speed, and the volume of the storage wells. The radiation effects in each generation of CPCCD prototype will be measured over a wide range of temperature and other operating conditions. If other things are equal, a CPCCD clocked rapidly can be expected to have much higher radiation hardness than conventional CCDs, since the time available for traps to emit their electrons is greatly reduced.

The study of radiation effects in CCDs has received far less attention than for example in microstrip detectors. It will be important to build up a comprehensive understanding of these effects, and there is a possibility of international experts at CERN joining in these studies. Such studies will also be of great value to astronomers, since radiation damage in space-based instruments, particularly from slow protons, can be a serious problem. The test facilities at RAL and Liverpool University are suitable for studying this subject, and will be used initially to characterise radiation effects in the CCD 58 devices now being tested.

6. Conclusions

Progress towards the future linear collider is advancing rapidly. A huge investment in various options for the accelerator design is coming to fruition, with a technical selection foreseen during 2004. The International LC Steering Group is now being formed under the guidance of ICFA. This should be the vehicle to secure agreement for the project and bring into being the Global Accelerator Network (GAN) to build and operate the machine. The current best estimate for first physics is around 2014.

It is essential that the relatively inexpensive detector R&D should keep pace with the overall project. To this end, an international LC detector coordination group has been formed with three representatives from each region, chaired by Rolf Heuer and including Settles and Damerell from Europe. The most challenging detector topics are the vertex detector and the calorimeter.

The LCFI collaboration has grown into probably the strongest group in the world engaged in the LC vertex detector development. The work builds on the SLD experience plus studies since the first linear collider physics and experiments workshop in 1991. Since its inception in 1998, the collaboration has built up its manpower, expertise and infrastructure, and established a strong track record (the physics studies, CCD 58 and thin ladder experimental results). This powerful unit is now well-matched to the necessary R&D programme. Ongoing studies have confirmed that a CCD-based vertex detector growing out of the SLD experience remains the most likely option to satisfy the physics requirements.

We envisage 5 or 6 generations of prototype detector in order to prove the design concept. On the present planning, with 15 month cycles, CPC-5 will be completed in 2007-2008. The prototype ladder constructed with full-scale CCDs will be completed by 2010. Its performance will be compared with other options that may also have evolved to this point (MAPS, DEPFET, HAPS,…). By this time, one or two LC 'General Purpose Detector' collaborations will have formed (analogous to ATLAS and CMS) and they will select the vertex detectors for their physics programmes. Based on the SLD experience, the construction of a 1 Gpixel detector could be completed in two and a half years, starting at the beginning of 2011 and being completed in mid 2013, allowing a short time for installation on the LC beamline and commissioning before the startup of physics in 2014.

It is quite possible that the two GPD collaborations will choose to back different vertex detector technologies. It is also possible that they will choose one technology for startup and upgrade to a superior one later. This happened at SLC, where Mark II used silicon microstrips since a CCD detector could not be built on their timescale. With this in mind, the TESLA detector (Figure 25) has been designed to provide convenient access to the vertex detector for repairs or upgrades. During the LC physics programme, it is certain that the collaborations will upgrade their vertex detectors in line with technological advances (as happened at SLD). The need for access is also being incorporated into the design of the NLC detector.

Since a CCD-based detector is widely considered to be the front-running option for the vertex detector at the future LC, not to pursue it would be unthinkable. We are fortunate in having a powerful combination of intellectual leadership from the academic and industrial communities, in driving this project forward. Furthermore, in pursuing this option, the LCFI collaboration is working at the leading edge of the global R&D programme. The physics studies and development of thin ladders are relevant to all technologies now under consideration. The development of innovative silicon pixel sensors and readout ICs with massive data sparsification capability, is again relevant to all future Gigapixel systems, to be read out through a few optical fibres. The LCFI collaboration is therefore stretching the capabilities of experienced physicists and engineers in directions which focus on this wonderful future tool for physics. We envisage a 'no-lose' scenario for those pursuing all silicon pixel options, in which everyone involved can look forward to playing a major part in the 'Global Detector Network' and thereby leading the way to physics at the TeV-scale collider.

There is increasing optimism that the UK will become a significant participant in the Global Accelerator Network to construct this new machine, which will greatly benefit the academic accelerator community and our national industry. The LCFI collaboration is sustaining and developing one of the physics communities which will justify this accelerator work. Having constructed one of the new vertex detectors, we expect to be in the forefront of extracting the new physics. Working in close collaboration with our LHC colleagues, we will explore the TeV energy frontier together, confident of answering some of the most pressing open questions in particle physics.

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[9] K.D. Stefanov PhD thesis, Saga University, Japan (2001), available from the LCFI web page.

Appendix A: Collaboration publications since October 1998

Ideas for a Vertex Detector at the Future e^+e^- Linear Collider.
CJS Damerell for the LCFI Collaboration.
Nucl Instr and Methods **A435** (1999) 16.

A TESLA-Compatible Vertex Detector Design.
T Greenshaw, for the LCFI Collaboration.
Physics and Experiments with Future Linear e^+e^- Colliders.
University of Barcelona publication (2000) 901.

A CCD Vertex Detector for a High Energy Linear e^+e^- Collider.
P Burrows, for the LCFI Collaboration.
Nucl Instr and Methods **A447** (2000) 194.

A Fast CCD Vertex Detector for the Future Linear Collider: Some Recent Developments.
A Gillman for the LCFI Collaboration.
Vertex 2000 Conference, Michigan 2000.
Nucl Instr and Methods **A473** (2001) 86.

A CCD Vertex Detector for the future Linear Collider.
T Greenshaw for the LCFI Collaboration.
Proc IEEE 2000 Conference, Lyon (2000). CD-ROM. Saclay 2001.

A CCD Vertex Detector for the future Linear Collider.
CJS Damerell for the LCFI Collaboration.
Physics and Experiments with Future Linear e^+e^- Collider.
AIP Conference Proceedings (2001) 782.

Flavour tagging studies for the future Linear Collider.
S Xella Hansen et al.
Physics and Experiments with Future Linear e^+e^- Collider.
AIP Conference Proceedings (2001) 799.

A CCD-based vertex detector for TESLA.
CJS Damerell for the LCFI Collaboration.
LC-DET-2001-023 DESY Linear Collider Note (2001).

Flavour tagging studies for the TESLA linear collider.
S Xella Hansen et al.
LC-PHSM-2001-024 DESY Linear Collider Note (2001).

Linear collider flavour identification.
S Xella Hansen.
Snowmass 2001 (to be published).

R&D for a CCD vertex detector for the high energy linear e^+e^- collider
PN Burrows.
Snowmass 2001 (to be published) and hep-ex/0112035.

Flavour tagging at FLC.
S Xella Hansen.
Vertex 2001 workshop (to be published).

Pixel vertex algorithms.
N de Groot.
Vertex 2001 workshop (to be published).

Summary talk.
CJS Damerell.
Vertex 2001 workshop (to be published).

Appendix B: Conference talks since October 1998

Ideas for a Vertex Detector at the Future e^+e^- Linear Collider.
CJS Damerell, Vertex 98 Workshop, Santorini, Greece

A TESLA-Compatible Vertex Detector Design.
T Greenshaw, LCWS 99 Workshop, Sitges, Spain

A CCD Vertex Detector for a High Energy Linear e^+e^- Collider.
P Burrows, Vertex 99 Workshop, Texel, Netherlands

A Fast CCD Vertex Detector for the Future Linear Collider: Some Recent Developments.
A Gillman, Vertex 2000 Workshop, Michigan, USA

A CCD Vertex Detector for the future Linear Collider.
T Greenshaw, IEEE 2000 conference, Lyon, France

A CCD Vertex Detector for the future Linear Collider.
CJS Damerell, LCWS 2000 conference, FNAL, Batavia, USA

Flavour tagging studies for the future Linear Collider.
S Xella Hansen, LCWS 2000 conference, FNAL, Batavia, USA

Silicon detectors for high energy physics.
CJS Damerell, Detector Workshop for the SR Community, March 2001, Manchester

Flavour tagging studies for the TESLA Linear Collider.
S Xella Hansen, IOP HEP Conference, April 2001, Southampton

CCD vertex detector for future Linear Collider.
E Johnson, IOP HEP Conference, April 2001, Southampton

Linear Collider detector concepts.
CJS Damerell
Snowmass particle physics workshop, July 2001, Snowmass, Colorado

Linear Collider Flavour Identification.
S Xella Hansen
Snowmass particle physics workshop, July 2001, Snowmass Colorado

R&D for a CCD vertex detector for the high energy linear e^+e^- collider
PN Burrows
Snowmass particle physics workshop, July 2001, Snowmass Colorado

CCD detector R&D – LCFI collaboration.
PN Burrows
ECFA/DESY LC workshop, September 2001, Krakow, Poland

Flavour ID studies of LCFI collaboration.
M Wing
ECFA/DESY LC workshop, September 2001, Krakow, Poland

Vertex detector: working group report
CJS Damerell
ECFA/DESY LC workshop, September 2001, Krakow, Poland

Flavour tagging at FLC.
S Xella Hansen
Vertex 2001 workshop, September 2001, Brunnen, Switzerland

Pixel vertex algorithms.
N de Groot
Vertex 2001 workshop, September 2001, Brunnen, Switzerland

CCD vertex detectors.
K Stefanov
Vertex 2001 workshop, September 2001, Brunnen, Switzerland

Summary talk.
CJS Damerell
Vertex 2001 workshop, September 2001, Brunnen, Switzerland

LCFI status report.
CJS Damerell
LCUK meeting, October 2001, Daresbury Laboratory

New ideas for CCDs.
CJS Damerell
RHIC detector workshop, November 2001, Brookhaven National Laboratory

A CCD vertex detector for the future TeV-scale e^+e^- linear collider.
CJS Damerell
Workshop on radiation hard semiconductor devices, November 2001, CERN

A CCD-based vertex detector for the future linear collider; LCFI status report.
CJS Damerell
North American LC workshop, January 2002, Chicago, Illinois

Appendix G: Project Management

The LCFI project management will continue along the lines that have been in place since 1999, and is based on proven procedures over the past 20 years.

At the level of geographical groupings, arrangements are variable according to the number of participants and the nature of their responsibilities. For the Bristol/Oxford/RAL group (soon to be joined by QMUL) there are weekly group meetings, with minutes issued normally within 24 hours. This is an effective way of providing local project leadership and of ensuring that everyone is engaged in solving the critical problems.

The overall LCFI collaboration holds monthly meetings in the form of conference phone calls, with visual information (plots and photographs as well as text and calculations) made available from our web site. People phone in to these meetings from wherever they are; we have had participants from as far as Krakow to the east and SLAC to the west. Again, minutes of these meetings are normally issued within 24 hours. The short term strategy and milestones are embedded in the meetings notes, and are constantly updated in the light of progress and new ideas.

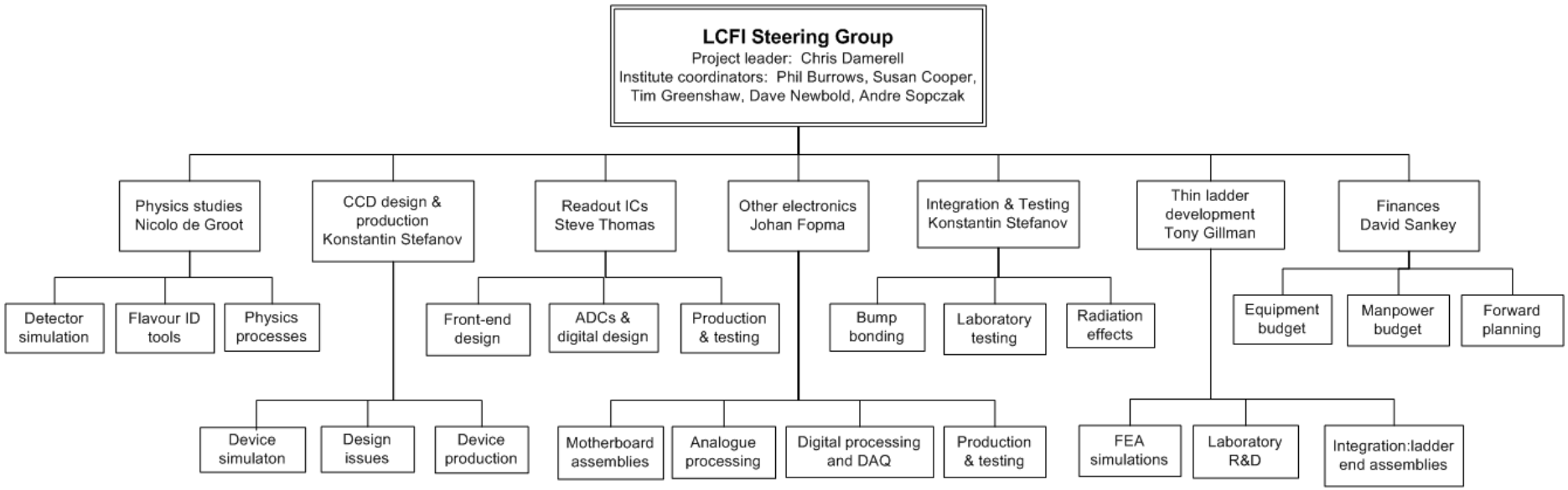
MoUs with institutional responsibility will become relevant at the full detector construction stage, as was done with the SLC vertex detector. During the R&D programme (which took 6 years for SLD) a flexible allocation of work is essential. Ours is a responsive R&D project, in which opportunities for new sub-projects frequently present themselves.

A vital component of our project management relies on excellent information exchange with the other LC vertex detector collaborations. In this regard, specialist parallel sessions at the regional LC physics and detector workshops in Asia, the USA and Europe are particularly useful.

It is essential to have a project leader dedicated 100% to LCFI, and this has been in place since October 2001, soon after we were granted a major budget. Without this, one could not guarantee responsible management of such a diverse and fast-moving programme.

The organogram on the next page indicates the internal structure of the project management, and on the following page there is a description of the Project Management Committee which will from now on provide external monitoring and guidance, at 6-monthly intervals.

LCFI Internal Project Management



LCFI

Interim Project Management Committee

Membership:

Director, Particle Physics CLRC (Chair)
UK Spokesperson
1 Representative from each of the UK groups
Project Engineer (microelectronics)
Secretary
Head of Particle Physics Division PPARC (ex officio)

Marconi Applied Technologies will be invited to send an observer.

Terms of Reference

1. To oversee the project.

2. To review progress against agreed milestones, financial estimates and timescales.

3. To receive technical reports from the UK collaboration.

4. To prepare financial statements.

The PPARC Executive is informed through the Head of Particle Physics Division, PPARC, and the PPRP through the Director, Particle Physics, CLRC.

The project management committee (PMC) will meet at least twice each year.

Appendix H: Risk Analysis

We were asked by the PPRP to discuss three possible areas of risk to the project.

The first is the risk of a serious mismatch to the LC schedule, which could be in either direction. Indeed, there was a mild complaint at last week's ECFA/DESY workshop that we would be "two years late", and this was with respect to our '15 month' GANTT chart. In our opinion, the chances of completing the LC by 2012 are not high. Were this to become a reality, we would obviously push hard for a faster R&D programme. However at SLC the CCD vertex detector was 'late' in the sense that Mark II would have much preferred to build one, but the R&D could not be completed on their timescale. The short answer is that a late detector will always be welcome, provided it is technically superior to what has already been installed.

What if the LC becomes another ITER, and is delayed by 10 years? In this case, it would be unwise of LCFI to push for the early development of the vertex detector, since the technology will move forward enormously during the next decade. However, the consequences of an early termination of the LCFI programme would be small by comparison with the catastrophe that such stagnation would cause to particle physics world-wide. Planning for such a major disaster is not particularly useful, even it this risk is not entirely negligible.

The second risk we were asked to consider was that of MTech going bankrupt. Here, it should be pointed out that the CCD company is one of the best in the world, is profitable, has a full order book, and is most likely to be sold as a going concern by the disastrous parent company. Such things have happened on a number of previous occasions in the world of scientific CCD manufacturers (Loral, RCA, Philips, EG&G and others) and the design and manufacturing teams and facilities have in all these cases been maintained, very much to the benefit of their important scientific customers. After working with the wonderful MTech team for 20 years, we hope the same will apply to them. If not, it will be a sad day for UK science and industry. Having said this, there are other CCD manufacturers (Sarnoff, Hamamatsu) who are keen to work with us. We already are exchanging non-confidential information via our vertex detector colleagues in the USA and Japan, and the LCFI collaboration would be welcomed as part of a more international effort working with one of these companies, were this to prove necessary. However, once again, we feel privileged to be a small part of the customer base which is keeping MTech viable, and would be extremely reluctant to fail to support them at this critical time for their company.

The third risk identified by the PPRP was that of a competing technology proving superior, for the LC vertex detector. Indeed, there is an increasing number of alternative suggestions. At last week's ECFA/DESY workshop, a fifth option emerged (SoI-inspired). So far, we see absolutely no reason to lose confidence in the statement from last year's DESY PRC that the CCD option 'exhibits the highest potential for reaching ultimate performance'. Indeed, some recent ideas for a no-implant CCD design, based on a channel with variable potential, exploiting the narrow channel effect in MOSFETs, may provide a clear solution to the power dissipation challenge. If this is the case (which will be tested with CPC-2) one will be assured of being able to construct a vertex detector satisfying the LC design requirements. Judging from last week's ECFA/DESY parallel session, no other technology is close to being able to make such a claim.

Having said this, it is entirely possible that the CCD option will hit an unpredicted brick wall, and that another option will be successful. This area of R&D has attracted some of the finest detector physicists in the business, and it would be rash to claim that any of them will fail. At some level, one should not see this in terms of 'risk'. The collaborations pushing the different technologies are constantly exchanging ideas. We helped some of our 'competitors' in our specialist session at the ECFA/DESY workshop, and they helped us with interesting ideas. At the end of the day, we intend to merge into a global collaboration to build this detector. As long as we remain objective, and make the selection on the basis of what is truly the best available technology when the time comes, we can look forward to a harmonious construction programme, in which the LCFI collaboration will play a large

part, whatever the technology chosen for the project. People with experience and understanding of one variety of silicon pixel detector are always useful if they get interested in one of the alternatives.

Appendix I: Outlook beyond March 2005

It must be emphasised that this R&D programme is necessarily more uncertain than (for example) a 10-year capital project to construct a detector system for an approved experiment. The linear collider is not yet an approved project, despite the fact that huge R&D budgets are devoted to the accelerator development, particularly in the USA, Germany and Japan. However, the world-wide consensus achieved in 2001, that this should be the next major international HEP project, is a firm basis for the detector R&D which is under way all over the world, gathering momentum over the past few years.

The risk of a major schedule change was discussed in Appendix H. Leaving this aside, there remains the lower level problem of predicting the precise start-date for physics, and hence the necessary pace of detector R&D. This problem is faced by all the LC detector collaborations. At the Chicago regional workshop in January, the start-date was predicted to be 2014, and on this basis the GANTT charts on pages 52 and 53 were drawn up. They indicate that a programme run steadily at 15 month cycles (the first chart) would be in time, whereas one run at 21 month cycles (the second chart) risks being two years late. This would not necessarily be catastrophic (a superior detector will always be welcome) but it would clearly be much better to install the desired detector at the beginning of the physics programme. This is the basis for our enthusiasm to achieve 15 month cycles for the CCD development as soon as funds allow.

At the ECFA/DESY workshop earlier this month, the opinion of the DESY directorate was that even our 15 month programme would be late, since they are aiming for completion of TESLA in 2012. This indicates the general level of uncertainty at present, which affects all the R&D planning. The situation encourages the fastest pace and most efficient R&D programme possible. As well as accelerating the cycles, it would be wonderful if we could find a way to eliminate one of the five cycles completely, and thereby definitely be in time. Whether this may be possible depends partly on which collider technology is chosen. We firstly discuss the part of our long term plan which is common to TESLA and NLC, then the differences.

The average readout rate and power dissipation are similar for both machine options. The need for reduced clock amplitudes is critical. This will first be pursued in CPC-3, by a shallow barrier implant, by a variable dielectric thickness, or by a variable width *n*-channel (using the narrow channel effect well known in MOSFET design). The other important parameter influencing power dissipation is the inter-gate capacitance. Pioneering work by MTech in collaboration with Leicester U space science in developing open phase electrodes suggests one way forward. Ideas based on this and other options will be pursued in CPC-4.

By this time, (end of 2005) we expect the mechanical R&D programme to have arrived at a preferred ladder design. Judging from where we are now, some form of semi-supported architecture seems most likely. In this case, CPC-4 devices will be thinned and mounted on the chosen substrate using the chosen adhesive, so as to begin to correspond mechanically and electrically to part of a realistic ladder.

The development of an optimised driver IC will be one of the last parts of the R&D programme, not least because the technical specifications will not be defined till the outcome of the CPC-4 tests are known. For CPC-5, we envisage constructing CCDs of the full layer-1 width, attached to the chosen substrate, equipped with full width readout ICs (CPR-9 then 10) and compact drivers. The CCDs will be provided with additional capacitive loads to correspond to full length layer-1 ladders. For the first time, we will construct an assembly which closely resembles Figure 4. This will be operated with LC-compatible cooling of both the active detector and the region at the end of the ladder.

Turning to the influence of the accelerator technology choice on our R&D programme, let us first consider NLC. If this is chosen, reading the detector in the 8 ms between each bunch train will suffice. The column-parallel architecture is still preferred, since this will provide enhanced radiation tolerance, the most convenient data flow for optimal correlated double sampling, and the advantages

of truly continuous clocking with 2-phase sinusoidal drive signals. However, if the R&D programme were to expose some unexpected problems with the column parallel approach (eg related to the bump bonding), the NLC environment would allow other architectures to be considered. Assuming that the column parallel approach continues to be generally favoured, the main simplification offered by NLC is a less challenging requirement for metallised gate electrodes. Initial studies suggest that this feature of the R&D may be straightforward. However, if it proves difficult, the NLC would again be tolerant of a shortfall in the parallel clocking rate capability. It is possible that these simplifications will permit a significantly faster route to a prototype ladder in the NLC case; possibly one could move there directly from CPC-4.

If TESLA is selected, there are two general aspects of the R&D which are more challenging. Firstly, we need the layer-1 ladders to operate at 50 MHz row clocking frequency. At present, we see no showstoppers to achieving this performance. Indeed, on completion of the CPC-1 design, attention has begun to move to CPC-2, and some beautiful ideas have emerged for achieving this long range goal. The second requirement, which seems to have been overlooked by some competing technologies, is the much greater pickup immunity needed for TESLA. While the heart of a detector encased in thousands of tons of iron is electrically extremely quiet, this does not apply to beam pickup, which at small radius will be severe. At SLD, it was possible to avoid the problem by starting the readout about 1 ms after the bunch had passed, which was more than sufficient. The same will be possible at NLC. However, for TESLA, the readout must start at most some tens of ns after each bunch within the train. Here, the column parallel CCD architecture appears to offer the highest possible pickup immunity. By transporting the signal electrons to the edge of the CCD, true correlated double sampling is possible with 20 ns intervals between sampling the 'reset' level and the signal, and the entire charge sensing circuit is extremely compact (dimensions around 100 microns). While it is difficult to imagine a more robust architecture in terms of pickup immunity, tests will be imperative, and these will take place with CPC-4 and beyond. They will be covered within the 'integration and testing' work package as it evolves.

The construction of the prototype ladder implies continuation for a further 2 years at a similar funding level. Details of this step can only be assessed towards the end of the overall R&D programme. Work packages for this final phase of the project will be similar to those for any other generation of CCDs and associated equipment. However, the CCD production costs will be somewhat higher due to the larger area devices needed. Against that, the costs per unit area of scientific CCDs can be expected to fall significantly by 2008, as they have done steadily over the past decade.

In summary, we are confident that our R&D programme will lead to a competitive ladder prototype that can be produced in time for the startup of the linear collider for physics, or shortly afterwards. In any case, the quality of the detector is much more important than the precise schedule on which it is completed.

For the programme beyond March 2005, as for the next 3 years, we suggest ongoing formal PPRP reviews phased with the CCD development cycles (21 month intervals initially, hopefully accelerating to 15 month intervals later). Funding for future cycles should be entirely dependent on the outcome of these reviews. In contrast to capital projects, we are not requesting blanket approval for the full R&D programme, nor for any specific responsibilities in the detector construction project in the far future. The most likely outcome is that the UK, building on its strong track record in this field, will continue to play a major part in the international collaboration which will eventually form to construct, operate and extract the physics from this exceptional detector system. The construction project will be the subject of MoUs to be negotiated within the overall collaborations once they have formed and when the vertex detector technology choice has been made, in the period 2010 to 2012.

Finally, we would like to explain that some of the requests in the new 'STANDARD FORMAT FOR PROPOSALS FOR INVOLVEMENT IN MAJOR PROJECTS', on which these appendices are based, are premature when considering a long term R&D programme. Questions related to the operating phase of the linear collider, such as the estimated size and standing of the UK community,

the number of UK graduate students, security of funding of international partners, the integrated cost of scientific exploitation, are all premature. It is not possible to see clearly that far ahead, but it is certain that doing physics at the LC will be very different from today. Control rooms both for the accelerator and for the detector will be distributed among the participating laboratories. Wherever the machine is built, UK physicists may be able to work at their home laboratory, or at most travel to Daresbury (for example) to commission their detector and run shifts taking data. There will need to be a few people based at the accelerator, but the work on physics analysis will be distributed all over the world, even more than today. This will be an ideal learning environment for UK graduate students who will not need to emigrate to the accelerator laboratory. Already, the detector R&D forms an informal 'Global Network' of which the LCFI collaboration is a prominent example. We are experiencing a much better integration of particle physicists in the UK academic and national laboratory infrastructure, while they continue to contribute strongly to the scientific programmes, just as most UK astronomers do not spend much time at the HST or Hawaii.


ID
Task Name
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
FLC Vertex Detector Schedule 1
CPC-1 fabrication - Cycle 1
Design
Manufacture
Design/manufacture CPR-1
CPR-1 design iteration -> CPR-2
Laboratory tests
CPC-2 fabrication - Cycle 2
Design
Manufacture
Design/manufacture CPR-3
CPR-3 design iteration -> CPR-4
Laboratory tests
CPC-3 fabrication - Cycle 3
Design
Manufacture
Design/manufacture CPR-5
CPR-5 design iteration -> CPR-6
Laboratory tests
CPC-4 fabrication - Cycle 4
Design
Manufacture
Design/manufacture CPR-7
CPR-7 design iteration -> CPR-8
Laboratory tests
CPC-5 fabrication - Cycle 5
Design
Manufacture
Design/manufacture CPR-9
CPR-9 design iteration -> CPR-10
Laboratory tests
DESIGN CONCEPT PROVEN
Prototype ladders construction
L1 CPCCD and Readout Chip design
Manufacture
Laboratory tests
L2-L5 CPCCD and Readout Chip design
Manufacture
Laboratory tests
Ladders assembly and evaluation
TECHNOLOGY CHOICE
Vertex Detector construction
Installation and Commissioning
FLC START-UP
21/03/08
21/12/10
25/12/13
P
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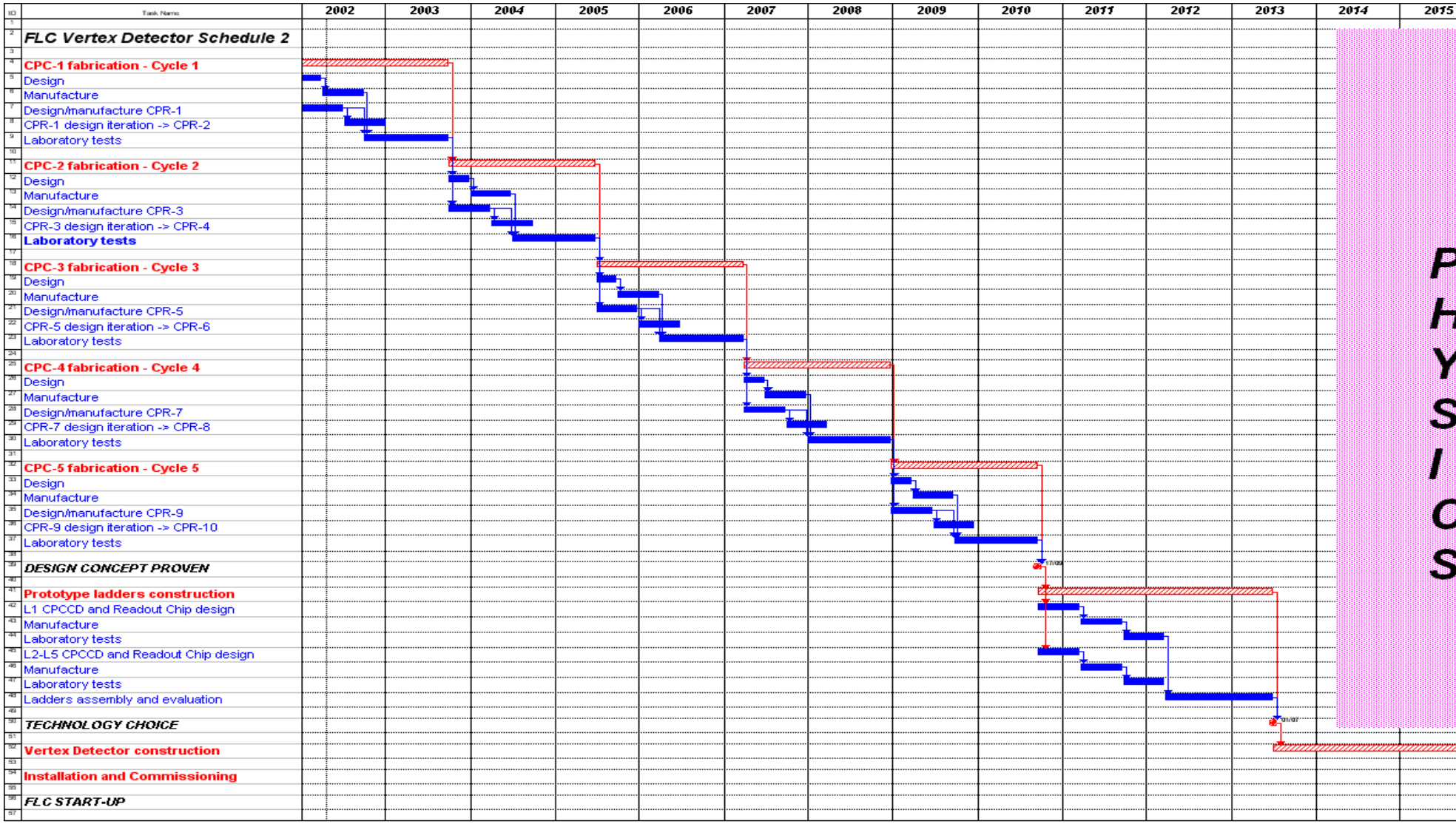
S


FLC Vertex Detector Schedule 2
CPC-1 fabrication - Cycle 1
Design
Manufacture
Design/manufacture CPR-1
CPR-1 design iteration -> CPR-2
Laboratory tests
CPC-2 fabrication - Cycle 2
Design
Manufacture
Design/manufacture CPR-3
CPR-3 design iteration -> CPR-4
Laboratory tests
CPC-3 fabrication - Cycle 3
Design
Manufacture
Design/manufacture CPR-5
CPR-5 design iteration -> CPR-6
Laboratory tests
CPC-4 fabrication - Cycle 4
Design
Manufacture
Design/manufacture CPR-7
CPR-7 design iteration -> CPR-8
Laboratory tests
CPC-5 fabrication - Cycle 5
Design
Manufacture
Design/manufacture CPR-9
CPR-9 design iteration -> CPR-10
Laboratory tests
DESIGN CONCEPT PROVEN
Prototype ladders construction
L1 CPCCD and Readout Chip design
Manufacture
Laboratory tests
L2-L5 CPCCD and Readout Chip design
Manufacture
Laboratory tests
Ladders assembly and evaluation
TECHNOLOGY CHOICE
Vertex Detector construction
Installation and Commissioning
FLC START-UP
2002
2003
2004
2005
2006
2007
2008
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2012
2013
2014
2015
PHYSICS