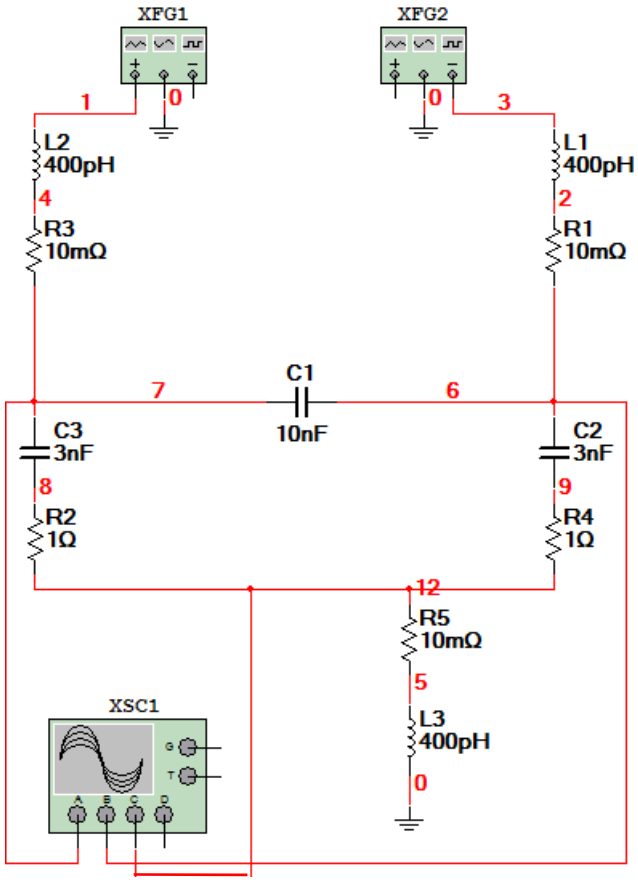
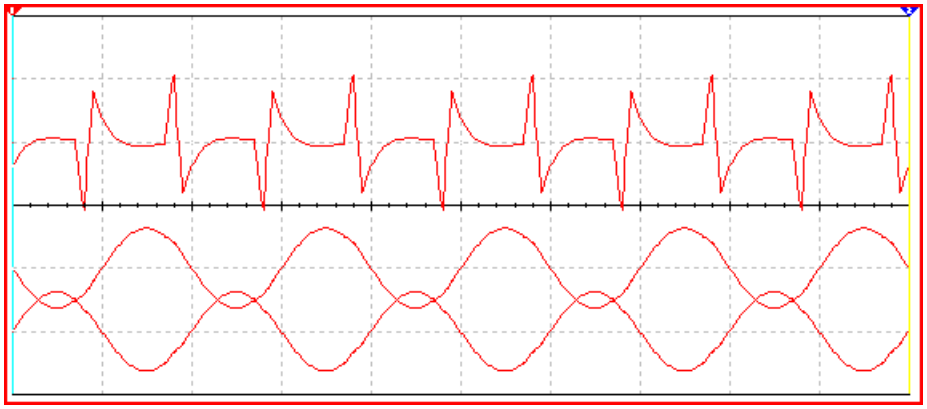
Substrate bounce – multiple wire bonds

- Circuit:



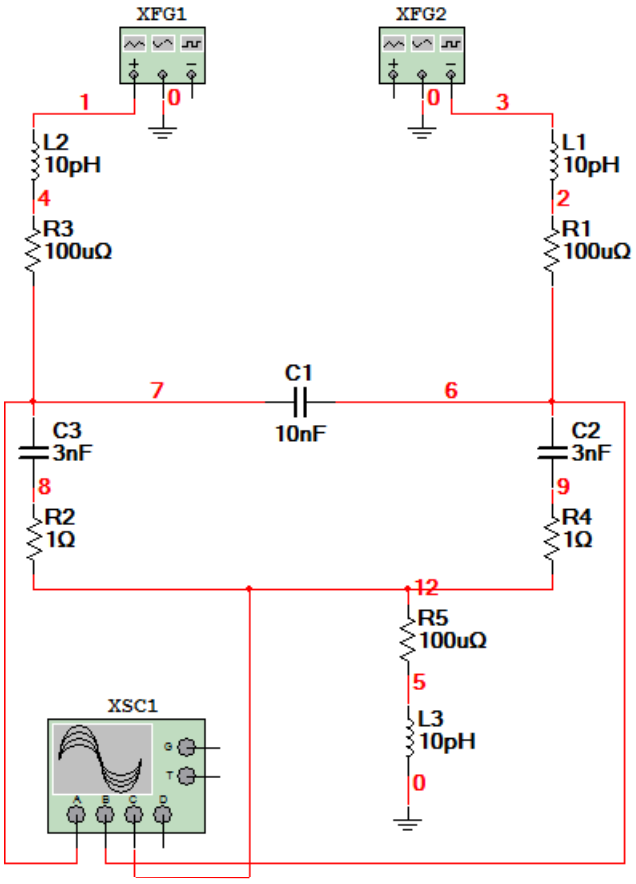
- Phase 1 and 2 square, 1 V_{pp}, 50 MHz, 1 ns/2 ns rise times:



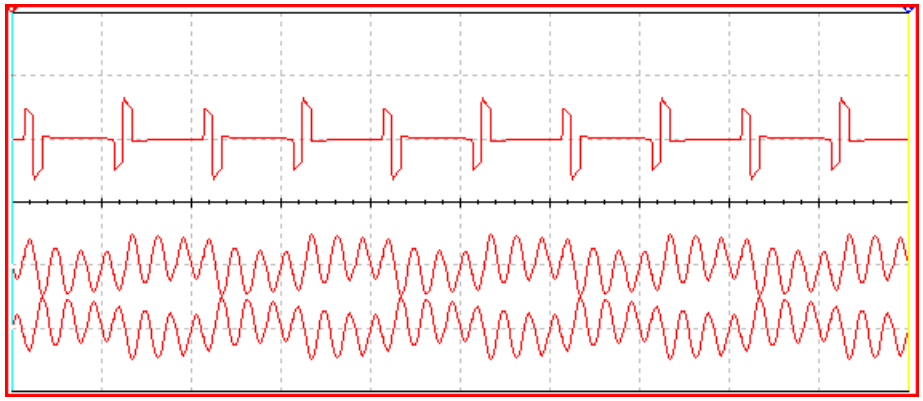
- Phases 1 and 2 (lower two traces) both 10V/div.
- Substrate bounce (upper trace) 200 mV per division.
- Bounce voltage ± 40 mV for 2 V_{PP} gate voltage.

Substrate bounce – multiple bump bonds

- Circuit:



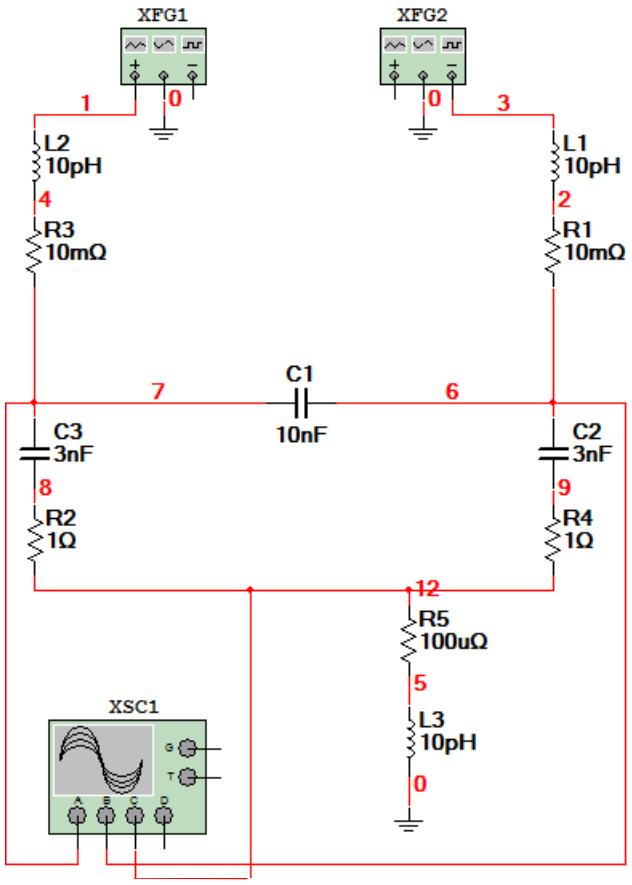
- Phase 1 and 2 square, 1 V_{pp}, 50 MHz, 1 ns/2 ns rise times:



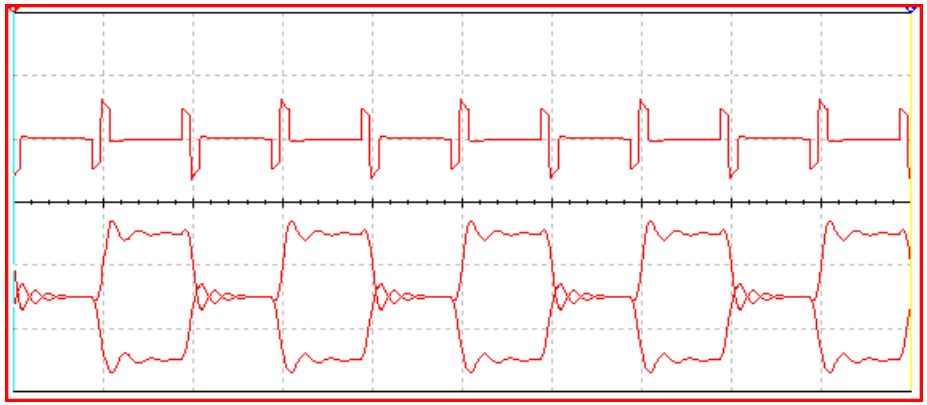
- Phases 1 and 2 (lower two traces) both 10V/div.
- Substrate bounce (upper trace) 20 mV per division.

Multiple bump bonds take two

- Circuit:



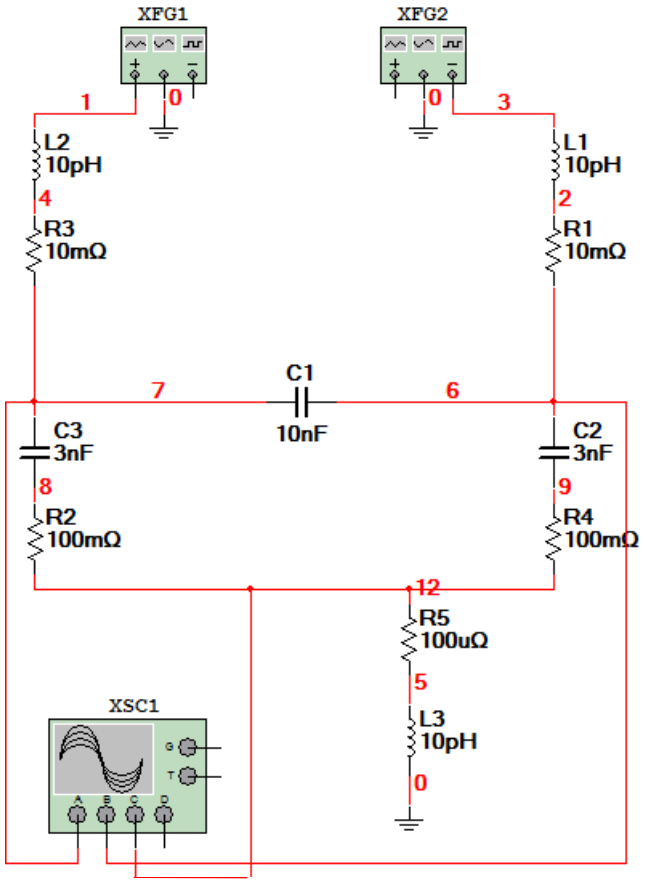
- Phase 1 and 2 square, 1 V_{pp}, 50 MHz, 1 ns/2 ns rise times:



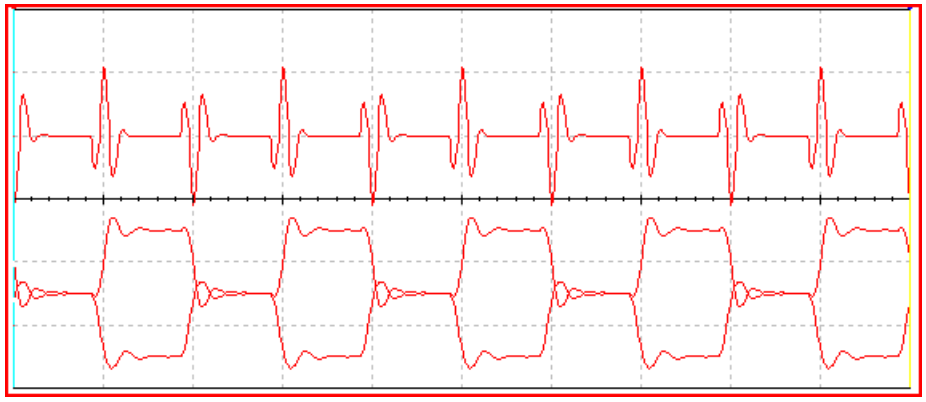
- Phases 1 and 2 (lower two traces) both 2V/div.
- Substrate bounce (upper trace) 20 mV per division.
- Bounce voltage about ±14 mV for 2 V_{PP} gate voltage.

Effects of “substrate resistance”?

- Circuit:



- Phase 1 and 2 square, 1 V_{pp}, 50 MHz, 1 ns/2 ns rise times:



- Phases 1 and 2 (lower two traces) both 2V/div.
- Substrate bounce (upper trace) 100 mV per division.
- Bounce voltage about ±100 mV for 2 V_{PP} gate voltage.