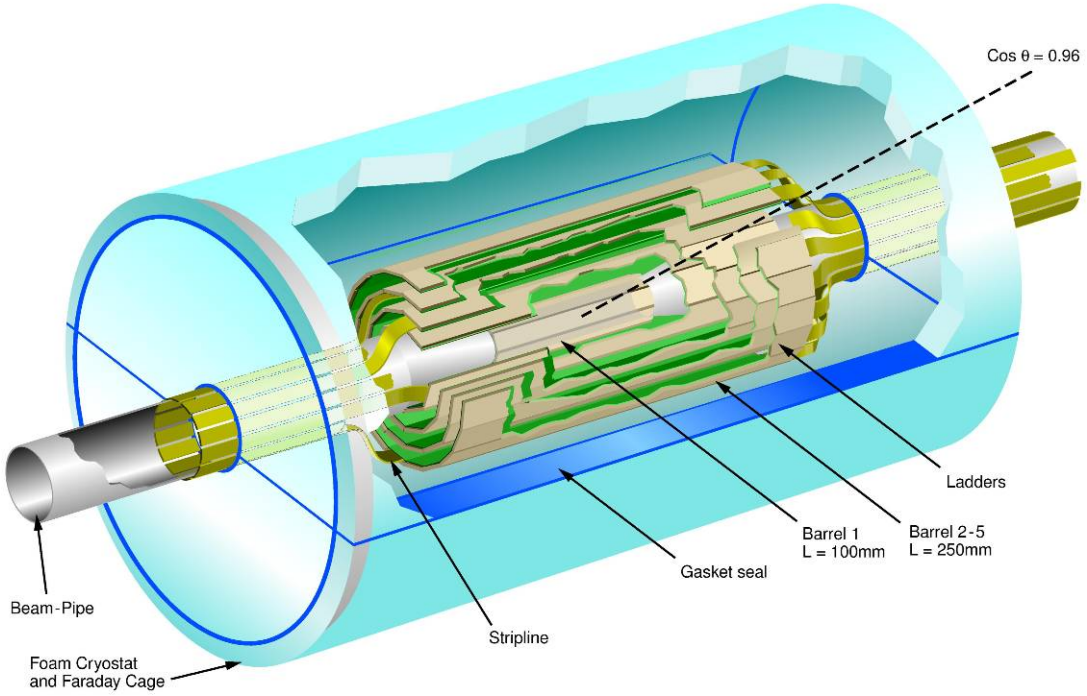
LCFI Report for the Vertex Detector Review at Fermilab

October 2007



The Universities of Bristol, Edinburgh, Glasgow, Lancaster, Liverpool, Nijmegen, Montenegro and Oxford and the Rutherford Appleton Laboratory

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LCFI: Introduction and Scientific Goals

Introduction

This report describes the status of the research programme of the Linear Collider Flavour Identification (LCFI) Collaboration and presents the work the Collaboration proposes to carry out in the period from the end of 2007 until 2012. This represents a continuation of LCFI's current research, with the goal of developing the sensors for the Vertex Detector (VXD) of the International Linear Collider (ILC), the associated mechanical support structures and the necessary ancillary electronics. In addition, the algorithms and software that LCFI has produced for the VXD, allowing its use for quark flavour and charge identification at the ILC, will be further developed and optimised and other uses of the VXD in physics analysis further explored. The design of the VXD will be optimised and the associated software tested using Monte Carlo simulations of "benchmark" physics processes, chosen to be particularly sensitive to VXD performance.

The objective of the LCFI group is to ensure that it, with international partners, is in a position to make a major contribution to the construction of one of the ILC VXDs. Once the ILC, with its VXD, is operational, LCFI physicists will participate in physics analysis at the ILC, focussing on the many measurements in which the identification of the flavour and charge of heavy quarks is crucial.

The timescale for the research programme presented here is determined by progress with the design and construction of the ILC. A major step forward was taken when the Reference Design Report[1] (RDR) was published. This is to be followed by an Engineering Design Report (EDR), to be released in 2010, and the detectors for the ILC must be planned on a timescale concomitant with this. Letters of Intent to produce Engineering Design Reports for ILC detectors will be requested soon, and LCFI foresees contributing to the VXD sections of two detectors concepts, the SiD and the ILD. The detector EDRs will be produced on the same timescale as that for the ILC, and it is hoped that construction of the ILC and its detectors will start in around 2013. The VXD R&D programme outlined here must therefore be completed by 2012.

In the following, a brief description of the motivation for the ILC and for high performance flavour identification is given. The LCFI programme is then summarised. This programme is broken down into Work Packages, which are described in more detail in the latter section of the report. The descriptions of the Work Packages include estimates of the resources needed to complete the LCFI programme. Finally, a summary is given.

Scientific Motivation

Our current understanding of the fundamental interactions of nature is encapsulated in the Standard Model (SM) of Particle Physics. Aspects of this model remain to be experimentally demonstrated and, despite its many successes, it is clear that the Model is not complete. An example of the former is the Higgs sector, where the Higgs boson has yet to be observed. Examples of the latter are provided by the fact that the SM does not provide an explanation for the observed number of generations of quarks and leptons, nor does it account for the relative strengths of the strong and electroweak interactions: no attempt is made to describe gravitational interactions. New experimental data are needed both to fully understand the SM and to determine which, if any, of the many proposed extensions of this theory are able to provide a more complete description of nature. These data will be provided by the Large Hadron Collider (LHC), which will commence

operation at CERN in 2008 and will collide two proton beams at a centre-of-mass energy of 14 TeV, and by the ILC, which will collide electron and positron beams at a centre-of-mass energy ranging from about 90 GeV to initially 500 GeV; this latter energy will later be increased to 1 TeV.

Flavour Identification at the ILC

The examples of the physics to be studied at the ILC given above illustrate a further point of interest: many of the measurements can be greatly enhanced by the identification of the flavour of the heavy c and b quarks produced in the electron-positron collisions at the ILC. The determination of the branching ratios of the Higgs boson's decays to heavy quarks and leptons, assuming that the Higgs is observed at the ILC, require the identification of b and c quarks and of τ leptons. As the cross sections for the Higgs production and decay are small, this flavour identification must be efficient. Even at the ILC, the backgrounds are significant, so high purity must also be achieved. The b and c quarks are identified via their characteristic lifetimes and hence the distances they travel between their production and decay. For these decays, the impact parameters of the decay products are typically of the order of a few 100 μm. Identifying these requires that several space points on the tracks of the b and c decay products be measured with a precision of better than 5 μm within a few centimetres of the production vertex and that this be done with minimal disturbance of the flight paths of those decay particles. The VXD necessary to accomplish this measurement must thus perform significantly better than even the best such detector constructed to date, the VXD3[2] of the SLAC Large Detector (SLD) Collaboration which used Charge-Coupled Devices (CCDs) that were designed and manufactured by e2v technologies.

The ILC and Vertex Detector Design

The baseline LCFI VXD is illustrated in Figure 1. As is shown later in this report, it has been demonstrated to be a powerful tool for flavour identification at the ILC. The detector consists of five layers of CCDs with 20 x 20 μm^2 pixels which provide a point resolution of about 3.5 μm in both the rϕ direction transverse to the beam-line and the z direction along the beam-line. The sensors are arranged in concentric "barrels" around the beampipe. The innermost layer is at a radius of 1.5 cm and the outermost at 6 cm. In the design shown, the innermost barrel is made up of 8 modules or "ladders", each of which is composed of a sensor of dimensions 1.3 x 10 cm^2 with readout and other electronics at both ends. The further layers are constructed using up to 20 ladders, each of which is composed of two sensors of dimensions 2.2 x 12.5 cm^2 with electronics located at the outer ends only. This design results in a total number of pixels of nearly 10^9.

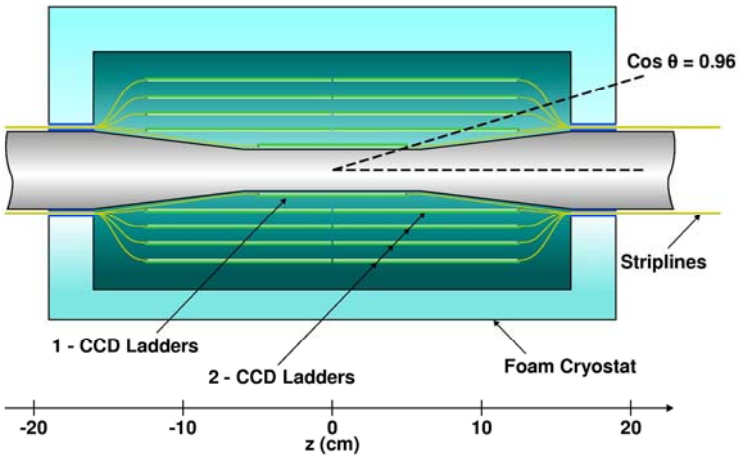

Figure 1 The CCD-based vertex detector design developed and studied by the LCFI Collaboration.

Location of the electronics at the extremes of the polar angle θ ensures the amount of material in the central tracking volume is minimised. This is essential, as the momentum of the charged tracks in heavy quark decays at the ILC extends to momenta as low as a GeV and below, implying that multiple scattering effects must be minimised. The goal is to produce ladders with a thickness of only 0.1% X_0 (c.f. SLD VXD3, 0.4% X_0). Minimisation of the material budget also dictates that only gas may be used for cooling the sensors in the sensitive volume of the detector. The sensors must therefore consume at most a few tens of watts of power.

The ILC environment presents many challenges to the designers of vertex detector sensors. For example, at a centre-of-mass energy of $\sqrt{s} = 500\,\text{GeV}$, trains of about 3000 bunches (or about 5000 at $\sqrt{s} = 1\,\text{TeV}$) will pass through the beampipe within the ILC detector at a frequency of approximately 5 Hz. Within these trains, tightly focused electron and positron bunches collide roughly every 350 nanoseconds (about 150 ns at $\sqrt{s} = 1\,\text{TeV}$) generating not only the e^+e^- interactions of interest but also large numbers of electron-positron pairs which cause background hits in the vertex detector. With pixel sizes of 20 x 20 μm^2, in order to ensure that the occupancy in the sensors in the inner layer of the VXD remains below about 1% so track finding is not compromised, the signals in the sensors must be read out or stored about 20 times during the bunch train, or roughly every 50 μs.

A further challenge at the ILC is illustrated by the experience of the SLD vertex detector, the only vertex detector operated in a linear collider environment to date. This detector suffered from beam-induced pickup, caused by the leakage of RF power generated by the wake fields of the passing electron and positron bunches. Fortunately, at SLD, where the time between bunch crossings was 8 ms, it was possible to wait a few hundred microseconds for the electromagnetic interference (EMI) to die out and the electronics to recover before initiating the read out.

The LCFI Programme

Sensors for the vertex detector

As is discussed above, the sensors used at the ILC must provide high point precision, good two-track resolution and be extremely thin. It has already been demonstrated that Charge-Coupled Devices

(CCDs) can satisfy some of these requirements, for example, the CCDs used in the vertex detector of the SLD experiment achieved hit resolutions of 3.5 μm. However, the sequential readout of these CCDs cannot achieve the readout speeds needed at the ILC. This has prompted LCFI to develop, with e2v technologies, Column Parallel CCDs (CPCCDs). Two generations of these devices have now been tested and speeds close to those required at the ILC demonstrated. Devices of a size similar to that required for the VXD have also been manufactured.

One of the major challenges in operating the CPCCD arises from the relatively large intergate capacitance of the device. Achieving the gate voltages necessary to drive charge through the CPCCD requires large currents to charge this capacitance. This is a challenge for the drive circuitry and affects the power dissipation. Although LCFI has designed and tested a chip capable of producing the necessary drive currents, reducing the integrate capacitance remains an attractive goal. Several possible design modifications are under test that may allow thus to be achieved. Similarly, reduction of the dopant induced potential barriers between the pixels of the CPCCD will result in decreased drive voltages and reduced power dissipation. LCFI is pursuing studies with e2v designed to produce a better understanding of the required dopant levels.

A different approach to achieving low occupancies in the inner layers of the VXD is to store hit information locally in the pixels during the ILC bunch train, with readout being performed in the long inter-train gap. LCFI has proposed a device which uses this technique, the In-situ Storage Image Sensor (ISIS). In the ISIS, small CCDs in each pixel store the charge released by particle hits. Proof-of-principle devices have been constructed and successfully tested. There are many advantages to this approach. For example, a readout speed of a few MHz suffices. The ISIS will also be more radiation tolerant than the CPCCD due to the reduced number of charge transfers necessary. In addition, the storage of the raw charge associated with the hit makes it possible to design in a high degree of robustness against electromagnetic interference (EMI), the importance of which is illustrated by the SLD experience. If the ISIS is constructed using CMOS technology, it may be possible to make the sensor and readout electronics on the same piece of silicon, reducing the detector mass, especially in the forward region.

The advantages of each of these sensors must be balanced against the challenges that must be overcome before they can be used at the ILC. The primary challenge for the CPCCD development has been the achievement of the necessary readout speed using low-mass drive electronics: significant progress has been made in this area. The ISIS sensors are more attractive than the CPCCD in some respects, for example their radiation hardness, the relaxed readout speed requirement and their resistance to EMI, but CCD-like storage registers have yet to be incorporated in CMOS devices, so the production of the ISIS is likely to take longer than that of the CPCCD. LCFI thus propose to pursue the development of both devices to ensure that they have a sensor ready for use at the ILC if the most aggressive timescales are realised, while continuing development of the sensor optimally matched to the conditions at the ILC either for a later upgrade of the VXD or for the eventuality that construction of the ILC is delayed.

Simulation of the vertex detector and its physics performance

LCFI has invested considerable effort in the development of tools for using the VXD for flavour and charge identification and in physics studies. The Collaboration's Vertex Package, released early in 2007, provides a comprehensive set of routines for flavour and charge identification at the ILC. LCFI

has also performed some VXD optimisation studies, repeatedly emphasized the importance of a small beam pipe radius, for example, which has influenced the design of the ILC interaction region. The Collaboration also presented the first studies of the physics possibilities opened up by the identification of the charge of the b and c quarks at the ILC. It was shown that this is feasible for a large proportion of heavy flavour events by identifying the charges of all the tracks associated with the b and c decay vertices. As the association of tracks to vertices must be correct for all charged particles, even those of lowest momentum, b and c charge identification further sharpens the requirement that multiple scattering in the vertex detector be minimised.

In the coming years, the Collaboration proposes to continue and extend these studies. Effort will be devoted to refining the heavy flavour identification algorithms and to improving the b and c charge identification provided by our Vertex Package. For example, heavy flavour identification will be improved by including further information on the correlations between the positions of the decay vertices identified in an event, while quark charge identification will be extended to cover cases in which neutral B hadrons are produced by using correlations between the charges associated with the b and c decay vertices.

A further focus of the LCFI studies will be the optimisation of the VXD design. For example, vertex detectors with various sensor layouts will be simulated and the effects on flavour and charge identification investigated. The performance of the detector designs with regard to various benchmark physics processes will also be studied.

LCFI will continue to provide input to international discussions on the possibilities opened up by the addition of new capabilities to the ILC detector. An example here is the question of particle identification. So far this has been thought to be largely irrelevant at the ILC, but the physics gains arising from identification of the charge of b and c quarks are now becoming apparent due to the work of LCFI. Such charge identification can be enhanced by kaon detection, for example[3].

Ancillary electronics

In addition to the sensors, the VXD requires readout and control electronics for its successful operation. LCFI has designed and produced three generations of column parallel readout chip, which have been bump-bonded to the CPCCDs and successfully tested. The latest of these chips incorporates not only amplification and digitisation circuitry but also cluster finding and data sparsification. Further generations of this chip are planned, culminating in a device that is suitable for the VXD. While this development has been driven by the CPCCD, it is also applicable to the ISIS. Indeed, use with the ISIS is considerably simpler due to the relaxed readout speed of this device.

Particularly challenging is the design of a chip to produce the clock signals for the CPCCDs. Clock voltages of around 2 V_{PP} are needed for efficient charge transfer, and the relatively large intergate capacitance of the current generation of CPCCDs implies that currents of about 20 A are needed to generate these drive voltages. Tests of the first Column Parallel Drive chip designed by LCFI, CPD1, have shown that this goal has been achieved, provided low inductance connections to the CPCCD can be established. Future tests will involve bump-bonding CPD chips to CPCCDs to achieve this.

Of considerable importance for the LCFI R&D programme is the design and construction of the many printed circuit boards and other external electronics systems necessary for the testing of the sensors, the readout chips and the drive circuitry. LCFI has developed an expert electronic

engineering support team that has acquired considerable experience in the design of these systems. This team will continue to support LCFI programme and will contribute to studies of the integration of the sensors, readout and drive chips necessary for the VXD.

Mechanical studies

Sensors capable of particle tracking at the few micron level are of little value if they cannot be mechanically supported in a structure whose behaviour is understood to a similar or better level of precision. LCFI has investigated various designs for sensor support, including attaching sensors thinned to about 20 μm to a beryllium substrate, an "unsupported" option in which a sensor of thickness about 50 μm is held under tension and the use of new materials such as reticulated vitreous carbon (RVC) and silicon carbide foams. The differing coefficients of expansion of silicon and beryllium were shown to make Be unsuitable as a substrate, while unsupported silicon sensors were shown to suffer from bowing in the direction transverse to that in which tension was applied. (This arises due to the tensions introduced when the silicon is processed in sensor manufacture.) Both RVC/silicon sandwiches and SiC as a substrate look to be very promising options for ladder construction. LCFI is further investigating these materials, developing metrology and machining techniques. Studies of VXD designs based on carbon fibre have also started.

A further issue in the construction of the VXD is the need to cool the sensors and electronics. Here, exploitation of the duty cycle of the ILC will allow the heat budget to be kept to a few hundred watts, making cooling using a gentle gas flow feasible. LCFI has constructed a cooling prototype to investigate this possibility and compared the results from the prototype with finite element calculations. Future simulations will study the dynamics of the system introduced, for example, when the CPCCD drive is operated only during the ILC bunch train. This is likely to result in temperature fluctuations: the vertex detector will heat up during the approximately 1 ms long bunch train then cool down in the 0.2 s between bunch trains. The effect of these fluctuations must be understood at the micron level if the detector is to provide the required precision.

Test-beam studies

LCFI is in the process of performing its first test beam studies, but this programme will grow as the Collaboration progresses to testing fully integrated sensor, readout and drive assemblies.

Summary

There is widespread agreement that progress in Particle Physics in the next two decades will best be achieved through the construction of the International Linear e^+e^- Collider with a centre-of-mass energy ranging between the Z mass and 1 TeV. In this report, the LCFI Collaboration presents a coherent programme of research, the goal of which is to ensure that, with our international partners, LCFI physicists are in a position to contribute to the construction of the VXD for the ILC. To facilitate the detailed discussion of the programme, six Work Packages (WPs) are defined. These are:

WP1 This covers simulations of the vertex detector and the physics studies that must be undertaken in order to optimise the sensors and vertex detector and guide the designers of the ILC as well as the development of the software tools that are needed to use the VXD.

WP2 This covers the design and construction of CPCCDs which have the potential to satisfy the demanding requirements for operation at the ILC and of ISIS devices which may offer better performance than that of the CPCCD.

WP3 This Work Package is responsible for the Application Specific Integrated Circuits that must be designed, produced, and tested for the readout of the sensors as well as the chips required to drive the CPCCD.

WP4 This covers the design and production of the many PCBs and electronics needed for the testing of the various sensors in the laboratory.

WP5 This Work Package is responsible for the programme of tests of the various sensor types, including studies of the achievable readout speed and the radiation hardness of the sensors and the testing of sensors in beams.

WP6 This covers the design of the mechanical support structures for the sensor modules and of the overall vertex detector.

The remainder of this report discusses the programme of these WPs.

WP1 – Physics Studies

Introduction

The aim of the LCFI physics studies is to guide the design of the VXD by assessing different detector designs, to strengthen the case for the ILC by demonstrating the physics made accessible by the collider and its detectors, and to develop the tools necessary for such studies. Work by the LCFI Collaboration has already contributed to all these areas, demonstrating for example the importance of small beam pipe radius and the physics gains of measuring quark charge. The Collaboration has also expended considerable effort in developing a Vertex Package to exploit the information provided by the VXD. This important tool is described briefly in the following, as are LCFI's plans for future physics studies

The LCFI Vertex Package

The LCFI Vertex Package is a comprehensive tool for using the information provided by the VXD for quark flavour and charge identification. Figure 2 shows a schematic overview of the Package. Input to and output from which is handled in LCIO[4] format, permitting data to be exchanged between the different ILC software frameworks. For example, input can either be provided by the fast MC simulation SGV[5], used by LCFI so far, thus allowing detailed comparisons and cross checks with previous results, or by MarlinReco[6], the event reconstruction framework under development in Europe.

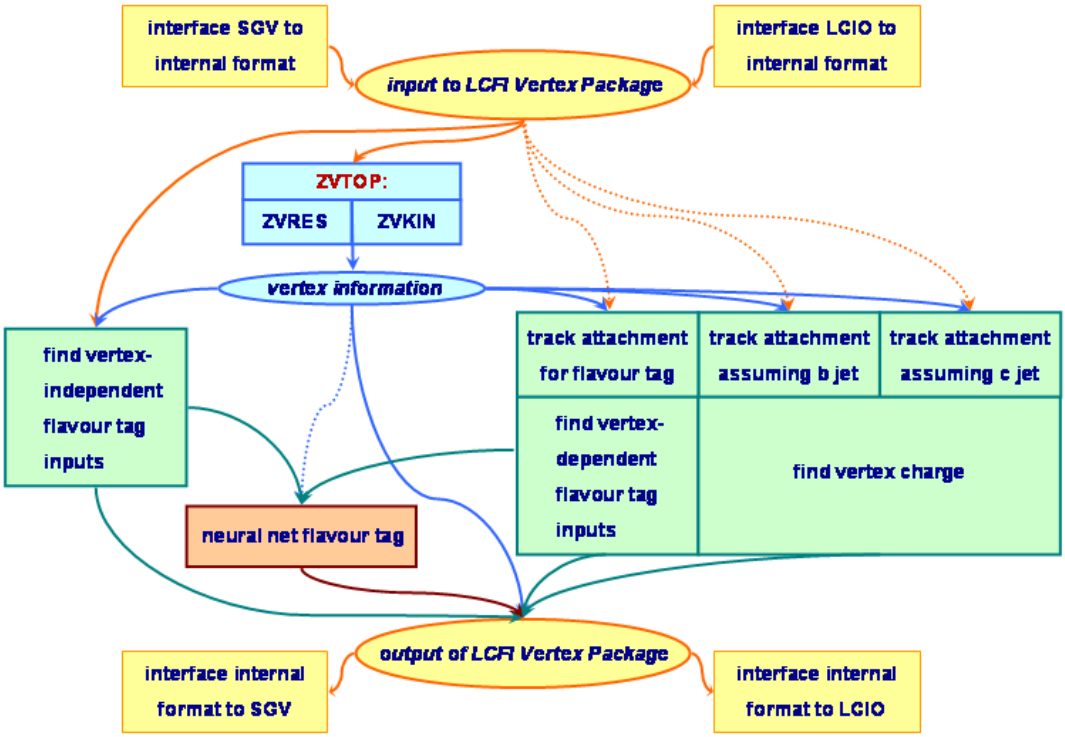

Figure 2 Structure of the LCFI Vertex Package and flow of information between the different parts of the software.

The vertex finder ZVTOP provides two vertexing algorithms, called ZVRES and ZVKIN, the latter is also known as the ghost track algorithm. While the ZVRES branch is a very general algorithm coping with arbitrary multi-prong decay topologies, ZVKIN is more specialised. Using additional kinematic information, the ghost track algorithm is able to correctly assign tracks to vertices in decay topologies with one or more 1-prong vertices, thus extending coverage and improving the flavour tagging capabilities as shown for SLD[7] where this code was first developed. Our package is the first to provide this algorithm for ILC studies.

The default flavour tag procedure provided was developed for the ILC by Richard Hawkings[8]. It is based on nine neural networks, three each for the three cases of one-, two- or more vertices found by ZVTOP. Separate networks are used to identify b-jets and c-jets for arbitrary background. For some physics processes the background only consists of b-jets, permitting improved c-jet identification. Therefore dedicated networks are provided for that case.

If only the IP is found by ZVTOP, the flavour tag is based on information from the two tracks in the jet that have the highest impact parameter significance, plus the "joint probability", i.e. the probability for all tracks to come from the IP. If secondary vertices are found, the neural net inputs are calculated from a set of tracks which contains one or two vertices from ZVTOP and in some cases further tracks assigned by a specific procedure devised to recover some 1-prong topologies for b-jets when running ZVRES. This "track attachment" step, in which additional tracks are added to the set of tracks contained in secondary ZVTOP vertices, may need to be tuned depending on whether the tracks are to be used for obtaining flavour tag inputs or the vertex charge, and for vertex charge calculation, track attachment differs depending on whether the jet is assumed to arise from a b- or from a c-quark. Track attachment for b-jets was optimised by LCFI in 2004 using the SGV fast Monte Carlo (MC) simulation. A similar procedure is used for c-jets.

For training the neural networks and for obtaining the output from pre-trained neural nets we use C++ based neural network software developed within the Bristol LCFI group. This allows flexible definition of the network architecture (number of layers and nodes), transfer function and training algorithm.

Studies of the LCFI package have so far been performed largely within the European ILC analysis framework MARLIN. The MARLIN package is based on a modular approach, permitting distributed code development. The modules, called processors, are activated and configured by a steering file. The LCFI Vertex Package provides eight MARLIN processors. One processor is needed for track selection and two for the two branches of ZVTOP. In addition, one processor provides the true jet flavour from the Monte Carlo, one is used calculate the neural net inputs and the vertex charge, one to train and one to use the neural networks that provide the tags. Furthermore, one processor is provided to determine and plot flavour tag purity versus efficiency.

Validation of the Vertex Package was completed early in 2007. Tests with the fast MC simulation SGV were followed by checks with the full MOKKA Monte Carlo and MarlinReco event reconstruction. The first version of the LCFI Vertex Package, v00-01, was released in April 2007 as announced on the ILC software forum[9].The Package has been presented in detail at ILC workshops.

Using input from SGV in LCIO format, a system test was performed by running the full vertex finding chain using the ZVRES branch, calculation of the vertex charge and the flavour tag inputs, which were fed into the neural network processor, followed by determination of flavour tag purity as a function of efficiency. Agreement between the Vertex Package and earlier FORTRAN versions of the code is excellent, as is shown in Figure 3. This result has been included in the Physics section of the Detector Concept Report (DCR). Results agree equally well over the full ILC energy range.

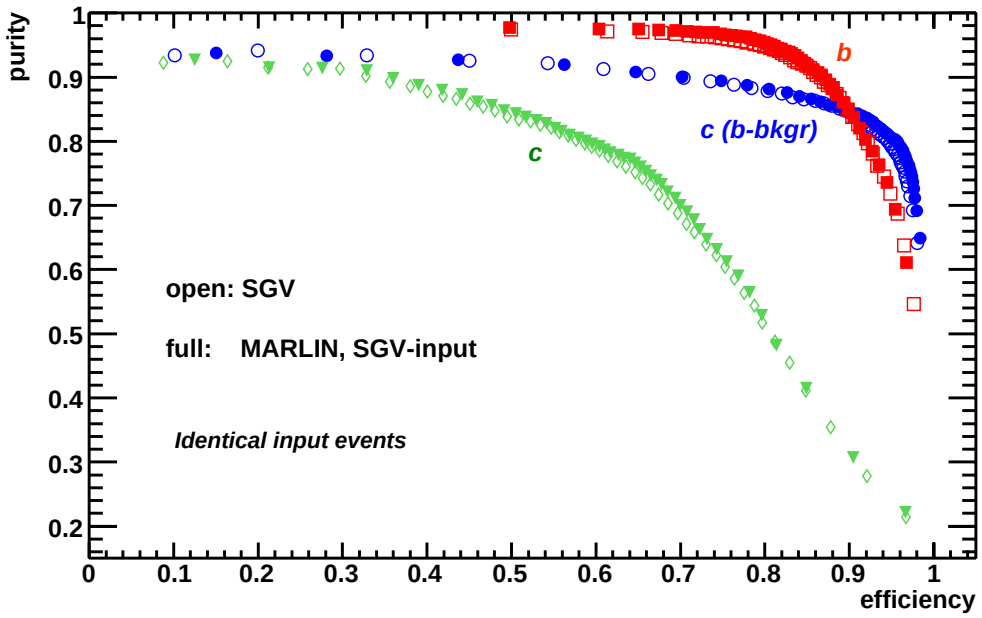

Figure 3 Comparison of purity of the flavour tags for b-jets, c-jets and c-jets with b-background only, plotted as function of efficiency, for a CMS energy of 92 GeV. Full symbols correspond to the result from our package in MARLIN, open symbols to the performance of previous SGV-FORTRAN code.

The system test with full MC was performed with events from the Pythia event generator, passed through the MOKKA detector simulation. The LDC01Sc detector model was used. This assumes a simplified vertex detector geometry consisting of sensitive cylinders. Photon conversions were switched off at the GEANT level, since these can be efficiently suppressed using the results of the full reconstruction once the necessary software is available and would unrealistically degrade performance if included in our studies.

The simulation of tracker hit digitization and track reconstruction was performed using the LDC tracking package by A. Raspereza[10], run in track cheater mode with the “silicon only” option (i.e. omitting the TPC). Initial comparisons of the results obtained with the different tracking options have also been made, as is described in the following. Jets were found using the Durham jet finding algorithm as provided by the “Satoru jet finder package” within MarlinReco.

The selection of tracks input to our package is identical to that derived in an earlier LCFI study using the GEANT3-based BRAHMS full MC simulation[11]. Within our package, tracks originating from hadronic interactions are removed using MC information, as explained below in more detail.

In Figure 4, the resulting performance at the energy of the Z-resonance is compared to the earlier BRAHMS result. Over a large efficiency range, the result from our code yields higher purity values

than found previously. However, one should keep in mind that this comparison is less rigorous than that with SGV input and the results are thus expected to differ to some extent, given that boundary conditions are not exactly the same. For instance, the BRAHMS result included pattern recognition effects, whereas the result shown here does not. Comparisons with different tracking options also suggest that the BRAHMS result may have been affected by an error in the tracking code, which was identified within the new framework and corrected as result of the feedback given by LCFI, as described below. The new LCFI result, shown in Figure 4, has been included in the Detector part of the DCR document.

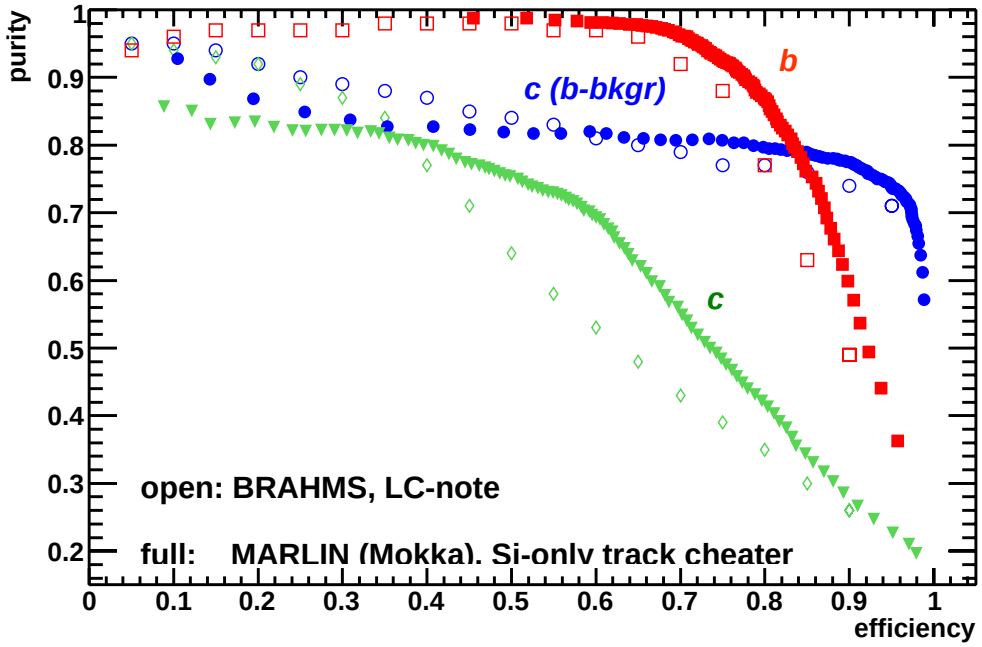

Figure 4 Comparison of purity of the flavour tags for b-jets, c-jets and c-jets with b-background only, plotted as function of efficiency, for a CMS energy of 92 GeV. Full symbols correspond to the result from our package in MARLIN with input from the full MC simulation MOKKA and the track cheater using only the silicon tracking detectors, open symbols to the performance obtained with the earlier GEANT3-based full MC simulation BRAHMS.

The LCFI code is available via the Zeuthen CVS repository for ILC software. In addition, another directory has been set up for descriptions of neural networks and information on the training conditions used for those networks, such as physics process, sample size, input variables etc. A central repository for these networks will contribute to making analyses based on these flavour tags more transparent and should facilitate comparisons between similar studies performed by different ILC groups.

Future Programme

The optimisation of vertex detector parameters will continue until construction of the detector begins. This optimisation will be based on detailed performance comparisons both at the level of benchmark quantities and of physics processes sensitive to the vertex detector design. To yield reliable results, they must be based on realistic descriptions of the designs that are compared and be performed using adequate vertex detector simulation and reconstruction tools, requiring further development of the software in parallel to the optimisation process.

The benchmark quantities to be considered will include both direct measures of performance, such as impact parameter resolution, and measures of the overall performance of the flavour tagging and vertex charge reconstruction. These will all be studied as function of energy and polar angle. Various benchmark physics processes have been chosen in consultation with the ILC community. Clearly, as LHC results become available and new models are developed there will be changes in the physics processes for which the ILC machine and detectors should be optimised. LCFI will work in closely with the global detector concept groups and our theoretical colleagues in this area.

The following subsections cover the improvements to the Vertex Package software currently envisaged, the benchmark physics processes that will be used for detector optimisation and the parameters and aspects of the vertex detector design to be improved as a result.

Work related to the Vertex Package software

Near-term improvements of the code

While the first version of the LCFI Vertex Package is already fully functional, providing a complete vertex finding package in ZVTOP, flexible flavour tag and vertex charge reconstruction and extensive documentation, near term improvements are envisaged to increase further the flexibility of the package and to permit the user to better monitor the effects of changing parameters in the Package. For this purpose, the possibility to write out diagnostic plots and tables with raw numbers will be added to all three parts of the package and the documentation further extended.

Calculation of the joint probability variable, one of the inputs of the default flavour tag algorithm, depends on parameters that have to be obtained from a fit to the track impact parameter distribution. In the first version, “hard-coded” approximate numbers obtained from fast Monte Carlo were used in this calculation. The next release will include a module to perform the fit required to ensure optimum parameter values are used.

Another known deficiency of the first version of the Vertex Package is that the vertex fitter implemented has not been optimised for run time performance and thus requires a large proportion of execution time. This issue is currently being addressed by interfacing a fitter developed by the Darmstadt ALICE group to our code. The new diagnostic features will be used to ensure that vertexing results from the new fitter are compatible with those obtained from the first release version. These new features will be released to the community in autumn 2007.

The current Vertex Package uses MC information to suppress tracks resulting from photon conversions, hadronic interactions and from the decay of K_S mesons and Λ baryons. Development of masking algorithms based on information from reconstructed tracks is required and is underway. Adequate treatment of these effects will have to be in place, for example, for a realistic study of the effect of varying the material budget.

A further point that requires improvement is the treatment of the interaction point (IP). As no routine was available to determine the position of the IP, and in order to make our code available to the community as early as possible, a rather crude fit procedure was implemented. Throughout the Vertex Package, this should consistently be replaced by an IP based on averaging the event vertex over an adequate number of events. Development of code to do this has started.

Further work is also required on the default parameters of the package. While the current parameters partly stem from a combination of different previous studies with fast and GEANT3-based full MC, a systematic study is planned in which these parameters will be varied and new improved default values derived. Using these optimised parameters, new default neural networks for the flavour tag will be trained, which will replace the current networks that were trained using a fast MC sample.

To permit the Vertex Package to be used in conjunction with the ALCPG software framework, mainly developed and used in the US, compatibility with that framework is will be ensured, e.g. through support for development of the appropriate "drivers", i.e. the java-modules corresponding to the processors already available in the MarlinReco framework.

Improvements to flavour tag and vertex charge

It is expected that the flavour tagging algorithm and vertex charge reconstruction can be improved by using more of the information provided by the vertex detector and other subdetector systems than is currently the case, and by exploring new approaches to the tagging.

Both the flavour tag and vertex charge reconstruction will profit from the use of the ZVKIN vertexing algorithm for special decay topologies. The ZVKIN branch of ZVTOP, made available as part of the first release of the Vertex Package, has not yet been optimised for use at the ILC. In the ZVKIN implementation, the IP position is currently hard-coded and will have to be replaced by the fitted IP, as described above. The parameters of the ZVKIN branch were chosen on the basis of the SLD vertex detector performance, and may need to be changed to make full use of the improved ILC vertex detector design. Beginning with studies at the Z-resonance, where a comparison with SLD performance is possible, this parameter optimisation will subsequently be extended to higher energies. Once the ZVKIN branch is optimised, its use for improving the flavour tag and the vertex charge performance will be explored. Beginning with obvious areas where this algorithm could be helpful, e.g. for B hadrons with short decay lengths and single-prong decays, we will investigate how best to combine ZVKIN results with information from the ZVRES section of the vertex finder. For example, we will assess if a subset of cases can be identified, in which ZVKIN results should replace those of ZVRES (e.g. in the flavour tag), or if results from both branches should both be used as inputs to the flavour tagging neural network (i.e. for the same jet).

Currently, the default flavour tag is based on the approach developed by R. Hawkings[12]. Variations on this approach will be studied in order to see if it can be improved. Possible changes include a different choice of input variables and a different set-up of the neural nets that combine these inputs to obtain the tag. For example, currently different neural networks are used, depending on the number of vertices identified in the jet. We will investigate whether this provides optimal performance. The network architecture, i.e. the number of layers and the number of nodes as well as their transfer function, will be changed, and the performance of the different training algorithms provided by the Package investigated. Further, we have started to use new "data mining" approaches to the flavour classification problem, rather than neural networks. Initial studies suggest that methods such as decision trees may provide similar levels of performance.

Using information from other detector subsystems may allow further improvements in the tagging performance. For example, increasing the precision measurements of the effective mass of jets using

high-energy neutral pions reconstructed in the fine-grained calorimeter may result in noticeable improvements in flavour tagging as this is one of the most powerful separation variables. Similarly, identification of leptons will help distinguish between b- and c-jets. Given that energy can be precisely measured for hadronic jets, while for semi-leptonic decays part of the energy is carried away by the neutrino, the ability to distinguish between jets containing semi-leptonic heavy hadron decays and purely hadronic jets would allow an improvement in the precision of the jet energy measurement. Another way in which one may profit from linking information from the different subsystems would be to use vertex-information to improve the assignment of tracks to jets.

So far, optimisation of vertex charge reconstruction for ILC conditions has been performed using a fast MC simulation. In the future, we will need study if the algorithm is still optimal when using GEANT4-based MC samples and realistic tracking as input. Determination of the quark charge sign is so far is restricted to cases in which a non-zero vertex charge has been reconstructed. In b-jets containing a neutral hadron, the quark charge sign can in some cases be determined from the charge-dipole procedure, developed at SLD, which is based on the results of the ZVKIN branch of ZVTOP.

Longer term plans

Tagging performance strongly depends on the errors of the input tracks. These track errors in turn depend on the hit errors from which the tracks are reconstructed. The hit locations and errors differ depending on the sensor technology assumed for the vertex detector. Currently, Gaussian smearing of the MC hit positions is used. The existing more sophisticated code is specific to the DEPFET sensor technology. For CPCCD and ISIS technologies, simulation code to adequately describe the processes in the sensors and the subsequent cluster finding step in the readout chip will have to be developed and used to address some of detector design issues that one can expect to show a significant dependence on these effects.

An example is the performance in the forward region, which is particularly relevant for the physics processes of interest at the ILC. This is related to the question of whether better performance is achieved with a long barrel vertex detector or with a design with a short barrel plus end-caps.

Software to simulate the alignment procedure for the detector will be needed to study the effects of misalignment and tolerances for the positions of sensors along the beam and perpendicular to it, determining the amount of sensor overlap required and hence influencing the detector design. Such software thus either has to be developed or existing software adapted and/or interfaced to the ILC software framework to perform these studies.

Studies of benchmark physics processes

While performance studies of impact parameter resolution, flavour tag and vertex charge reconstruction can already provide a wealth of information on which detector designs are preferable, a realistic investigation of the trade-offs between different designs will require comparing them at the level of the resulting measurement precisions achieved for relevant benchmark processes. Care needs to be taken in the choice of these processes, since they have to be both typical of the physics that the ILC will give access to and be sensitive to the vertex detector design. Theorists and experimentalists from the ILC community have studied which processes would best be suited for this purpose, and a report on recommended processes, chosen by a dedicated

"physics benchmark panel" has been published some time ago, and will form the baseline for the selection the processes that will be studied in the phase of preparation of the LOIs and the engineering designs.

Processes sensitive to the vertex detector design cover the areas of Higgs physics, SUSY studies and indirect searches for new physics. The remainder of this subsection describes which studies are currently underway, with further ones likely to be added in future.

Measurement of the Higgs branching ratios, especially for the decays of a light Higgs boson into $b\bar{b}$ and $c\bar{c}$ will be demanding in terms of vertex detector performance. While the recent study by Kuhl and Desch[13] was based on a fast MC simulation, with a parameterization of vertex detector performance derived from GEANT3-based full MC, new GEANT4-based studies are now under way in the Bristol and Edinburgh groups, aiming at a realistic comparison of different detector designs.

A study of $e^+e^- \to ZHH$, performed by Oxford in coordination with the SiD benchmarking group is also beginning. Analysis of the resulting multi-jet final states, with a large number of b-jets, will require excellent flavour tagging performance, and could profit from quark charge sign selection and the possibility to improve track-to-jet assignment using vertexing information.

As shown by Hewett and Riemann[14], the process $e^+e^- \to b\bar{b}$ will provide excellent sensitivity to new physics at the ILC. The study of this process, now begun in Oxford, will for the first time take into account the experimental limitations that arise from realistic flavour tagging, as well as from quark charge sign selection.

Another indirect search for new physics, being performed in Oxford and at RAL, is the study of anomalous Wtb coupling in $e^+e^- \to t\bar{t}$. Key observables for this study, such as forward-backward asymmetries and spin correlations, strongly depend on vertex detector information and hence permit the detector design to be optimised.

Cosmological data, such as the recent WMAP results, strongly constrain SUSY parameter space. Some minimal supersymmetric models could favour a light sbottom decaying to give rise to a low-momentum b-jet in the final state. Detection of these jets with sufficient precision will be sensitive to the material amount in the vertex detector. Guided by theoretical studies of which SUSY parameters correspond to a small sbottom neutralino-mass splitting, performed at RAL/Southampton, the Montenegro group in collaboration with Oxford will use a GEANT4-based detector description to study detector effects, and determine the ILC-sensitivity to the process using realistic tracking and vertexing.

Optimisation of the Vertex Detector design

Different vertex detector designs will be simulated in GEANT4 and compared both at the level of performance of flavour tag and vertex charge reconstruction and at the level of resulting measurement precision obtained in physics benchmark processes such as the ones described in the previous subsection.

Different geometrical arrangements of the sensors will be compared, related to questions of support material and sensor overlap required, linked to alignment studies, see above. GEANT permits

different support structure materials to be simulated, including foams such as silicon carbide foam and reticulated vitreous carbon foam. Material type and material amount of support, sensors, readout, drive etc, will be varied and resulting performance compared, and fed back into the ongoing design work in the mechanics work package.

It should be noted that not only the material amount in terms of interaction and radiation lengths is relevant, but also the fraction of the total space volume taken up by sensors and support. This is because the suppression of hadronic interactions may require discarding vertices found in the volume occupied by material. If this is a large fraction of the total vertex detector volume, inevitably decay vertices important for the reconstruction of physics processes will also be discarded, MC simulations having shown that for $e^+e^- \to b\bar{b}$ events at the nominal centre-of-mass energy of 500 GeV over 40% of tertiary vertices and roughly 25% of secondary vertices decay beyond the first vertex detector layer.

A study of the effect of varying the beam-pipe radius should be performed which, in contrast to the earlier LCFI study presented at Snowmass[15], should be based on full MC, take into account the effects of e^+e^- pair background and include the evaluation of flavour tag, vertex charge and resulting physics benchmark performance.

WP2 – Sensor Design and Production

Introduction

This Work Package is responsible for the design and production of the two sensor types that LCFI is developing for the VXD of the ILC, the Column Parallel CCD and the In-situ Storage Image Sensor. Two generations of CPCCD have now been manufactured by e2v technologies. With the first of these, CPC1, LCFI was able to demonstrate that the parallel readout concept it developed with e2v can be successfully realised. CPC1 is a two-phase device, with pixels of size 20 × 20 μm^2. Testing thus required the bump-bonding of a Column Parallel Readout chip to the CPC1 on a 20 μm pitch which carried out by VTT and represents the first time bump-bonding has been performed with an e2v CCD.

The second generation of CPCCDs, the CPC2, includes devices close to the size required for the VXD, as is shown in Figure 5. In particular for the largest version of these CCDs, the distribution of the high speed clock pulses becomes problematic. The resistance of the buslines and the polysilicon gates to which they supply the clock signals is sufficient to significantly degrade the clock amplitude at the points most remote from the drive signal input. Metal buttressing of the polysilicon gates goes some way to solving this problem, but the large intergate capacitance of the CCDs and the large clock currents that are needed as a consequence thereof ensure that this is not enough. Some of the CPC2 devices therefore incorporate a further innovation developed by LCFI, a double metal layer which allows the entire CCD surface to be used for distribution of the clock signals. The first metal layer is separated from the gates by a layer of silicon dioxide, through which connections are made to the phase one gates. The second metal layer is insulated from the first using a layer of polyimide. Connections are made from it to the phase two gates through holes in the lower metal layer. Similar holes are introduced into the upper metal layer to ensure the clock distribution is as symmetric as possible. The testing of these “busline free” CPC2 devices is described in the WP5 section of this report.

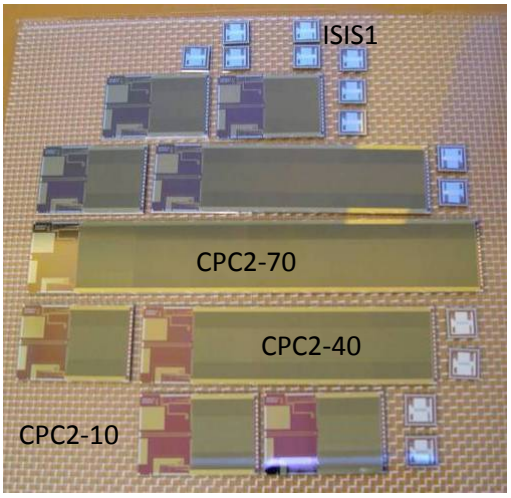

Figure 5 The sensors resulting from dicing one CPC2 wafer; the size of the imaging area of the CPC2 sensors varies from 13 × 15 mm^2 (CPC2-10) to 92 × 15 mm^2 (CPC2-70). Several In-situ Storage Image Sensor (ISIS1) chips were also incorporated on this wafer.

While the double-level metal concept provides a route to clock distribution in the CPCCD, reducing the capacitance of the device and hence the currents needed to drive it remains desirable. This would simplify the drive circuitry and also reduce the power consumption of the device. LCFI has therefore designed a range of novel structures aimed at reducing the main component of the CPCCD capacitance, that between the gates. These CPC-T devices, currently being manufactured by e2v, include structures such as that illustrated in Figure 6. In this "open phase" concept, the geometrical overlap between the gates is reduced, leading to decreased capacitance. More than twenty variants of the CPC-T will soon be available for testing and promise to provide reductions in the intergate capacitance as large as a factor of 4. The most successful of these new concepts will be incorporated in subsequent designs of the CPCCD.

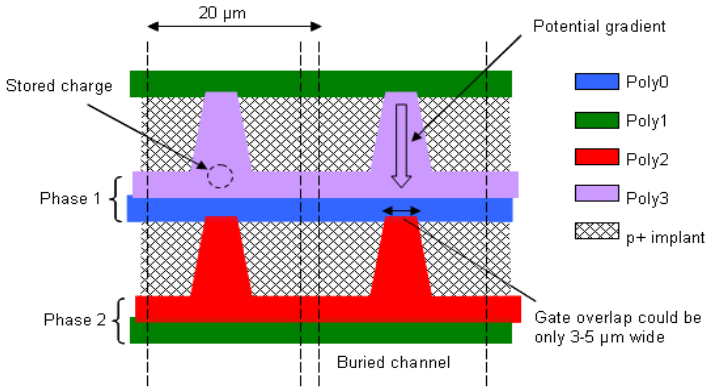

Figure 6 An "open phase" CCD structure, one of the approaches to reducing the intergate capacitance of CPCCDs being explored by LCFI.

Progress with the design of the second sensor that LCFI is developing, the ISIS, is as yet less advanced. This new sensor is ideally matched to the ILC environment. The concept, illustrated in Figure 7, allows storage of the signals in small CCD-registers incorporated in each pixel during the bunch train. This is extremely robust, making the signal charge of 2000 e^- or so immune to any electromagnetic interference (EMI) that is present at the ILC. Conversion of the stored charge and readout occurs during the intertrain gap, when the major source of EMI has been removed and allowing relaxed column parallel readout speeds of about 1 MHz.

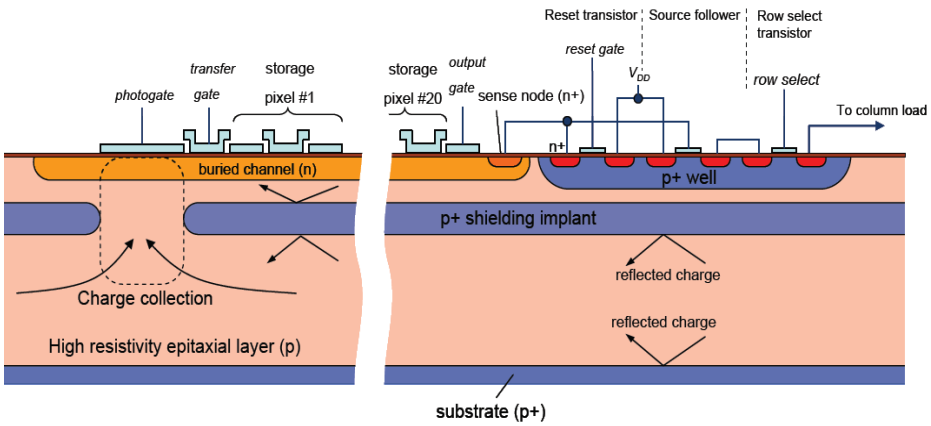

Figure 7 The operating principle of the ISIS sensor, signals produced in the epitaxial silicon are collected on the photogate and transferred to an in-pixel CCD register 20 times during the ILC bunch train. The CCD and on-pixel electronics are protected from the signal charge by the deep p+ shielding implant.

Proof of principle devices, with and without the p-well illustrated in Figure 7, have been successfully tested by LCFI. All control signals were generated externally in these large pixel proof-of-principle devices and efforts in this WP are now concentrating on designing devices with pixel sizes closer to those ultimately needed and in which the control signals can be produced on chip. This requires the production of very small CCD registers and the marrying of CMOS and CCD processes in the fabrication procedure.

Small pixel CCDs are already routinely produced by several manufacturers. Typically, however, these devices do not have the overlapping polysilicon gates found on the larger pixel devices manufactured by e2v. This can lead to problems when they are irradiated. Electron-hole pairs are produced in the SiO_2 insulation between the gates and while the electrons rapidly diffuse away, the holes remain trapped in the SiO_2. With overlapping gates, where the gate polysilicon extends over the intergate SiO, this does not cause potential shifts in the silicon between the gates. If, however, the gates do not extend over the intergate SiO_2, the trapped positive charge may significantly affect the potential in the underlying silicon. The signal electrons may then be prevented from travelling through the silicon by the potential pocket caused by the trapped charge and hence never reach the readout electronics.

A further requirement is that the small CCD registers can be driven with voltages compatible with CMOS electronics. CCDs are typically operated at relatively high gate voltages and reducing these may lead to increases in the Charge Transfer Inefficiency (CTI).

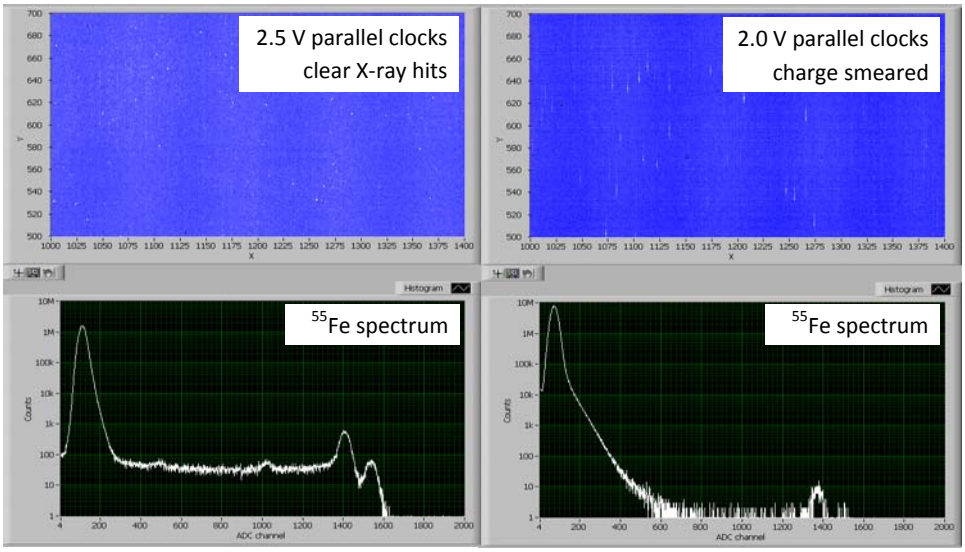

Figure 8 Performance of DALSA FTF2416 at very low parallel clock amplitudes. Even at 2.1 V, the Mn K_α and K_β lines are clearly resolved due to the very low readout noise. The serial clock frequency is 20 MHz. This level of performance was maintained after irradiation.

LCFI has studied these problems using several FTF2416 CCDs which were provided by DALSA. These are 4 Mpixel image sensors with 9 μm square pixels and non-overlapping gates, a technology which could produce 3-phase pixels as small as 2.5 μm. The FTF2416 CCDs were tested, irradiated and tested again. As is shown in

Figure 8, these performed very well. Drive voltages as low as 2.1 V resulted in excellent performance, which was maintained after irradiation with a ^{90}Sr source to doses of 76 krad. This gives us confidence that the CCD registers of the ISIS can be constructed using existing non-overlapping gate

fabrication procedures and design studies are now proceeding on this basis with several manufacturers.

Future Programme

Column Parallel CCD developments

LCFI will continue the CPCCD development by designing and manufacturing a third generation device in the second half of 2009. The CPC3 chip will be a fully custom, large CCD, manufactured on 6" wafers. The chips will have sizes of approximately 120×20 mm^2, large enough for construction of prototype ladders. The CCDs will be back-thinned to 20-50 μm as part of the integration process with the readout and driver chips. Due to the large device size only, 2…3 CCDs can fit on a wafer and the yield is expected to be below 10%, necessitating the production of the order of a few hundred wafers. The total design and manufacturing cost is estimated to be at least $900k.

The design of CPC3 will be influenced heavily by our two previous successful prototypes, CPC1 and CPC2. The results from our dedicated CCD test series for capacitance and clock amplitude reduction (CPC-T) will also be taken into account after evaluation in early 2008. The main goal of the CPC-T device tests is to verify that the effective CCD gate capacitance can be reduced by at least a factor of 2, which would greatly simplify the on-chip clock distribution. If no significant capacitance reduction can be achieved, then the "busline-free" 2-level metallisation from CPC2 is likely to be refined and used in CPC3.

The CPC3 mask set will also contain a smaller CCD with common design (CPC3-S) for tests of the readout and driver chips and some aspects of the integration without using the valuable large area CPC3.

One still unresolved issue is the type of CCD outputs to be used in CPC3. In CPC1 and CPC2 there are two types, voltage output via a single stage source follower and direct charge outputs. Single stage source followers require about 2 W of continuous power on the CCD, while the charge outputs consume no power. The voltage channels have been much better evaluated than the charge channels in CPR1 and CPR2. Both types of outputs are connected to voltage or charge CMOS amplifiers on the readout chips, which use similar power. Assuming 120 CCDs and a 1% duty cycle, the additional power dissipation from the single stage source follower outputs for the whole detector is 2.4W. Given this small difference in power, the final choice will depend upon the performance of the two types of readout chains. This is being evaluated in the present CPC2/CPR2 assemblies and will be studied further in the forthcoming CPC2/CPR2A configuration.

Due to the nature of the remaining R&D work, there is some uncertainty in the output of the CPCCD programme, in particular in the transfer of results from CPC-T to CPC3. This could delay the design of CPC3 or necessitate another small-scale device before the full size CCD is made.

ISIS developments

The ISIS programme is presently less mature than the CPCCD development, but the potential benefits of a successful ISIS device on the performance of the vertex detector make it worth pursuing.

LCFI plans to design and manufacture a second generation ISIS2 chip in the first half of 2008. ISIS2 will be a small device, of size about 1 cm^2, and will incorporate an array of pixels with all the necessary on-chip logic for addressing and clocking. No dedicated readout chip is envisaged for the ISIS2, instead a sufficiently wide contiguous block of columns (e.g. 16-32) will be read out by discrete external electronics.

With the ISIS2, LCFI will aim to demonstrate the functionality of a device with 20 CCD storage cells in a pixel that is not much larger than the target of $20 \times 20\ \mu m^2$. The most important goals for ISIS2 are:

- Demonstrate CCD buried channel operation in a submicron CMOS process.
- Successfully use a p+ implant to shield the CCD storage register from parasitic charge collection. This implant should not interfere with the buried channel doping.
- Integrate control and clock driving in CMOS logic on the chip.

The ISIS2 will probably be made on a 0.18 μm CMOS process. The CCD gates will be non-overlapping, unlike those of a traditional CCD, because 2-level polysilicon is not offered as part of the CMOS process. Our radiation damage tests of a CCD made with non-overlapping gate technology did not show any problems from the open gaps between the gates, and we are reasonably confident that there is no additional risk in using this design.

In ISIS2 we will integrate 256×256 or 512×512 pixels in the largest device, as well as several smaller arrays designed to test different variants of the architecture.

We are planning to manufacture the next generation ISIS3 in the second half of 2009. The ISIS3 will be a full-scale chip with similar dimensions to the CPC3. To achieve this, the ISIS3 will have to use stitching, which is routinely done in the CCD processes but is a relatively novel area for CMOS manufacturers. In addition to the standard costs for the masks and wafer production, we expect to contribute towards setup costs and development for the stitching. The yield of such large area CMOS chips is unknown and if it turns out to be very low this could be a showstopper. We are planning to start work with the chosen vendor during the ISIS2 design and manufacture phase to establish the potential risks as regards yield and develop methods to circumvent these where possible.

An additional advantage of using the CMOS process for the ISIS is the possibility this offers of integrating the readout electronics in a single monolithic device. Because the ISIS is read out in a column parallel fashion, as is the CPCCD, the front-end voltage channels and ADCs from the CPR development line are directly applicable to the ISIS. All the information from the ISIS can be transferred off-detector in the 199 ms available for readout in the intertrain gap without the need to for data sparsification. The transfer of the front-end architecture from the CPR chips into the CMOS process for ISIS3 may require some re-design because of the different feature size (0.25 μm in CPR1/2, 0.13 μm in CPR3).

We will also produce a smaller device (ISIS3-S) with the same design as ISIS3 but with a reduced number of rows. The yield of ISIS3-S is expected to be higher than that of the more expensive full size ISIS3 and the device will be used for most of the tests. The design and production costs for the ISIS3 are expected to be around $900k.

WP3 Readout and Drive Electronics

Introduction

This WP is concerned primarily with the design and production of the drive and readout ASICs for the Column Parallel CCDs which LCFI is developing. The device that has been designed to produce the clock signals is the Column Parallel Drive chip, CPD1. This chip is described here, and information on the results of its testing in the WP5 section of the report. Readout for the CPCCDs is provided by the Column Parallel Readout chips CPR1 and CPR2, the pitch of which must match the $20 \times 20\ \mu m^2$ size of the pixels of CPCCDs. The CPR1 and the CPR2 are described briefly here, as is the design of the CPR2A, which addresses some of the problems identified in the testing of the earlier readout chips.

CPD1

This CPCCD clock driver ASIC is optimised to produce the high currents of up to about 20 A that are necessary to drive the CPCCDs. The CPD1, shown in Figure 9, provides signals to drive the two-phase CCD gates at 50M Hz and 25 MHz in the inner and outer layers of the VXD, respectively. The capacitance of the sensors is 40 nF in the inner and 127 nF in the outer layer. Higher currents are thus needed to drive the larger outer layer sensor, despite the lower frequency at which these are operated.

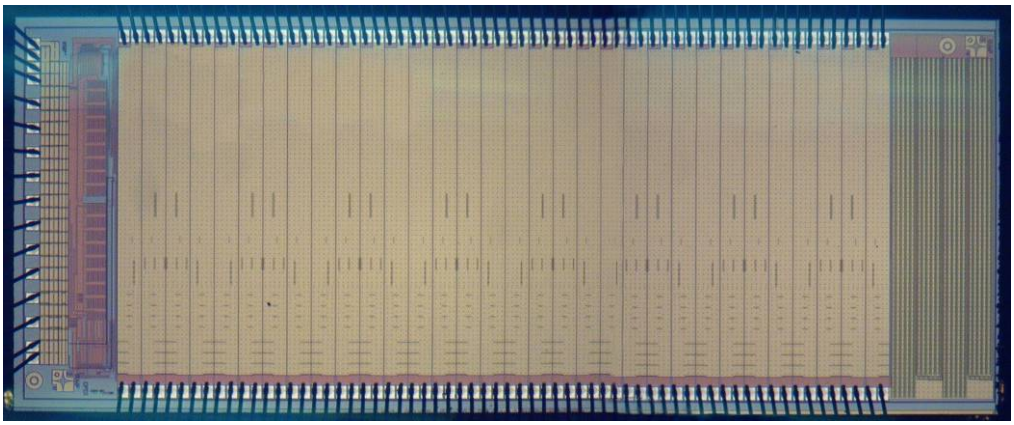

Figure 9 Photograph of a CPD1.

The CPD1 has a size of $8 \times 3\ mm^2$, with the main power supply pads, on a 100 micron pitch, along one of the long edges of the chip and the clock outputs on the other. The control pads are place along one of the short edges, on a 200 micron pitch. The CPD1 layout is segmented into 8 blocks, each with 4 pads for Phase 1 and 4 for Phase 2. The segments are enabled when the corresponding bits in the control register are set high. This allows the CPD1 to be used with a wide range of load capacitors. Testing this chip is complicated by the effects of the inductance of any wire bonds used to connect it to an external load. Hence, for test purposes, two Driver outputs are permanently connected to an on-chip 2 nF capacitor via wide metal tracks. The Driver performance for these channels will not be limited by the external bond wire inductance and is closer to that achievable when the CPD1 is wire-bonded to a sensor. The configuration of the drive pads on the CPC1 and CPC2 does not allow this, so tests with a wore-bonded CPD1 must await further generations of the CPCCD.

The chips have programmable current limits, so triangular-wave drive is possible over a range of frequencies down to about 100 kHz. The triangular signal shape results in lower currents than for square waves, which minimises clock feed-through and power supply transients. Positive and negative currents are independently adjustable, which allows balancing of the two clock phases.

CPR1

The CPR1 is an ASIC that can readout 250 columns of the CPC1 and CPC2 sensors. Half of the CCD columns are connected to voltage amplifiers which are driven by the source followers on the CCD. The other columns, which do not have source followers, are connected directly to charge amplifiers on the readout chip which have 3 fF feedback capacitors. Both types of amplifier are designed to produce signals of about 100 mV for the signal of 2000 electrons that is typically produced when a minimum ionising particle traverses the 20 μm thick epitaxial layer of the CCD.

The signals are digitised by 5-bit flash converters laid out on the same pitch as the CCD (20 microns) and the results are stored in a memory array, accessed via read and write pointers.

The CPR1 has been bump-bonded to the CPC1 and tested with X-rays. Both the voltage and the charge channels worked well, but there were some variations between channels and limitations in the operating range of the ADC.

CPR2

The CPR2 is a considerably more ambitious development of the CPR1. The same layout is maintained, with charge and voltage sections on a pitch allowing the chip to be bump-bonded to the CPC1 and CPC2 and the chip is fabricated using the same IBM 0.25 μm CMOS process. Improvements to the analogue circuitry are made and data sparsification logic is added to the chip. The distribution of the ADC clock signals is also improved, allowing faster clock edges across the whole chip width. This overcomes the ADC range problems observed in CPD1 and gives better uniformity.

The sparsification logic detects cluster kernels of 2 x 2 pixels in which the signal is above a global threshold. An extended cluster of size 4 × 9 is then defined around this kernel and read out. Time-stamp and positional information are attached to the charge data from the pixels.

As is described in the WP5 section of this report, the voltage amplifier sections of the bump-bonded CPR2/CPC2 assembly work well over a wide range of ADC settings. The charge amplifiers, however, suffer from some noise or instability, perhaps due to fluctuations in the substrate voltage. It is possible that this is caused by the increased amount of clock buffering in the ADC, with its associated power supply transients. Such interactions illustrate the necessity to plan for several development cycles in a project as complex as the design of the readout chip for the VXD sensors. It is extremely difficult to anticipate or simulate all aspects of the behaviour of such a chip. As is discussed below, LCFI anticipates that at least two further CPR generations will be needed before it has a chip able to readout full size sensors at the data rates imposed by the ILC.

Tests of the CPR2 have also shown that, while the analogue offset matching is improved compared to the CPR1, there is still some gain variation in the voltage amplifiers. The sparsification logic functions well, but dead-time is introduced at high occupancies due to the limited memory available on the CPR2.

CPR2A

The CPR2A is an iteration of CPR2. The same layout is maintained, allowing it to be used with the available CPC1 and CPC2 sensors. Major improvements have been in the data handling. Compaction of the CPR2 layouts has allowed an increase in memory depth by a factor of three as is illustrated in Figure 10. The CPR2A can process more complex sequences of clusters, including those close together in time. This makes a big difference in the ability to handle realistic patterns of data derived from physics simulations. The ADC clocking will operate with lower drive capacity: it has been tuned to allow propagation of the signals across the chip while reducing the power supply transients. This is expected to stabilise the charge amplifiers, allowing a realistic comparison between voltage and charge readout modes.

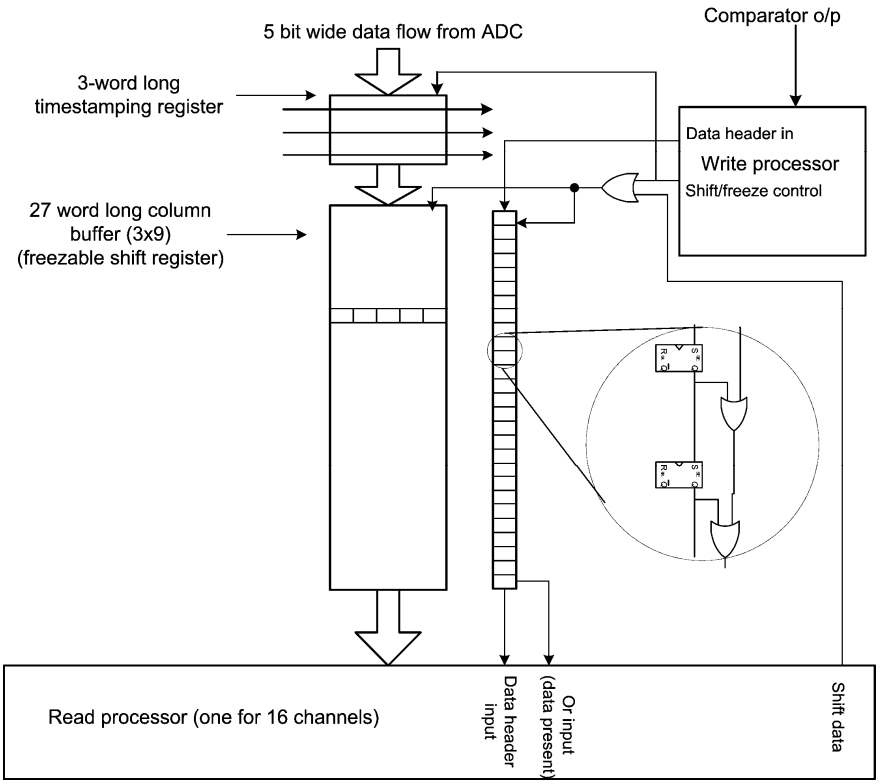

Figure 10 A block diagram of a section of the CPR2A showing the extended column buffer which can store 27 words of data, enough for 3 clusters including the time-stamp data. A data header register has been added in order to keep track of multiple clusters within the column.

Future Programme

The steps foreseen in the development of the readout and drive chips for the LCFI sensors, culminating in the production of chips that are suitable for use in the VXD, are described in the following.

CPR2A design and testing

The design of the CPR2A is largely complete, but some details still require implementation. One of these is the addition of a calibration test register. This will allow the injection of test signals directly to selected analogue inputs, a useful facility for the testing of the chip. Before submission for fabrication, simulations of the charge and voltage amplifiers will be performed, including a full description of parasitic effects, in order to understand the gain variations seen in CPR2. Some further

optimisation of the layout of the amplifiers and ADCs will be performed in order to improve analogue performance.

Once the CPR2A has been manufactured, a full evaluation of its digital functionality will be performed. Thorough tests of the charge and voltage-mode amplifiers and the ADC will also be carried out using for wire-bonded CPR2A chips. These tests will cover a wide frequency range, and will use the on-chip calibration register where appropriate.

Tests of bump-bonded assemblies of the CPR2A and the CPC2 will then be carried out, with particular emphasis on understanding and optimising the amplifier performance. One of the aims of these tests will be to decide whether to use the charge or voltage mode for future designs.

CPR3

The next generation readout chip, the CPR3, will have a width of about 11 mm and be designed to readout a CPCCD with 500 channels. The CPR2A design with the preferred amplifier configuration will be translated to the CPR3 dimensions on a 0.13 micron CMOS process. The chip will be modified to simplify the drive signals and analogue biasing, reducing the number of pads needed for control signals and the complexity of the test board. The digital circuitry will be optimised for the wider CCD format and more complex data handling algorithms will be implemented to minimise dead-time effects at higher occupancies. In particular, options for high-speed data transfer off the CPR3 will be explored. This will include investigation of non-sparsified read-out, which becomes favourable if background rates increase significantly over current predictions.

After final design, layout and manufacture, the performance of the CPR3 will be verified in wire-bonded format before full testing of the CPR3 bump bonded to the CPC3.

CPR4

Currently we foresee that the CPR4 will be the chip used in the VXD. It will have a width of 21 mm, matching that of the full scale CPCCDs, and will capable of reading out about 1000 channels. The CPR4 will be an adaptation and development of the CPR3 design, taking into account the results obtained in the testing of the CPR3. Particular care will be needed to the modelling of parasitic capacitances and resistances in order to maintain the high speed capability of the chip over its extended width.

Again, following final design, layout and manufacture, the performance of the CPR4 will be verified in wire-bonded format before full testing of bump-bonded CPR4/CPC3 assemblies is carried out.

Design challenges for CPR3 and CPR4:

The particular challenges we anticipate in the design of the CPR3 and CPR4 include the transmission of digital signals over the extended chip width without creating too much digital noise on the power supplies and the substrate. The switch to 0.13 micron technology will help here, as the additional metal layers have much reduced capacitance to substrate. Metal layers can also be connected in parallel to produce lower resistance.

A further challenge is that of getting the large amounts of data off the chip generated even at only 1% occupancy. This implies that a large number of digital output pads must be driven at high speed in order to cope with the data rate. It may be possible to adopt low-voltage and/or differential

signalling to minimise the resulting coupling to the sensitive analogue inputs. Such coupling could easily cause unacceptable noise levels.

Translation of the CPR2A design to a smaller CMOS process will be non-trivial in some area. The analogue designs may need to be reconfigured to work at the lower supply voltage. The 0.13 micron process has the option of dual power supplies, of 1.2 V and 2.5 V, which could be a solution for some blocks of circuitry.

Budget and time scales

Wafer costs for the above development are likely to be in the range of $800 k to $1000 k.

The time anticipated for the completion of the CPR2A is 2 months, with one engineer working full-time on the project. It is anticipated that the manufacture of the CPR2A will take 3 months and that testing of the CPR2A in wire-bonded mode will take an additional 2 months.

It is expected that the design of the CPR3 design will take about 12 months. We plan to start this work immediately after the submission of the CPR2A chip. CPR3 manufacture is likely to take 3 months, but would not be started until successful testing of bump-bonded CPR2A/CPC2 assemblies. As in the case of CPR2A, we anticipate that testing the CPR3 in wire-bonded mode will take 2 months.

Following successful CPR3 testing, a design period of 6 months is assumed for CPR4 design with subsequent periods of 3 months for manufacture and 2 months for testing in wire-bonded mode. We thus consider it possible to begin tests of a bump-bonded CPC3/CPR4 assembly in 2010.

WP4 – External Electronics

Introduction

The testing of the sensors described in this report requires the development of electronic systems which provide all the necessary control, biasing and monitoring functions needed for the sensors. This is the responsibility of Work Package 4, as is the provision of the interface for the CPCCD and its column parallel readout (CPR) chips to the external world, the test systems for the column parallel drive (CPD) chips, boards for the study of the CPC-T devices and test systems for the ISIS devices. This section presents examples of the developments necessary. These typically require careful design as drive signals with significant current have to be supplied at high frequency without causing noise which could disturb the small signals from the sensors. Significant electronic engineering expertise is therefore needed for the success of this Work Package.

In the following, examples are given of some of the developments that have recently been made, such as the test boards for the CPD1 and CPC-T, the latest motherboard for the testing of the CPC2 and the transformer drive that was developed for test purposes before future developments are discussed.

CPD1 test board

An example of the boards that have been constructed for the testing of individual components is that produced for the CPD1 driver chip. This was designed to allow the full functionality of the chip to be exercised and allows the connection of a capacitive load with low inductance. The board is controlled by the Collaboration's BVM2 VME module, which downloads control information to a shift register in the CPD1 through a serial link and also provides all the necessary timing signals. One such board is shown in Figure 11

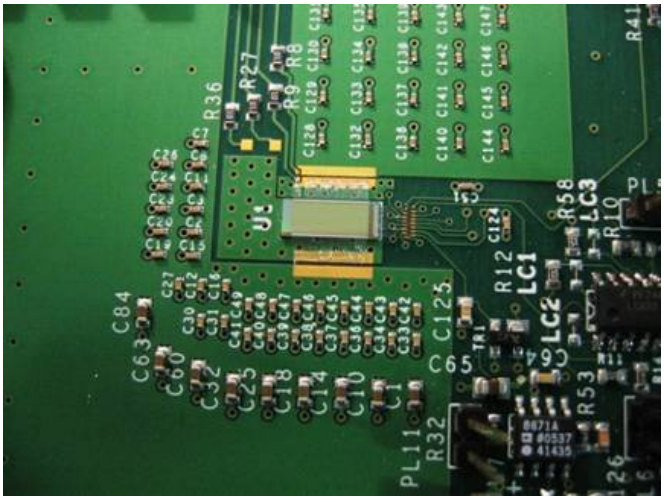

Figure 11 A CPD1 chip mounted on its test board.

CPC-T test board

A further board has been produced for studying the CPC-T test devices. The board has three main functions: to clock the CPC-T at frequencies up to 50 MHz, to amplify four output signals and to measure the gate capacitance. The capacitance is measured by observing the clock current in the

clock line. This is done using a differential amplifier to amplify the signal across a small series resistor.

CPCCD motherboards

The development of the motherboards for the testing of the hybrid CPCCD/CPR assemblies is a challenging task due to the large number of components and the overall complexity of the systems. The boards must provide all the bias voltages for the CPCCD, the necessary drive signals and cater for the electronics associated with the readout chips. In the motherboard, the assemblies are placed in a well in the PCB to minimize the length of the wire bonds connecting the CPCCD to the clock driver system. The boards are equipped with low noise amplifiers for the discrete source follower outputs on the CPCCD which allow access to the analogue output signals. They also feature temperature monitoring and control for work in a cryogenic environment.

The focus of recent work on motherboard design was the production of motherboard 5.0 (MB5.0) which uses the CPD1 driver chip. The part of the board responsible for the driver chip is a new addition to the motherboard designs. MB5.0 also uses an improved grounding scheme and four 50-pin onboard Flexible Flat Cable connectors provide a tidier solution for connections to and from the boards than the previous cabling arrangements. A photograph of a fully assembled MB5.0, with a CPC2-70 and two CPD1 chips attached, is shown in Figure 12. The first MB5.0 has been successfully used for the busline free CPC2 testing described in the WP5 section of this report.

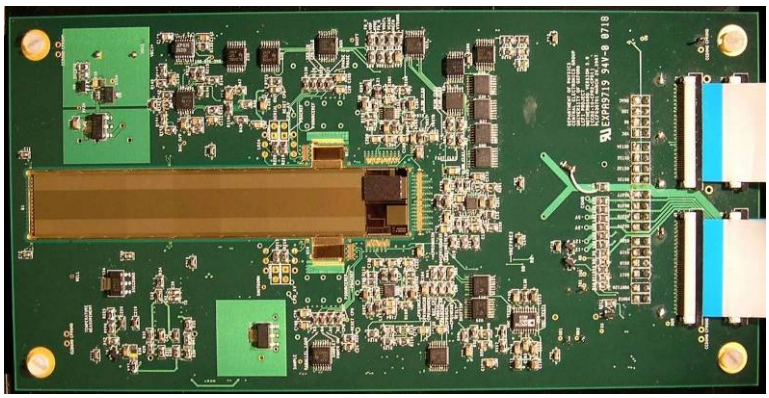

Figure 12 A CPC2-70 sensor mounted in a MB5.0 with one CPR2 readout and two CPD1 driver chips.

Earlier versions of the motherboard, assembled before the CPD1 ASIC was available, used either commercial driver MAX5057 chips or transformers constructed in the multilayer PCB and driven by a RF amplifier to provide the drive signals for the CPCCDs.

Transformer drive

Miniature air-cored planar transformers, implemented in a multi-layer PCB offer a relatively inexpensive and easy to implement solution for the drive system of the CPCCD. The gate impedance of the CPCCD at high frequencies is very low and is dominated by the capacitance. Step-down transformers can provide the high current needed to drive this large capacitance, in excess of 10 A even for the smaller CPCCDs. A transformer ratio of about 16:1 allows the primary winding to be driven from a commercial RF power amplifier.

Measurements of the double level metal CPC2 sensors performed using such a system successfully demonstrated operation at 45 MHz, but showed the limitations of our first implementation of the transformer drive. The tests revealed a phase imbalance at high clock frequency. Simulations showed that parasitic inter-winding capacitance in the transformer is responsible for this effect. An optimized transformer design with circular coils, see, is now under investigation. This will be implemented in the next revision of the motherboard with transformer drive. Now that it is clear that the CPC2 can be driven at frequencies of 45 MHz, as described in the WP5 section, this system can be optimised for a narrower range of frequencies.

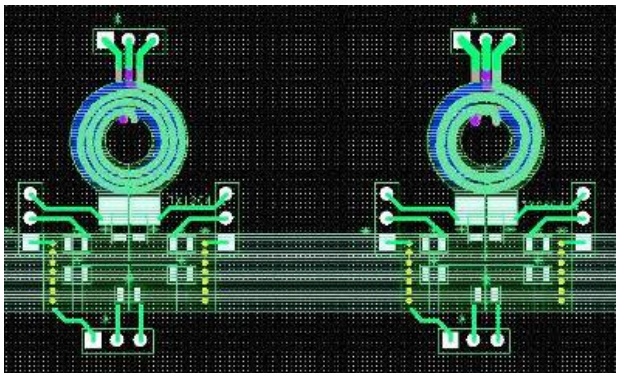

Figure 13 Clock transformers with circular design.

Data acquisition

The data acquisition and control system used so far is based around a VME module, BVM2, to which various daughter boards can be attached. These provide control for all commercial or custom-built electronics used in the LCFI test programme.

The core of the system is the VME Sequencer module which generates all the signals needed for clocking, synchronisation and timing. The data capture from the discrete CCD outputs is accomplished by a commercial 4-channel, 12-bit fast ADC. The data from the readout chips is collected in a RAM on the BVM2. The functionality of the VME system is defined by the Verilog code in the Field Programmable Gate Array (FPGA) on each board. The user interface and higher level programming for the DAQ is done using LabVIEW.

Presently, around 15 BVM2 sequencer modules are successfully used in multiple LCFI test stands in several institutions. Future DAQ work will require an improved version of the module, BVM3, with software control of many functions which are currently hardwired in BVM2. Other new features will include a more powerful FPGA, more LVDS I/O, increased memory and more diagnostic LEDs. The module will have dedicated connectors for synchronisation of several BVM3 daughter boards and also allow phase-locked loop clock distribution from the master to slave boards. These features will be especially useful for test beam studies.

Future Programme

Test and mother boards

The future programme for WP4 is closely coupled to the production and testing of the CPC3 and ISIS2 devices LCFI plans to produce, as well as to the testing of new CPR and perhaps CPD chips. This

work will build on the existing versions of the CPCCD motherboards, but will also require some serious modifications to accommodate new features of the chips.

A further set of boards must be developed for stand-alone tests of the new CPR and CPD chips. The experience gained with their operation will then be implemented in the designs of the CPCCD motherboards. It estimated that two revisions will be required for the CPR and CPD test boards and four revisions of the motherboards. The latter includes a special motherboard for use in test beams.

A similar series of boards to that required for the development of the CPCCD will be needed for future versions of the ISIS.

In order to satisfy the requirements of the vertex detector technology comparison, full scale ladders must be tested with electronic systems suitable for application at the ILC. For example, the drive and readout of the CPCCD must be incorporated at the end of a ladder, and the necessary control signals generated in “remote” electronics. Similar considerations apply for the ISIS, where the readout may be incorporated on the same wafer as the sensor, but control signals will be provided by external electronics. It is very possible that the electronics in the vicinity of the ladder may need to be implemented in a technology which can provide a finer pitch or greater mechanical flexibility than the PCBs used to date. Thin film ceramic or multi-layer kapton technologies will be investigated here.

The production of the external electronics required for the operation of the CPCCD, and the ISIS are complex tasks and will require significant engineering effort. The production of the multitude of systems necessary to test the CPCCD and its readout chips, and the ISIS will require sustained expert engineering involvement in the project. Once functioning sensors have been produced, further design work will be geared towards the production of prototype ladders.

LCFI estimate that years of electronic engineering effort are required for this section of the programme. Funding at the level of about $230k for the PCB boards and $60k for the ladder integration is needed, while a further $100k is needed for other equipment.

WP5 – Integration and Testing

Introduction

This Work Package is responsible for testing the sensors developed by LCFI, with their readout and control electronics. Some of the recent progress achieved in these tests is presented in the following before the future programme is discussed.

CPCCD, CPD and CPR tests

Successful operation of the CPCCD at the ILC requires that sensors of length about 10 cm be integrated into ladders with the necessary drive and readout chips. The sensors in the inner layer must be driven at about 50 MHz to avoid occupancy problems, while those in the outer layers, where the rate of e^+e^- pair background hits is smaller, must be driven at about 25 MHz. LCFI has demonstrated that the double level metal versions of CPC2-10 can be driven at 45 MHz, as is shown in Figure 14. This speed was achieved using the transformer drive system which introduced high noise levels for the reasons discussed in the WP4 section of this report, a problem that will be addressed with the boards currently under development.

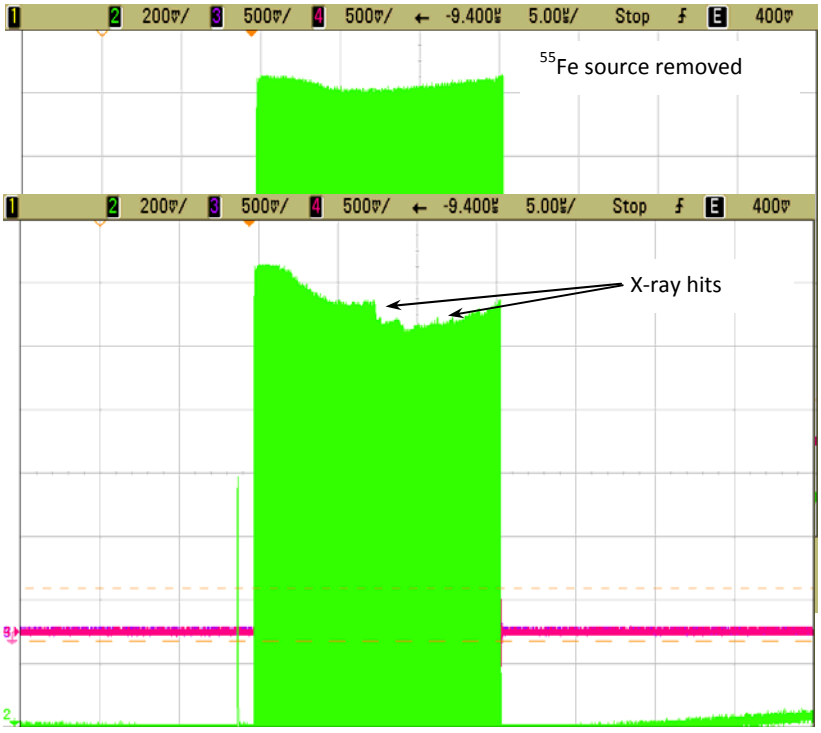

Figure 14 Oscilloscope traces of a discrete 2-stage CPC2-10 output at 45 MHz clock frequency with and without an ^{55}Fe source.

Studies of the CPD1, using the dedicated test board described in the WP4 section of this report, have shown that it can deliver the clock current of about 20 A needed to drive the largest CPCCDs. Clock currents of 20 A were demonstrated at 50 MHz using both the internal 2 nF and an external 40 nF capacitive loads. In the former case, the load is driven by one of the eight sections of the CPD1 and the current quoted is that obtained by extrapolating to the performance that would be obtained if all eight sections were driving a commensurately increased load. In the latter case, all eight sections

of the chip are driving the external load. An oscilloscope trace of the two clock phases and their difference is shown in Figure 15 for the 2 nF internal load.

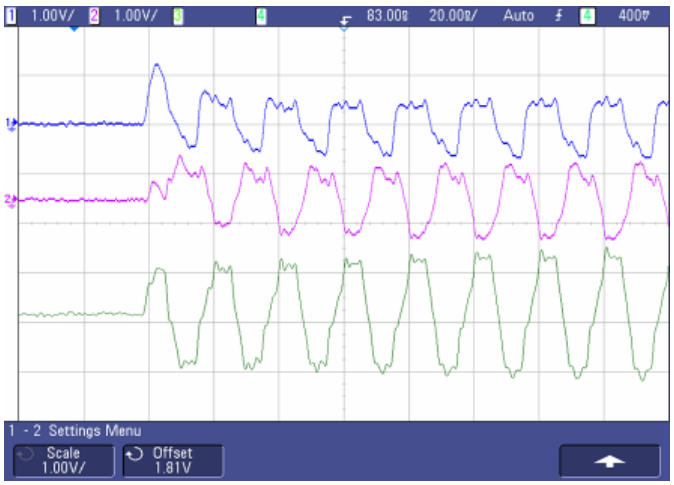

Figure 15 Oscilloscope trace of the two clock signals produced by the CPD1 and their difference.

That this chip can successfully be used to drive the CPC2 is illustrated in Figure 16. Shown is the X-ray spectrum obtained using an ^{55}Fe source with a CPC2 sensor driven using the CPD1. The noise performance of the system dramatically improved with respect to that obtained using the RF amplifier and transformer drive, confirming that it is the problems of this drive system that are causing the large noise levels visible in Figure 14.

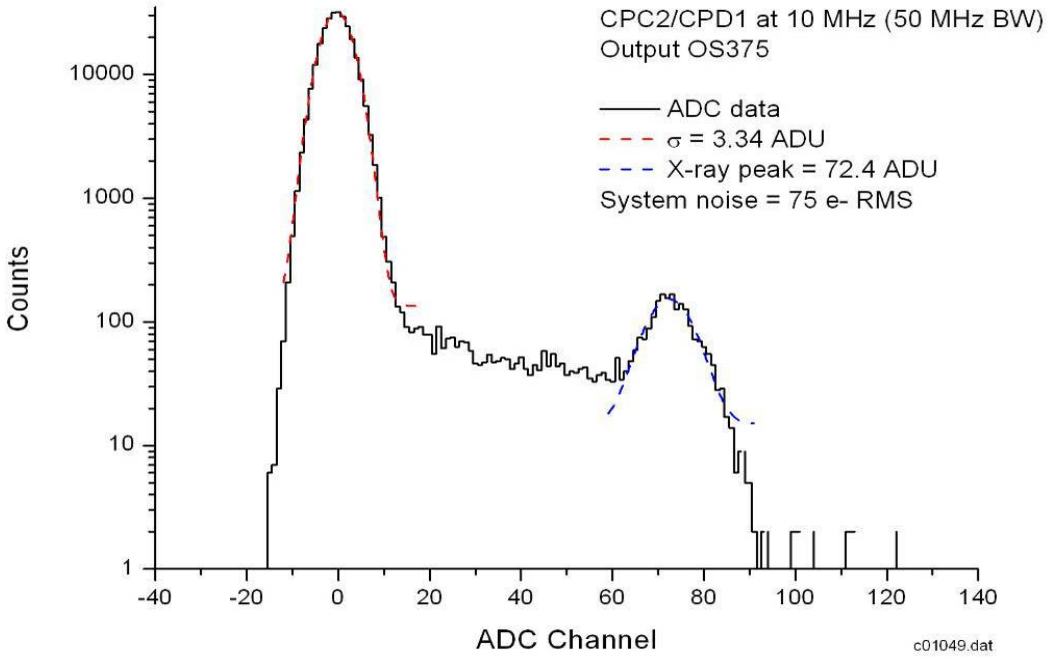

Figure 16 The 55Fe X-ray spectrum obtained using a CPD1 to drive a CPC2 sensor, comparison of the position of the X-ray peak with the width of the noise distribution show that the system noise is 75 e$^-$.

Following standalone tests of the CPR2 readout chip, which demonstrated the functionality of the sparsification logic, the CPR2 was bump-bonded to the CPC2 and the integrated package tested using an ^{55}Fe source. Hits due to the X-rays from this source can be seen in Figure 17, which

illustrates how the CPR2 has successfully identified the pixels of the CPC2 which contain X-ray signals and has flagged these and the surrounding pixels for readout.

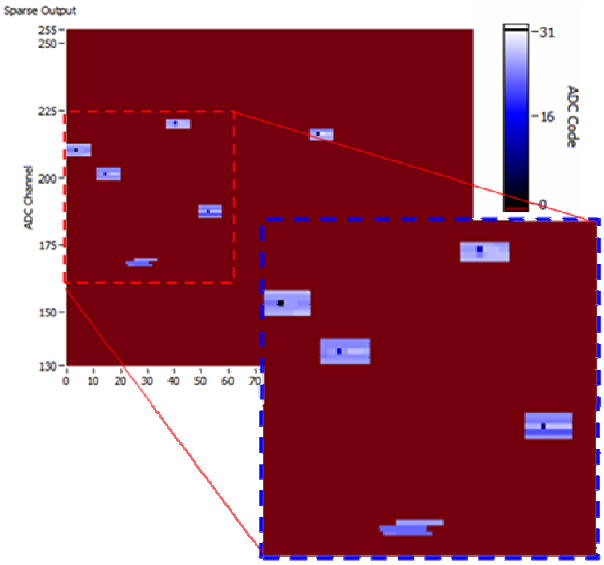

Figure 17 Output from a bump-bonded CPC2/CPR2 assembly, showing the hits recorded by the sensor and how these are identified and flagged for readout by the sparsification logic.

Using this bump-bonded assembly, ^{55}Fe spectra were produced for each channel of the chip, allowing the performance of the bump-bonded assembly to be mapped out. An example is shown in Figure 18.

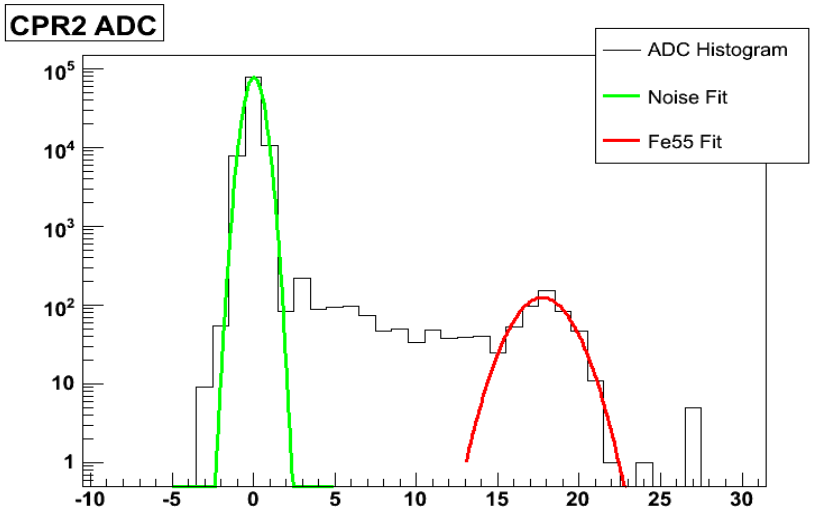

Figure 18 The ^{55}Fe X-ray spectrum recorded using a bump-bonded CPC2/CPR2 assembly.

The remaining step necessary to integrate all the components needed for a CPCCD ladder is to drive the CPC2 using a CPD1 chip. This cannot be done at high speed, as the CPC does not have clock input pads to which the CPD1 can be bump-bonded. However, the MB5.0 discussed in the WP4 section of this report and illustrated in Figure 12 uses wire-bonded CPD1 chips to provide the drive signals for the CPC2. First results from the operation of this CPC2, CPR2 and CPD1 assembly are shown in Figure 19.

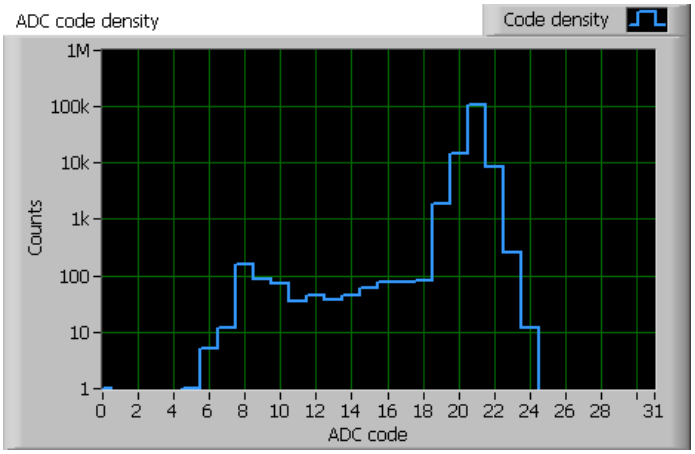

Figure 19 Spectrum of X-rays from an ^{55}Fe source recorded using a CPC2 sensor with CPD1 drive and CPR2 readout chips, demonstrating for the first time the operation of all the elements needed for the production of a CCD ladder.

Future Programme

Improvements to the CPCCD efficiency – CPC-T Tests

The first batch of CPC-T devices is expected to arrive in October 2007. Two of the designs in this batch target studies of operation at low clock amplitudes and achieving low inter-gate barrier by carefully controlling dopant implantation or using different thickness of dielectric. Six designs explore the reduction of the inter-gate capacitance by using pedestal gate, open phase and variable gate overlap architectures. Two devices will have only clock bus lines to allow accurate capacitance calibration. This large range of devices will be tested for 6 months and the final results should be available by mid-2008, before the design of CPC3 is scheduled to commence.

Testing of the CPC2/CPR2A hybrid assembly driven by CPD1

We expect the next generation CPR2A chip to be manufactured and delivered in the first quarter of 2008. The chip will be tested in stand-alone mode first, with the emphasis being on the sparsification circuitry and the performance of the amplifiers and the ADCs. The newly added calibration register allows injection of charge and voltage signals to the front-end amplifiers and the testing of their response without the need to bump-bond to a CCD. This allows verification of their basic performance, but is no substitute for operation in a bump bonded configuration.

Immediately after receiving the CPR2A wafers, they will be sent to VTT for bump bonding to 4 already available CPC2 wafers. The bump bonding is expected to take 3 months to complete, with delivery of assemblies in mid-2008.

The CPC2/CPR2A combination will be tested in a motherboard based on the successful MB5.0 design and driven by 1 or 2 CPD1 chips. The main goals are to verify the performance of the front end amplifiers and ADCs at clock rates higher than 5 MHz (the maximum achieved so far with CPR2) using MIP-like X-ray signals. Particular attention will be paid to the charge amplifiers. Most of the tests on the cluster finder and sparsification sections will be done in stand-alone mode. Simulated hit data can be loaded and passed through the logic via a scan register as was done with CPR2.

Testing of the CPC3/CPR3 assemblies

LCFI plans to produce 2 generations of readout chips for the CPC3: CPR3 in 2009 and CPR4 in 2010. Small test versions of the CPC3 sensor, CPC3-S, will be bump bonded to CPR3 in the second half of 2009 and the standalone performance of both chips investigated. The hybrid CPC3/CPR3 will be clocked using CPD2 drivers and fully tested in the first half of 2010.

Test beam studies of the hybrid assembly CPC3-S/CPR3 will be carried out at the beginning of 2010. The goals are to measure the point resolution of the sensor in a magnetic field, test the electronics and the DAQ and gather experience for the next round of full ladder beam tests.

The full-size CPC3 will be bump bonded to CPR4 in late 2010 as part of the ladder integration process described below. CPR4 will also be evaluated extensively in stand-alone mode. These studies will be performed concurrently with the ladder integration work.

Testing of the ISIS2 and ISIS3

The evaluation of ISIS2 will commence in the second half of 2008.

ISIS3 is expected to be available by the end of 2009 and tests should be completed by the second half of 2010. Both ISIS3 and ISIS3-S, the small test version of the sensor, can be studied independently of the ladder integration work if they do not require bump bonding and can be operated stand-alone.

Integration and ladder electronics – CPCCD

The integration of a CPC/CPR/CPD hybrid assembly and its external support electronics into a low-mass detector ladder is one of the most challenging areas for WP5. For the CPCCD line of sensors, we have established a reliable process for bump bonding the readout chips to the CCDs using eutectic solder at VTT (Finland). A similar process is used for the production modules for the ALICE experiment at LHC and was developed in collaboration between the company and CERN. LCFI is planning to continue to use VTT for bump bonding and extend the scope of our work to match the requirements for producing low-mass assemblies.

If we decide to follow the standard procedure for bump bonding, a significant difficulty could develop in the process of attachment of the readout chip (and possibly the driver chip) to a CCD thinned down to 20-50 μm. Given the significant forces applied during bond compression, there is some risk that the CCD could fracture. In this case, we would modify the bump bonding procedure so that the compression is exerted before the chips have been thinned. The bonding, mounting and connection of a hybrid assembly to the mechanical support would then proceed as follows:

1. Bump bond readout/driver chips to the CPC wafer without dicing it.

2. Attach a handle wafer to the top side of the CPC using wax, maintaining good flatness.

3. Grind and polish the back side of the CPC wafer to a thickness of 20-50 μm, with subsequent backside implantation and laser annealing if the epitaxial layer is reached in the thinning process.

4. Cut the CPC and the handle wafer into individual bump bonded assemblies.

5. Glue the assemblies to the mechanical support structure.
6. Heat the assemblies to melt the wax and release the handle wafer pieces.
7. Clean off any residual wax and glue thin kapton cables to the mechanical support.
8. Wire-bond the CPC/CPR/CPD chips to the kapton cable using jigs.

This procedure requires that thinned CPR and CPD chips are bonded to whole CPCCD wafers. After the bump bonding, the wafers will be returned to e2v technologies for thinning and possible backside implantation and annealing. These two steps are not normally done by this vendor some collaborative work will be required to develop the procedures.

It may prove difficult to be bump-bond the driver chips to the CPCCDs due to space constraints and difficulties in routing the clock and power lines on low impedance tracks on the CPCCD. In this case, they can instead be bump bonded to a kapton strip cable connected to the CCD clock pads with soldered connections. The advantage of this approach is that the CPD and its storage capacitors can be placed outside the active CCD area, behind the readout chips.

The integration and the building of the test detector ladders will be carried out in close coordination with WP6. The developments outlined above are expected to take 2 years and will require close collaboration between LCFI and the companies involved. The equipment cost is estimated to be around $200k.

Integration and ladder electronics – ISIS

The integration of an ISIS sensor into a low-mass detector ladder should be much easier than is the case for the CPCCD and will draw upon the experience gained with the CPCCD. Bump bonding could be avoided if the ISIS readout can be integrated on-chip and the thinning procedure could therefore be much simpler. The thinning and mounting of the ISIS chips could be done in a similar fashion to that outlined for the CPCCD.

Full ladder tests

The prototype ladders will be subjected to a range of detailed tests to verify their operation and find any potential problems:

- Electrical – this test will verify the correct operation of the CPC/CPR/CPD and ISIS assemblies in fully functional ladders using ^{55}Fe X-rays at the working temperature.
- Mechanical – measurements of the surface flatness and vibration tests will verify the robustness of the ladders.
- Thermal – temperature profiles obtained with IR camera scans and studies of the effects of temperature cycling will confirm the thermal properties of the system.
- Test Beam – full ladder tests will measure the resolution at different incident angles in a magnetic field at the operating temperature. These studies are expected to begin in the first half of 2011.

- System radiation damage tests – these will check the radiation tolerance of the sensors, readout and driver chips and storage capacitors together with all the materials used in the ladder construction such as adhesives etc.

Radiation hardness studies

The radiation damage effects in CPCCD have been extensively simulated, but so far we have not conducted any measurements. The simulations indicate that at clock rates of 50 MHz the radiation-induced Charge Transfer Inefficiency (CTI) is very low in the temperature window between –50 °C and 0 °C. The operating temperature of the CPCCD will probably lie within this range, but this has to be confirmed by experimental data.

Presently we are starting radiation damage tests on a CPC1 chip. The measurements will be representative of CPC2 as well, as the two devices share common pixel architecture. This device can be clocked at up to 25 MHz and is read out by four 2-stage source follower outputs. The CCD will be irradiated initially using soft β-rays from a ^{90}Sr source (average energy 700 keV), which will create both surface and bulk damage effects. The device will receive doses of up to 100 krad in several steps. The temperature and frequency dependence of the CTI will be measured after each irradiation, and the results compared with the simulations.

We are also planning to further irradiate the CCD with neutrons from a ^{252}Cf source (average energy 2 MeV) to a fluence of 10^{10} cm^{-2} 1 MeV-equivalent.

The expected pair background at ILC has an average energy of 10 MeV, which produces about 3 times more radiation damage than the ^{90}Sr source. This will be taken into account when the expected lifetime of the sensor is calculated.

The next step will be to study the radiation hardness of the most promising CPC-T chips. Some CPC-T devices could potentially reduce the radiation-induced CTI due to the implementation of design measures to contain the charge packet in a smaller volume than in the CPC1/2. Such measures are the “notch channel” and the potential gradients achieved by doping profiles and gate design. Because the CTI is inversely proportional to the density of the signal charge (i.e. proportional to the storage volume) we expect to see visible reduction of the CTI compared to the standard CPC1/2 devices.

The third round of radiation damage tests will take place at a system level on fully functional ladders with CPC3/CPR3 and driver chips.

Similar tests with electron and neutron irradiation will be carried out on ISIS2. The radiation hardness of the ISIS is expected to be significantly higher than that of the CPCCD. Radiation-induced bulk defects should cause orders of magnitude less charge loss than in CPCCDs because of the small number of transfers in the ISIS. Excellent surface radiation hardness is expected due to the very thin oxides used in the CMOS process. Because of this, we expect the ISIS to need just moderate cooling for reduction of the dark current, in the range –20 °C to 0 °C.

The second radiation damage tests for the ISIS will be the system ladder tests as outlined above.

WP6 – Mechanical Studies

Introduction

LCFI has investigated a range of support technologies for its thinned silicon sensors. Early studies investigated the possibility of stretching a sensor thinned to about 50 μm between the end plates of the VXD and attaching sensor of thickness about 50 μm to a beryllium substrate. The former approach was abandoned as it was observed that the sensors bowed in the direction transverse to that along which tension was applied. This was found to be due to the stresses induced in the silicon during processing. The latter approach also performs poorly. This time the differing temperature coefficients of expansion of the silicon and beryllium are the cause of the problem. As the assembly is cooled, the silicon is seen to buckle, as is shown in Figure 20.

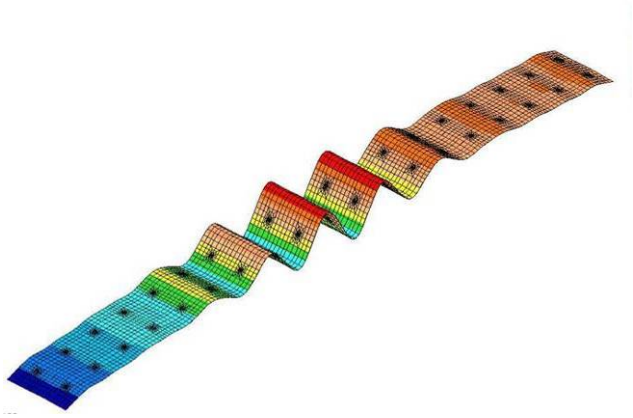

Figure 20 Finite Element Analysis showing the buckling induced in a thinned silicon sensor attached to a beryllium substrate as the assembly is cooled.

Following these results, LCFI sought light materials with a good thermal match to silicon. Some of the foams used in the aircraft industry were found to be suitable, in particular silicon carbide and reticulated vitreous carbon (RVC) foams are of interest. Ladders were constructed using these and their performance under cooling tested. As SiC foam is extremely rigid, ladders can be constructed by attaching thinned silicon sensors to one side of the foam using glue pillars. RVC foams must be used in sandwich structures to provide the necessary stiffness. LCFI has constructed full length ladders using both approaches. (Thinned unprocessed silicon is used for these studies to reduce costs.) The results obtained when a silicon/RVC foam ladder was surveyed at a range of temperatures are shown in Figure 21. The observed deviations due to the temperature change are less than 1 μm/K: the thickness of this ladder is less than the target value of 0.1% X_0.

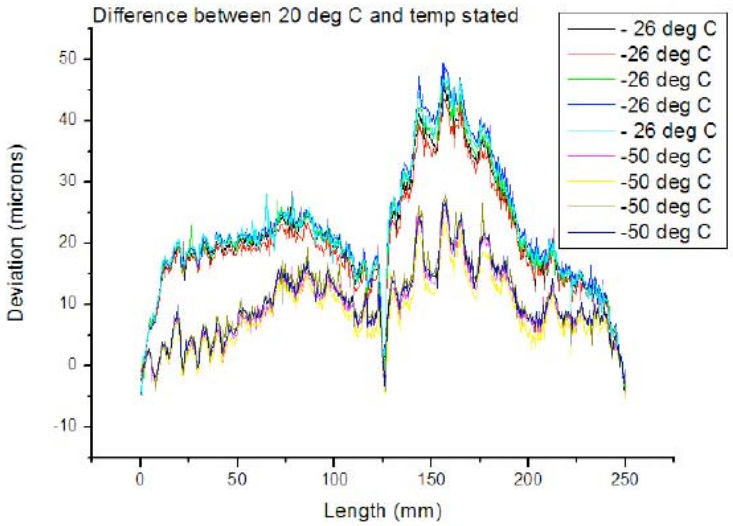

Figure 21 Distortions introduced by cooling a silicon/RVC foam sandwich ladder.

Using foams for the support of the sensors introduces a range of challenges. For example, how can the flatness of a foam structure be measured and how can foams be machined to improve their flatness? LCFI is currently exploring the use of large diameter, low force touch probes to measure foams, defining the flatness to be the root mean square of the probe measurements with a defined probe size. The measurements used to calculate the flatness in a recent study are shown in Figure 22. The flatness of this sample was 320 μm before machining and 80 μm after.

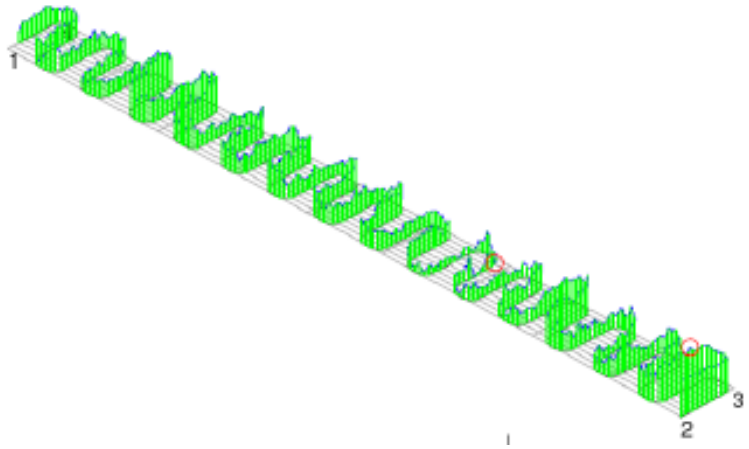

Figure 22 Measurements made using a low force large diameter touch probe to define the flatness of a sample of SiC foam, the highest and lowest points found in the scan are marked with red circles.

LCFI has also started to develop the tools needed to simulate the thermal behaviour of the ladders in the VXD. Finite Element calculations are being compared with the results of a full-scale model of one quarter of the VXD so the software can be tuned and its reliability tested. First designs of carbon fibre support structures are also underway.

Future Programme

By 2012, LCFI must have realistic prototype detector modules operational, and an essentially complete engineering design for the whole vertex detector. Although some details (e.g. external services) may not be completely specified, all technologies and design choices must have been

verified and any major potential problems solved. In order to achieve this, the mechanical studies will have to progress from their current phase of basic studies of support technologies to full engineering designs via the following steps:

1. Completion of basic support studies.
2. Choice of support technology.
3. Design of detector modules.
4. Thermal studies of modules.
5. Prototyping with blank silicon.
6. Detailed testing of mechanical prototypes.
7. Development and testing of production techniques.
8. Prototyping with mechanical grade sensors.
9. Prototyping with electrical grade sensors.
10. Global detector engineering design.
11. Global detector thermal studies.

The separation of the work into these tasks is, of course, somewhat arbitrary. Many of them will be conducted in parallel and will influence each other.

Basic support studies

There are many potential support technologies for an ILC vertex detector. As is illustrated in Figure 23, these can be divided into “ladder”-based, in which each one or two electrically separate sensor modules are attached to their own mechanical support which in turn is attached to a bulkhead or other global support structure, and “shell” based, in which several modules (typically half a layer) are attached to an integrated mechanical support structure. Ladders could consist of thinned silicon attached to a thin substrate (e.g. carbon fibre) held under tension, or a rigid foam/silicon structure (e.g. silicon attached to SiC foam or a silicon-RVC foam sandwich), and integrated shell structures could be made from various materials including carbon fibre and silicon carbide foam.

The programme of basic studies involves making simple models (both physical and in simulation) of all of the available support options and investigating their basic characteristics and behaviour under temperature cycling. Any major potential problems in terms of handling, production accuracy and low temperature behaviour (hysteresis, buckling, repeatability etc.) should be identified and solved.

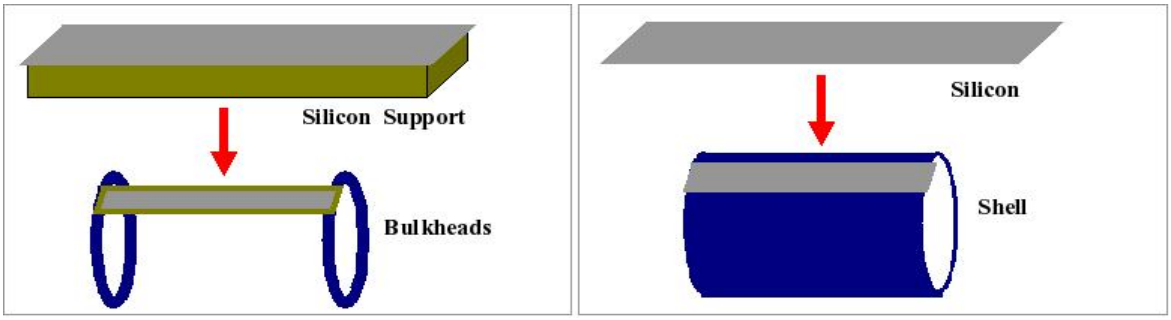

Figure 23 Ladder (left) and shell (right) support concepts.

Choice of support technology

The basic support studies should give enough information for one or two candidate technologies to be chosen for further detailed studies. Although options should be left open, limited financial and manpower resources require a concentration of effort on the most promising ideas.

Design of detector modules

It is necessary to move from simple models towards realistic designs that will incorporate sensors, mechanical elements, the additional necessary electronics infrastructure and external interfaces (both mechanical and electrical). This will depend heavily on input from developments in other areas within this work package and in other work packages, particularly with regards to sensor technology choices.

Potential designs will have to be carefully evaluated, both for their mechanical feasibility (as described in the following sections) and using sophisticated simulation tools to establish their physics potential. Possible design choices are described later.

Thermal studies of modules

Computer simulations will be used to evaluate potential module designs. These will establish the expected behaviour under temperature and power cycling and under power cycling, allowing identification of potential problems and the fine tuning of designs.

Prototyping with blank silicon

Detailed prototypes of the designs will be made initially with thinned silicon blanks, for reasons of economy. Commercial suppliers (e.g. Aptek Industries) can now provide silicon wafers diced and thinned to 20 µm with a reasonable yield and no significant internal stresses. These prototypes will be constructed with realistic materials and can be used to evaluate mounting techniques.

Detailed testing of mechanical prototypes

A comprehensive testing programme must be undertaken to ensure that the designs are suitable for use in the ILC vertex detector. These involve both short- and long-term issues such as:

- Deformation under temperature changes.
- Stability under temperature cycling.
- Vibration and resonance.

- Radiation hardness.
- Thermal, mechanical, chemical and electrochemical aging.
- Creep.

Development and testing of production techniques

Procedures and fixtures to produce detector-quality modules must be developed. Several iterations are to be expected, particularly if module designs change and as experience is gained.

It is likely that various specialist procedures such as bump- and wire-bonding will be necessary. The compatibility of the mechanical designs and procedures with such processes must be checked. For example, wire-bonding to thin silicon could prove problematic and thicker silicon in the bonding region could be required. Similarly, the use of particular solvents or temperatures during bump processing could limit the materials and adhesives that are suitable.

Prototyping with mechanical grade sensors

Failed or partially processed electrical sensors must be used to prototype to expose any additional problems cause by the intrinsic stresses in processed silicon. Any such problems should be visible in short-term tests such as surveying during temperature cycling.

Prototyping with electrical grade sensors

Full, electrically functioning modules will be built to examine not only their performance as particle detectors, but also to check their mechanical properties. The effects of steady-state and pulsed power loading, handling, cabling and cooling will have to be shown to be acceptable.

Global detector engineering design

The global design has to proceed in parallel with the module design, at least at the conceptual level. As module designs become more mature, detailed detector layouts will have to be evaluated both for mechanical properties and physics performance (via simulation). Design choices which will be considered include:

- Ladder/bulkhead layouts.
- Single and double-sided ladders.
- Integrated shell structures.
- Long barrels.
- Short barrels with endcaps.

Different global designs will be considered and compared in parallel with the module design effort. Once a favoured design has been identified, detailed engineering can begin, including the layout of infrastructure and external services.

Global detector thermal studies

Computational techniques, calibrated in simple cases against test models, will be used to evaluate the performance of the gas cooling for potential detector designs. There is some scope for modifying the cooling patterns by changing the number and placement of inlets and outlets and by tuning the flow rate and temperature of the coolant.

Summary

The LCFI Collaboration is pursuing a comprehensive programme geared towards the production of a Vertex Detector (VXD) for the International Linear Collider (ILC). The Collaboration has developed Column Parallel CCDs (CPCCDs) which have the potential to satisfy the requirements for operation at the ILC. The major challenges involved in the production of these devices are achieving the two-track and point resolution needed at the ILC, reaching the readout speed of about 50 MHz necessary to ensure low occupancy in the inner layer of the VXD, developing a readout chip capable of coping with the large data rates produced by the CPCCD and designing small drive chips able to produce the large currents of about 20 A needed to clock the sensors. The necessary two-track and point resolution have been demonstrated in previous CCD-based vertex detectors and recent LCFI results have shown that the CPCCD can be operated at speeds of 45 MHz, albeit with large noise with the current drive system, and that the readout and drive chips are approaching the performance required for the VXD. Furthermore, these systems have successfully operated together.

The second sensor which the Collaboration is developing, the In-situ Storage Image Sensor (ISIS), is not yet as mature as the CPCCD, but offers significant advantages. This device stores signals in pixel during the bunch train, resulting in relaxed readout speed requirements and very high resistance to any electromagnetic interference that may be caused by the ILC beams.

The programme described here allows the development of both of these sensors to the level at which they could be considered for use in the VXD on a timescale commensurate with the most rapid possible construction of the ILC. It requires the investment of significant resources in the development of test systems for studying the sensors.

LCFI is also studying the technologies needed for construction of a VXD that is stable at the level demanded if the precision of the sensors is to be exploited. The Collaboration has identified and is studying two materials that promise to allow the construction of extremely low mass sensor ladders and is investigating the design of a VXD incorporating such ladders.

The LCFI Collaboration has also invested significant effort in developing the tools needed to use the information produced by the VXD. It has developed a comprehensive and sophisticated Vertex Package which allows quark flavour and charge tagging. This package will be further developed and refined as part of the programme described here. Studies will also be carried out of the physics that the VXD makes possible. Various benchmark interactions which depend on quark flavour and charge determination will be studied and the results of these studies used to optimise the VXD design. Practical considerations, such as the internal alignment of the VXD sensors and the alignment of the VXD with respect to the detector within which it sits, will also be investigated.

The resources required to realise this programme are discussed in the sections dedicated to the various LCFI Work Packages in this report.

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