

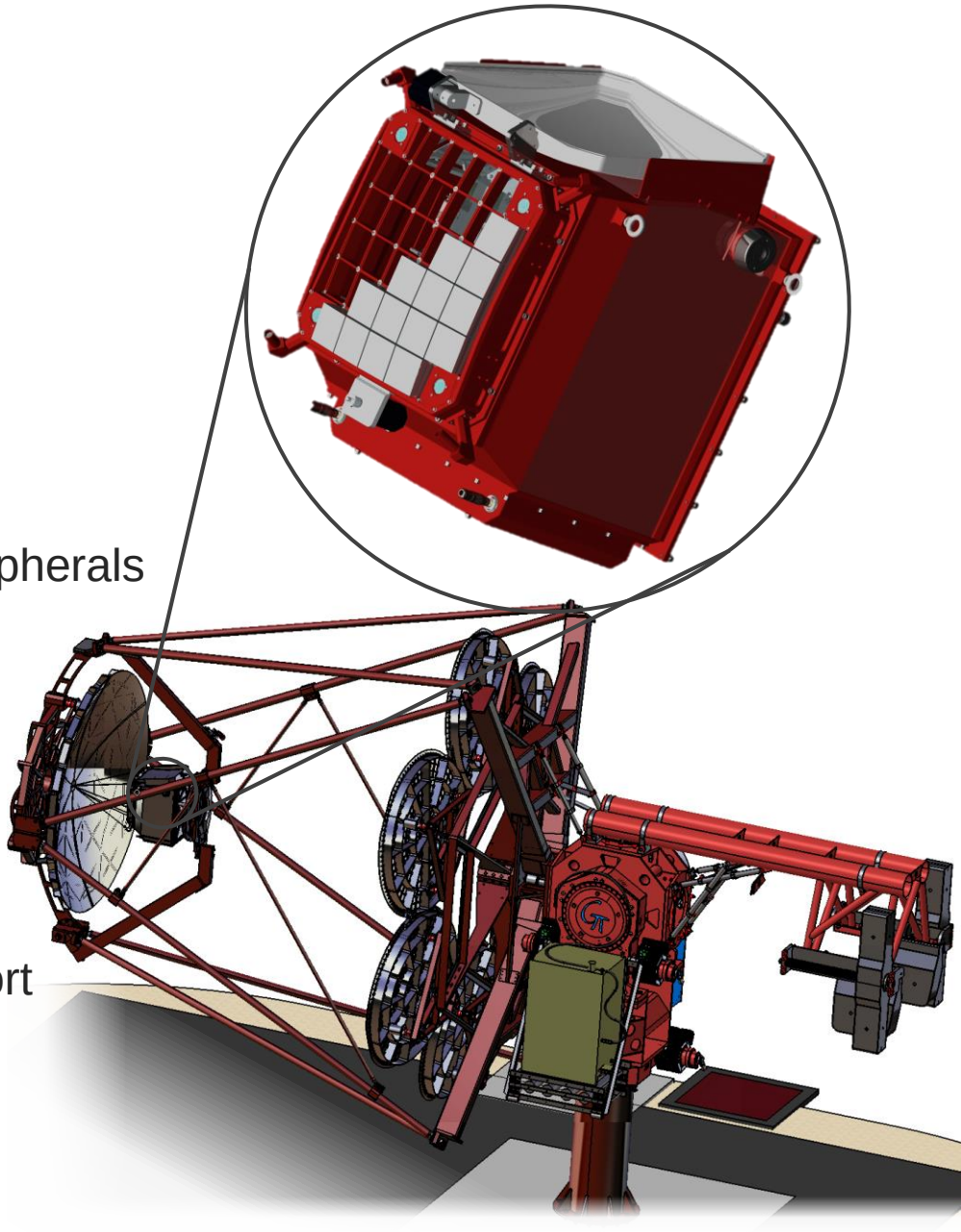
GCT Camera Progress

Jon Lapington, CTA Consortium Meeting,
Turku, May 2015

Science & Technology Facilities Council
University of Leicester
ERLANGEN CENTRE FOR ASTROPARTICLE PHYSICS
THE UNIVERSITY OF ADELAIDE AUSTRALIA
UNIVERSITY OF LIVERPOOL
Durham University
MAX-PLANCK-INSTITUT FÜR KERNPHYSIK
SLAC NATIONAL ACCELERATOR LABORATORY

GCT: The Gamma Cherenkov Telescope

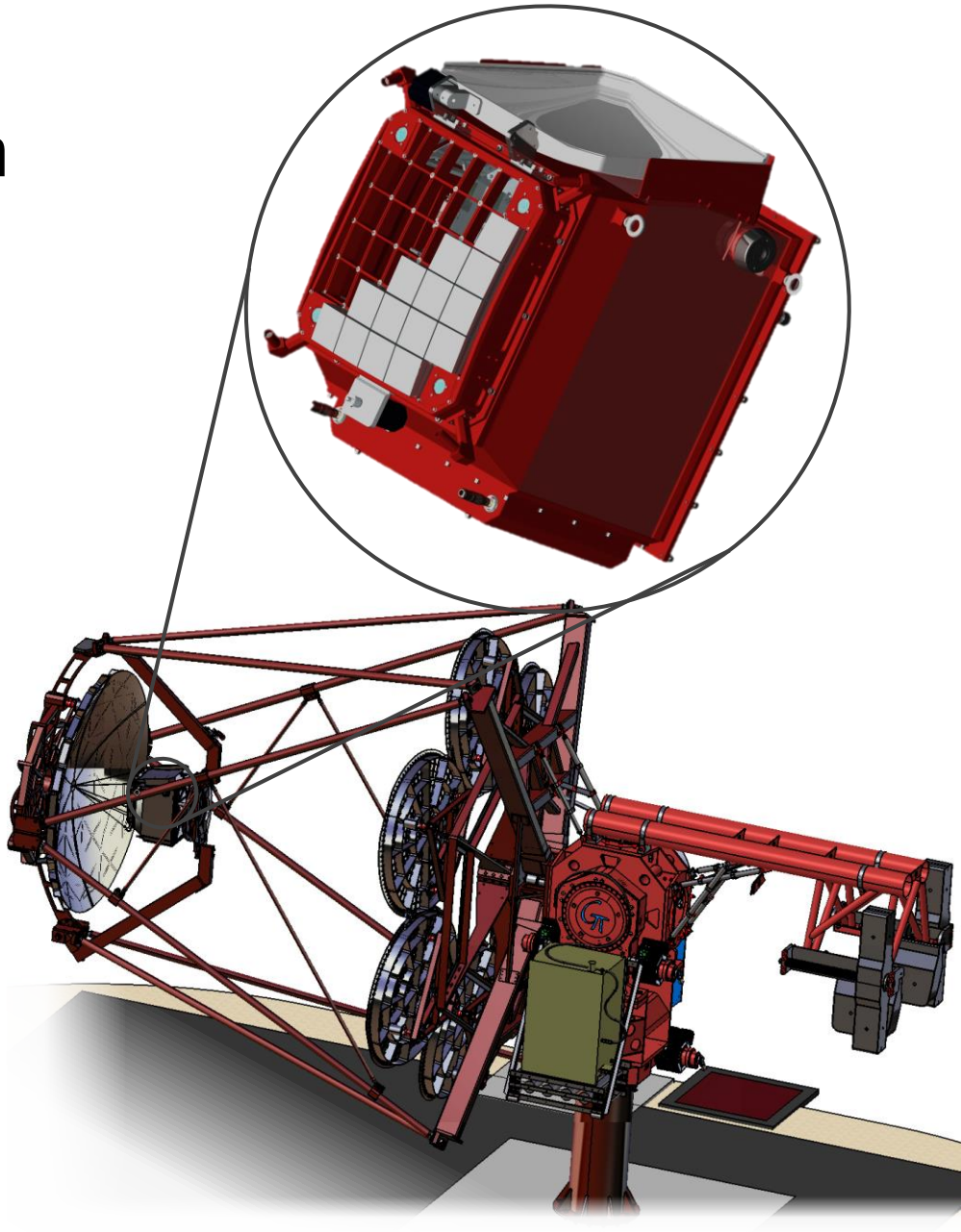
- Talks at this meeting:
  - Monday SST
    - SST configuration 3: GCT
  - Tuesday SST
    - GCT structure and optics
    - GCT MC Studies
    - Control of GCT camera peripherals
    - GCT Camera Progress
    - GCT Camera Software
    - GCT Calibration
  - Thursday Plenary
    - SST-2M GCT progress report
    - CHEC progress report



GCT: The Gamma Cherenkov Telescope

Contents:

- Camera team evolution
- CHEC-M
  - Overview
  - Mechanics
  - Electronics
  - Commissioning
  - Auxiliary Systems
- CHEC-S and beyond
  - SiPMs
  - Front-end electronics
- Summary



Evolution of the camera team

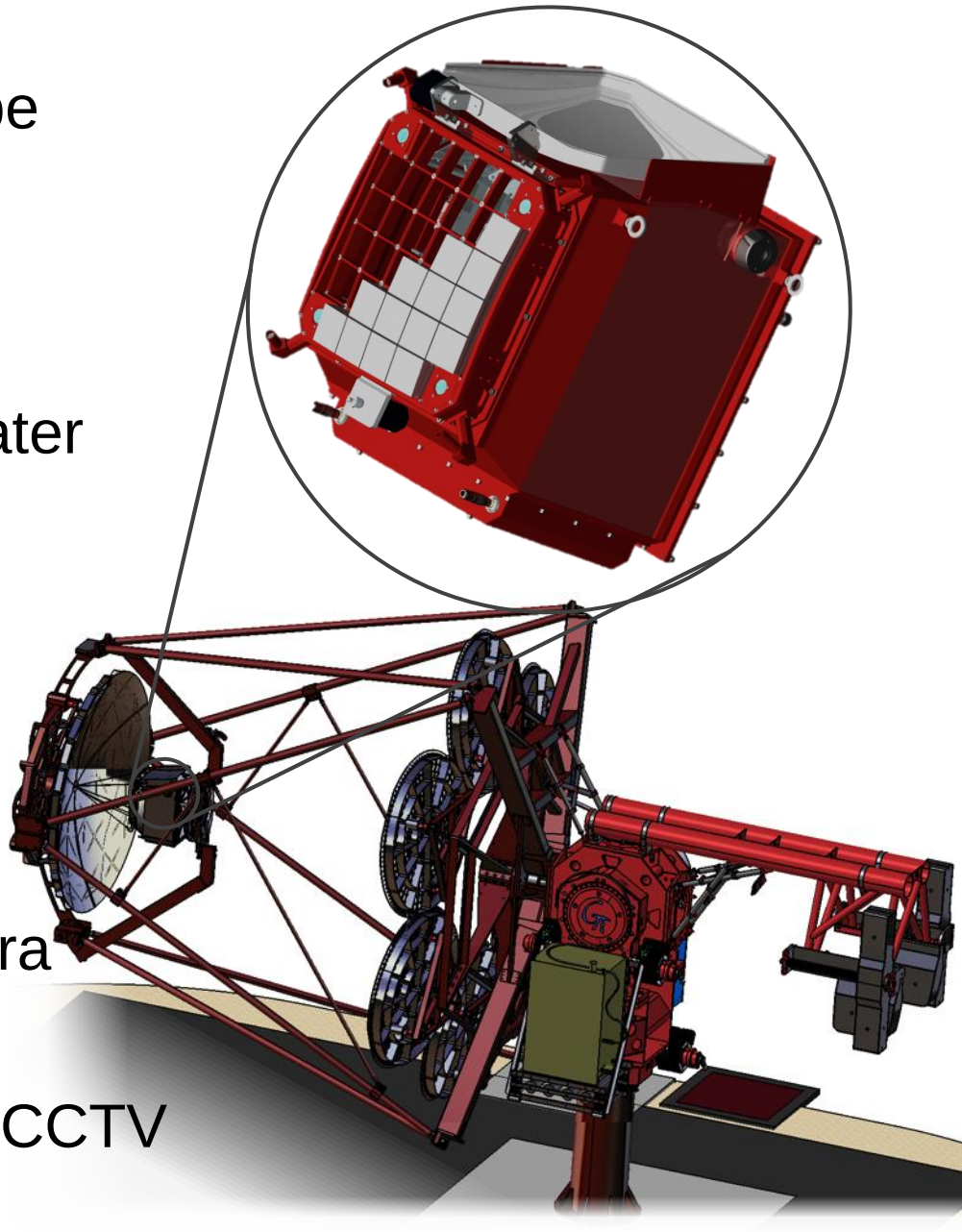
- UK collaboration
  - Leicester, Durham, Liverpool, Oxford, Liverpool John Moores (2015)
- 1st STFC funding 04/2012 – 03/2015, PI – Jim Hinton
- March 2015: Jim, Rich, Akira → MPIK, Heidelberg
- Proposed STFC funding 2015-2017, PI – Tim Greenshaw
- Main camera development remains at Leicester
  - Jon Lapington – lead (since 1st April 2015)
  - Duncan Ross – mechanics
  - Julian Thornhill – electronics
  - Pippa Molyneux – commissioning
  - External team
    - Rich White, Akira Okumura, Arnim Balzer, Andrea De Franco, Jason Watson, Manuel Kraus, Tom Armstrong
- Lab reorganization
  - CHEC-M, CHEC-S, GCT assembly & commissioning

CHEC-M in context

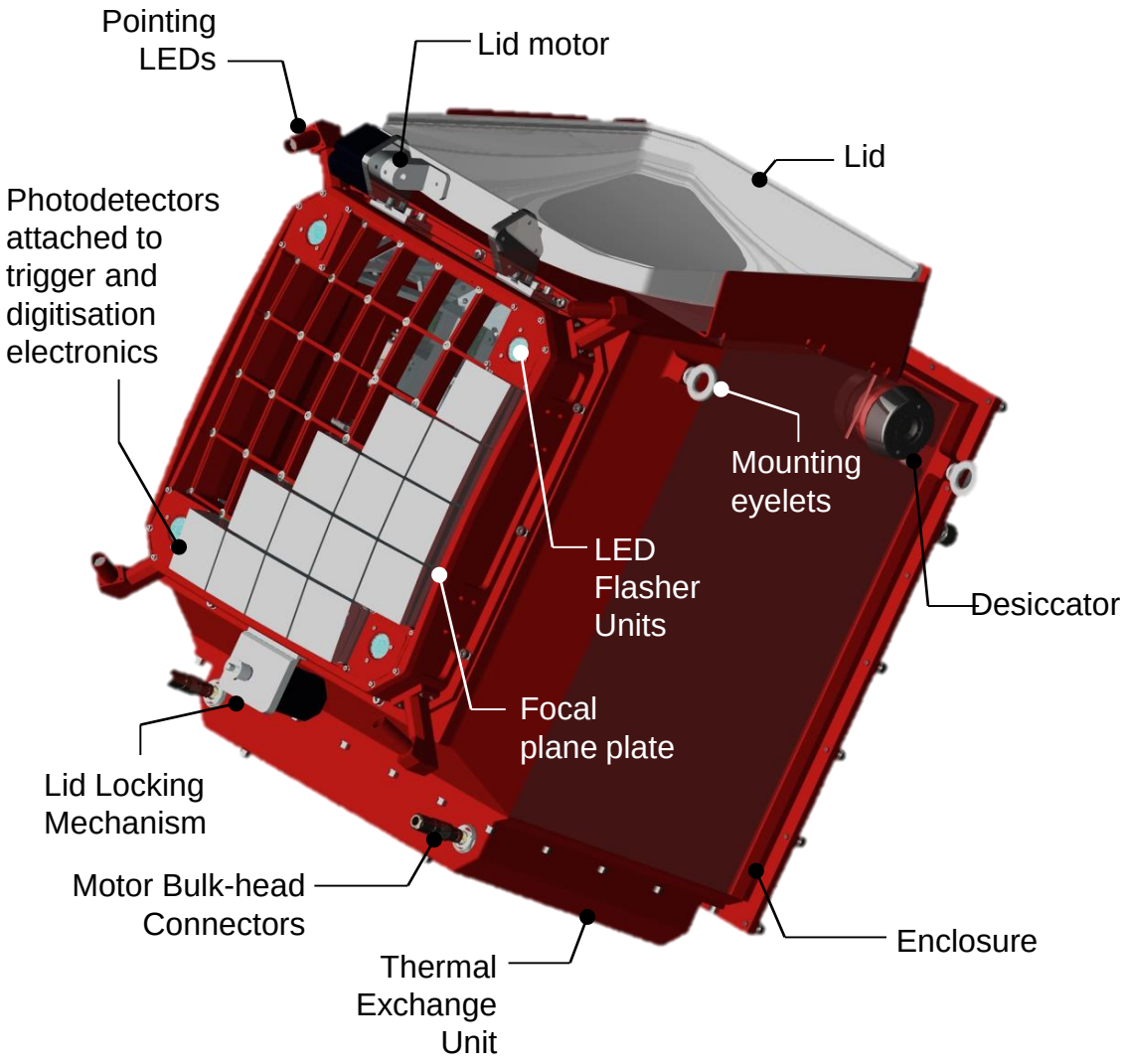
- First GCT camera prototype
- Properties:
  - MAPMs
  - TARGET 5 ASICs
- To be installed on GATE later this year
- The next step is CHEC-S
- Properties:
  - SiPMs
  - TARGET 7 ASICs

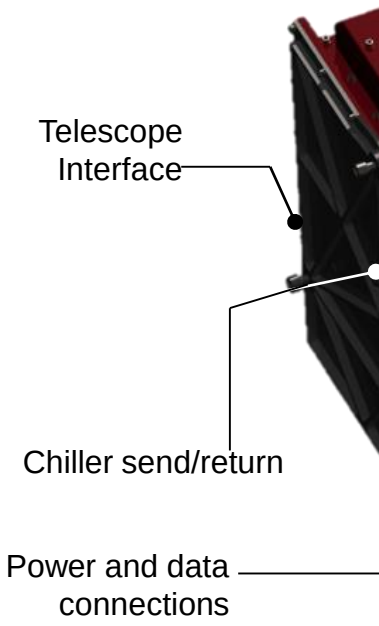
→ GCT pre-production camera

  - SiPMs (LCT5, etc.)
  - TARGET-C &TARGET-CCTV

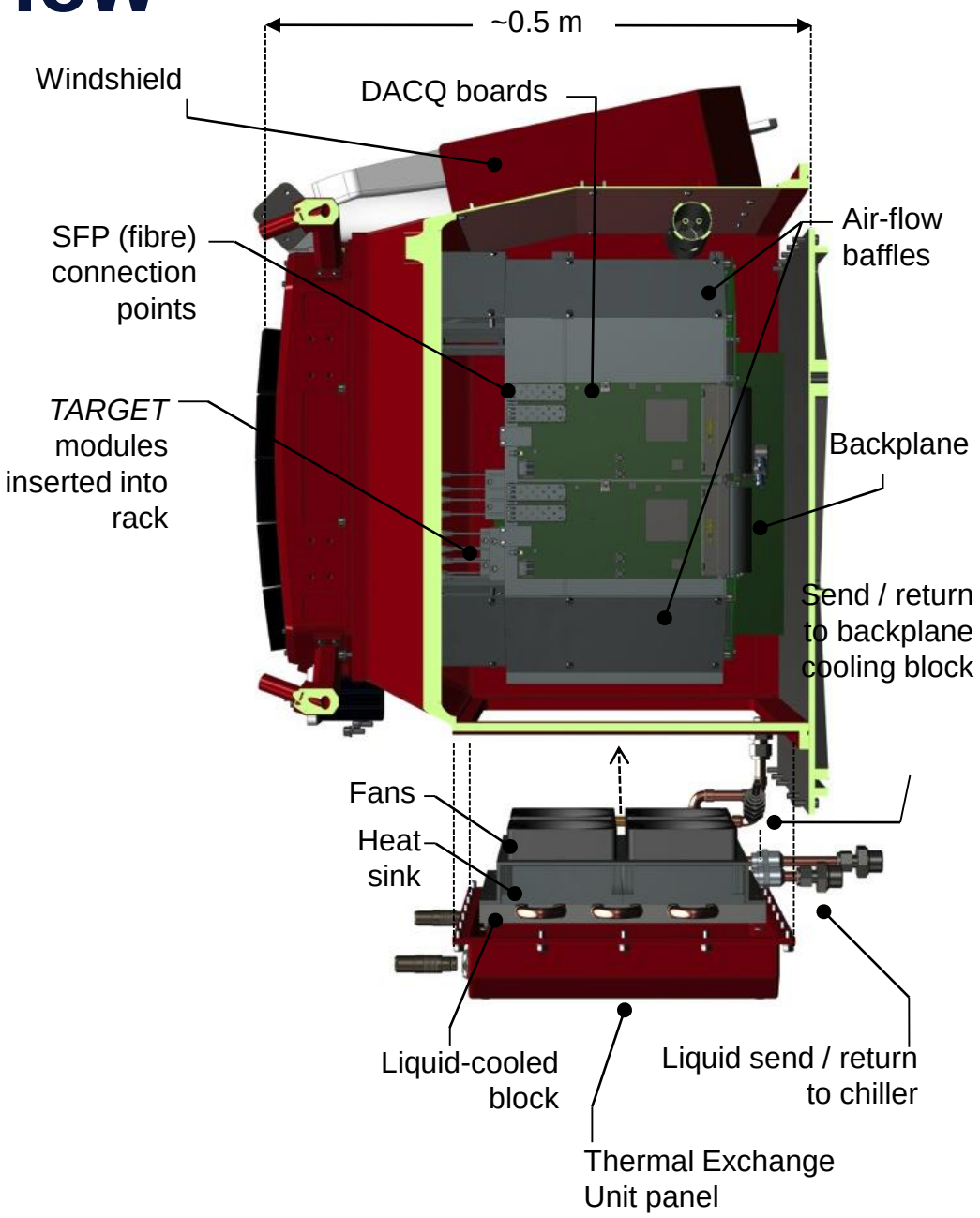


Overview

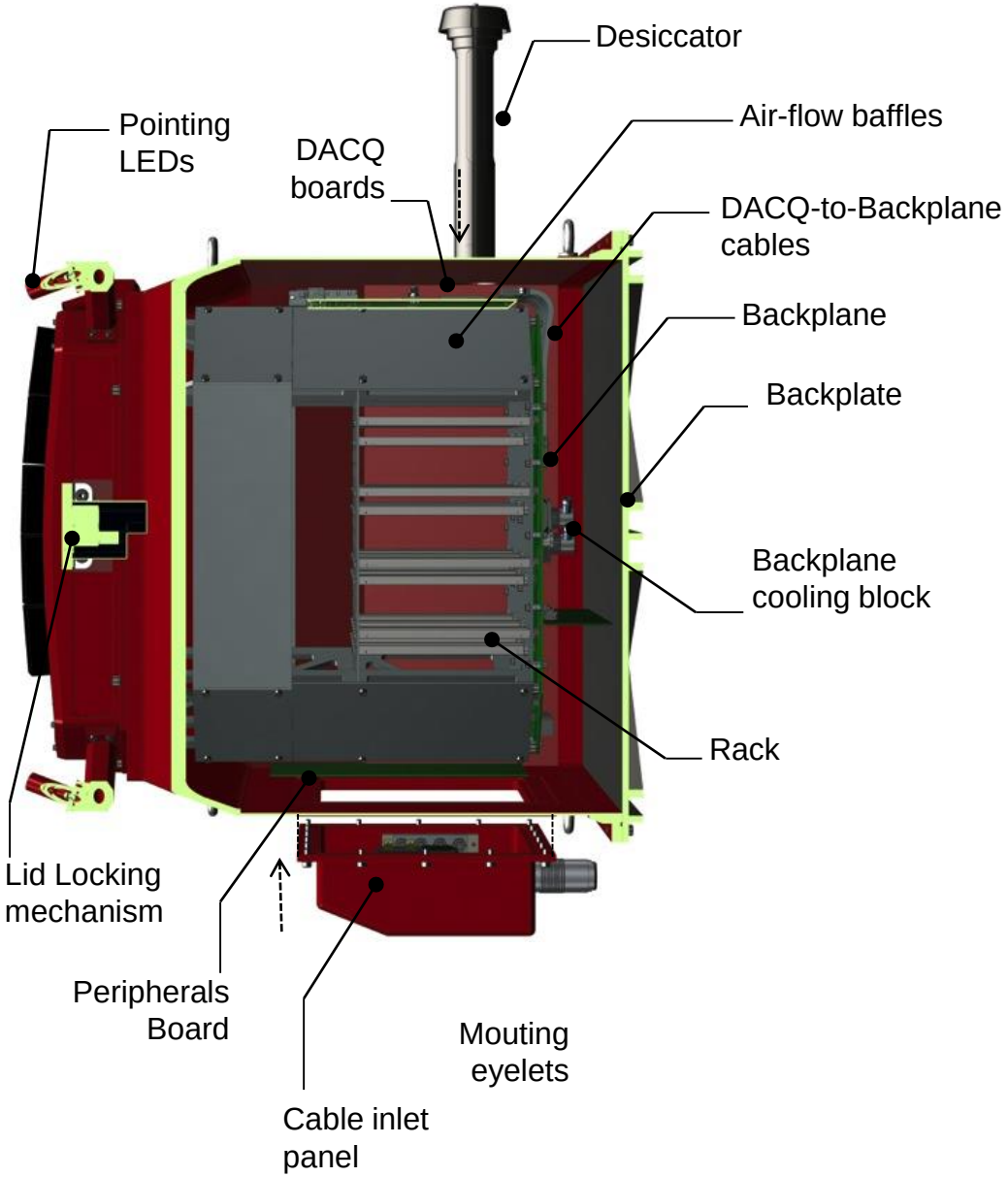

Pointing LEDs
Lid motor
Lid
Photodetectors attached to trigger and digitisation electronics
Mounting eyelets
LED Flasher Units
Desiccator
Focal plane plate
Lid Locking Mechanism
Motor Bulk-head Connectors
Thermal Exchange Unit
Enclosure


Telescope Interface
Chiller send/return
Power and data connections

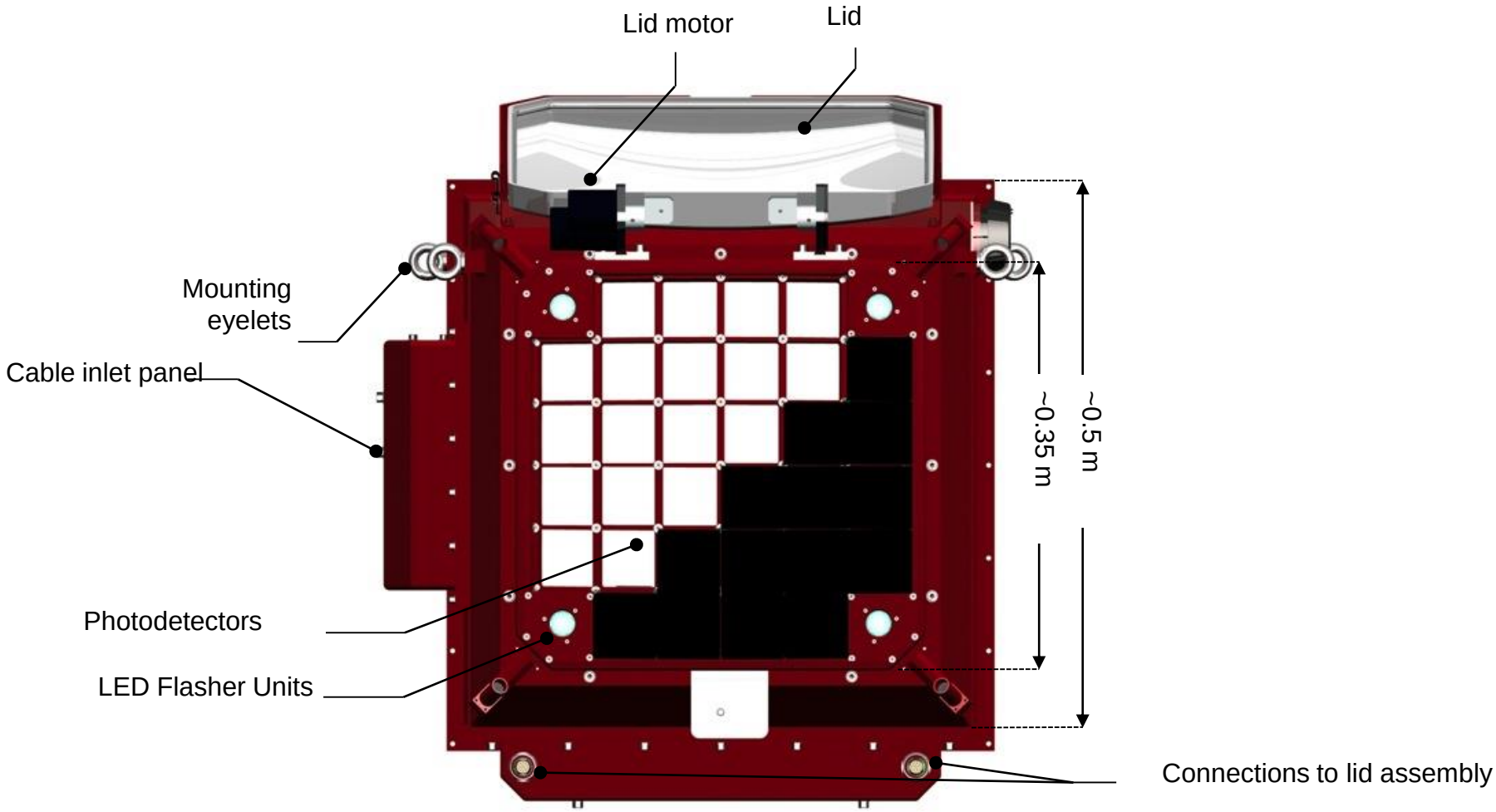
Overview


~0.5 m
Windshield
DACQ boards
SFP (fibre) connection points
Air-flow baffles
TARGET modules inserted into rack
Backplane
Send / return to backplane cooling block
Fans
Heat sink
Liquid-cooled block
Liquid send / return to chiller
Thermal Exchange Unit panel

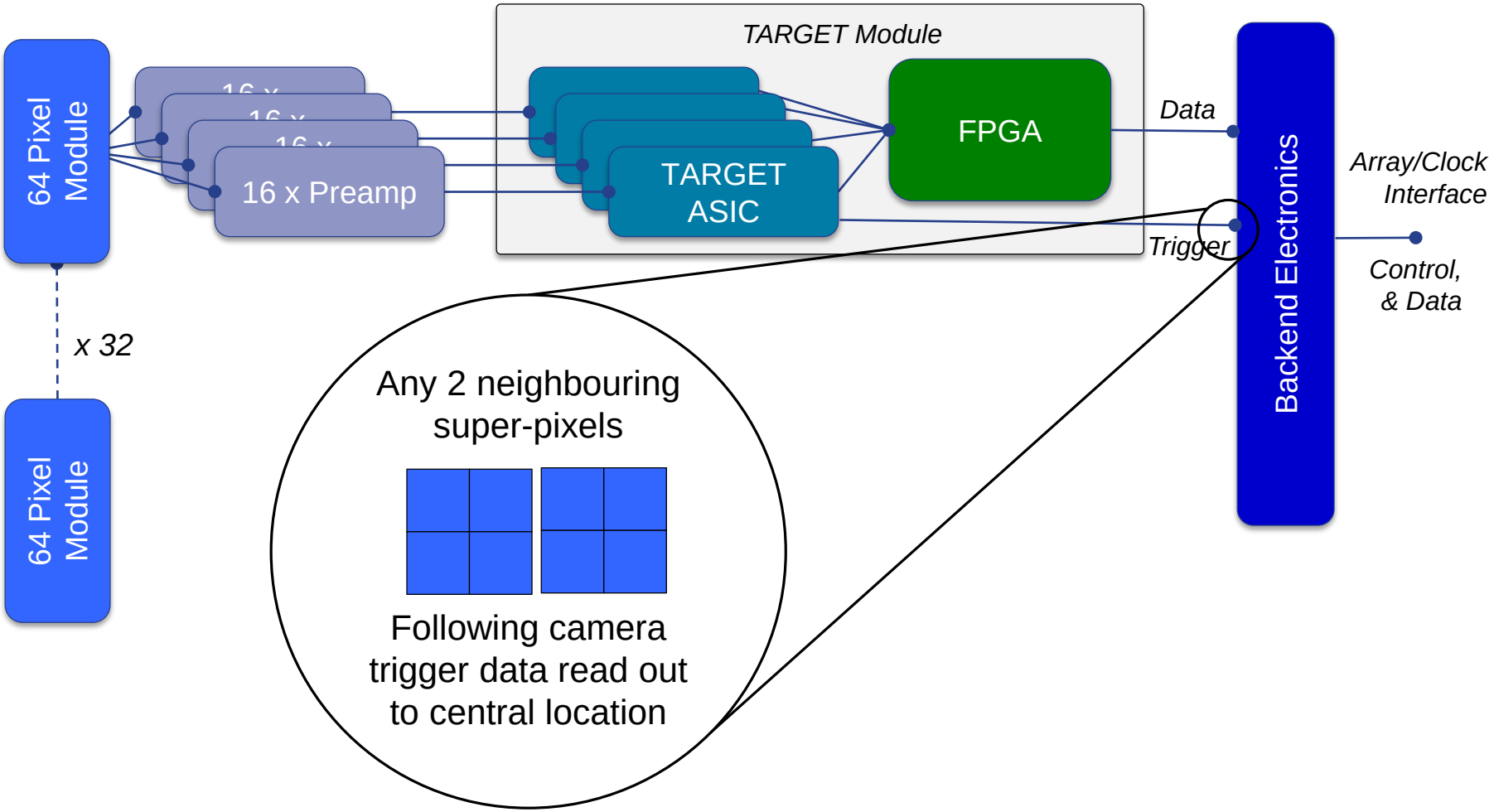
Overview


Desiccator
Pointing LEDs
DACQ boards
Air-flow baffles
DACQ-to-Backplane cables
Backplane
Backplate
Backplane cooling block
Rack
Lid Locking mechanism
Peripherals Board
Mouting eyelets
Cable inlet panel

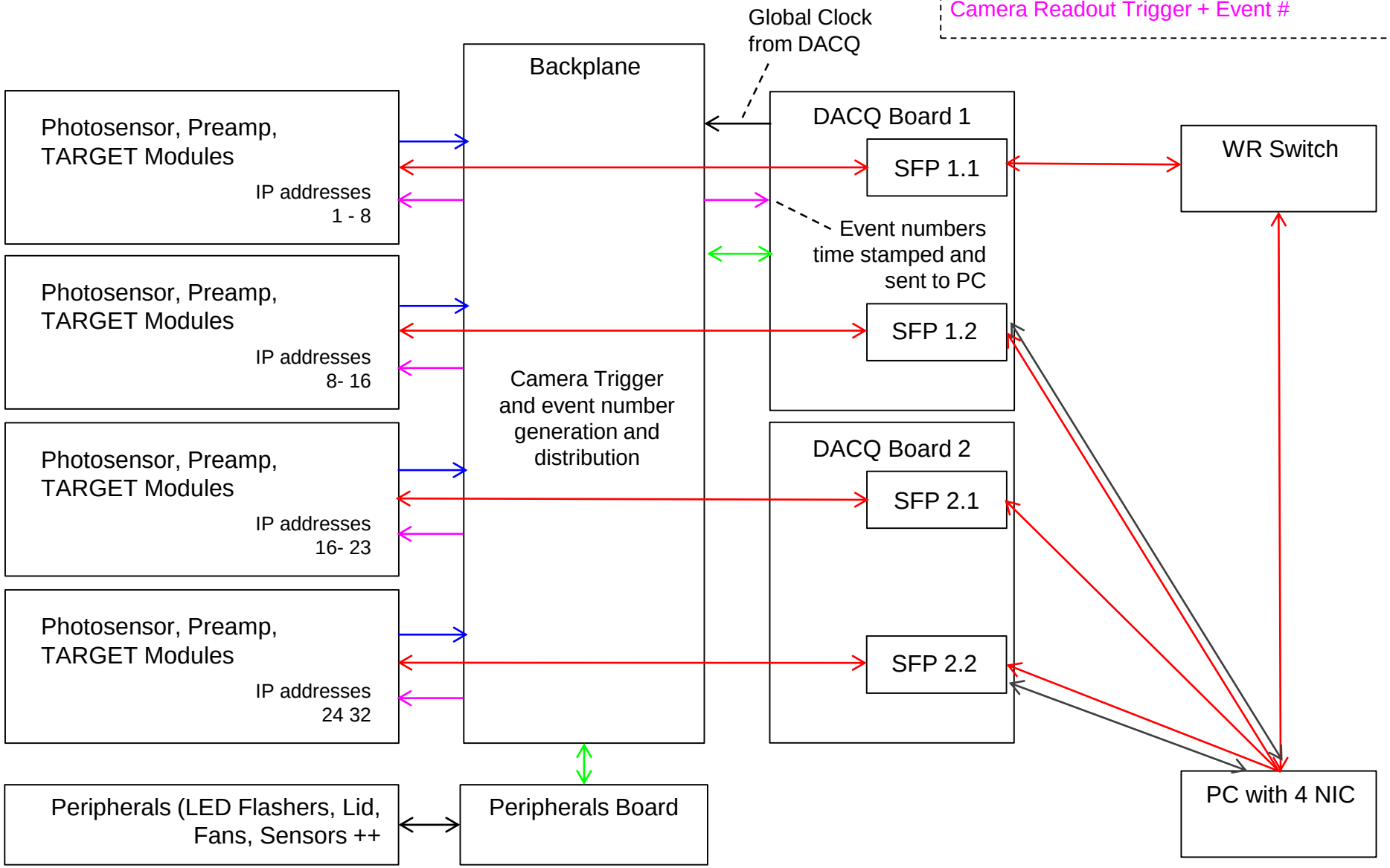
Overview


Lid motor
Lid
Mounting eyelets
Cable inlet panel
Photodetectors
LED Flasher Units
~0.35 m
~0.5 m
Connections to lid assembly

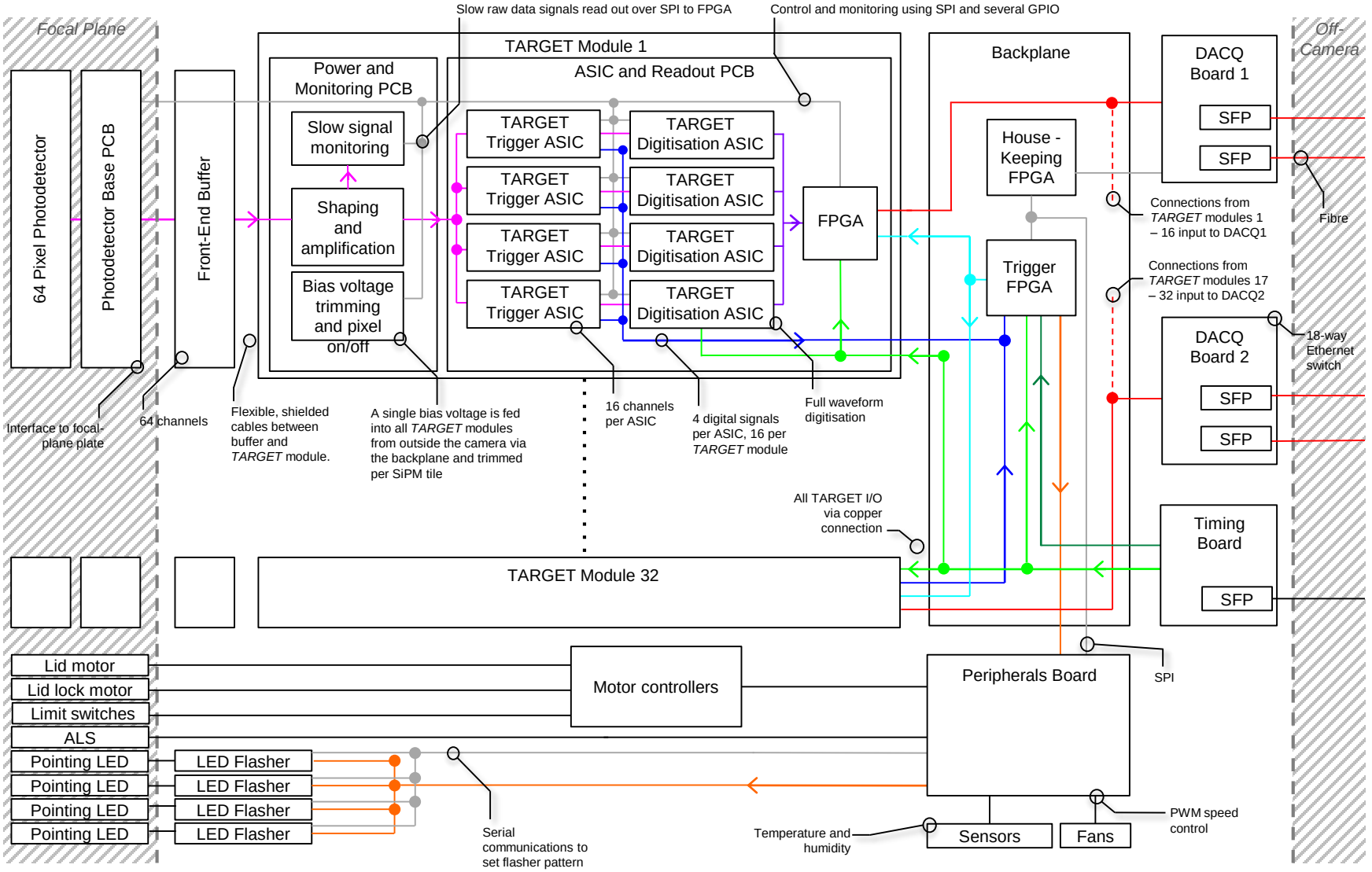
Electronics and Readout



CHEC Back-End Electronics

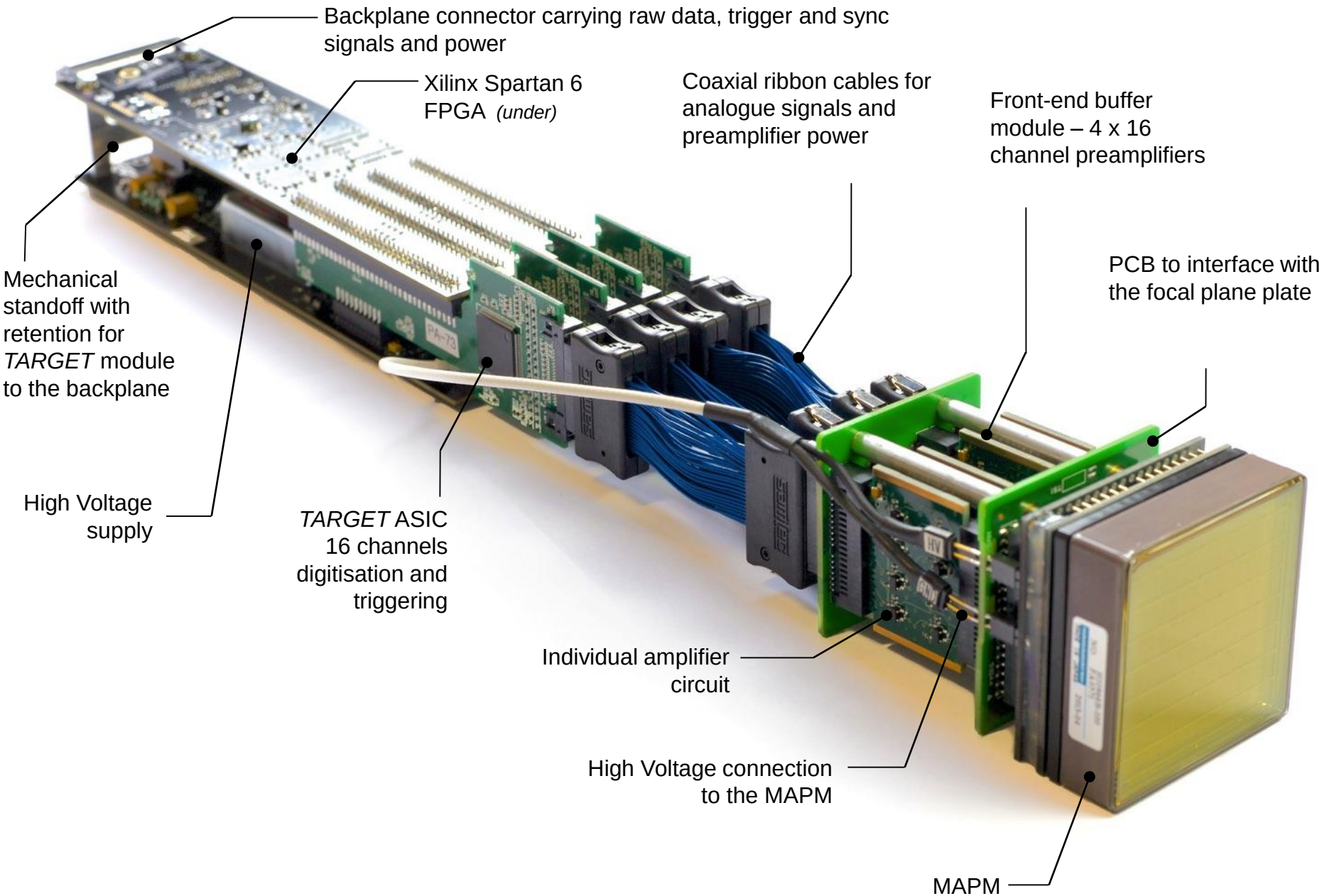


Electronics and Readout

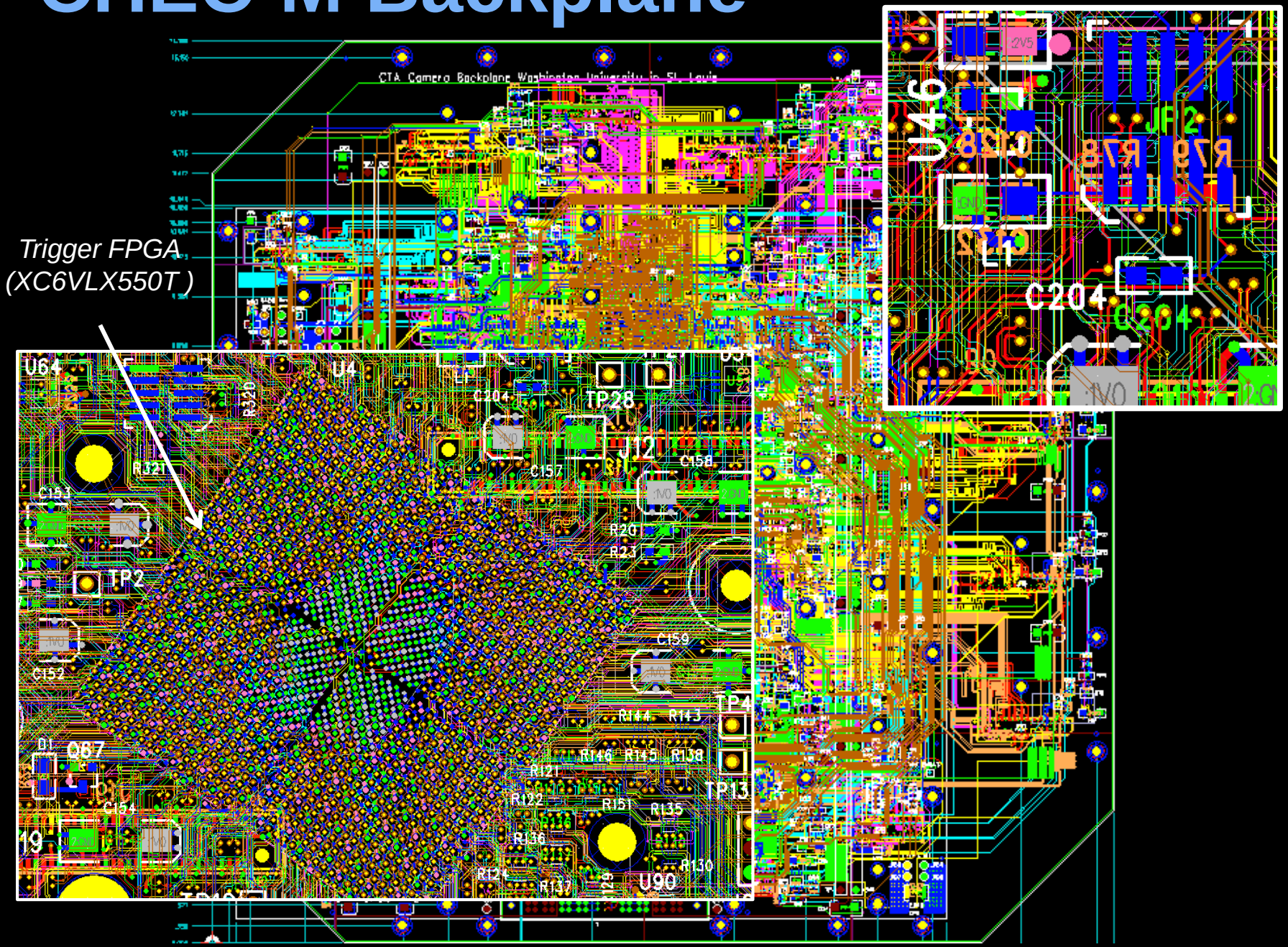


- Raw analogue data
- Raw digitised data
- 1 Gbps UDP over Ethernet link (copper or fibre) for raw data, control and monitoring
- Discriminated analogue sum of 4-pixel digital trigger signals, 16 per TARGET module
- Camera readout out and re-sync serial connection
- Array-wide White Rabbit timing link input on 1 Gpbs fibre-optic link
- 1 PPS array-synchronous clock used to re-sync internal counters and sampling
- 62.5 MHz array-synchronous clock, multiplied to 125 MHz on the backplane
- Asynchronous TTL pulse from the backplane to trigger the LED flashers
- Internal serial communications for control and monitoring

CHEC-M Camera Module

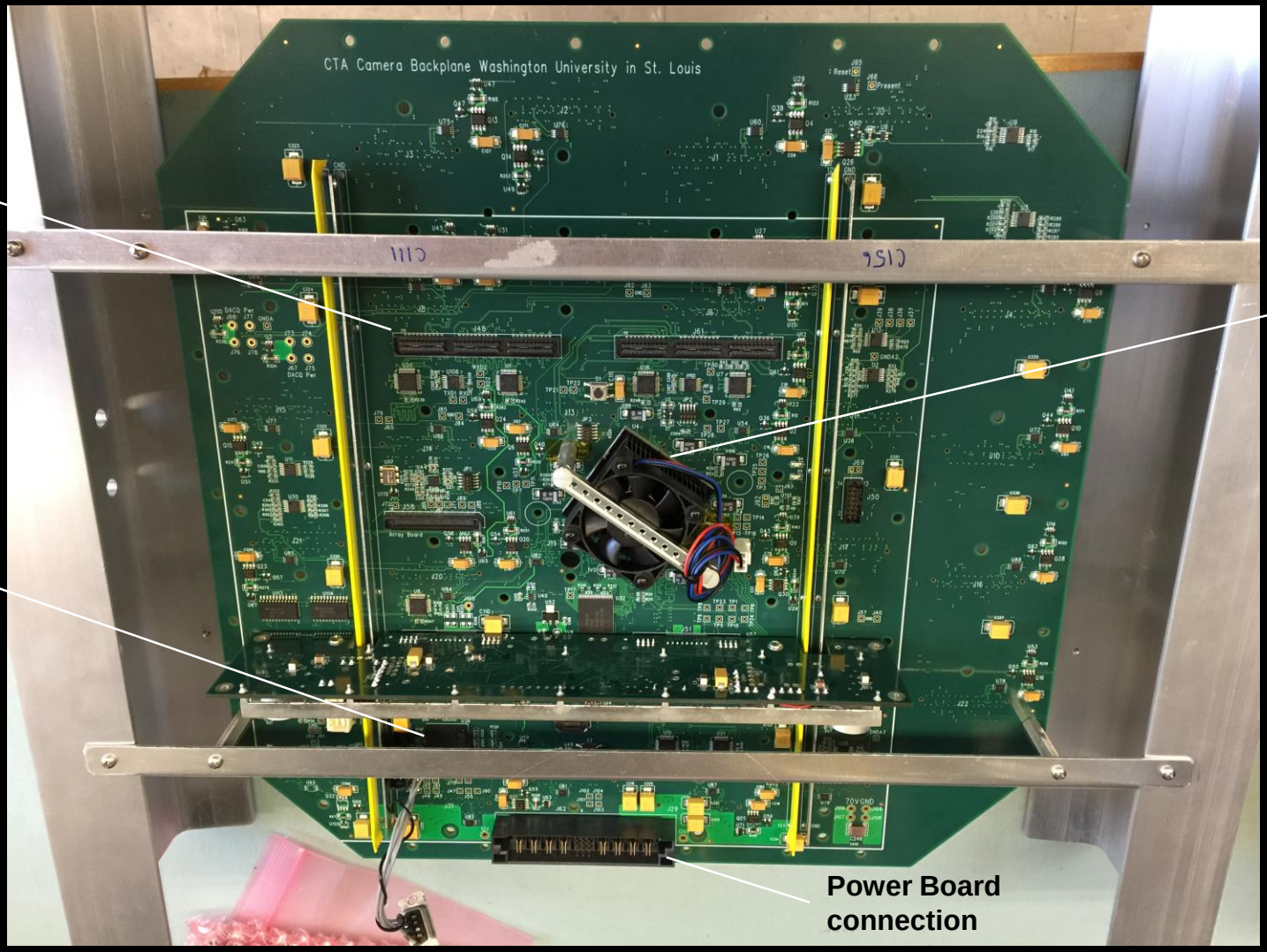


CHEC-M Backplane

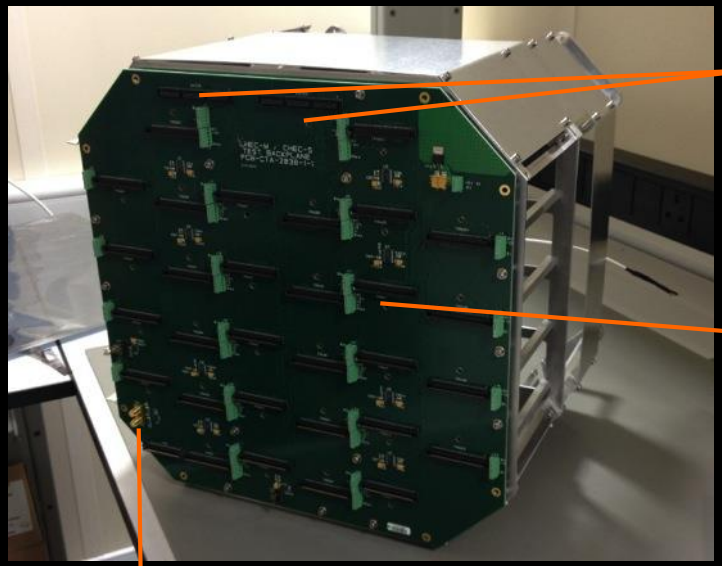


CHEC-M Backplane

- Hardware complete – firmware under development



CHEC-M Backplane



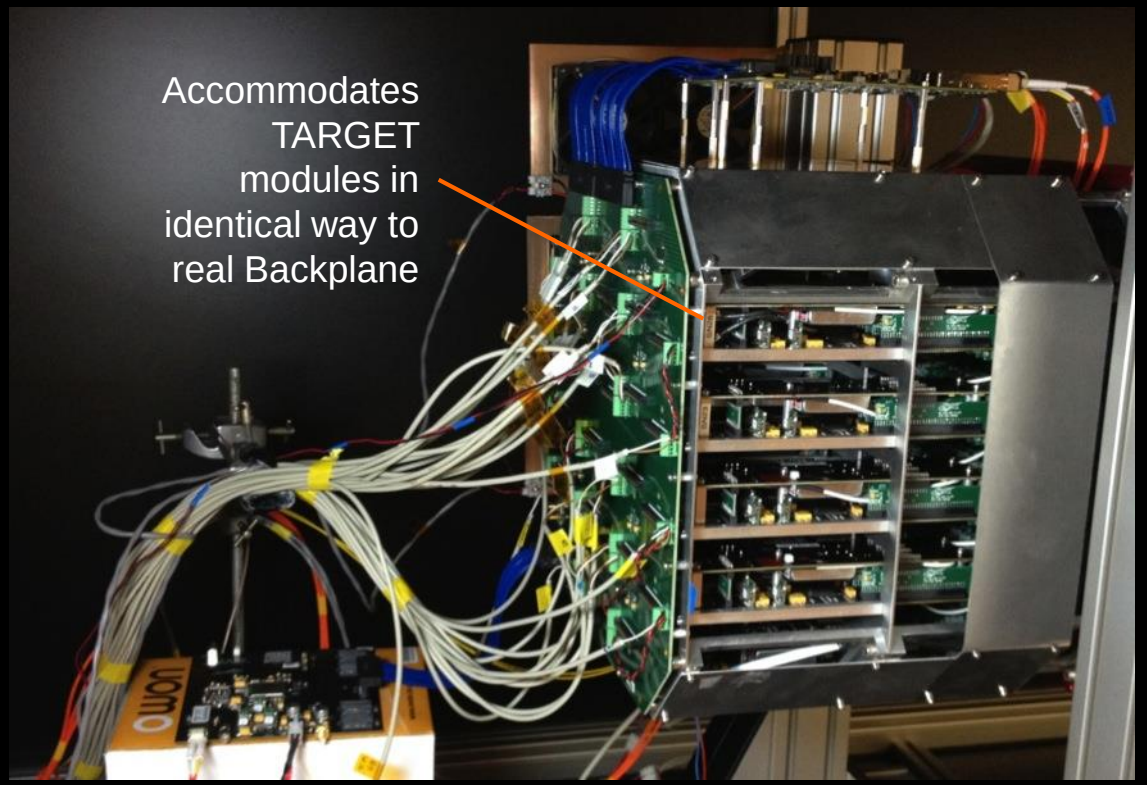
Connection to DACQs

Power to TARGET modules

Trigger and CLK input & fan-out

PSU and switch box

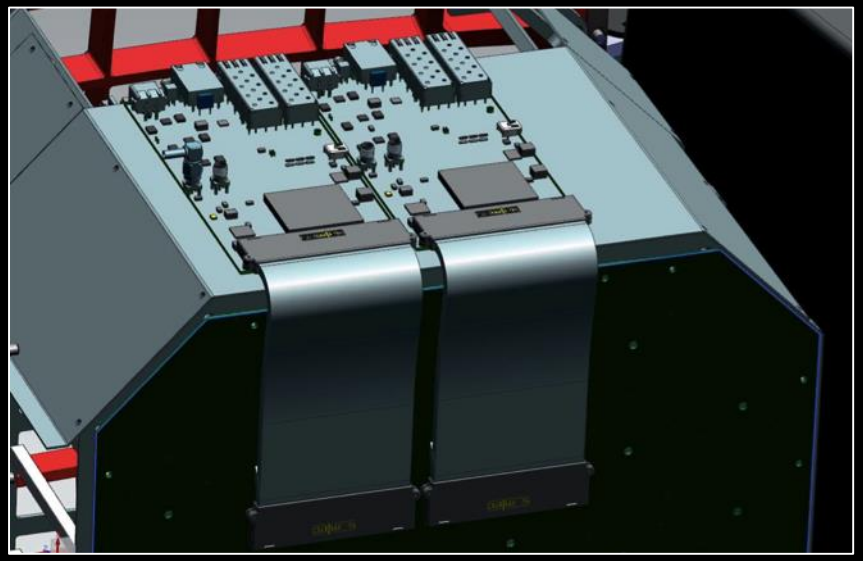
- Lab tests proceeding with a proto-Backplane
- All tests apart from triggering possible

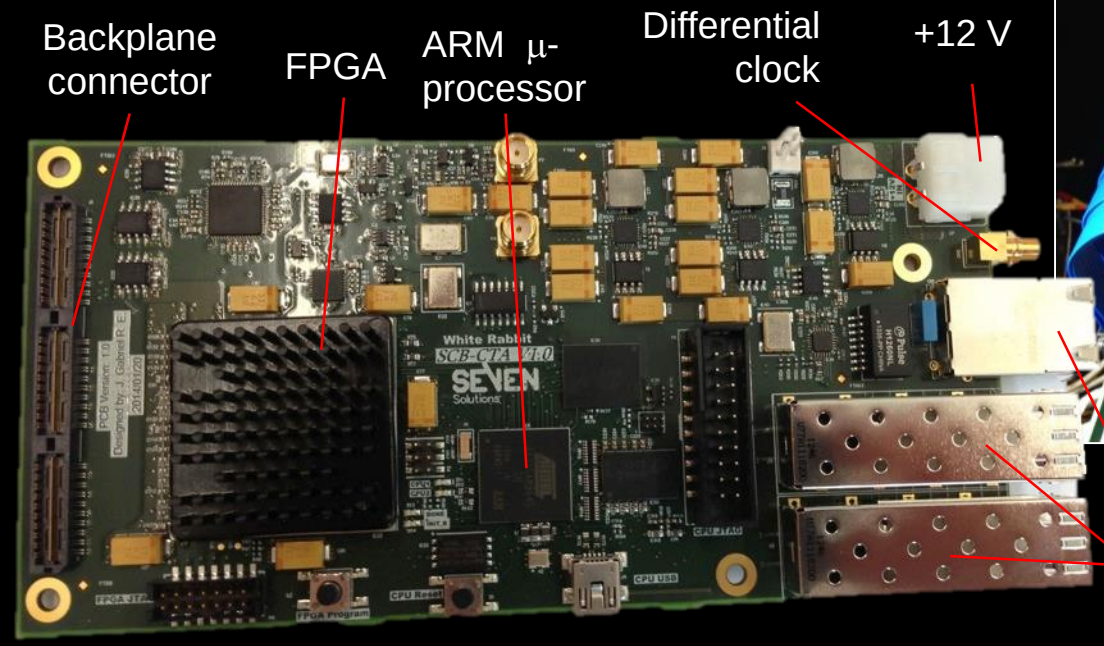


Accommodates TARGET modules in identical way to real Backplane

CHEC-M DACQ Boards

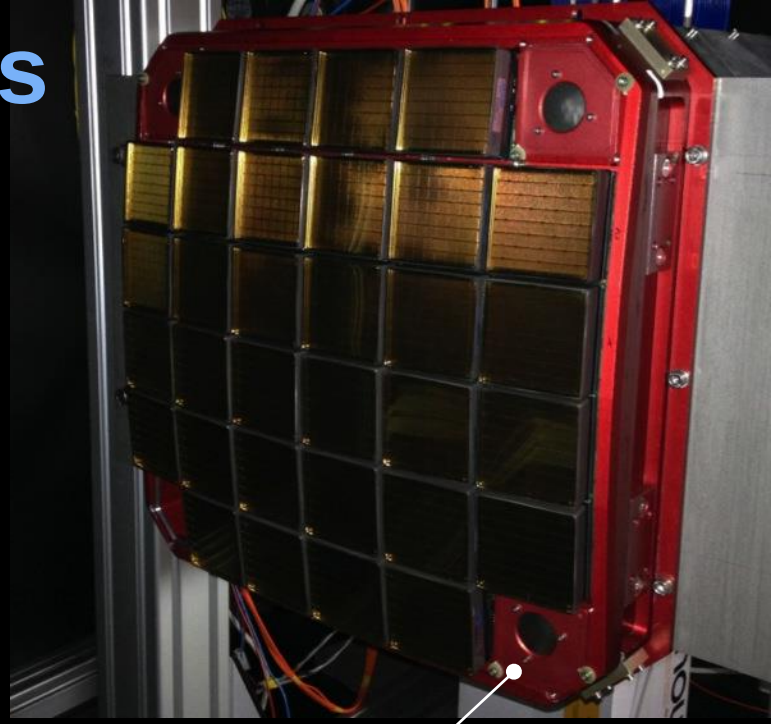
- University of Amsterdam & Seven Solutions:
  - 5 boards for manufactured, 2 iterations, both work, 2 for CHEC-M
- 2 boards provide:
  - 36 port switch
  - 4 x 1 Gb/s uplinks
  - Absolute time synchronisation (using White Rabbit)

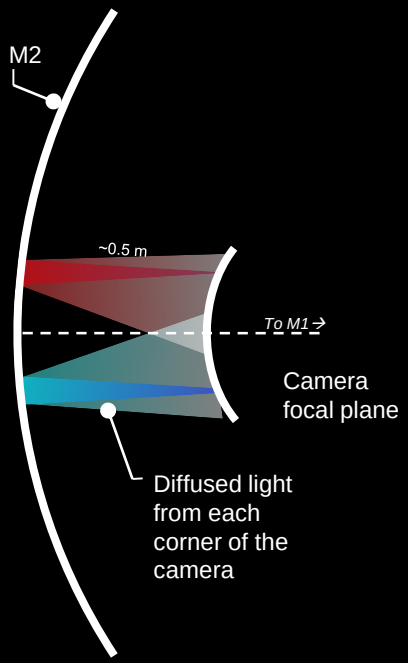


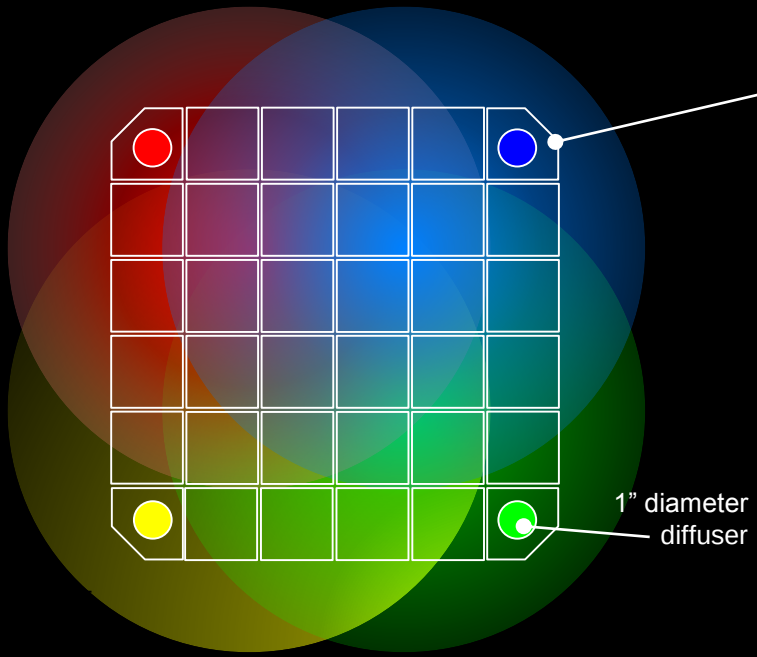


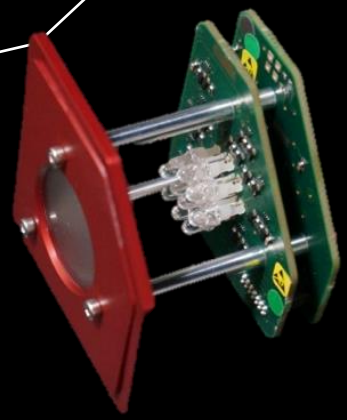
CHEC-M Calibration Units

- Illumination of the focal plane via reflection from the secondary mirror
- Installed in each corner of the camera
- Performance:
  - Multi-LED provides ~1 - 1000 pe
  - Pulse width ~4 ns



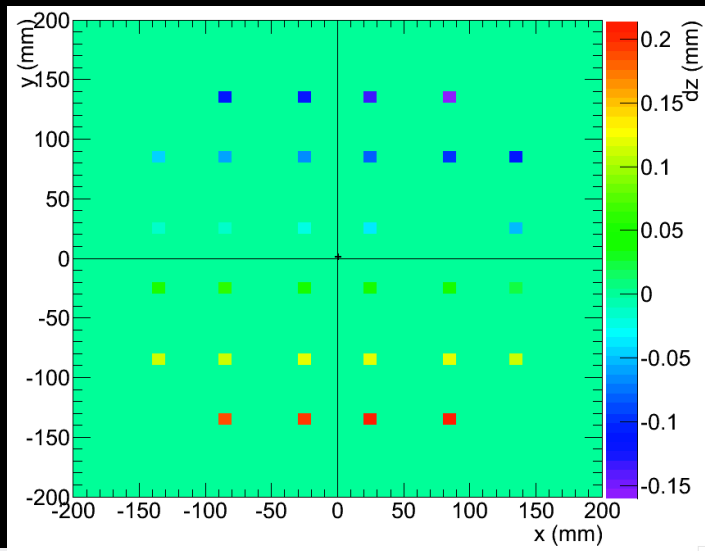


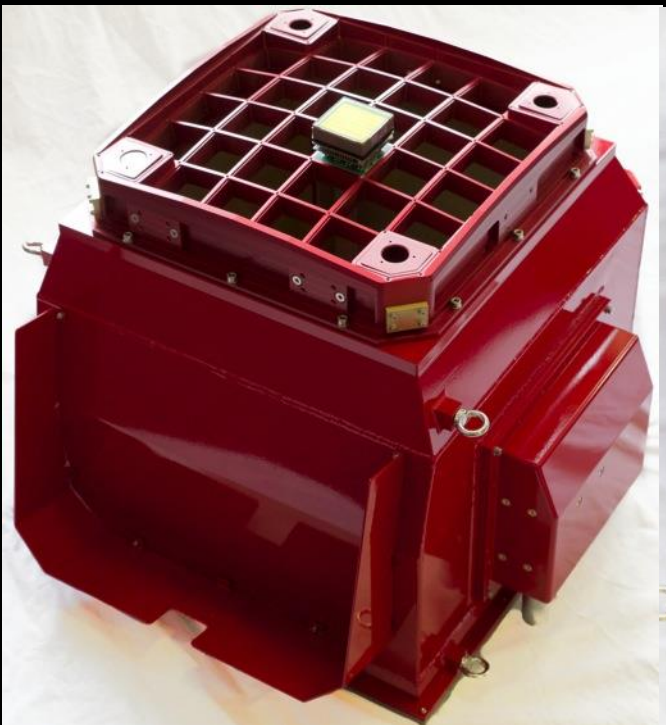




CHEC-M Mechanics

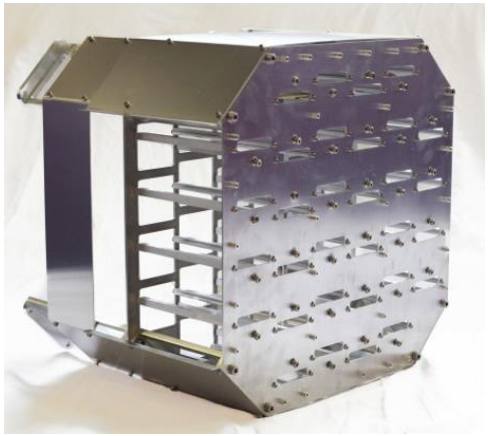
- Machined and bent Aluminum
- Defocus of 1 mm → PSF degradation of 10% (on axis)
  - Achieve ~0.35 mm spread between MAPM centres with no adjustment
  - Can be reduced to 0.035 mm

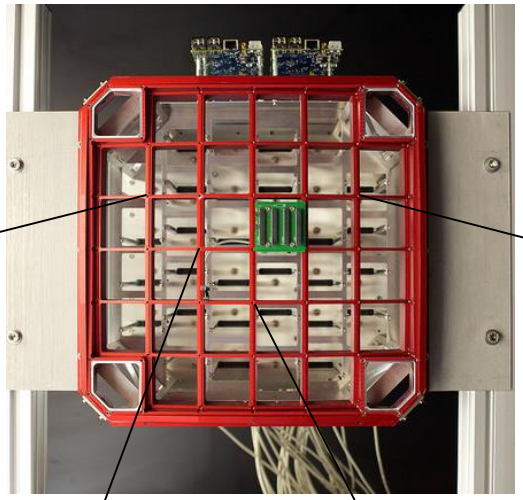


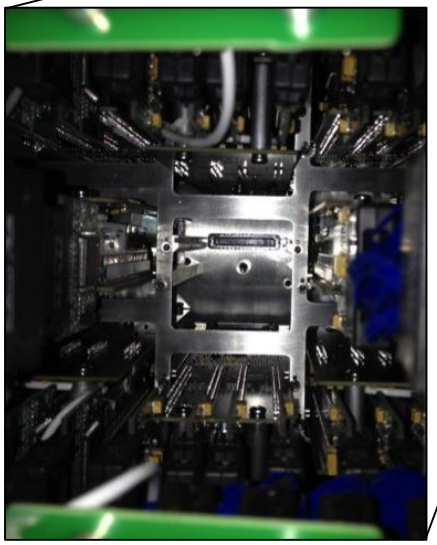


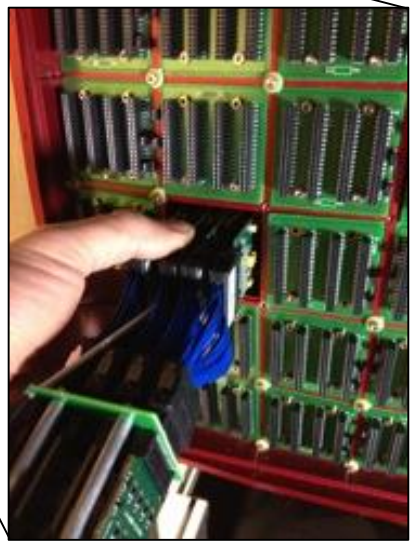
Assembly

- Internal rack built
- Focal plane attached
- Backplane and DACQ boards attached
- TMs inserted



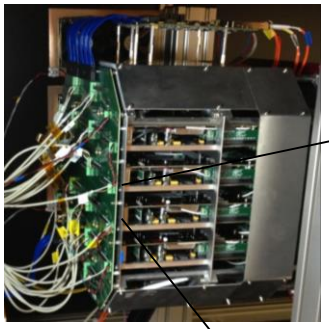


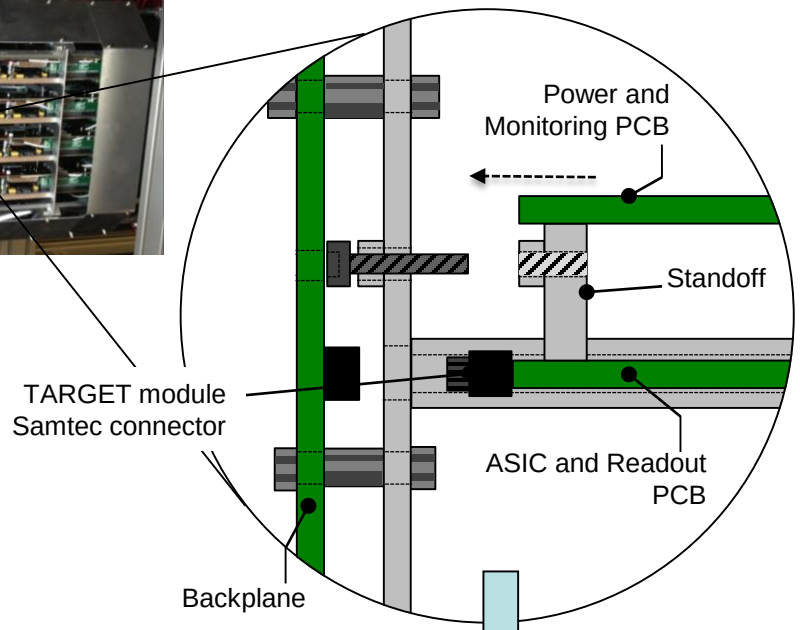


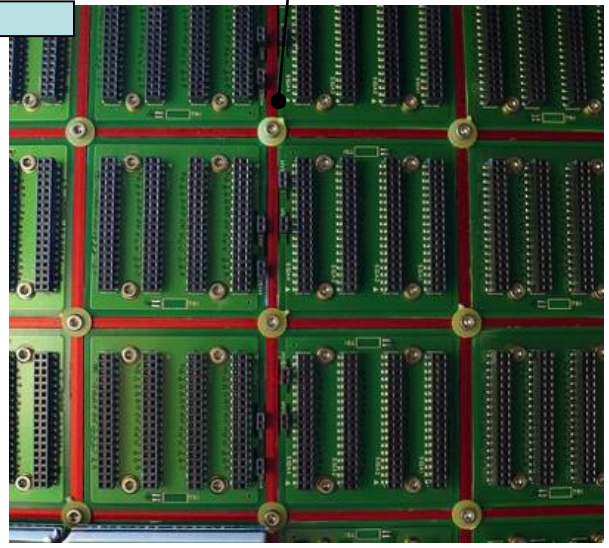


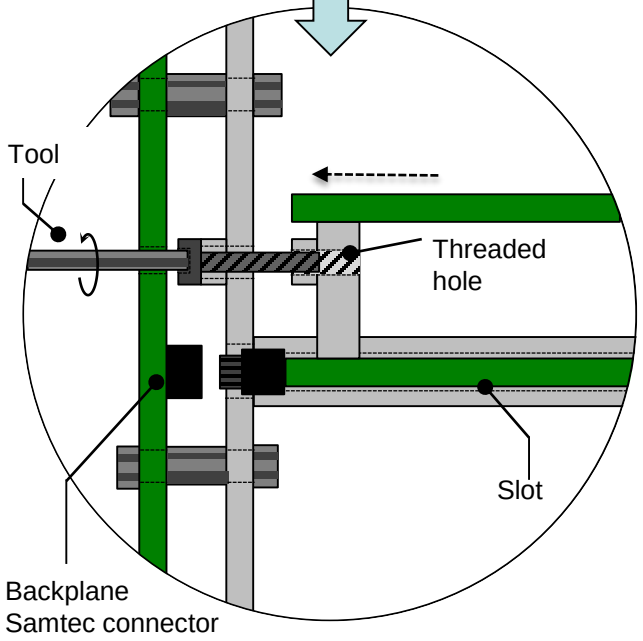
Assembly

- TMs pulled in from rear
  - TARGET module inserted into slot in rack until screw mates with standoff
  - TARGET module pulled into place with screw via tool inserted through backplane access hole
  - TARGET module fully mated with backplane and secured in place
- Pre-amps secured from front
- MAPMs added
- Enclosure added



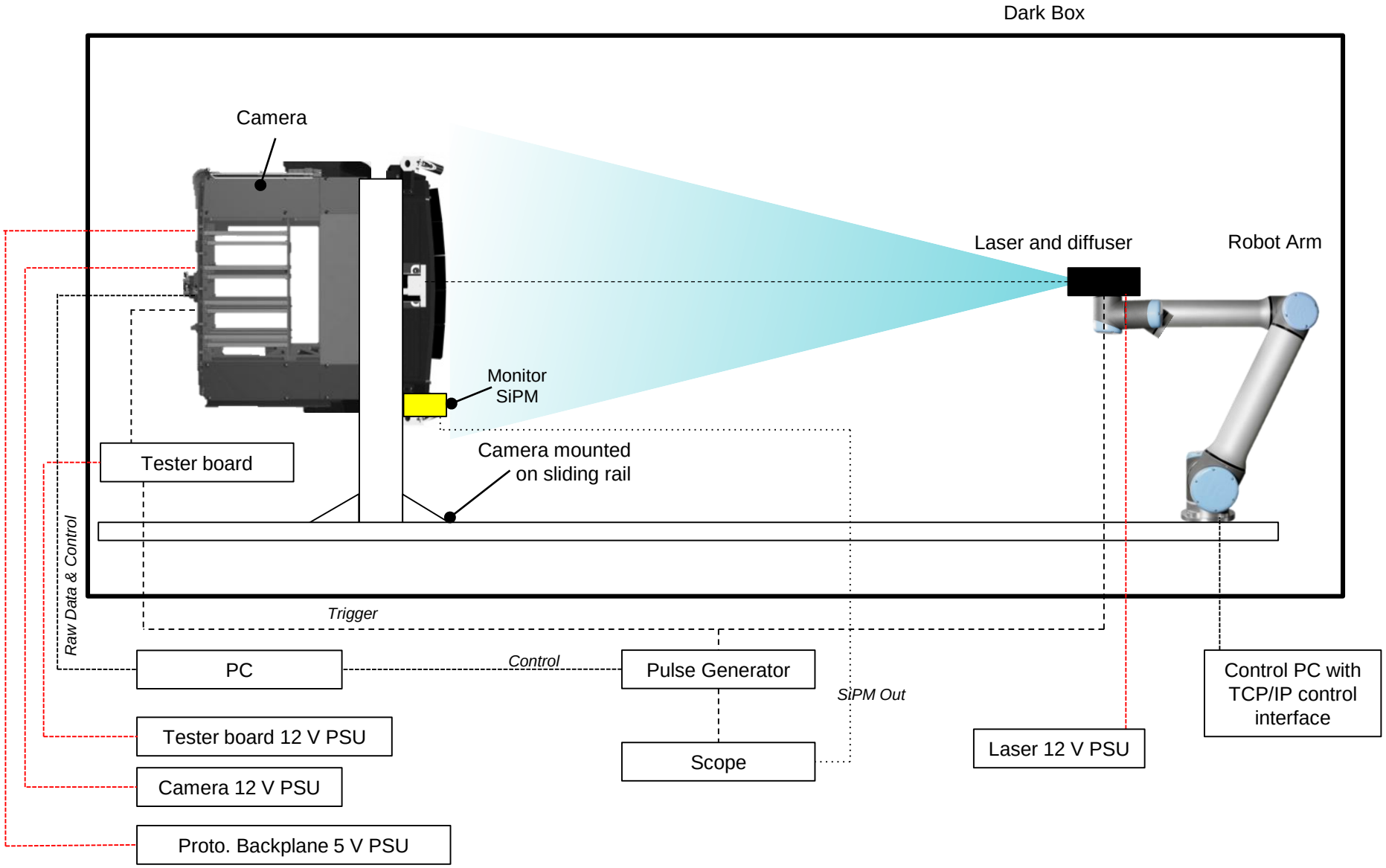






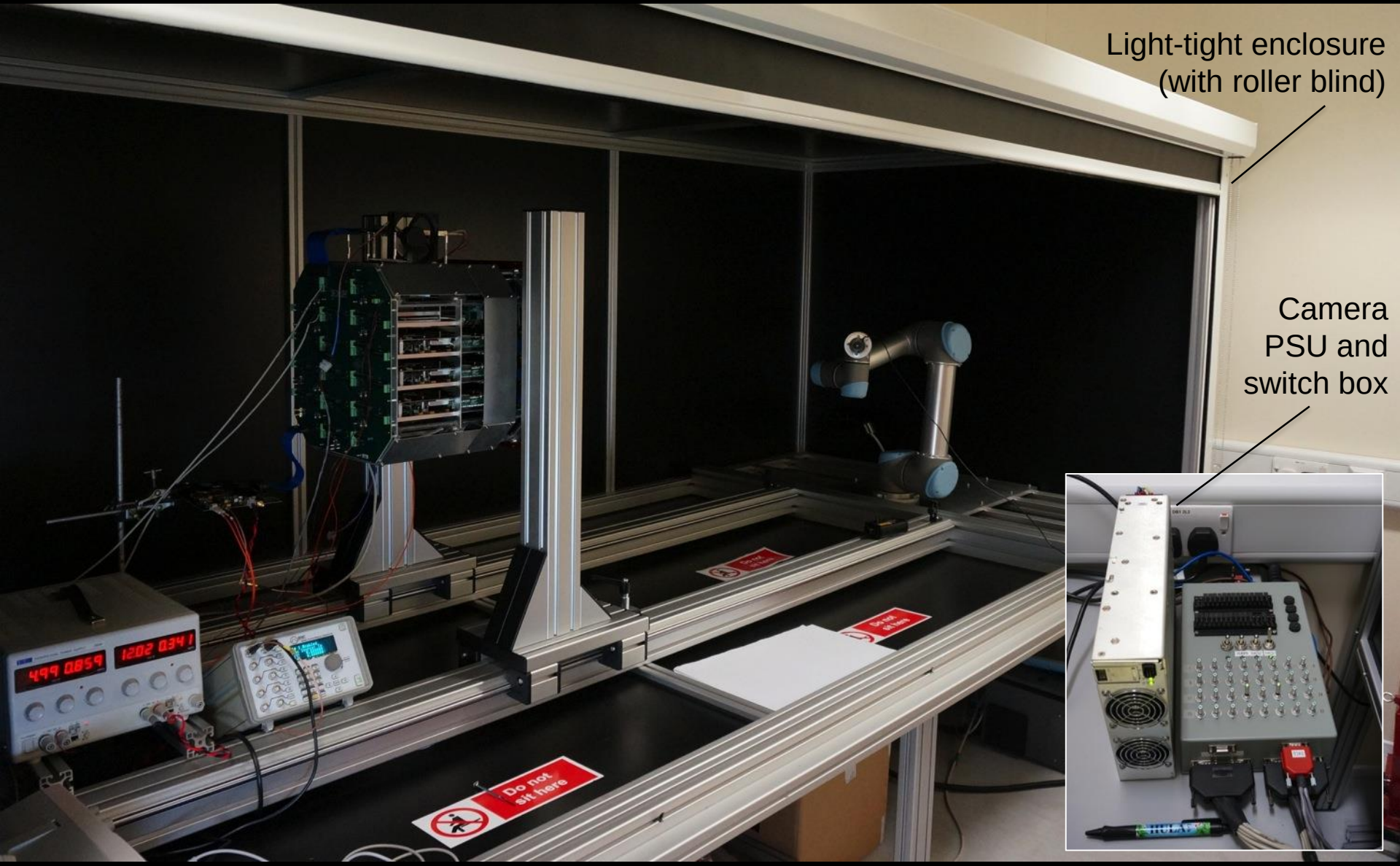
Commissioning Lab Setup

Initial setup for uniform illumination



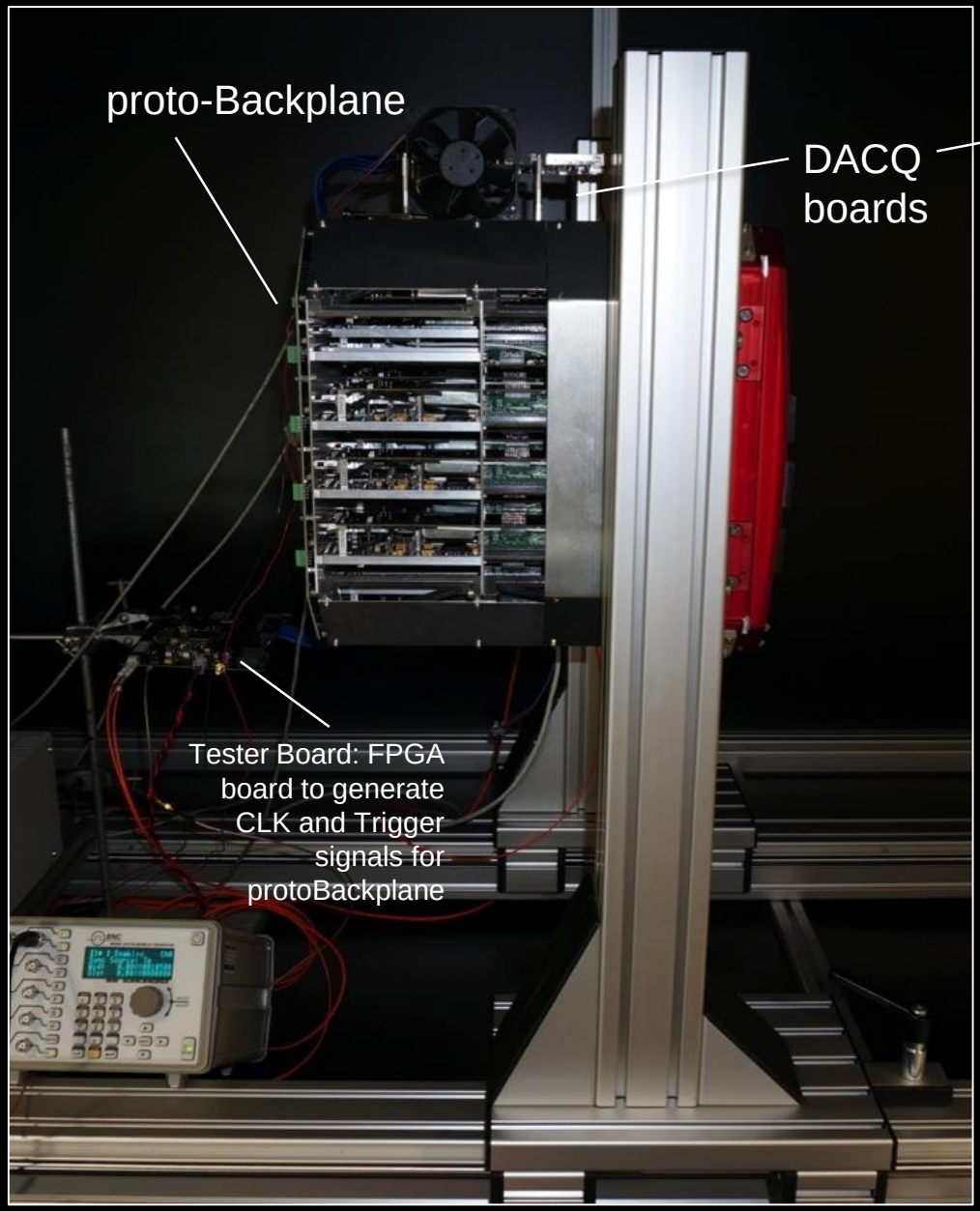
Commissioning Lab Setup

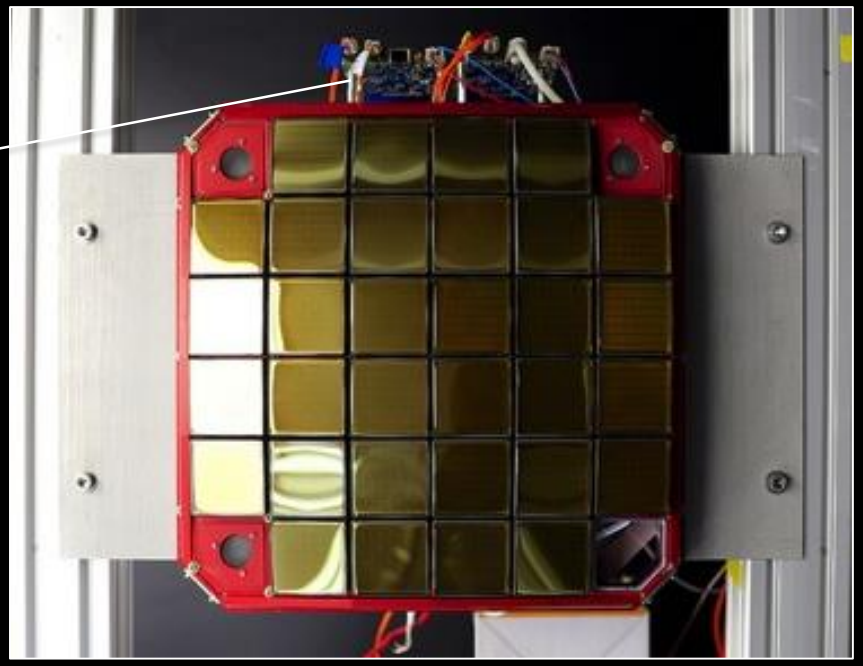
University of Leicester



Commissioning Lab Setup

University of Leicester



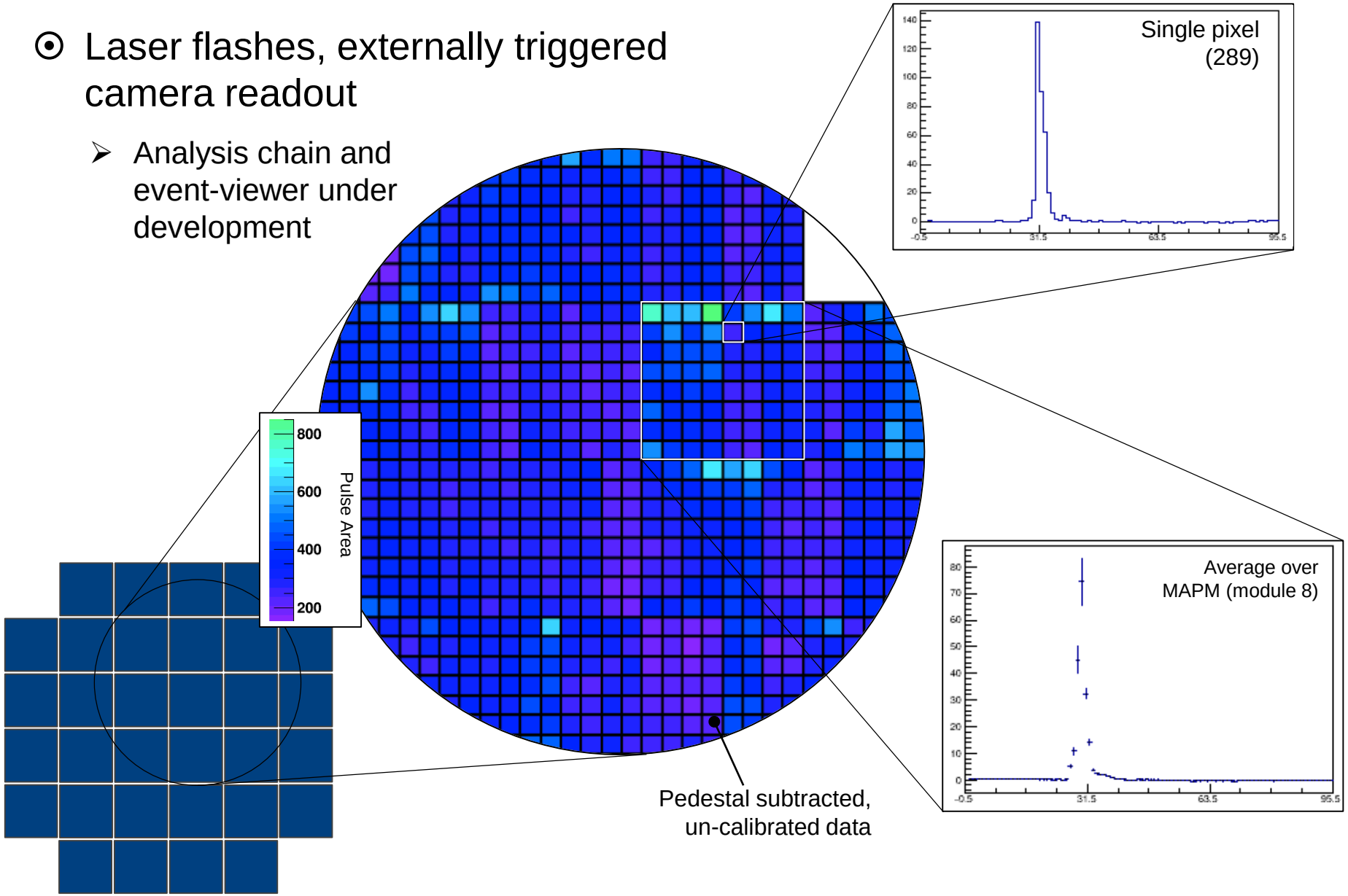


Camera Readout

- Raw data and slow control over 4 x 1 Gbps
- Camera Server and Camera Controller software running as separate processes on 1 PC
- Camera Server
  - Listens for raw data, builds events, writes to disk (binary format stored in fits files, with protobuf headers)
  - Receives run start / stop messages from Camera Controller
- Camera Controller
  - Reads in camera config (protobufs)
  - Setups up the hardware (UDP raw socket to TM, zmq to DACQs)
  - Signals run start / stop to Camera Server and sends run header
  - Monitors camera (e.g. temperature) and writes to a fits file with time stamps
- Offline
  - Analysis chain, uses same protobuf structure for headers / config as online
  - Assembles slow control and raw data based on timestamps
- A lot of manpower has gone into this: libCHEC, see Andrea's talk next…

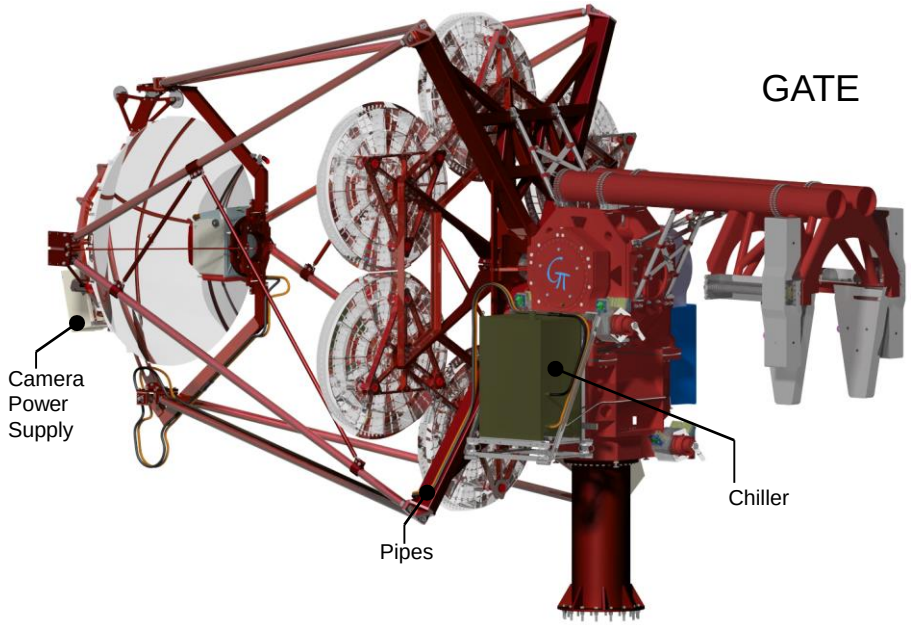
Commissioning Progress

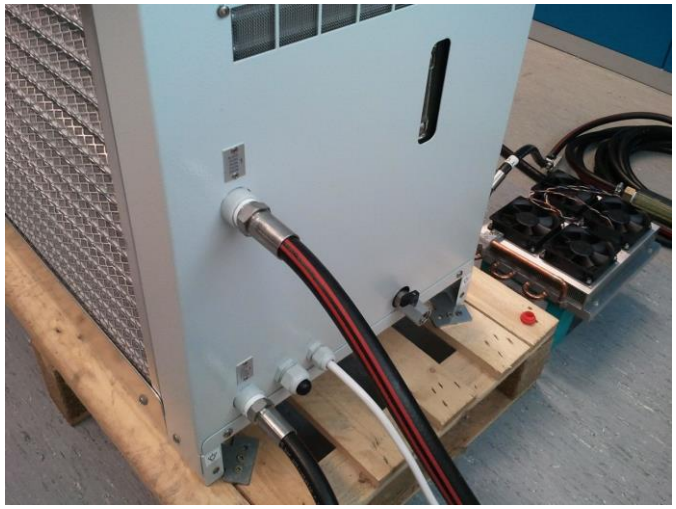
- Laser flashes, externally triggered camera readout
  - Analysis chain and event-viewer under development

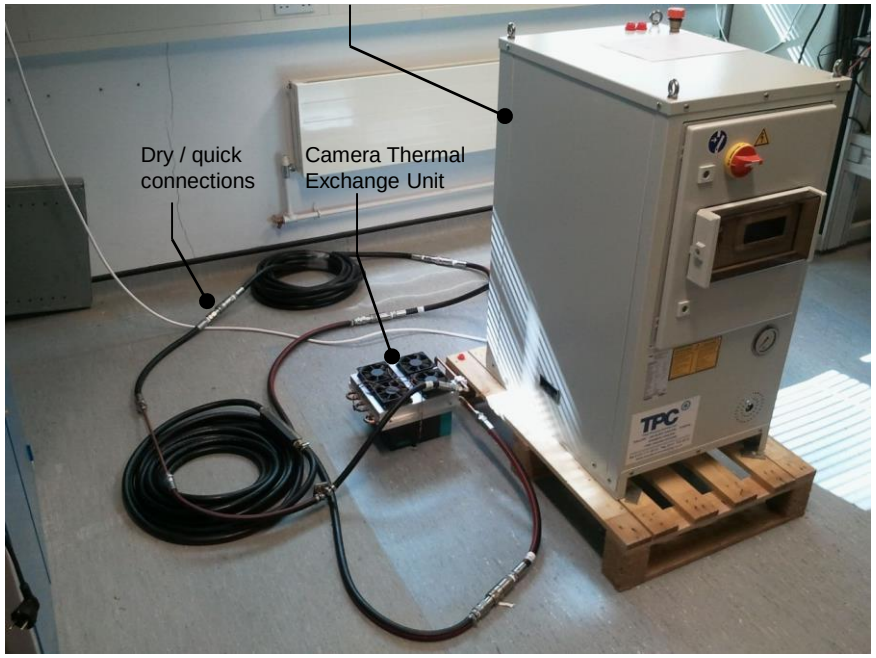


Auxiliary Systems

- PSU
  - Located behind M2
  - Identical to the one being used in the lab
- Chiller
  - Cooling loop now tested in Leicester

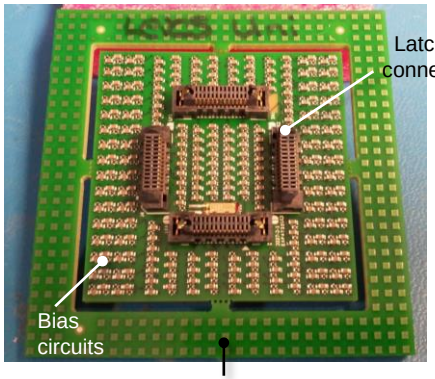


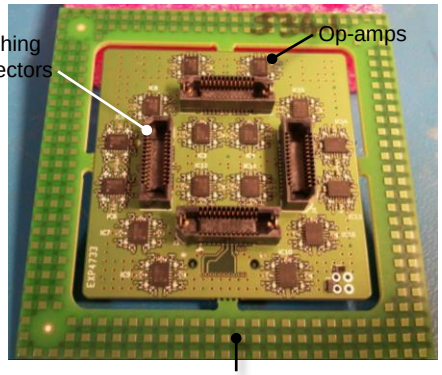


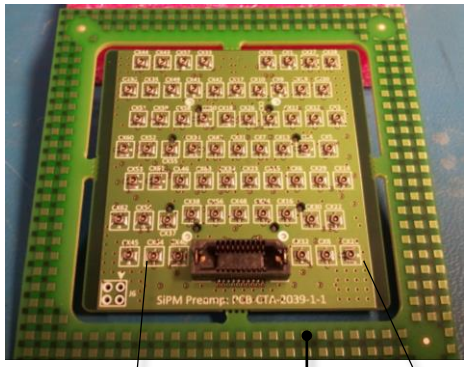


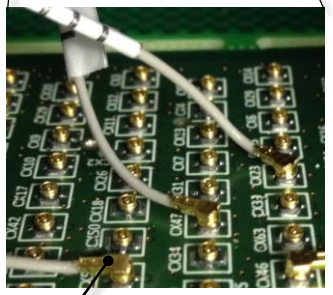
CHEC-S

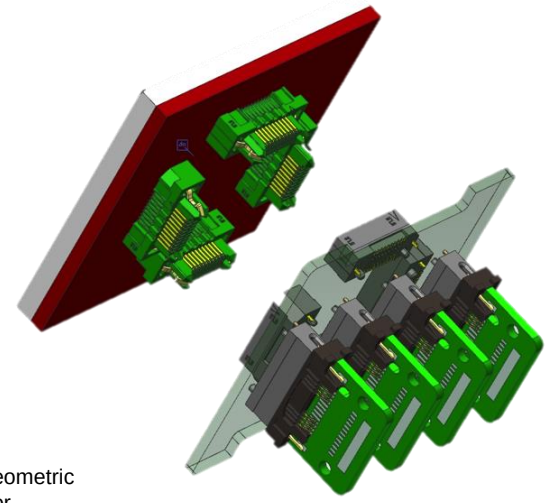
- See previous meetings for overview
- Latest news:
  - TARGET-7 modules under test at ECAP
  - Last part of SiPM tile delivery delayed
  - Front-end buffer and preamp now under test at Leicester with full SiPM tile attached to base



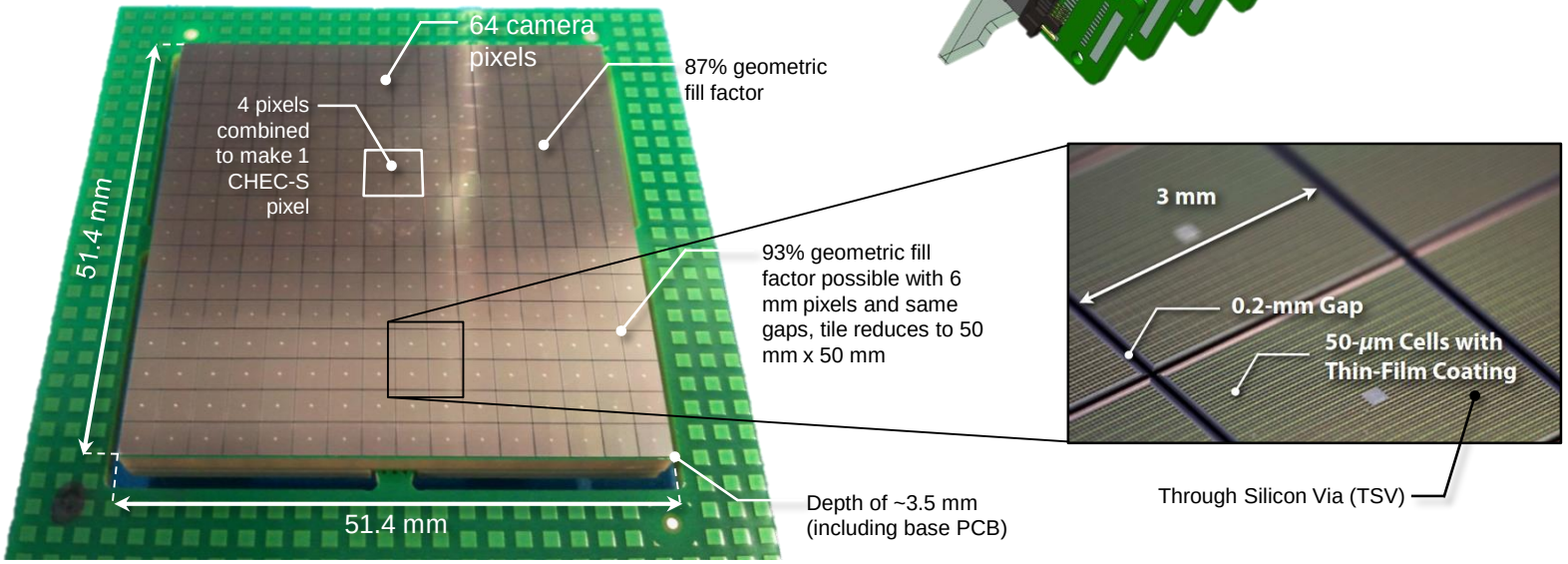






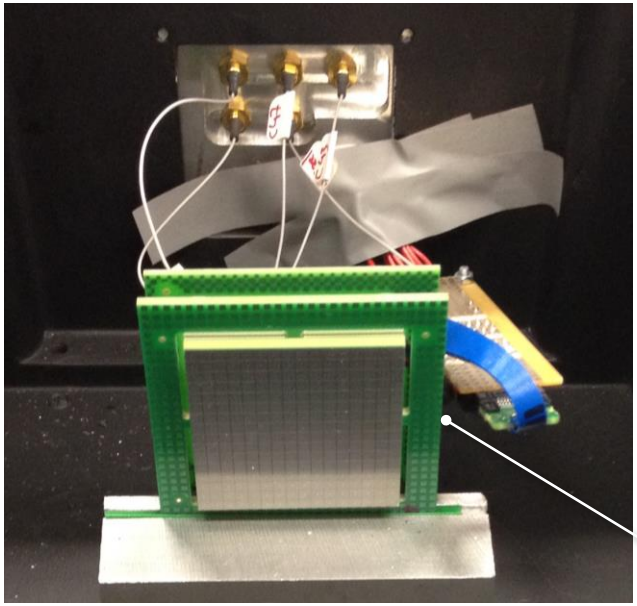


CHEC-S SiPM:
Hamamatsu S12642-1616PA-50

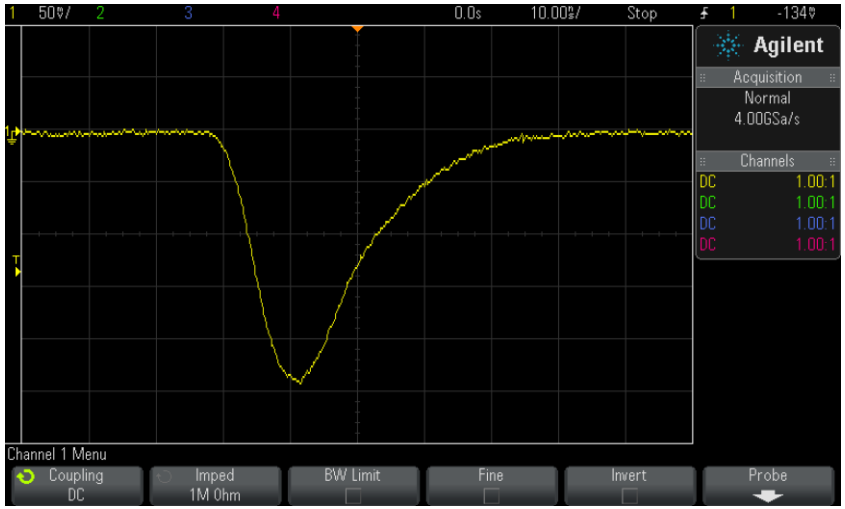


CHEC-S

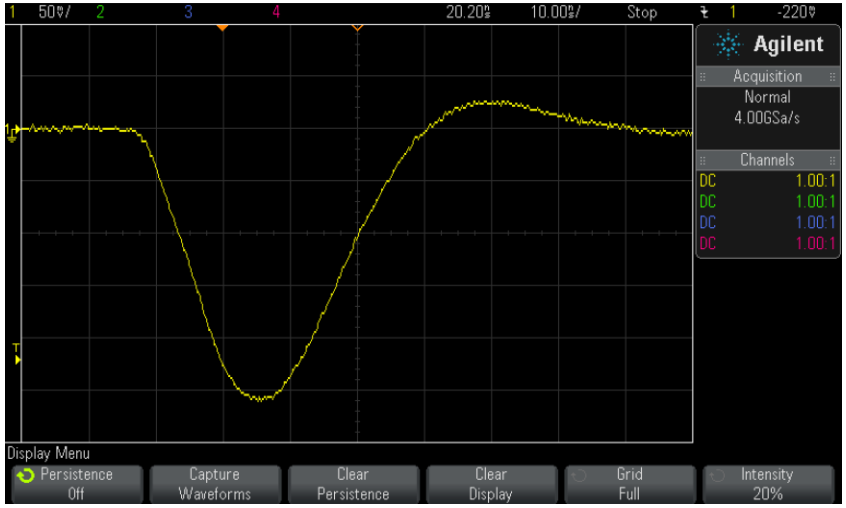
- Front end buffer tests
- Only using mechanical samples thus far
- Faster pulse rise time than previous devices
- Ideal pulse requires more than p/z correction



SiPM tile, base and front-end buffer test in dark box



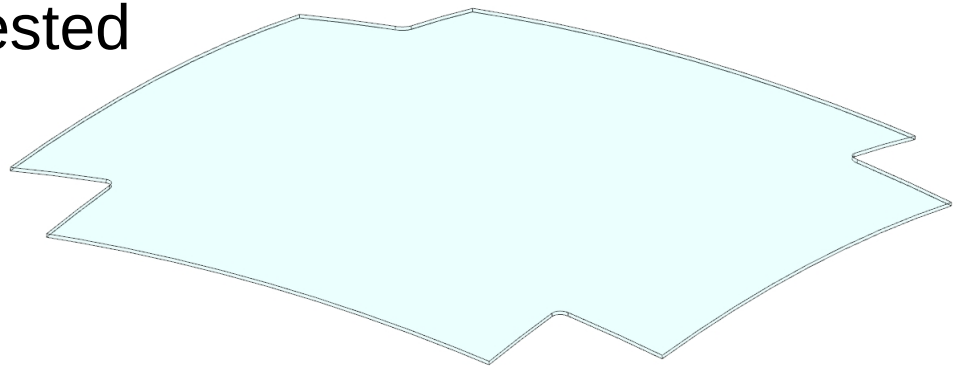
Preamp response with 1 pixel

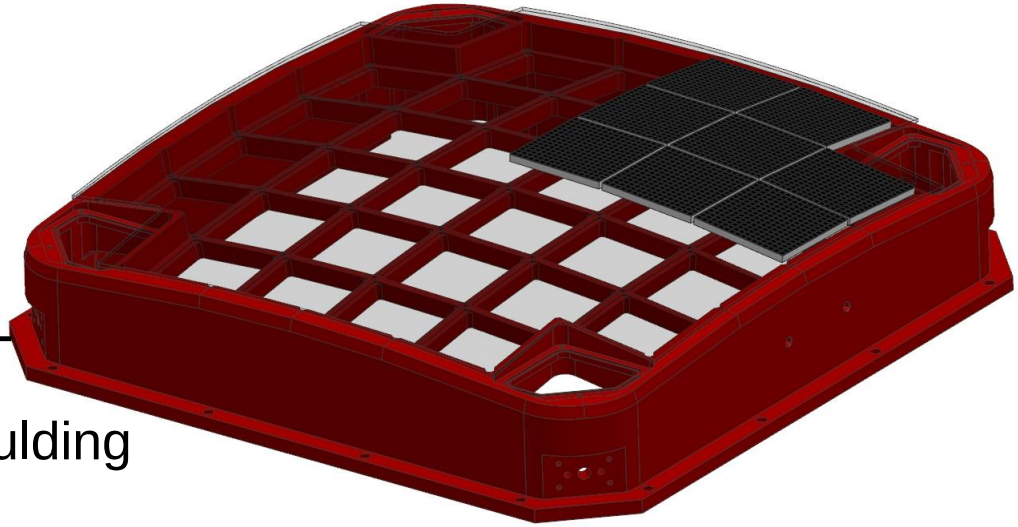


Preamp response with 4 pixels

CHEC-S

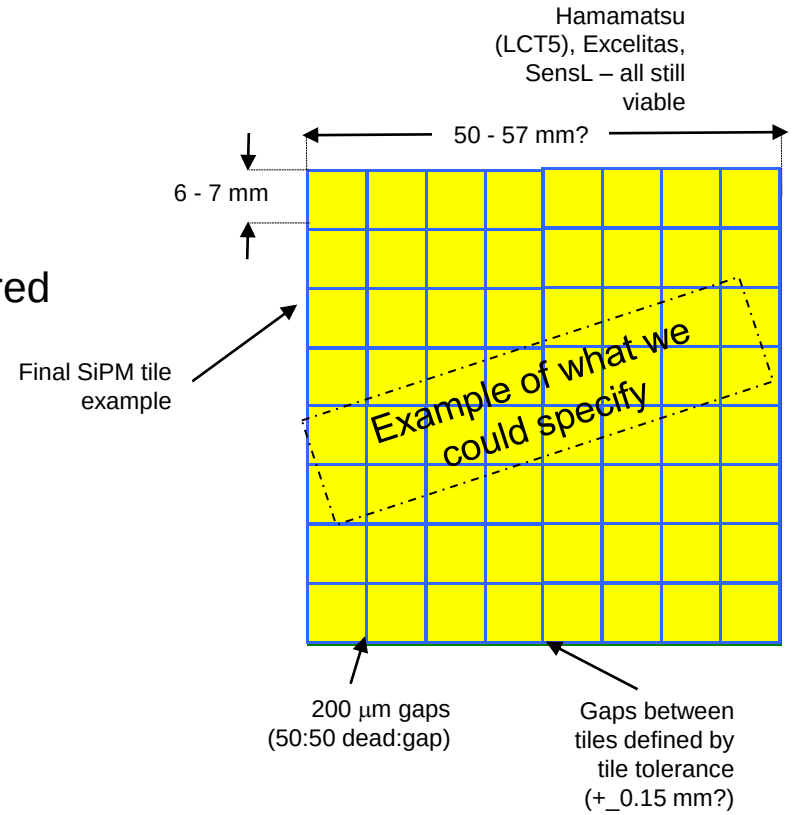
- SiPM – epoxy coating requested
  - Not supplied by Hamamatsu
  - Thin (paralene?) coating only
  - No waterproofing
- Camera window required
- Borofloat-33 glass
  - Not obtainable thin enough
- Shinkolite plastic
  - Not obtainable thin enough
- PMMA – Polycasa XT-UVT
  - Thermal forming or blow moulding
  - 2mm thick→82% trans.
  - But high thermal expansion
  - Need flexible seals





Beyond CHEC-S

- Conventional front-end electronics options
  - CHEC-S discrete solution (integrated near sensor)
  - Existing TARGET7 daughterboard design
- PACTA chip – ICC-UB
  - Multichannel ASIC front-end electronics
  - Initially developed for LST/MST
  - Designed for SiPMs (high capacitance)
  - Integrated additional functionality for SST
- TARGET-C and TARGET-CCTV
  - Substrate noise → 2 separate ASICs required
- Latest SiPMs?
  - Technology still improving
  - No imp. from Hamamatsu after LCT5
  - Other manufacturers still viable
  - Larger pixel size



Summary

- CHEC-M commissioning in progress
- Full testing limited by BP delay
  - ..but delivery imminent
- Meudon field trials
  - Later in 2015
- CHEC-S progressing
  - First batch MPPCs delivered
  - ..and will be attached to PCBs next
  - Second MPPC batch due end-May