The Beetle Reference Manual

— chip version 1.3 —

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document version: 1.3 — preliminary

Abstract

This paper details the electrical specifications, operating conditions and port definitions of the readout chip *Beetle*. The chip is developed for the LHCb experiment and fulfils the requirements of the silicon vertex detector (VELO, VETO), the silicon tracker and the RICH detector in case of multi-anode photomultiplier readout.

It integrates 128 channels with low-noise charge-sensitive preamplifiers and shapers. The pulse shape can be chosen such that it complies with LHCb specifications: a peaking time of 25 ns with a remainder of the peak voltage after 25 ns of less than 30%. A comparator per channel with configurable polarity provides a binary signal. Four adjacent comparator channels are being ORed and brought off chip via LVDS ports. Either the shaper or comparator output is sampled with the LHC-bunch-crossing frequency of 40 MHz into an analog pipeline. This ring buffer has a programmable latency of max. 160 sampling intervals and an integrated derandomising buffer of 16 stages. For analog readout data is multiplexed with up to 40 MHz onto 1 or 4 ports. A binary readout mode operates at up to 80 MHz output rate on two ports. Current drivers bring the serialised data off chip. The chip can accept trigger rates of up to 1.1 MHz to perform a dead-timeless readout within 900 ns per trigger. For testability and calibration purposes, a charge injector with adjustable pulse height is implemented. The bias settings and various other parameters can be controlled via a standard I^2C-interface.

Appropriate design measures have been taken to ensure the radiation hardness against total ionising dose effects in excess of 10 Mrad. A robustness against Single Event Upset is achieved by redundant logic.

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Contents

Document Edition History

This manual describes the chip version 1.3. For versions 1.0, 1.1 and 1.2 please refer to the corresponding version of this manual (LHCb-note 2001-046 and 2002-055).

Version	Date	Author	Description
1.0	11.03.2004	DB, SL	document created
1.1	04.04.2004	SL	updated missing measurement values
1.2	12.04.2004	SL	pulse-parameters
1.3	16.04.2004	SL	modified chap. 4.2, Rclk divider

Chip Version History

Version	Submission Date	Changes relating to previous version
Beetle1.0	April 2000	
Beetle1.1	March 2001	extended test channel including pipeamp output modified pipeline layout analog delay element for I^2C-SDA line added modified pipeamp modified bias network of pipeamp modified multiplexer modified tristate buffer in control circuit
Beetle1.2	April 2002	implementation of a new front-end (set 2c of *BeetleFE1.1*) modified analog input pad geometry (elongated pad opening) introduction of SEU robustness scheme restriction of readout time to 900 ns introduction of 8 additional status bits in data header introduction of a power-up reset introduction of comparator mask bit per channel introduction of test pulse selection bit per channel additional LVDS mode of current output buffer on-chip trigger synchronisation increase of pipeline depth by 1 hard-wired I^2C-chip address (defined via bond pads) introduction of SCHMITT-triggers in the I^2C-pads reduction of DAC resolution from 10 to 8 bits increase of max. deliverable bias current to 2 mA additional power pads at the back side
Beetle1.3	June 2003	fix of sticky charge effect: analog delay of `MuxTrack` signal increased comparator channel threshold resolution (5 bits) improved output buffer: fully diff. current buffer, increased gain improved multiplexer switching control minor bug fixes in control logic: daisy chain operation, operation at reduced Rclk frequency new I^2C-pads: 5 V compatible reduced number of flip-flops in multiplexer (from 414 to 138) reduced number of clock buffers in logic core (from 275 to 104) on-chip blocking of power nets (total blocking capacitance: $\mathcal{O}(1\,\mathrm{nF})$) modified front-end power pad distribution improved shaper power routing improved front-end biasing scheme separation of comparator core power from comparator LVDS power improved pipeamp power routing separation of power supply of multiplexer and logic core implementation of two new power pads for logic core merged pad openings of adjacent power pads (in total $\sim$0.9 nF) improved guard-ring structures (n-well and substrate contacts) increased overall chip size by 300 μm in x: $5400\times6100\mu\mathrm{m}^2$

1 Chip Architecture

The *Beetle* can be operated as analog or alternatively as binary pipelined readout chip. It implements the basic RD20 front-end electronics architecture [1, 2, 3]. Fig. 1 shows a schematic block diagram of the chip.

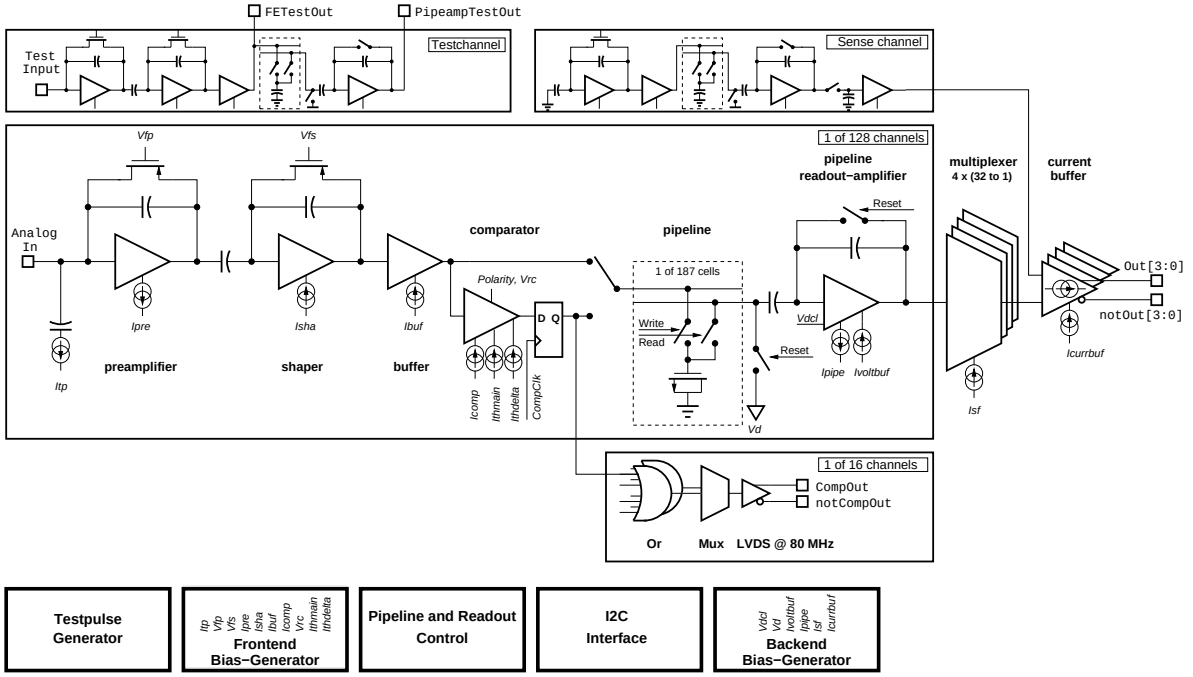


Figure 1: Schematic block diagram of the *Beetle* readout chip[‡].

The chip integrates 128 channels, each consisting of a low-noise charge-sensitive preamplifier, an active CR-RC pulse shaper and a buffer. They form the analog front-end. The equivalent noise charge (ENC) of the front-end has been measured as ENC = $497\,\mathrm{e}^- + 48.3\,\mathrm{e}^-/\mathrm{pF} \cdot \mathrm{C}_{in}$. The shape of the front-end pulse can be chosen according to the specific requirements of the application. The minimum risetime (10-90%) is well below 25 ns, the remainder of the peak voltage after 25 ns can be adjusted to less than 30% for load capacitances $\mathrm{C}_{in} \leq 35\,\mathrm{pF}$. A comparator discriminates the front-end's output pulse. The threshold is adjustable per channel and input signals of both polarities can be processed. Four adjacent comparator channels are grouped by a logic OR, latched, multiplexed by a factor of 2 and routed off the chip via low voltage differential signalling (LVDS) ports at 80 MHz. Either the shaper- or the comparator output is sampled with the LHC bunch-crossing frequency at 40 MHz into an analog pipeline which has a programmable latency of max. 160 sampling intervals and an integrated multi-event buffer of 16 stages. The signal stored in the pipeline is transfered to the multiplexer via a resettable charge-sensitive amplifier (pipeamp). Within a readout time of 900 ns current drivers bring the serialised data off chip. The output of a dummy channel is subtracted from the analog data to compensate common mode effects. All amplifier stages are biased by forced currents. On-chip digital-to-analog converters (DACs) with 8 bit resolution generate the bias currents and voltages. For test and calibration purposes a charge injector with adjustable pulse height is implemented on each channel. The bias settings and various other parameters like the trigger latency can be controlled via a standard $\mathrm{I}^2\mathrm{C}$-interface [7]. All digital control and data signals, except those for the $\mathrm{I}^2\mathrm{C}$-ports, are routed via LVDS ports.

The choice of a deep-submicron process technology (0.25 μm standard CMOS) with a thin gate oxide ($t_{ox} \approx 62\,\text{Å}$) and the consistent use of enclosed NMOS transistors reduces a shift in the transistor

[‡]For a derivation of the pipeline depth refer to [4].

threshold voltage and eliminates "end-around" leakage current paths. This establishes a total ionising dose (TID) radiation hardness in excess of 45 Mrad. Single Event Latch-up (SEL) is suppressed due to the implementation of guard-rings. The continuous use of triple-redundant logic ensures a robustness against Single Event Upset (SEU).

2 Electrical Specifications

2.1 DC Characteristics

Table 1: DC characteristics of *Beetle1.3*

Supply	Min. [V]	Nom. [V]	Max. [V]	Description
Vdda	2.2	2.5	2.7	Positive analog supply
Gnda	-0.2	0.0	0.2	Negative analog supply
Vddd	2.2	2.5	2.7	Positive digital supply
Gndd	-0.2	0.0	0.2	Negative digital supply
VddPre	2.2	2.5	2.7	Positive preamplifier supply
GndPre	-0.2	0.0	0.2	Negative preamplifier supply (detector ground)
VddComp	2.2	2.5	2.7	Positive comparator output supply
GndComp	-0.2	0.0	0.2	Negative comparator output supply
VddCPB	2.2	2.5	2.7	Positive comparator pad supply at bottom side
GndCPB	-0.2	0.0	0.2	Negative comparator pad supply at bottom side
VddCPT	2.2	2.5	2.7	Positive comparator pad supply at top side
GndCPT	-0.2	0.0	0.2	Negative comparator pad supply at top side
VddMux	2.2	2.5	2.7	Positive multiplexer supply
GndMux	-0.2	0.0	0.2	Negative multiplexer supply
VddTX	2.2	2.5	2.7	Positive output driver supply
GndTX	-0.2	0.0	0.2	Negative output driver supply

Power Consumption Typical values for the power consumption of a *Beetle1.3* chip are given in Table 2 for various setup configurations. Nominal register settings refer to Table 13.

Table 2: Typical power consumption.

Chip configuration					I_{supply} [mA]		P [mW/ch]	
Comparator		Clock	Trigger		analog readout ports			
LVDS term.	digital	40 MHz	1.1 MHz	Registers	1	4	1	4
open	disabled	no	no	0	24.5	24.5	0.48	0.48
open	disabled	yes	no	0	64.5	64.5	1.26	1.26
open	disabled	yes	yes	0	64.5	64.5	1.26	1.26
open	disabled	no	no	nom.	192.0	221.5	3.75	4.33
open	disabled	yes	no	nom.	232.0	261.5	4.53	5.11
open	disabled	yes	yes	nom.	237.0	267.0	4.63	5.21

2.2 Signal Levels

The *Beetle* chip has 3 different kind of I/O pads. The signal levels for these pads are given in Table 3.

Table 3: Specification of signal levels.

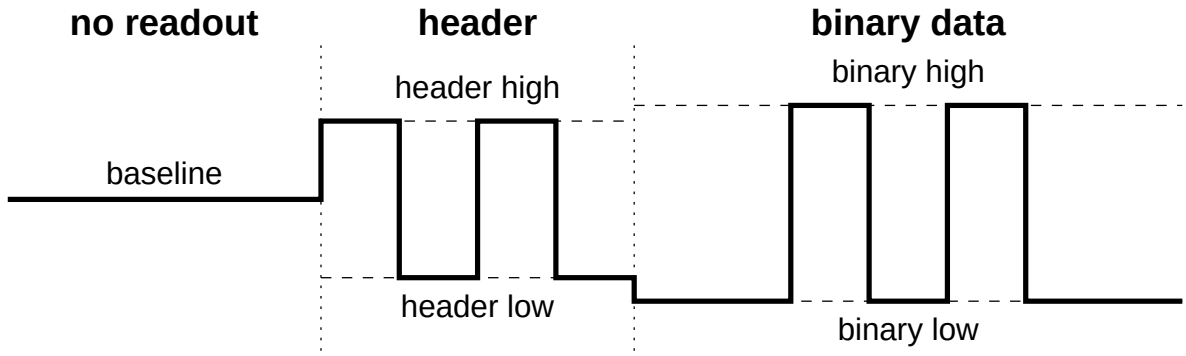
I^2C							
	logic 0			logic 1			Unit
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	-0.7	1.1	0.0	1.5	7.0	2.5	V
output	—	—	2.5	—	—	2.5	V
CMOS							
	logic 0			logic 1			Unit
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	-0.7	1.1	0.0	1.4	3.3	2.5	V
output	—	—	0.0	—	—	2.5	V
LVDS (100 Ω termination)							
	offset voltage			differential voltage			Unit
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	0.0	2.5	1.2	0.1	2.5	0.2	V
output	—	—	1.02	—	—	1.38	V

2.3 Output Characteristics

The *Beetle* chip provides an *analog* as well as a *binary* output mode. A differential current is transmitted in each case by the *Beetle* current output driver.

Fig. 2 specify the signal levels of the *Beetle* current output driver for different modes of operation. All levels were measured with a 100 Ω termination resistor between `AnalogOut<X>` and `notAnalogOut<X>`. The internal current of the output driver was programmed to the nominal value given in Table 3.

Fig. 3 gives an example of a receiver circuit for analog signals using the AD8130 transimpedance amplifier [5] and binary signals using the DS90C032 [6] LVDS receiver.



		BinaryHeader: ON CompDisable: OFF PipelineMode: ON			BinaryHeader: OFF CompDisable: OFF PipelineMode: ON			BinaryHeader: OFF CompDisable: ON PipelineMode: ON			BinaryHeader: OFF CompDisable: ON PipelineMode: OFF		
		AO [mV]	nAO [mV]	Iout [mA]	AO [mV]	nAO [mV]	Iout [mA]	AO [mV]	nAO [mV]	Iout [mA]	AO [mV]	nAO [mV]	Iout [mA]
baseline		1152	824	3.28	973	978	-0.05	973	978	-0.05	973	978	-0.05
header	high	840	1184	-3.44	916	1058	-1.42	916	1058	-1.42	916	1058	-1.42
	low	1152	824	3.28	1014	912	1.29	1014	912	1.29	1014	912	1.29
binary	high	760	1432	-6.72	760	1432	-6.72	1121	842	2.79	analog readout		
	low	1164	816	3.48	1164	816	3.48						

Figure 2: Current output driver levels, measured over a 100 Ω resistor

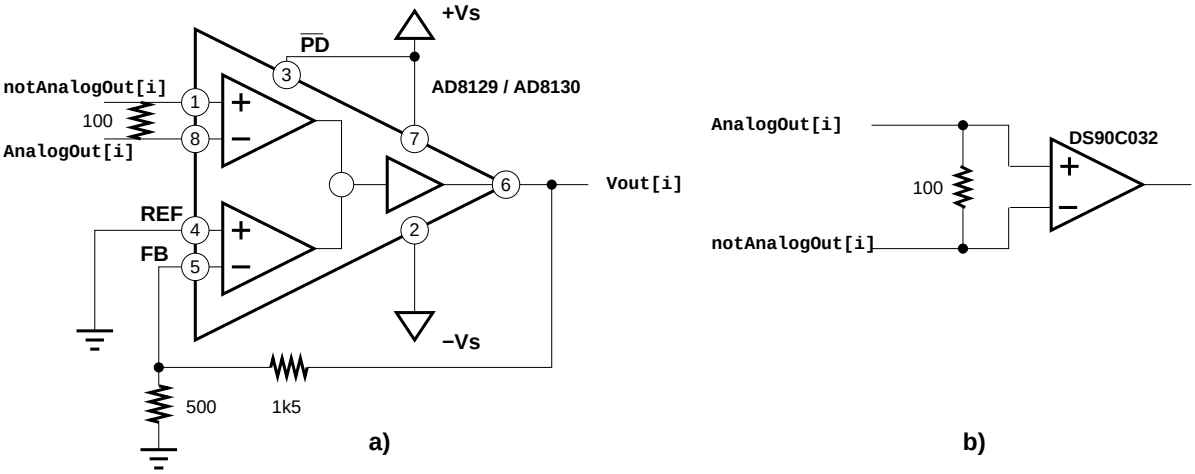


Figure 3: Example of a receiver circuit for the analog (a) and binary (b) output signals. In case of analog signals the AD8130 amplifier is used, in case of binary signals the DS90C032 LVDS receiver.

3 Operating the *Beetle* Chip

3.1 Front-end Pulse Shape

The front-end output signal is a semi-Gaussian pulse which can be characterised by three parameters:

- peaking time t_p $(0-100\%)$ or rise time t_r $(10-90\%)$,
- peaking voltage V_p and
- remainder R, which is the ratio between the signal voltage 25 ns after the peak (V_{25+}) and V_p.

The peaking time is sometimes hard to measure since the starting point of the pulse is not well defined, so the rise time t_r $(10-90\%)$ is usually quoted. Fig. 4 explains the various parameters.

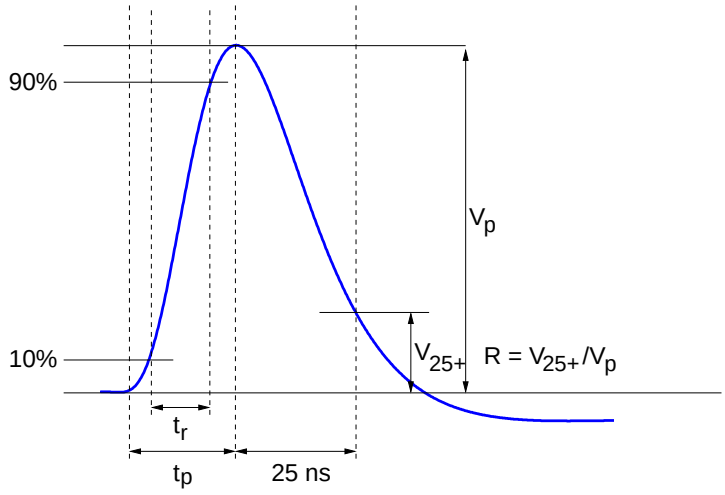


Figure 4: Semi-Gaussian pulse with the corresponding parameters characterising the shape.

Information about the front-end's pulse shape can be obtained on a *Beetle* readout chip from either the test channel output (`TestOutput`, pad no. 242) or from a *pulse shape scan*. Here, the front-end's output is read out via the pipelined path while the preamplifier input signal is shifted w. r. t. the sampling clock.

The pulse shape can be varied by 5 bias parameters:

Ipre sets the preamplifier bias current. Higher currents decrease the rise time and the remainder and increase the pulse undershoot.

Isha defines the shaper bias current. Increasing currents shift the DC-offset to lower values and result in a slightly decreasing rise time, remainder and undershoot.

Ibuf sets the buffer bias current. It does not affect the shape of the pulse, but the DC-offset.

Vfp determines the preamplifier feedback resistance. It defines the time constant for discharging the preamplifier's integration capacitor and therefore the tolerable input charge rate.

Vfs controls the shaper feedback resistance. Increasing *Vfs* values enlarge the peaking time, the peaking voltage as well as the remainder (cf. Fig. 6).

Fig. 5 depicts the variation of the pulse shape for four example bias parameter settings. For the nominal settings listed in Table 13, i.e. Ipre = 600 μA, Isha = Ibuf = 80 μA, Vfp = Vfs = 0 V, the front-end

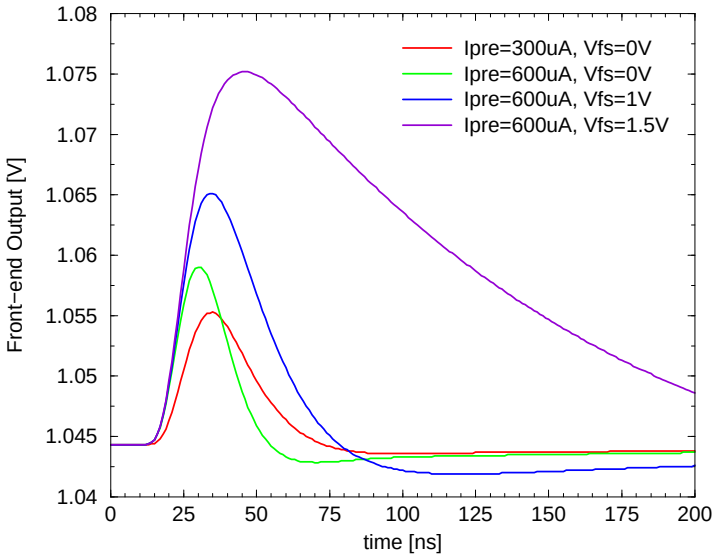


Figure 5: Variation of the front-end pulse shape for different bias settings (Isha = Ibuf = 80 μA, Vfp = 0 V).

sensitivity $A_Q = V_{FEout}/Q_{in} = 38\,mV/22,000\,\mathrm{e}^- = 38\,mV/\mathrm{MIP}$.

The behaviour of the front-end pulse parameters is strongly coupled to the detector load capacitances. Fig. 6 shows the variation of

- peaking time t_p $(0-100\%)$ [upper left plot],
- rise time t_r $(10-90\%)$ [upper right plot],
- peaking voltage V_p [lower left plot] and
- remainder R [lower right plot]

for different detector capacitances and for four different shaper feedback settings *Vfs*.

3.2 Equivalent Noise Charge

The equivalent noise charge (ENC) of a complete *Beetle1.3* readout chip has been measured for different front-end settings. ENC values are given in Table 4 for different shaper feedback settings *Vfs*. Nominal register settings refer to Table 13.

Table 4: Measured equivalent noise charge for different shaper feedback settings *Vfs*.

Vfs [mV]	Equivalent noise charge
0	$\mathrm{ENC} = 547.7\,\mathrm{e}^- + 52.64\,\mathrm{e}^-/\mathrm{pF} \cdot \mathrm{C}_{in}$
100	$\mathrm{ENC} = 539.1\,\mathrm{e}^- + 51.89\,\mathrm{e}^-/\mathrm{pF} \cdot \mathrm{C}_{in}$
400	$\mathrm{ENC} = 542.8\,\mathrm{e}^- + 49.38\,\mathrm{e}^-/\mathrm{pF} \cdot \mathrm{C}_{in}$
1000	$\mathrm{ENC} = 465.1\,\mathrm{e}^- + 45.22\,\mathrm{e}^-/\mathrm{pF} \cdot \mathrm{C}_{in}$

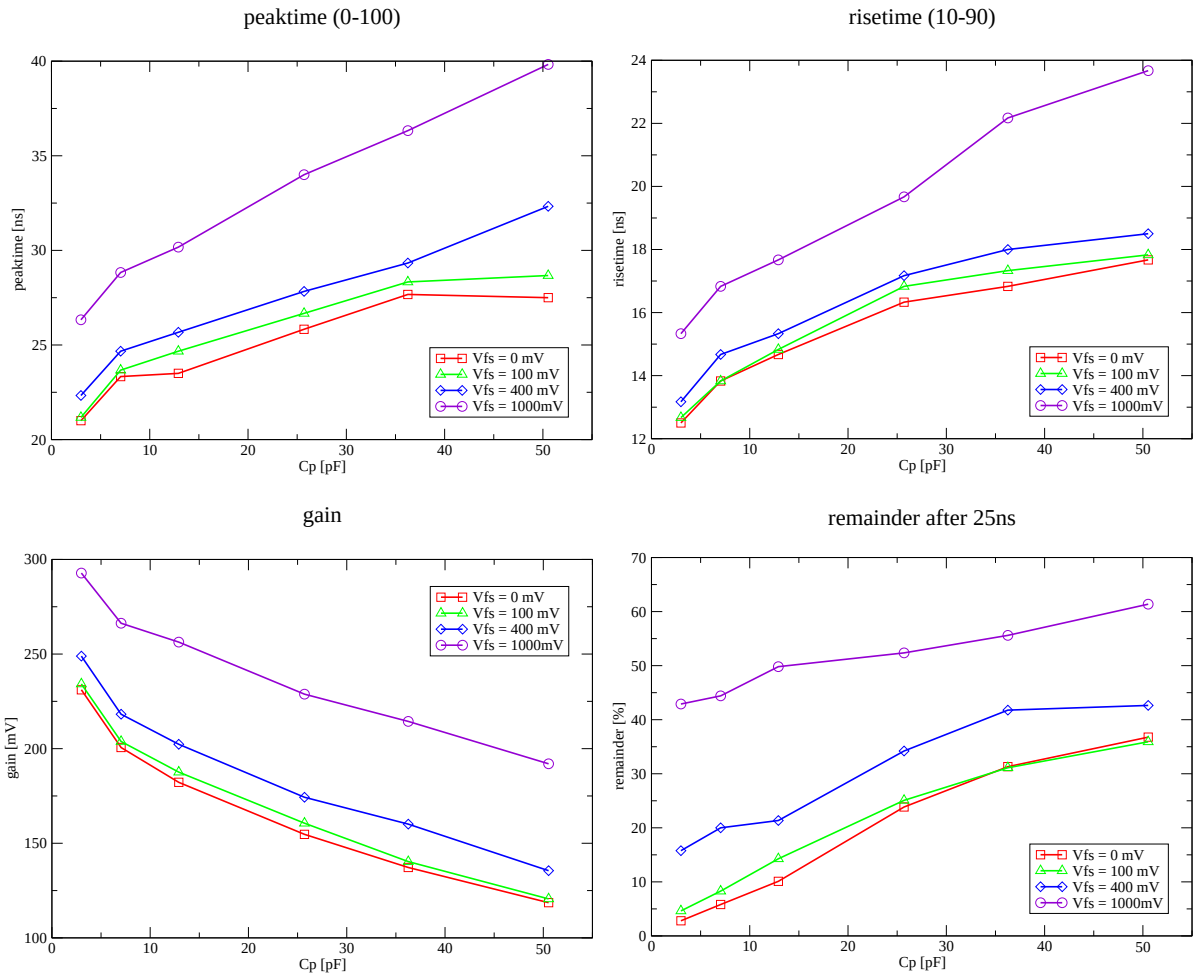


Figure 6: Front-end pulse parameters for different shaper settings *Vfs* and different detector load capacitances

3.3 Test Channel

The *Beetle* chip integrates beside the 128 channels a *test channel* with direct access to the front-end output (`TestOutput`, pad no. 242) as well as the pipeamp output (`PipeampTestOut`, pad no. 218). An input charge can be injected either via the `TestInput` port (pad no. 6) or via the internal test pulse generator (+1 step, cf. 3.6). Additionally, 5 internal voltage nodes of the test channel's front-end are accessible on pads: `Prebias` (pad no. 247), `Prebias1` (pad no. 246), `Shabias` (pad no. 245), `Shabias1` (pad no. 244) and `Bufbias` (pad no. 243). Fig. 7 illustrates the various bias nodes.

3.4 Reset Modes

Two different types of reset exist on *Beetle1.3*.

- *Power-up reset* is activated immediately when the power of the chip is switched on. The reset's time-constant, i.e. the time between "power-on" and the reset becoming inactive, can be adjusted via an external capacitance connected to the `PowerupReset` pad no. 192. For typical capacitance values like C_{ext} =10 nF (100 nF), the time constant τ = 28 ms (280 ms). All *Beetle* registers are reset to 0 and the I^2C-interface is initialised.

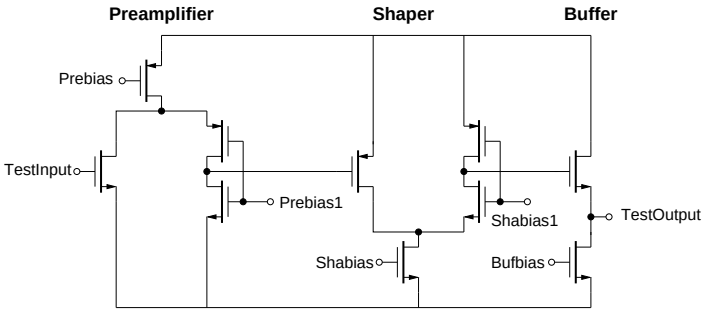


Figure 7: Test channel bias nodes.

- *External reset* follows the `Reset` port (see section A.3). It resets the pipeline write and trigger pointer to column number 0 and initialises the control logic's state machines. The rising edge of `Reset` re-initialises the I^2C-interface. The minimum reset width is 25 ns, i.e. one sampling clock cycle.

3.5 Readout Modes

The readout of the *Beetle* chip is synchronous to the readout clock *Rclk*, which is generated on-chip from the sampling clock *Sclk* (`Clk` port). For operation at LHC, sampling and readout clock have the same frequency. For other applications, the readout clock frequency can be reduced to a fraction of *Sclk* (cf. 4.2).

Beetle1.3 provides three different readout modes[§]:

Analog readout on 4 ports Each port carries 4 header bits plus 32 channels. Data is transmitted synchronous to the rising edge of the readout clock and takes 900 ns.

Binary readout on 2 ports Each port carries 8 header bits plus 64 channels. Data is transmitted synchronous to both edges of *Rclk*. The readout takes 900 ns.

Analog readout on 1 port This is for applications with less demanding readout speed requirements. The readout lasts 3.6 μs.

Fig. 8 shows the assignment of the header bits and analog input channels to the output channels in the different modes. The meaning of the various header bits is given in Table 5.

3.6 Internal Test Pulses

Test pulses can be injected into the preamplifier with an on-chip generator. A step like pattern corresponding to +1 and −1 times a reference signal amplitude is coupled modulo 2 to the 128 channels (Table 6). The amplitude of the reference pulse can be adjusted with the *Itp* bias register (cf. Table 13). A test pulse is triggered via the `Testpulse` port (pad no. 177, 178) and can be enabled per channel by the *TpSelect* register (cf. 4.2). Fig. 9 shows the correlation between the `Testpulse` port and the internal test pulse trigger.

Calibration The relation between *Itp* and the injected charge Q_{in} is given:

- $Q_{in} = 131.2\,e^-/\mu A \cdot I_{tp}$

or

- $Q_{in} = 1025\,e^-/[\text{regbit}] \cdot I_{tp}\,[regbit]$

[§]The specification of the readout time assumes *Rclk* = *Sclk* = 40 MHz.

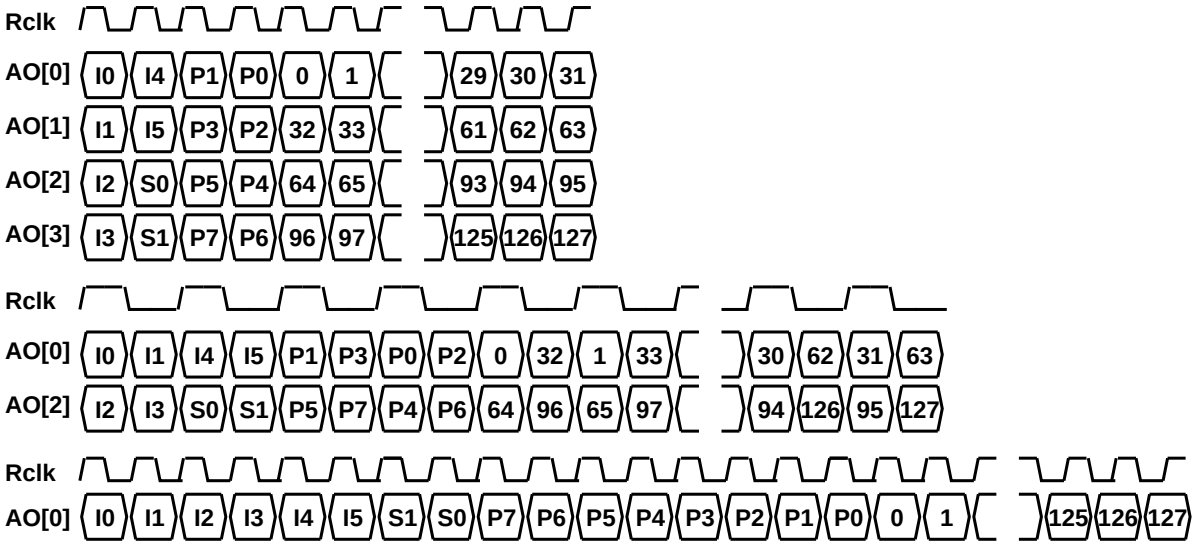


Figure 8: *Beetle1.3* readout data formats. From top to bottom: Analog readout mode: 32 analog channels are multiplexed onto 4 ports with up to 40 MHz. Binary readout mode: 64 binary channels are multiplexed onto 2 ports with up to 80 MHz. Readout mode for less demanding readout speed requirements: 128 analog channels are multiplexed onto 1 port with up to 40 MHz.

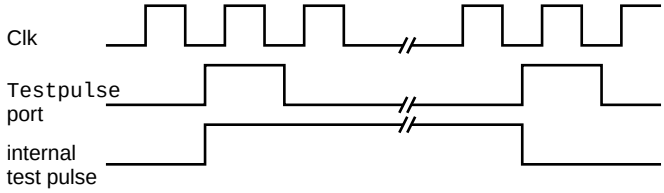


Figure 9: Test pulse triggering.

3.7 Comparator Operation

The comparator circuit consists of an integrator, a threshold generator and a discriminator. The integrator extracts the DC-offset of the shaped pulse with a variable time constant between 1 and 20 μs, which can be adjusted via the *Vrc* register (cf. Table 13). The DC-offset varies from channel to channel and is added to the threshold voltage. The threshold level is adjustable per channel with a resolution of 5 bits.

3.7.1 Comparator Configuration

The comparator is configured via the register *CompControl* (see Table 13 and Table 11). *PipelineMode* defines the mode of operation of the comparator. *PipelineMode* = 0 selects the analog mode, in which the output of the front-end amplifier is transferred to the pipeline. In binary mode (*PipelineMode* = 1) the comparator output is fed into the pipeline. *CompDisable* = 1 turns off the comparator's bias current. *CompPolarity* selects between an inverting (0) or non-inverting (1) comparator operation. *CompMode* switches between two different kinds of output signal. With *CompMode* = 0 the output is active as long as the comparator input signal is above the threshold level. With *CompMode* = 1 the output is only one CompClk cycle active, independent of the time, that the input signal is above the threshold.

Table 5: Header bits in *Beetle1.3*'s data burst.

Bit		Description
I0	LeadingBit	always active (= 1)
I1	ParPCN	(even) parity of pipeline column number (PCN)
I2	ActiveEDC	1 indicates active error detection and correction (EDC) logic
I3	ParCompChTh	(even) parity of register *CompChTh* (reg. no. 20, cf. Table 13)
I4	ParCompMask	(even) parity of register *CompMask* (reg. no. 21, cf. Table 13)
I5	ParTpSelect	(even) parity of register *TpSelect* (reg. no. 22, cf. Table 13)
S0		LSB of register *SEUcounter* (reg. no. 23, cf. Table 13)
S1		bit 1 of register *SEUcounter* (reg. no. 23, cf. Table 13)
P0		LSB of pipeline column number
P1		bit 1 of pipeline column number
P2		bit 2 of pipeline column number
P3		bit 3 of pipeline column number
P4		bit 4 of pipeline column number
P5		bit 5 of pipeline column number
P6		bit 6 of pipeline column number
P7		MSB of pipeline column number

Table 6: Mapping of test pulse amplitudes to analog channels.

Channel no.	0	1	2	3	...	124	125	126	127
Test pulse step height	+1	−1	+1	−1	...	+1	−1	+1	−1

3.7.2 Threshold Adjustment

The threshold level is generated from two programmable currents. *Ithmain* (register address 8) determines the global threshold, which is common to all channels. *Ithdelta* (register address 7) defines an additional delta threshold.

The comparator threshold register (*CompChTh*, address 20) selects the number of delta thresholds which are being added to the global threshold. This register is operated as a shift register. The bits `CompChTh[4:0]` are being assigned to channel *k*. To define the delta threshold of all channels, the *CompChTh* register has to be programmed 128 times consecutively. A shift mechanism provides the bits to the channels in the order Ch[0], Ch[1], Ch[2],..., Ch[126], Ch[127].

3.7.3 Comparator Channel Mapping

The comparator outputs are LVDS drivers. Each driver sends data of two combined comparator groups, the first group of ORed channels during the high phase of `CompClock`, the second during the low phase. The mapping of the channels to the comparator outputs is shown in Table 7.

3.8 Timing Specifications

Reset, Trigger, Testpulse The timing relation between *Reset* and *Trigger* in order to trigger on pipeline column number n can be depicted from Fig. 10, whereas $n = k$ modulo 187. k must be equal or greater than 1, *Latency* refers to the content of the Latency register (no. 16). *Reset* and *Trigger* are sampled internally to the negative edge of *Clk*.

Fig. 11 depicts the timing relation between *Testpulse* and *Trigger*. *Latency* refers again to the content of the Latency register.

Table 7: Mapping of analog input channels to comparator output channels on *Beetle1.3*.

Output port	High phase of `CompClock`	Low phase of `CompClock`
CompOut[15]	Ch[127]∨Ch[126]∨Ch[125]∨Ch[124]	Ch[123]∨Ch[122]∨Ch[121]∨Ch[120]
CompOut[14]	Ch[119]∨Ch[118]∨Ch[117]∨Ch[116]	Ch[115]∨Ch[114]∨Ch[113]∨Ch[112]
CompOut[13]	Ch[111]∨Ch[110]∨Ch[109]∨Ch[108]	Ch[107]∨Ch[106]∨Ch[105]∨Ch[104]
CompOut[12]	Ch[103]∨Ch[102]∨Ch[101]∨Ch[100]	Ch[99]∨Ch[98]∨Ch[97]∨Ch[96]
CompOut[11]	Ch[95]∨Ch[94]∨Ch[93]∨Ch[92]	Ch[91]∨Ch[90]∨Ch[89]∨Ch[88]
CompOut[10]	Ch[87]∨Ch[86]∨Ch[85]∨Ch[84]	Ch[83]∨Ch[82]∨Ch[81]∨Ch[80]
CompOut[9]	Ch[79]∨Ch[78]∨Ch[77]∨Ch[76]	Ch[75]∨Ch[74]∨Ch[73]∨Ch[72]
CompOut[8]	Ch[71]∨Ch[70]∨Ch[69]∨Ch[68]	Ch[67]∨Ch[66]∨Ch[65]∨Ch[64]
CompOut[7]	Ch[63]∨Ch[62]∨Ch[61]∨Ch[60]	Ch[59]∨Ch[58]∨Ch[57]∨Ch[56]
CompOut[6]	Ch[55]∨Ch[54]∨Ch[53]∨Ch[52]	Ch[51]∨Ch[50]∨Ch[49]∨Ch[48]
CompOut[5]	Ch[47]∨Ch[46]∨Ch[45]∨Ch[44]	Ch[43]∨Ch[42]∨Ch[41]∨Ch[40]
CompOut[4]	Ch[39]∨Ch[38]∨Ch[37]∨Ch[36]	Ch[35]∨Ch[34]∨Ch[33]∨Ch[32]
CompOut[3]	Ch[31]∨Ch[30]∨Ch[29]∨Ch[28]	Ch[27]∨Ch[26]∨Ch[25]∨Ch[24]
CompOut[2]	Ch[23]∨Ch[22]∨Ch[21]∨Ch[20]	Ch[19]∨Ch[18]∨Ch[17]∨Ch[16]
CompOut[1]	Ch[15]∨Ch[14]∨Ch[13]∨Ch[12]	Ch[11]∨Ch[10]∨Ch[9]∨Ch[8]
CompOut[0]	Ch[7]∨Ch[6]∨Ch[5]∨Ch[4]	Ch[3]∨Ch[2]∨Ch[1]∨Ch[0]

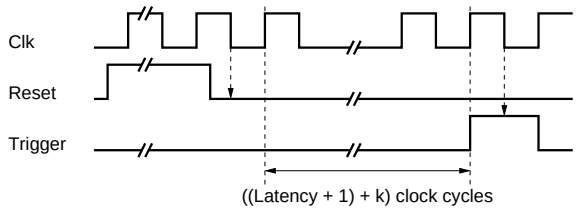


Figure 10: Timing relation between *Reset* and *Trigger* in order to trigger on a defined pipeline column number.

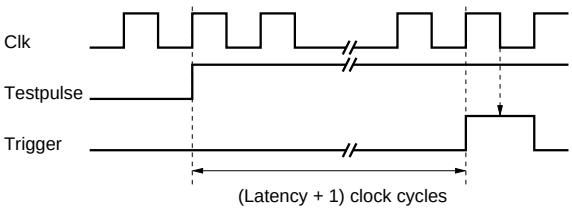


Figure 11: Timing relation between *Testpulse* and *Trigger*. *Latency* refers to the content of the latency register.

Readout Timing The *Beetle* chip has two different possible readout timings called *non-consecutive* and *consecutive* readout. A non-consecutive readout starts after a trigger occurs during a non-readout. If the *Beetle* receives a second trigger before a last readout is completed, the next readout is send as a consecutive readout. Fig. 13 depicts the timing condition where the next readout starts as a consecutive readout (upper scheme) respectively the first condition where the next readout starts as a non-consecutive readout (lower scheme).

Fig. 12 describe the readout timing of *Trigger*, *DataValid* and *AnalogOut* of the analog readout mode on 4 ports. The upper plot shows a single readout burst (non-consecutive readout), the lower the case of a consecutive readout.

3.9 Diagnostic Signals

The *Beetle* chip provides several digital signals for monitoring or diagnostics purposes which are explained briefly in Table 8.

`WriteMon` and `TrigMon` allow to check the physical latency of the chip. They are pulses with a width of one sampling clock cycle and a period of 187 cycles. Their relative distance is (*Latency + 1*) clock cycles.

Table 8: Digital signals for monitoring or diagnostics purposes. All signals are active-high.

signal name	pad no.	description
`DataValid`	181, 182	indicates presence of valid data on the `AnalogOut` ports; see Fig. 12 for timing specifications
`FifoFull`	166	indicates full derandomising trigger buffer; with 15 occupied FIFO entries, the next trigger activates `FifoFull`
`TrigMon`	171	indicates if pipeline trigger pointer passes column number 0
`WriteMon`	172	indicates if pipeline write pointer passes column number 0

3.10 Daisy Chain

The daisy chain allows several chips to share one, two or four output lines. It consists of two signal paths, a *token* and a *return token* path. They are built up by connecting the `RoTokenOut` (`RoReTokenIn`) pad of one chip with the `RoTokenIn` (`RoReTokenOut`) of the neighbouring chip (see Fig. 14). The chip position in the chain has to be configured in the *ROCtrl* register (bits 3 and 4). A chip can be the first (`DaisyFirst` = 1), an intermediate or the last (`DaisyLast` = 1) in the daisy chain.

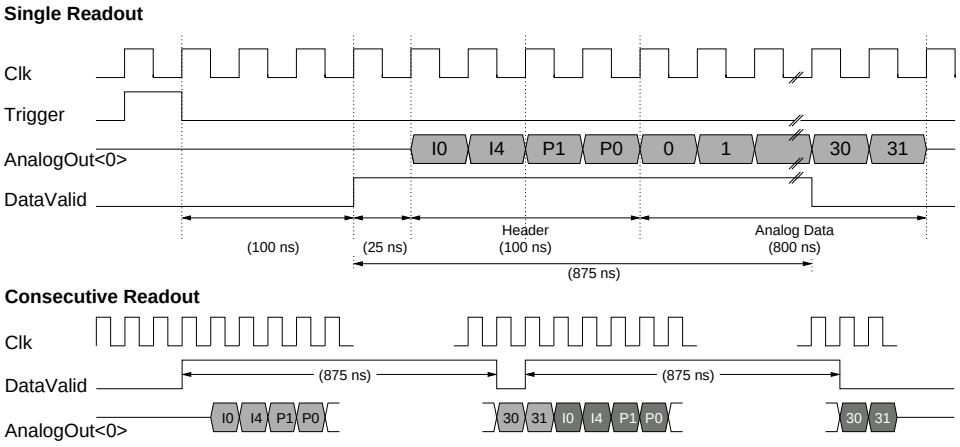


Figure 12: Readout timing schemes of the analog readout mode on 4 ports. Only channel 0 is depicted. The upper plot shows a single readout burst, the lower the case of consecutive readout.

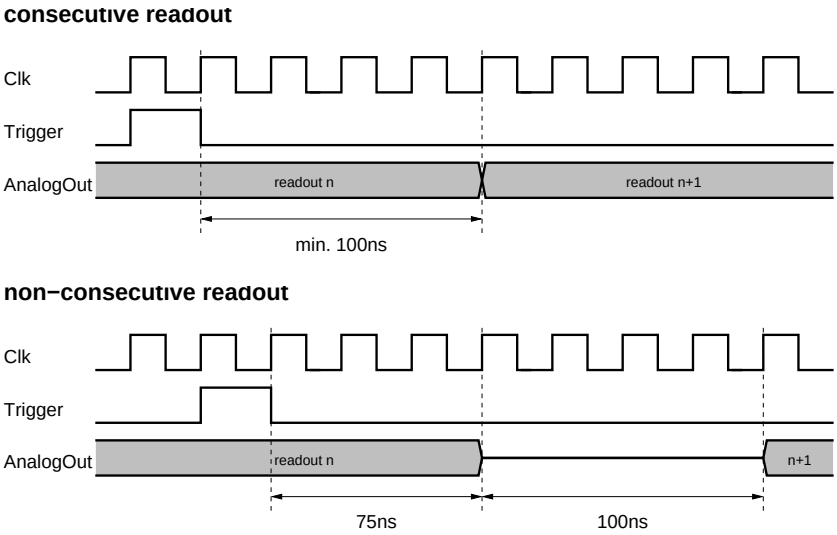


Figure 13: Non-consecutive and consecutive readout condition. The upper timing plot shows the last possible timing condition of a trigger where the next readout starts as a consecutive readout. The lower plot shows the first condition where the next readout starts as a non-consecutive readout.

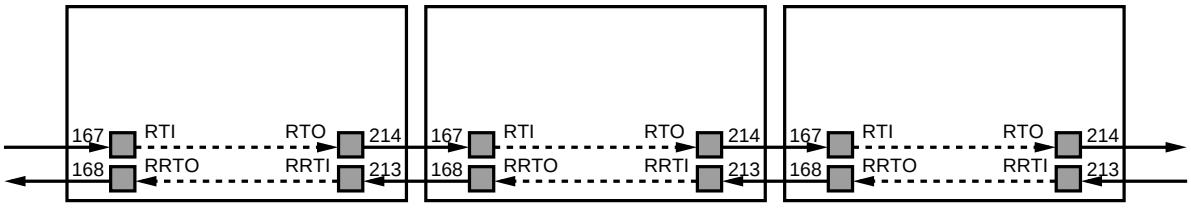


Figure 14: Daisy chain composition. The figures indicate the pad reference numbers (RTI = RoTokenIn, RRTO = RoReTokenOut, RTO = RoTokenOut, RRTI = RoReTokenIn).

4 Slow Control

4.1 I^{2}C-Interface

The chip's slow control interface is a standard mode I^{2}C-slave device featuring a transfer rate of 100 kbit/s. The chip address, necessary to access a single device via the I^{2}C-bus, is 7 bits wide and assigned via the address pads `I2CAddr[6:0]` (cf. section A.3). The *Beetle* chip responds to addresses in the range $8 - 119$. The addresses `0000XXX` and `1111XXX` are reserved in the I^{2}C-standard for other purposes [7].

The internal registers are being accessed via a*pointer register*. This contains the address of the register to be written or read first. The pointer is internally incremented by 1 after each transferred data frame. In this way registers with adjacent addresses can be accessed consecutively. The pointer register itself remains unchanged, i.e. a new transfer will start at the same pointer position. Fig. 15 explains the transfer sequences in write and read mode. Data is always transferred with the most significant bit (MSB) first. In write mode the chip address is transmitted after initialising the transfer, followed by the pointer byte and the data. After the transmission of one data frame, the pointer addresses the successive register because of its auto-incrementing function. The registers with addresses $20 - 23$ have an exceptional status. The registers $20 - 22$ are implemented as 128-bit shift-registers (cf. 4.2), register 23 is the output of the SEU counter. A write access to this register resets it to 0. Hence, the auto-incrementing of the address pointer is only performed for addresses ≤ 19. To access the addresses $20 - 23$ the corresponding register has to be addressed directly.

The transfer of the pointer byte is obligatory in write mode. In read mode there are two versions:

- Preset pointer
  After initialising the transfer and sending the chip address data is immediately read out. The pointer has been set in a previous transfer.
- Pointer set followed by immediate read-out
  After initialising the transfer and sending the chip address the pointer byte is transferred. The I^{2}C-bus is re-initialised, the chip address is sent and data is read out.

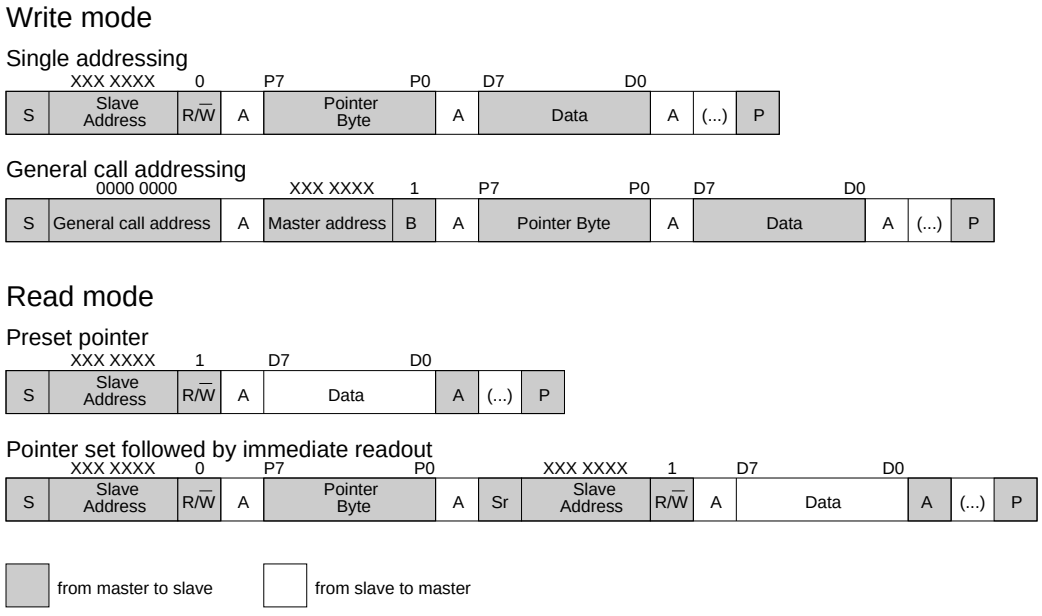


Figure 15: I^{2}C-bus write and read sequences for accessing registers on the *Beetle1.3*.

Commercially available I^2C-devices usually operate at 3.3 V or 5 V. With version 1.3 or higher, external devices can be connected directly to the *Beetle* I^2C-interface.

4.2 Bias and Configuration Registers

Beetle1.3 contains 24 8-bit registers with the addresses $0-23$. Table 13 lists all registers with physical range, resolution and nominal setting. Registers $0-15$ are bias registers for the analog stages.

Pipeamp reset potential: *Vd* Register 11 determines the potential to which the pipeamp is reset. This voltage should correspond to the DC output level of the front-end and is is therefore depending on *Isha* and *Ibuf* (cf. 3.1). Table 9 gives typical values of *Vd* for *Isha*= 80 μA and various *Ibuf* settings.

Table 9: Corresponding bias settings of *Ibuf* and *Vd* for *Isha*= 80 μA.

Ibuf		*Vd*	
Value	Reg. content	Value	Reg. content
39 μA	0x05	1.314 mV	0x86
47 μA	0x06	1.304 mV	0x85
55 μA	0x07	1.294 mV	0x84
63 μA	0x08	1.284 mV	0x83
71 μA	0x09	1.284 mV	0x83
78 μA	0x0A	1.275 mV	0x82
86 μA	0x0B	1.275 mV	0x82
94 μA	0x0C	1.275 mV	0x82
102 μA	0x0D	1.265 mV	0x81
110 μA	0x0E	1.265 mV	0x81
118 μA	0x0F	1.265 mV	0x81
125 μA	0x10	1.255 mV	0x80
251 μA	0x20	1.216 mV	0x7C

Pipeamp reference potential: *Vdcl* Register 12 adjusts the potential of the non-inverting input of the pipeamp.

Latency Register 16 defines the latency which has to be ≥ 10 and ≤ 160 for reliable chip operation.
$\rightsquigarrow$ A change of the latency register will only have an effect after applying a reset.

Rclk divider: *RclkDiv* Register 18 defines the ratio between the readout clock `Rclk` and the sampling clock `Sclk`. The ratio $\nu_{\texttt{Rclk}}/\nu_{\texttt{Sclk}}$ is defined as

$$\frac{\nu_{\texttt{Rclk}}}{\nu_{\texttt{Sclk}}} = \begin{cases} 1 & \text{for } \mathit{RclkDiv} = 0 \\ \frac{1}{2 \cdot \mathit{RclkDiv}} & \text{for } \mathit{RclkDiv} > 0 \end{cases} \quad (1)$$

and allows `Rclk` frequencies from 40 MHz down to $\approx$ 78 kHz. *RclkDiv* = 0 means, that `Sclk` and `Rclk` have the same frequency.
$\rightsquigarrow$ A change of the *RclkDiv* register requires a succeeding reset for proper chip operation.

Mode of operation: *ROCtrl*, *CompCtrl* The registers 17 and 19 select the chip's mode of operation (readout mode, daisy chain configuration) and define the comparator configuration. Tables 10 and 11 show the detailed bit assignment of the registers *ROControl* and *CompControl*. Note, that the three

ModeSelect bits (*BinRO2*, *AnaRO1* and *AnaRO4*) are exclusive, i.e. only one bit is allowed to be set. RevId2 − 0 of *CompControl* are read-only bits and represents the *Beetle* version number. In case of *Beetle1.3* all bits are set to 1.

⇝ A change of the *ROCtrl* register bit 4 − 0 requires a succeeding reset for proper chip operation.

Table 10: Bit assignment of the configuration register *ROCtrl*.

Bit	Function	Description
0	BinRO2	binary readout on 2 ports
1	AnaRO1	analog readout on 1 port
2	AnaRO4	analog readout on 4 ports
3	DaisyFirst	first chip in daisy chain
4	DaisyLast	last chip in daisy chain
5	BinaryHeader	readout header levels of current driver
6	*not used*	—
7	ProbeEnable	enables probe pads `ProbeVrefBE` (pad no. 216)

All switches are active-high. 1 enables the switch, 0 disables it.

Table 11: Bit assignment of the configuration register *CompCtrl*.

Bit	Function	Description
0	DisableCompLVDS	0: enable comparator LVDS output ports 1: disable comparator LVDS output ports
1	CompPolarity	0: inverting 1: non-inverting
2	PipelineMode	1: binary readout 0: analog readout
3	CompDisable	0: enable comparator 1: disable comparator
4	CompMode	0: track mode 1: pulse mode
5	RevId2	1: *read-only bit*: rev. id no. 2
6	RevId1	1: *read-only bit*: rev. id no. 1
7	RevId1	1: *read-only bit*: rev. id no. 0

Shift registers Registers 20 − 22 (*CompChTh, CompMask, TpSelect*) are operated as shift-registers: *CompMask* and *TpSelect* form a 128-bit register each, segmented in 16 8-bit registers, *CompChTh* establishes a 1024 (= 128 × 8) bit register, whereas only 5 of the 8 bits per frame are assigned (cf. section 3.7.2). A consecutive write-access to the corresponding register address shifts the data in 8-bit frames starting from the largest channel number (see Table 12). A read access to such a register returns the bits corresponding to channels 7 − 0 in case of *CompMask* and *TpSelect* and 0 in case of *CompChTh*. This allows a verification of the shifted data.

Table 12: Channel sequence for write and read access to the shift registers.

	Write access	Read access
CompMask	Ch[127:120], Ch[119:112], ...	Ch[7:0]
TpSelect	Ch[127:120], Ch[119:112], ...	Ch[7:0]
CompChTh	Ch[127], Ch[126], ...	Ch[0]

SEU counter Register 23 is the output of the SEU counter (cf. 4.3). A write access to this register resets the content to 0. Note, that the two LSB of the register *SEUcounts* are transmitted in the header (`S[1:0]`) of the analog output stream (cf. 3.5).

Table 13: Bias and configuration registers of *Beetle1.3*.

Reg. no.	Reg. Name	Class	Range	Res.	Nominal Setting		Description
					Value	Reg. content	
0	*Itp*	I	$0-2\,\mathrm{mA}$	$8\,\mu\mathrm{A}$	$0\,\mu\mathrm{A}$	`0x00`	test pulse bias current
1	*Ipre*	I	$0-2\,\mathrm{mA}$	$8\,\mu\mathrm{A}$	$600\,\mu\mathrm{A}$	`0x4C`	preamplifier bias current
2	*Isha*	I	$0-2\,\mathrm{mA}$	$8\,\mu\mathrm{A}$	$80\,\mu\mathrm{A}$	`0x0A`	shaper bias current
3	*Ibuf*	I	$0-2\,\mathrm{mA}$	$8\,\mu\mathrm{A}$	$80\,\mu\mathrm{A}$	`0x0A`	front-end buffer bias current
4	*Vfp*	V	$0-2.5\,\mathrm{V}$	$9.8\,\mathrm{mV}$	$0\,\mathrm{V}$	`0x00`	preamplifier feedback voltage
5	*Vfs*	V	$0-2.5\,\mathrm{V}$	$9.8\,\mathrm{mV}$	$0\,\mathrm{V}$	`0x00`	shaper feedback voltage
6	*Icomp*	I	$0-2\,\mathrm{mA}$	$8\,\mu\mathrm{A}$	$40\,\mu\mathrm{A}$	`0x05`	comparator bias current
7	*Ithdelta*	I	$0-2\,\mathrm{mA}$	$8\,\mu\mathrm{A}$	—	—	current defining incremental comparator threshold
8	*Ithmain*	I	$0-2\,\mathrm{mA}$	$8\,\mu\mathrm{A}$	—	—	current defining common comparator threshold
9	*Vrc*	V	$0-1.25\,\mathrm{V}$	$4.9\,\mathrm{mV}$	$0\,\mathrm{V}$	`0x00`	comparator RC time constant
10	*Ipipe*	I	$0-2\,\mathrm{mA}$	$8\,\mu\mathrm{A}$	$100\,\mu\mathrm{A}$	`0x0D`	pipeamp bias current
11	*Vd*	V	$0-2.5\,\mathrm{V}$	$9.8\,\mathrm{mV}$	$1.275\,\mathrm{V}$	`0x82`	pipeamp reset potential
12	*Vdcl*	V	$0-2.5\,\mathrm{V}$	$9.8\,\mathrm{mV}$	$1\,\mathrm{V}$	`0x66`	pipeamp reference voltage
13	*Ivoltbuf*	I	$0-2\,\mathrm{mA}$	$8\,\mu\mathrm{A}$	$200\,\mu\mathrm{A}$	`0x1A`	pipeamp buffer bias current
14	*Isf*	I	$0-2\,\mathrm{mA}$	$8\,\mu\mathrm{A}$	$200\,\mu\mathrm{A}$	`0x1A`	multiplexer buffer bias current
15	*Icurrbuf*	I	$0-2\,\mathrm{mA}$	$8\,\mu\mathrm{A}$	$800\,\mu\mathrm{A}$	`0x66`	output buffer bias current
16	*Latency*	Dig.	$10-160$	—	160	`0xA0`	trigger latency
17	*ROCtrl*	Dig.	—	—	cf. Table 10		readout control
18	*RclkDiv*	Dig.	$0-255$[¶]	—	0	`0x00`	ratio between `Rclk` and `Sclk`
19	*CompCtrl*	Dig.	—	—	cf. Table 11		comparator control
20	*CompChTh*	Dig.	$0-31$	—	—	—	comparator channel threshold shift register implementation
21	*CompMask*	Dig.	—	—	0	`0x00`	comparator mask shift register implementation
22	*TpSelect*	Dig.	—	—	0	`0x00`	testpulse selection shift register implementation
23	*SEUcounts*	Dig.	$0-255$	—	—	—	sum of single event upsets

4.3 Single Event Upset Robustness

Beetle1.3 continuously uses triple-redundant logic in order to assure the robustness against Single Event Upset (SEU), i.e. the change of the state of a memory device induced by a single particle. A logic bit is represented by the majority of the outputs of three flip-flops. The flip-flops on *Beetle1.3* can be categorised into two groups:

Clocked flip-flops They are used in the control logic which operates with the sampling clock frequency of 40 MHz in case of the *Fast Control* and the I^2C-clock of 100 kHz in case of the *Slow Control*.

[¶] see section 6

Static flip-flops They form the bias and configuration registers. These flip-flops use triple-redundant majority voting in combination with a self-triggered correction mechanism. A single SEU per bit will be corrected.

An 8-bit counter is integrated in *Beetle1.3* to indicate the number of single event upsets in the bias and configuration registers. All registers, including the shift-registers *CompChTh*, *CompMask* and *TpSelect*, can increment the SEU counter. The bits used in the logic control circuits (clocked flip-flops) are *not* taken into account. The counter output is readable via the I^2C-bus (cf. 4.2). The two least significant bits are additionally transferred in the header of the analog output stream (Fig. 8, Table 5). This allows a fast monitoring of SEUs during readout. An I^2C-write access to the counter register resets it.

5 How to get the *Beetle* chip working

This section describes important steps to get the *Beetle* chip working. Some may be trivial, but ignoring them can cause lengthy trouble in running the chip.

Power and Blocking

- Power the chip:
  - for analog operation:
    connect to Vdd: pad no.: 3, 4, 135, 136, 141, 169, 205 – 207, 240
    connect to Gnd: pad no.: 1, 2, 5, 137, 138, 140, 170, 202 – 204, 241
  - for binary operation connect *additionally* to the above listed pads:
    to Vdd: pad no.: 142, 164, 221, 239
    to Gnd: pad no.: 143, 165, 220, 238
- Block the following pads with $\mathcal{O}(100\,\mathrm{nF})$ to ground: `Icurrbuf` (pad no. 208), `Isf` (pad no. 209), `Ipipe` (pad no. 210), `Vdclbuf` (pad no. 211), `Vdbuf` (pad no. 212).

Minimum number of pads to be bonded

The following list specifies the minimum number of *input ports* to be bonded for proper chip operation in addition to power and blocking pads:

- `Trigger` (pad no. 173, 174),
- `Clock` (pad no. 175, 176),
- `Reset` (pad no. 179, 180),
- `SCL, SDA` (pad no. 190, 191).

Beside the analog output ports `AnalogOut<i>` (pad no. 194 – 201) or the comparator output ports `CompOut<i>` (pad no. 149 – 164, 222 – 237), it is recommended to bond the *digital output pads* listed in 3.9.

LVDS ports

Define the levels of all LVDS input ports, e.g. *Clock*, *Trigger*, *Reset*, *Testpulse*, i.e. do not leave any input pads floating.

Power-up reset

Connect the `PowerupReset` port (pad no. 192) with $\mathcal{O}(100\,\mathrm{nF})$ to ground.

I^2C-bus

- Define the chip ID via the pads `I2CAddr[6:0]` for individual chip access, or use general call mode. The chip responds to addresses in the range 8 – 119.
- Assure, that different chips sharing one I^2C-bus line have unique addresses.
- Assure, that the `Reset` port has a defined logic level and does not change while programming the chip via I^2C-bus.

Fast Control

- Define the chip as *DaisyFirst* as well as *DaisyLast* (*ROCtrl* register is `XXX11XXX`).
- A change of the content of the *Latency* register (register ID 16) is taken over by the logic circuitry only after applying an external reset via the `Reset` port. To check the *physical* latency, determine the time distance of the `WriteMon` (pad no. 171) and `TrigMon` (pad no. 170) signals, which is *Latency + 1*.

  $\rightsquigarrow$ *Latency* has to be in the range $10 - 160$ for proper chip operation.

6 Known Problems and Limitations

Problem Parity of pipeline column number

In case of operating the *Beetle* in readout mode *Analog readout on 4 ports* (cf. 3.5) and *Rclk divider* ratio of 1 (cf. 4.2, $RclDiv = 0$), the parity bit in the header of a consecutive readout is wrong encoded.

Limitation Daisy chain

The readout of a second chip in a daisy chain starts to early.

Limitation *Rclk divider* ratio unequal 1

The last channel of each analog readout port is only valid for one `Sclk` cycle. For the remaining readout time the value is undefined.

A Pad Description

A reference number has been assigned to each pad. The numbering starts in the upper left corner of the die (with the analog input pads left) and runs counterclockwise (cf. Fig. 16). The following tables summarise the signals and explain them. The pad coordinates refer to the lower left corner of the pad opening, which is $120\,\mu m \times 95\,\mu m$ in case of the front pads and $95\,\mu m \times 95\,\mu m$ for all others with exception of the backside power pads. Their enlarged pad windows are listed in section A.3. The origin of the coordinate system is defined by the lower left chip corner $(0, 0)$. The dimensions of the chip die are $5{,}400\,\mu m \times 6{,}100\,\mu m$[‖]. The analog input pads have a pitch of $40.24\,\mu$m, all others $115\,\mu$m.

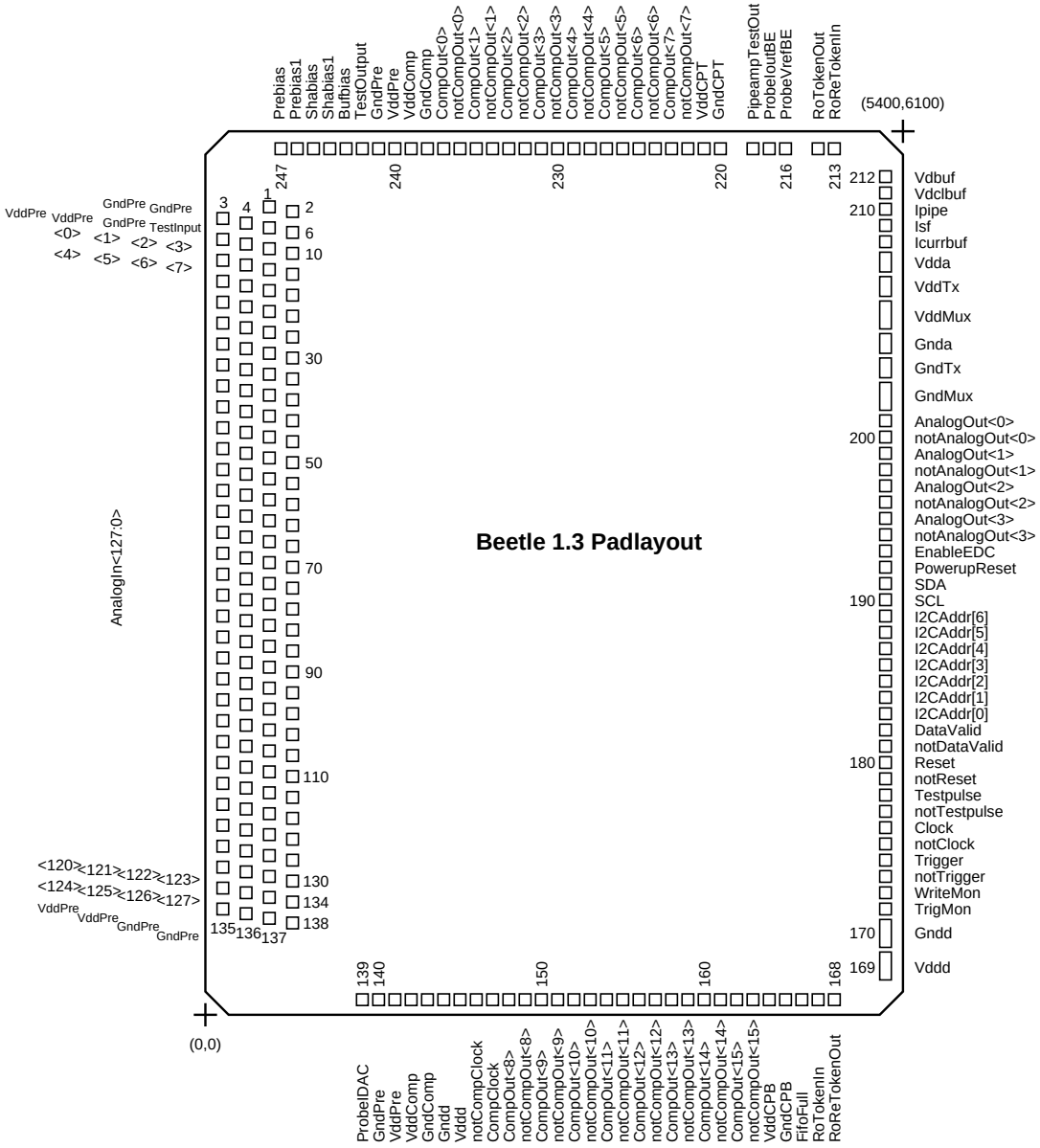


Figure 16: Pad layout of *Beetle1.3*. The die size is $(5.4 \times 6.1)\,\mathrm{mm}^2$.

[‖]Note, that this are the dimensions of the chip's scribe line, i.e. not including cutting margins. They could add some $100\,\mu$m to the chip dimensions.

A.1 Front Pads

Ref. no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
1	GndPre	335.00	5876.54	power input	negative preamplifier supply (detector gnd)
2	GndPre	490.00	5836.30	power input	negative preamplifier supply (detector gnd)
3	VddPre	25.00	5796.06	power input	positive preamplifier supply
4	VddPre	180.00	5755.82	power input	positive preamplifier supply
5	GndPre	335.00	5715.58	power input	negative preamplifier supply (detector gnd)
6	TestInput	490.00	5675.34	input	input of testchannel
7	AnalogIn<0>	25.00	5635.10	input	input of channel 0
8	AnalogIn<1>	180.00	5594.86	input	input of channel 1
9	AnalogIn<2>	335.00	5554.62	input	input of channel 2
10	AnalogIn<3>	490.00	5514.38	input	input of channel 3
11	AnalogIn<4>	25.00	5474.14	input	input of channel 4
12	AnalogIn<5>	180.00	5433.90	input	input of channel 5
13	AnalogIn<6>	335.00	5393.66	input	input of channel 6
14	AnalogIn<7>	490.00	5353.42	input	input of channel 7
15	AnalogIn<8>	25.00	5313.18	input	input of channel 8
16	AnalogIn<9>	180.00	5272.94	input	input of channel 9
17	AnalogIn<10>	335.00	5232.70	input	input of channel 10
18	AnalogIn<11>	490.00	5192.46	input	input of channel 11
19	AnalogIn<12>	25.00	5152.22	input	input of channel 12
20	AnalogIn<13>	180.00	5111.98	input	input of channel 13
21	AnalogIn<14>	335.00	5071.74	input	input of channel 14
22	AnalogIn<15>	490.00	5031.50	input	input of channel 15
23	AnalogIn<16>	25.00	4991.26	input	input of channel 16
24	AnalogIn<17>	180.00	4951.02	input	input of channel 17
25	AnalogIn<18>	335.00	4910.78	input	input of channel 18
26	AnalogIn<19>	490.00	4870.54	input	input of channel 19
27	AnalogIn<20>	25.00	4830.30	input	input of channel 20
28	AnalogIn<21>	180.00	4790.06	input	input of channel 21
29	AnalogIn<22>	335.00	4749.82	input	input of channel 22
30	AnalogIn<23>	490.00	4709.58	input	input of channel 23
31	AnalogIn<24>	25.00	4669.34	input	input of channel 24
32	AnalogIn<25>	180.00	4629.10	input	input of channel 25
33	AnalogIn<26>	335.00	4588.86	input	input of channel 26
34	AnalogIn<27>	490.00	4548.62	input	input of channel 27
35	AnalogIn<28>	25.00	4508.38	input	input of channel 28
36	AnalogIn<29>	180.00	4468.14	input	input of channel 29
37	AnalogIn<30>	335.00	4427.90	input	input of channel 30
38	AnalogIn<31>	490.00	4387.66	input	input of channel 31
39	AnalogIn<32>	25.00	4347.42	input	input of channel 32
40	AnalogIn<33>	180.00	4307.18	input	input of channel 33
41	AnalogIn<34>	335.00	4266.94	input	input of channel 34
42	AnalogIn<35>	490.00	4226.70	input	input of channel 35
43	AnalogIn<36>	25.00	4186.46	input	input of channel 36
44	AnalogIn<37>	180.00	4146.22	input	input of channel 37

Ref. no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
45	AnalogIn<38>	335.00	4105.98	input	input of channel 38
46	AnalogIn<39>	490.00	4065.74	input	input of channel 39
47	AnalogIn<40>	25.00	4025.50	input	input of channel 40
48	AnalogIn<41>	180.00	3985.26	input	input of channel 41
49	AnalogIn<42>	335.00	3945.02	input	input of channel 42
50	AnalogIn<43>	490.00	3904.78	input	input of channel 43
51	AnalogIn<44>	25.00	3864.54	input	input of channel 44
52	AnalogIn<45>	180.00	3824.30	input	input of channel 45
53	AnalogIn<46>	335.00	3784.06	input	input of channel 46
54	AnalogIn<47>	490.00	3743.82	input	input of channel 47
55	AnalogIn<48>	25.00	3703.58	input	input of channel 48
56	AnalogIn<49>	180.00	3663.34	input	input of channel 49
57	AnalogIn<50>	335.00	3623.10	input	input of channel 50
58	AnalogIn<51>	490.00	3582.86	input	input of channel 51
59	AnalogIn<52>	25.00	3542.62	input	input of channel 52
60	AnalogIn<53>	180.00	3502.38	input	input of channel 53
61	AnalogIn<54>	335.00	3462.14	input	input of channel 54
62	AnalogIn<55>	490.00	3421.90	input	input of channel 55
63	AnalogIn<56>	25.00	3381.66	input	input of channel 56
64	AnalogIn<57>	180.00	3341.42	input	input of channel 57
65	AnalogIn<58>	335.00	3301.18	input	input of channel 58
66	AnalogIn<59>	490.00	3260.94	input	input of channel 59
67	AnalogIn<60>	25.00	3220.70	input	input of channel 60
68	AnalogIn<61>	180.00	3180.46	input	input of channel 61
69	AnalogIn<62>	335.00	3140.22	input	input of channel 62
70	AnalogIn<63>	490.00	3099.98	input	input of channel 63
71	AnalogIn<64>	25.00	3059.74	input	input of channel 64
72	AnalogIn<65>	180.00	3019.50	input	input of channel 65
73	AnalogIn<66>	335.00	2979.26	input	input of channel 66
74	AnalogIn<67>	490.00	2939.02	input	input of channel 67
75	AnalogIn<68>	25.00	2898.78	input	input of channel 68
76	AnalogIn<69>	180.00	2858.54	input	input of channel 69
77	AnalogIn<70>	335.00	2818.30	input	input of channel 70
78	AnalogIn<71>	490.00	2778.06	input	input of channel 71
79	AnalogIn<72>	25.00	2737.82	input	input of channel 72
80	AnalogIn<73>	180.00	2697.58	input	input of channel 73
81	AnalogIn<74>	335.00	2657.34	input	input of channel 74
82	AnalogIn<75>	490.00	2617.10	input	input of channel 75
83	AnalogIn<76>	25.00	2576.86	input	input of channel 76
84	AnalogIn<77>	180.00	2536.62	input	input of channel 77
85	AnalogIn<78>	335.00	2496.38	input	input of channel 78
86	AnalogIn<79>	490.00	2456.14	input	input of channel 79
87	AnalogIn<80>	25.00	2415.90	input	input of channel 80
88	AnalogIn<81>	180.00	2375.66	input	input of channel 81
89	AnalogIn<82>	335.00	2335.42	input	input of channel 82
90	AnalogIn<83>	490.00	2295.18	input	input of channel 83
91	AnalogIn<84>	25.00	2254.94	input	input of channel 84
92	AnalogIn<85>	180.00	2214.70	input	input of channel 85

Ref. no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
93	AnalogIn<86>	335.00	2174.46	input	input of channel 86
94	AnalogIn<87>	490.00	2134.22	input	input of channel 87
95	AnalogIn<88>	25.00	2093.98	input	input of channel 88
96	AnalogIn<89>	180.00	2053.74	input	input of channel 89
97	AnalogIn<90>	335.00	2013.50	input	input of channel 90
98	AnalogIn<91>	490.00	1973.26	input	input of channel 91
99	AnalogIn<92>	25.00	1933.02	input	input of channel 92
100	AnalogIn<93>	180.00	1892.78	input	input of channel 93
101	AnalogIn<94>	335.00	1852.54	input	input of channel 94
102	AnalogIn<95>	490.00	1812.30	input	input of channel 95
103	AnalogIn<96>	25.00	1772.06	input	input of channel 96
104	AnalogIn<97>	180.00	1731.82	input	input of channel 97
105	AnalogIn<98>	335.00	1691.58	input	input of channel 98
106	AnalogIn<99>	490.00	1651.34	input	input of channel 99
107	AnalogIn<100>	25.00	1611.10	input	input of channel 100
108	AnalogIn<101>	180.00	1570.86	input	input of channel 101
109	AnalogIn<102>	335.00	1530.62	input	input of channel 102
110	AnalogIn<103>	490.00	1490.38	input	input of channel 103
111	AnalogIn<104>	25.00	1450.14	input	input of channel 104
112	AnalogIn<105>	180.00	1409.90	input	input of channel 105
113	AnalogIn<106>	335.00	1369.66	input	input of channel 106
114	AnalogIn<107>	490.00	1329.42	input	input of channel 107
115	AnalogIn<108>	25.00	1289.18	input	input of channel 108
116	AnalogIn<109>	180.00	1248.94	input	input of channel 109
117	AnalogIn<110>	335.00	1208.70	input	input of channel 110
118	AnalogIn<111>	490.00	1168.46	input	input of channel 111
119	AnalogIn<112>	25.00	1128.22	input	input of channel 112
120	AnalogIn<113>	180.00	1087.98	input	input of channel 113
121	AnalogIn<114>	335.00	1047.74	input	input of channel 114
122	AnalogIn<115>	490.00	1007.50	input	input of channel 115
123	AnalogIn<116>	25.00	967.26	input	input of channel 116
124	AnalogIn<117>	180.00	927.02	input	input of channel 117
125	AnalogIn<118>	335.00	886.78	input	input of channel 118
126	AnalogIn<119>	490.00	846.54	input	input of channel 119
127	AnalogIn<120>	25.00	806.30	input	input of channel 120
128	AnalogIn<121>	180.00	766.06	input	input of channel 121
129	AnalogIn<122>	335.00	725.82	input	input of channel 122
130	AnalogIn<123>	490.00	685.58	input	input of channel 123
131	AnalogIn<124>	25.00	645.34	input	input of channel 124
132	AnalogIn<125>	180.00	605.10	input	input of channel 125
133	AnalogIn<126>	335.00	564.86	input	input of channel 126
134	AnalogIn<127>	490.00	524.62	input	input of channel 127
135	VddPre	25.00	484.38	power input	positive preamplifier supply
136	VddPre	180.00	444.14	power input	positive preamplifier supply
137	GndPre	335.00	403.90	power input	negative preamplifier supply (detector gnd)
138	GndPre	490.00	363.66	power input	negative preamplifier supply (detector gnd)

A.2 Bottom Pads

Ref. no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
139	ProbeIDAC	1824.12	37.50	output	analog probe pad for current DAC *Ibuf*
140	GndPre	1939.12	37.50	power input	negative preamplifier supply (detector gnd)
141	VddPre	2054.12	37.50	power input	positive preamplifier supply
142	VddComp	2169.12	37.50	power input	positive comparator supply
143	GndComp	2284.12	37.50	power input	negative comparator supply
144	Gndd	2399.12	37.50	power input	negative digital supply
145	Vddd	2514.12	37.50	power input	positive digital supply
146	notCompClock	2629.12	37.50	LVDS input	comparator clock
147	CompClock	2744.12	37.50	LVDS input	comparator clock
148	CompOut<8>	2859.12	37.50	LVDS output	comparator output channel 8
149	notCompOut<8>	2974.12	37.50	LVDS output	comparator output channel 8
150	CompOut<9>	3089.12	37.50	LVDS output	comparator output channel 9
151	notCompOut<9>	3204.12	37.50	LVDS output	comparator output channel 9
152	CompOut<10>	3319.12	37.50	LVDS output	comparator output channel 10
153	notCompOut<10>	3434.12	37.50	LVDS output	comparator output channel 10
154	CompOut<11>	3549.12	37.50	LVDS output	comparator output channel 11
155	notCompOut<11>	3664.12	37.50	LVDS output	comparator output channel 11
156	CompOut<12>	3779.12	37.50	LVDS output	comparator output channel 12
157	notCompOut<12>	3894.12	37.50	LVDS output	comparator output channel 12
158	CompOut<13>	4009.12	37.50	LVDS output	comparator output channel 13
159	notCompOut<13>	4124.12	37.50	LVDS output	comparator output channel 13
160	CompOut<14>	4239.12	37.50	LVDS output	comparator output channel 14
161	notCompOut<14>	4354.12	37.50	LVDS output	comparator output channel 14
162	CompOut<15>	4469.12	37.50	LVDS output	comparator output channel 15
163	notCompOut<15>	4584.12	37.50	LVDS output	comparator output channel 15
164	VddCPB	4699.12	37.50	power input	positive comparator supply for LVDS pads
165	GndCPB	4814.12	37.50	power input	negative comparator supply for LVDS pads
166	FifoFull	4929.12	37.50	CMOS output	indicates full derandomizing buffer
167	RoTokenIn	5044.12	37.50	CMOS input (pull-down)	readout start token in daisy-chain mode
168	RoReTokenOut	5159.12	37.50	CMOS output	return token in daisy-chain mode

A.3 Backside Pads

Ref. no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
169	Vddd	5274.62	184.72	power input	positive digital supply (pad window: $(95 \times 210)\,\mu\mathrm{m}^2$)

Ref. no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
170	Gndd	5274.62	414.72	power input	negative digital supply (pad window: $(95 \times 210)\,\mu m^2$)
171	TrigMon	5274.62	644.72	CMOS output	indicates if trigger pointer passes column 0
172	WriteMon	5274.62	759.72	CMOS output	indicates if write pointer passes column 0
173	notTrigger	5274.62	874.72	LVDS input	trigger
174	Trigger	5274.62	989.72	LVDS input	trigger
175	notClock	5274.62	1104.72	LVDS input	system clock
176	Clock	5274.62	1219.72	LVDS input	system clock
177	notTestpulse	5274.62	1334.72	LVDS input	test pulse
178	Testpulse	5274.62	1449.72	LVDS input	test pulse
179	notReset	5274.62	1564.72	LVDS input	system reset
180	Reset	5274.62	1679.72	LVDS input	system reset
181	notDataValid	5274.62	1794.72	LVDS output	indicates presence of valid data
182	DataValid	5274.62	1909.72	LVDS output	indicates presence of valid data
183	I2CAddr<0>	5274.62	2024.72	CMOS input (pull-down)	Beetle chip id. bit 0
184	I2CAddr<1>	5274.62	2139.72	CMOS input (pull-down)	Beetle chip id. bit 1
185	I2CAddr<2>	5274.62	2254.72	CMOS input (pull-down)	Beetle chip id. bit 2
186	I2CAddr<3>	5274.62	2369.72	CMOS input (pull-down)	Beetle chip id. bit 3
187	I2CAddr<4>	5274.62	2484.72	CMOS input (pull-down)	Beetle chip id. bit 4
188	I2CAddr<5>	5274.62	2599.72	CMOS input (pull-down)	Beetle chip id. bit 5
189	I2CAddr<6>	5274.62	2714.72	CMOS input (pull-down)	Beetle chip id. bit 6
190	SCL	5274.62	2829.72	CMOS input (5V)	I^2C-bus clock port
191	SDA	5274.62	2944.72	CMOS inout (5V)	I^2C-bus data port
192	PowerupReset	5274.62	3059.72	block output	block pad for powerup Reset
193	EnableEDC	5274.62	3174.72	CMOS input pullup	enable Error Detection and Correction
194	notAnalogOut<3>	5274.62	3289.72	output	analog output channel 3
195	AnalogOut<3>	5274.62	3404.72	output	analog output channel 3
196	notAnalogOut<2>	5274.62	3519.72	output	analog output channel 2
197	AnalogOut<2>	5274.62	3634.72	output	analog output channel 2
198	notAnalogOut<1>	5274.62	3749.72	output	analog output channel 1
199	AnalogOut<1>	5274.62	3864.72	output	analog output channel 1
200	notAnalogOut<0>	5274.62	3979.72	output	analog output channel 0
201	AnalogOut<0>	5274.62	4094.72	output	analog output channel 0
202	GndMux	5274.62	4209.72	power input	neg. digital MUX supply (pad window: $(95 \times 210)\,\mu m^2$)
203	GndTx	5274.62	4439.72	power input	neg. supply output driver (pad window: $(95 \times 152.5)\,\mu m^2$)

Ref. no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
204	Gnda	5274.62	4612.22	power input	neg. analog supply (pad window: (95×152.5) μm^2)
205	VddMux	5274.62	4784.72	power input	pos. digital MUX supply (pad window: (95 × 210) μm^2)
206	VddTx	5274.62	5014.72	power input	pos. supply output driver (pad window: (95×152.5) μm^2)
207	Vdda	5274.62	5187.22	power input	pos. analog supply (pad window: (95×152.5) μm^2)
208	Icurrbuf	5274.62	5359.72	block output	analog probe pad (to be blocked)
209	Isf	5274.62	5474.72	block output	analog probe pad (to be blocked)
210	Ipipe	5274.62	5589.72	block output	analog probe pad (to be blocked)
211	Vdclbuf	5274.62	5704.72	block output	analog probe pad (to be blocked)
212	Vdbuf	5274.62	5819.72	block output	analog probe pad (to be blocked)

A.4 Top Pads

Ref. no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
213	RoReTokenIn	5159.12	5967.52	CMOS input (pull-down)	return token in daisy-chain mode
214	RoTokenOut	5044.12	5967.52	CMOS output	readout start token in daisy-chain mode
215					
216	ProbeVrefBE	4814.12	5967.52	output	analog probe pad for current source BE
217	ProbeIoutBE	4699.12	5967.52	output	analog probe pad for current source BE
218	PipeampTestOut	4584.12	5967.52	output	analog probe pad for pipeline-amplifier
219					
220	GndCPT	4354.12	5967.52	power input	negative comparator supply for LVDS pads
221	VddCPT	4239.12	5967.52	power input	positive comparator supply for LVDS pads
222	notCompOut<7>	4124.12	5967.52	LVDS output	comparator output channel 7
223	CompOut<7>	4009.12	5967.52	LVDS output	comparator output channel 7
224	notCompOut<6>	3894.12	5967.52	LVDS output	comparator output channel 6
225	CompOut<6>	3779.12	5967.52	LVDS output	comparator output channel 6
226	notCompOut<5>	3664.12	5967.52	LVDS output	comparator output channel 5
227	CompOut<5>	3549.12	5967.52	LVDS output	comparator output channel 5
228	notCompOut<4>	3434.12	5967.52	LVDS output	comparator output channel 4

Ref. no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
229	CompOut<4>	3319.12	5967.52	LVDS output	comparator output channel 4
230	notCompOut<3>	3204.12	5967.52	LVDS output	comparator output channel 3
231	CompOut<3>	3089.12	5967.52	LVDS output	comparator output channel 3
232	notCompOut<2>	2974.12	5967.52	LVDS output	comparator output channel 2
233	CompOut<2>	2859.12	5967.52	LVDS output	comparator output channel 2
234	notCompOut<1>	2744.12	5967.52	LVDS output	comparator output channel 1
235	CompOut<1>	2629.12	5967.52	LVDS output	comparator output channel 1
236	notCompOut<0>	2514.12	5967.52	LVDS output	comparator output channel 0
237	CompOut<0>	2399.12	5967.52	LVDS output	comparator output channel 0
238	GndComp	2284.12	5967.52	power input	negative comparator supply
239	VddComp	2169.12	5967.52	power input	positive comparator supply
240	VddPre	2054.12	5967.52	power input	positive preamplifier supply
241	GndPre	1939.12	5967.52	power input	negative preamplifier supply (detector gnd)
242	TestOutput	1824.12	5967.52	output	frontend output of testchannel
243	Bufbias	1709.12	5967.52	output	analog probe pad
244	Shabias1	1594.12	5967.52	output	analog probe pad
245	Shabias	1479.12	5967.52	output	analog probe pad
246	Prebias1	1364.12	5967.52	output	analog probe pad
247	Prebias	1249.12	5967.52	output	analog probe pad

B Heidelberg Test Boards

For a standalone characterisation of the *Beetle* chip, i.e. without a silicon sensor applied to it's input, a test setup consisting of two printed circuit boards has been developed in Heidelberg. This section summarises the pin configurations and bonding schemes of the two boards. The *daughter board* can carry two *Beetle* chips and is mounted on a second board, called *mother board*, which integrates the receiver circuitry for the analog output stages (Fig. 3) as well as a LVDS receiver. The setup allows the charge injection to 12 input channels per chip via a resistive voltage divider (located on the mother board) and a serial capacitance. Parallel capacitances can be applied as load. Serial and parallel capacitances are located on the daughter board.

Fig. 17 shows the pin configuration of the daughter board, Fig. 18 the layout of the top side and Fig. 19 the layout of the bottom side. Figs. 20 and 21 shows the corresponding bonding schemes with and without comparator operation. The pin configuration of the mother board is depicted in Fig. 22.

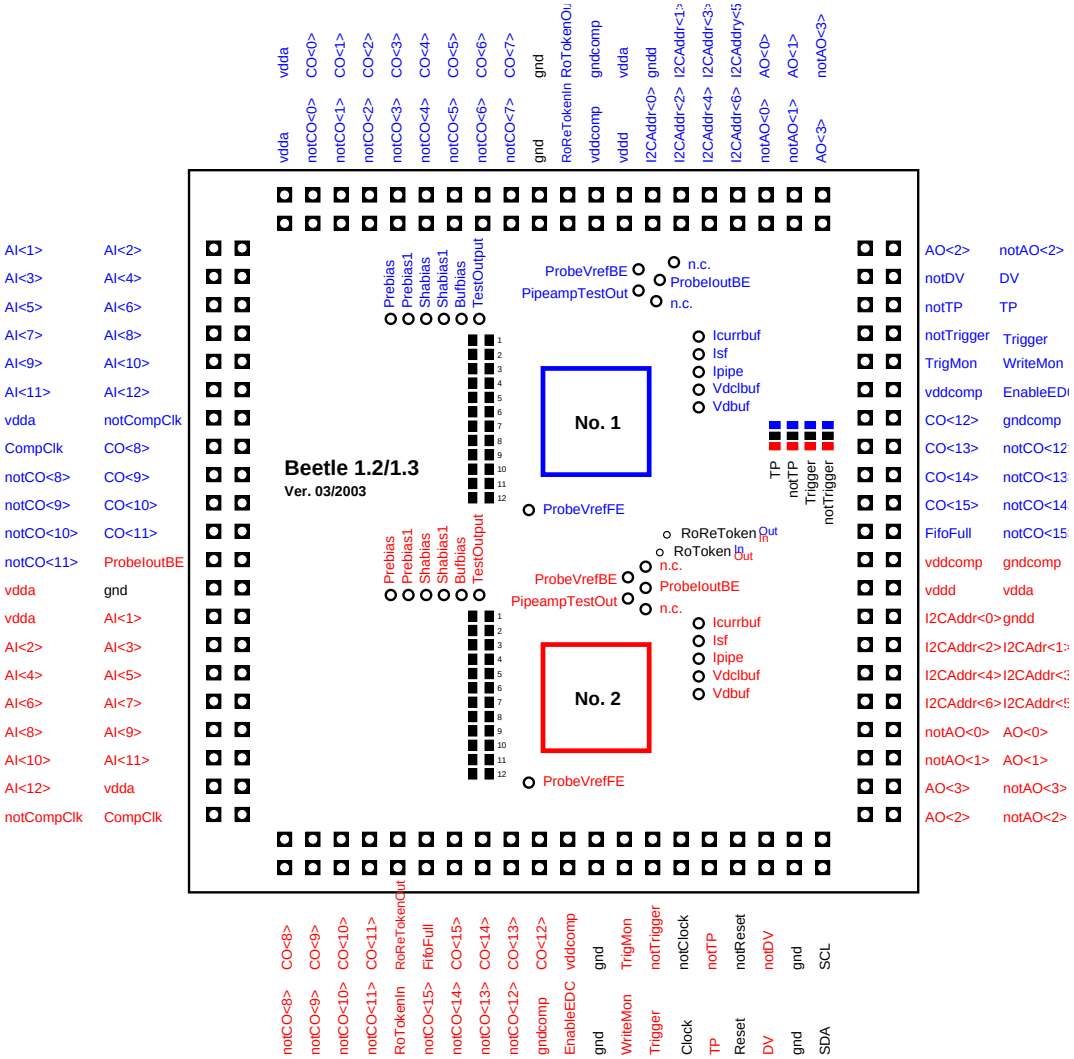


Figure 17: Pin configuration of the daughter board. The four jumper rows labelled *TP, notTP, Trigger, notTrigger* refer to chip no. 1 and select between the signal pins on the right side (upper position) and on the bottom side (lower position). Using the lower jumper positions, both chips receive *Trigger* and *TP* signals via the bottom side pins.

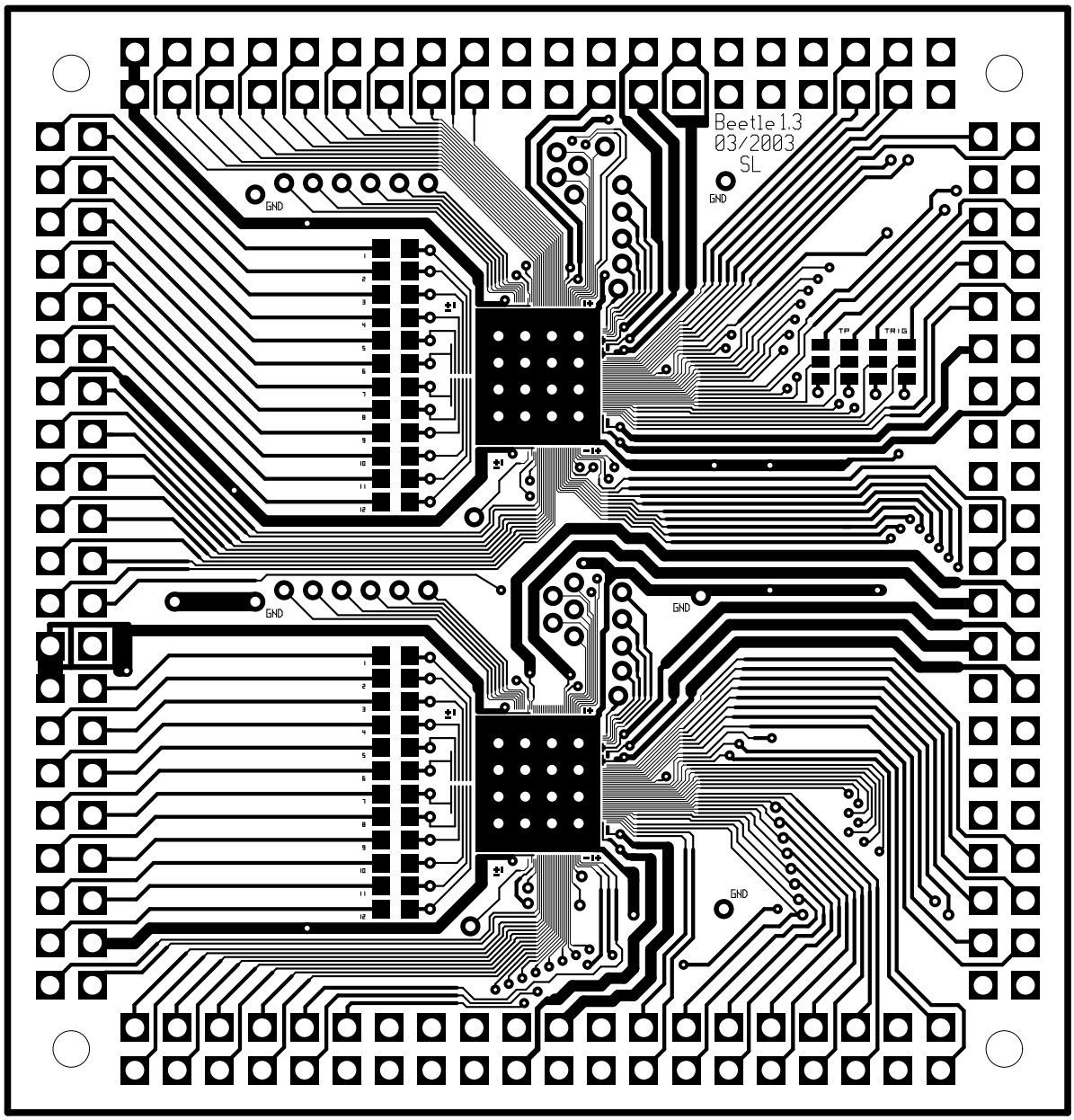


Figure 18: Top layer of the Heidelberg daughter PCB (version 03/2003).

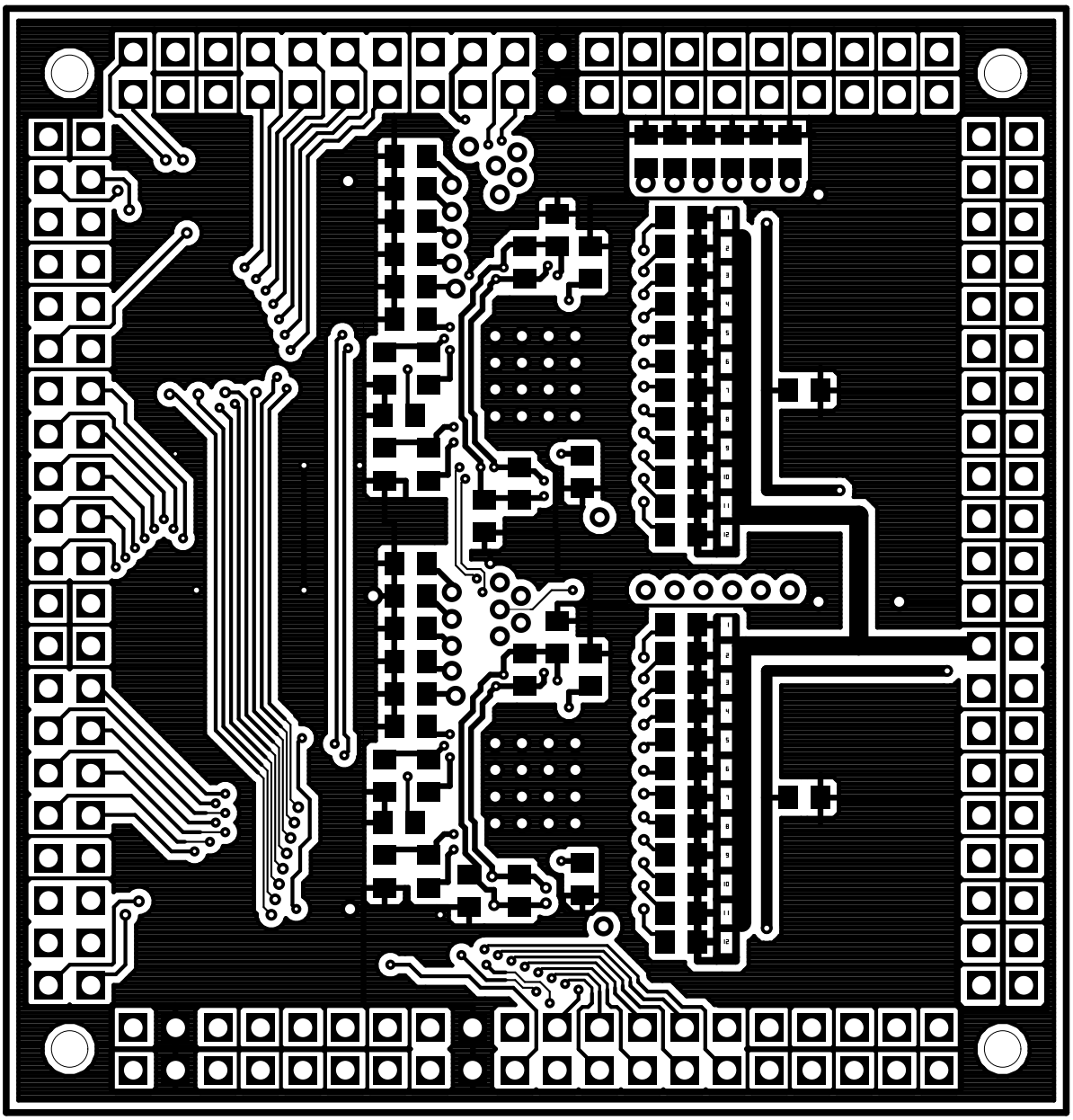


Figure 19: Bottom layer of the Heidelberg daughter PCB (version 03/2003).

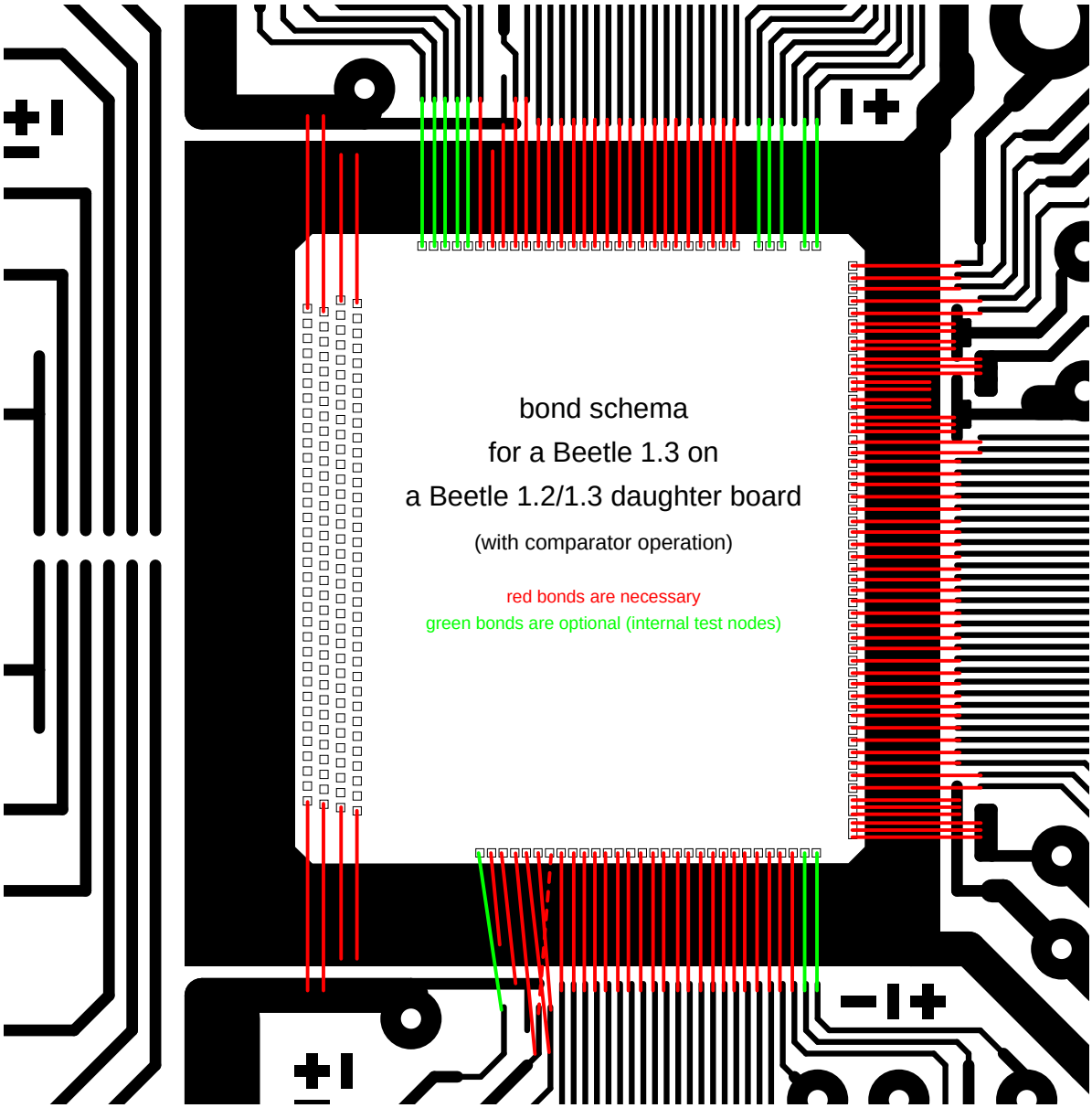


Figure 20: Bondplan for a *Beetle1.3* with comparator operation.

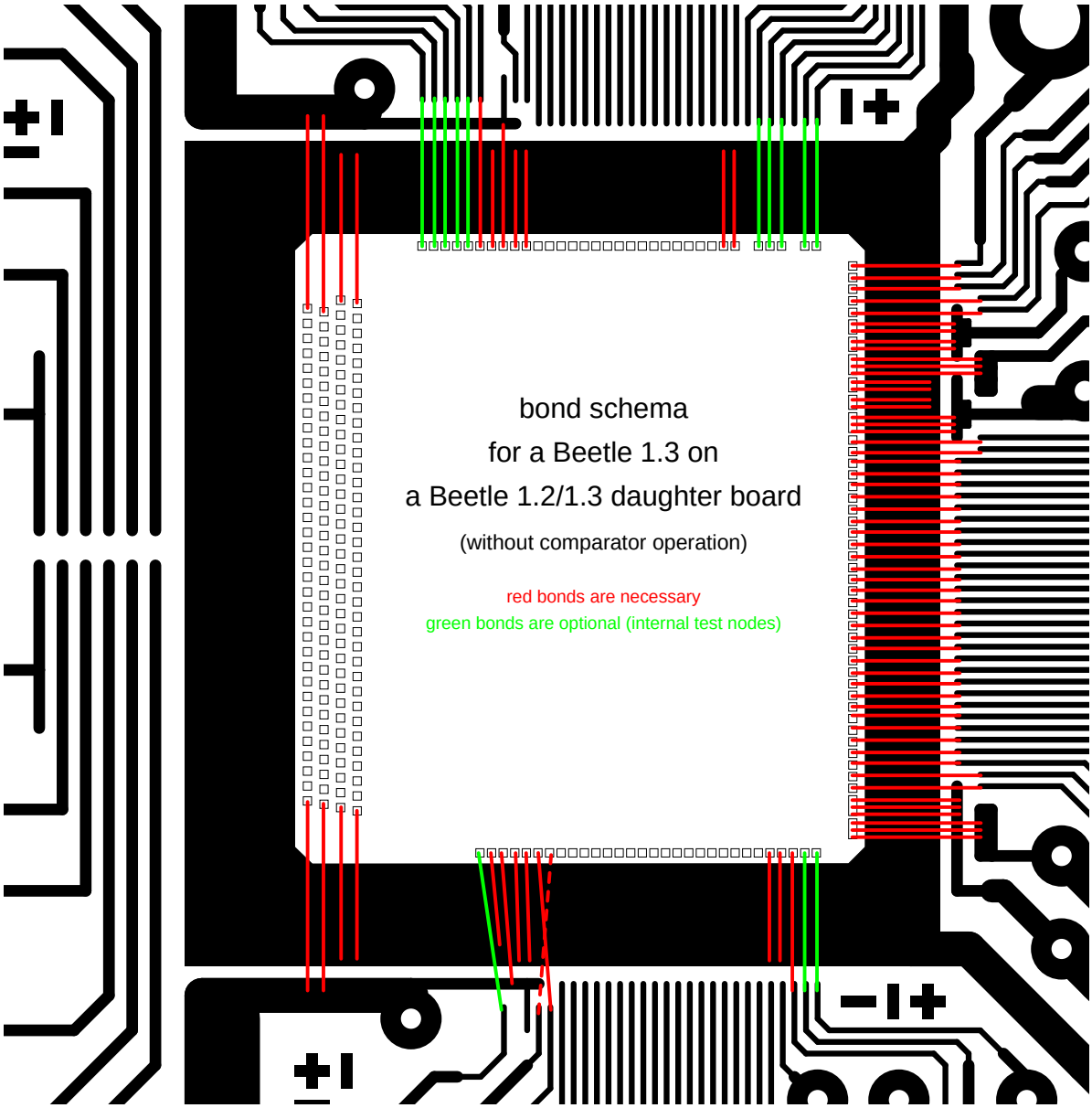


Figure 21: Bondplan for a *Beetle1.3* without comparator operation.

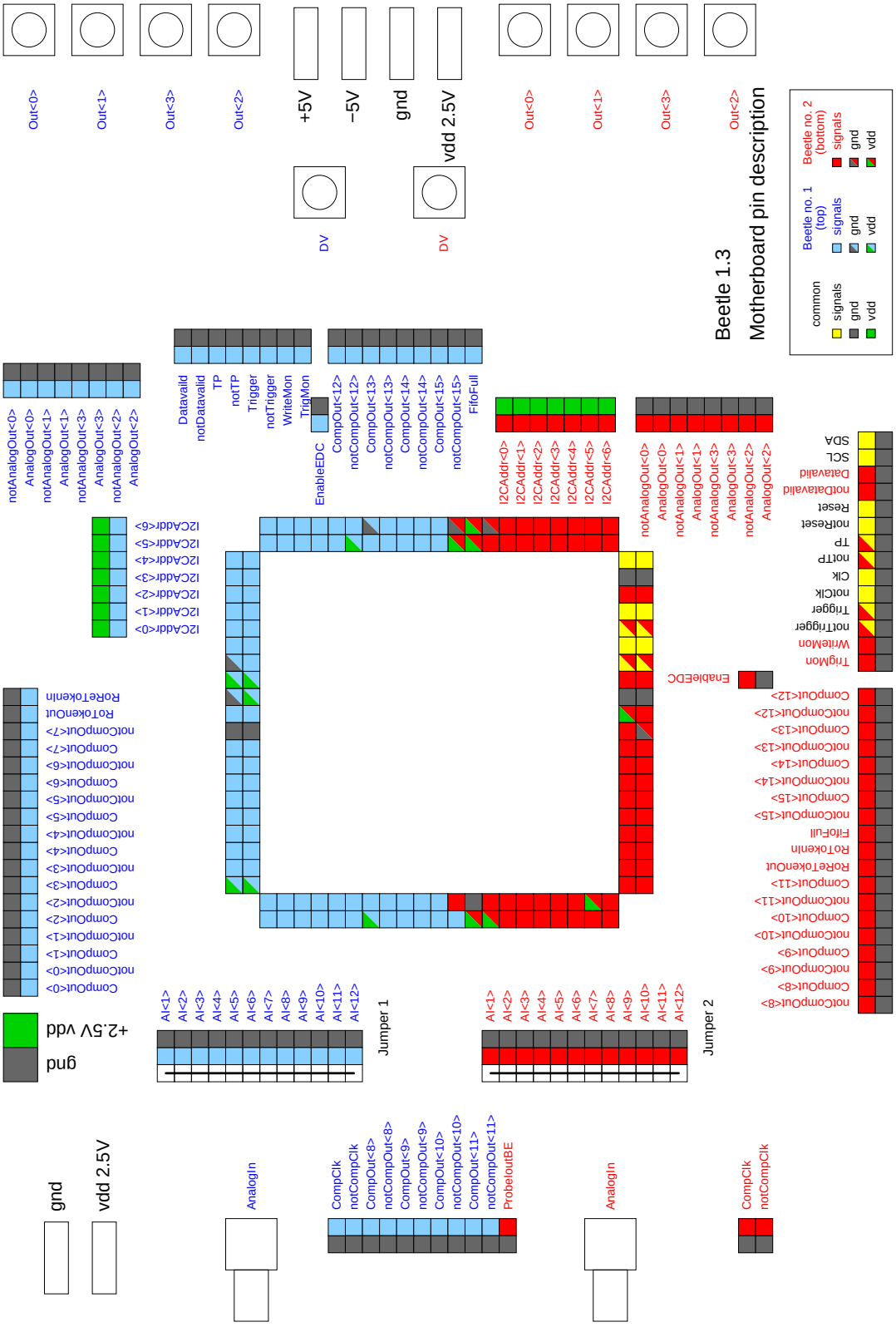


Figure 22: Pin configuration of the mother board.

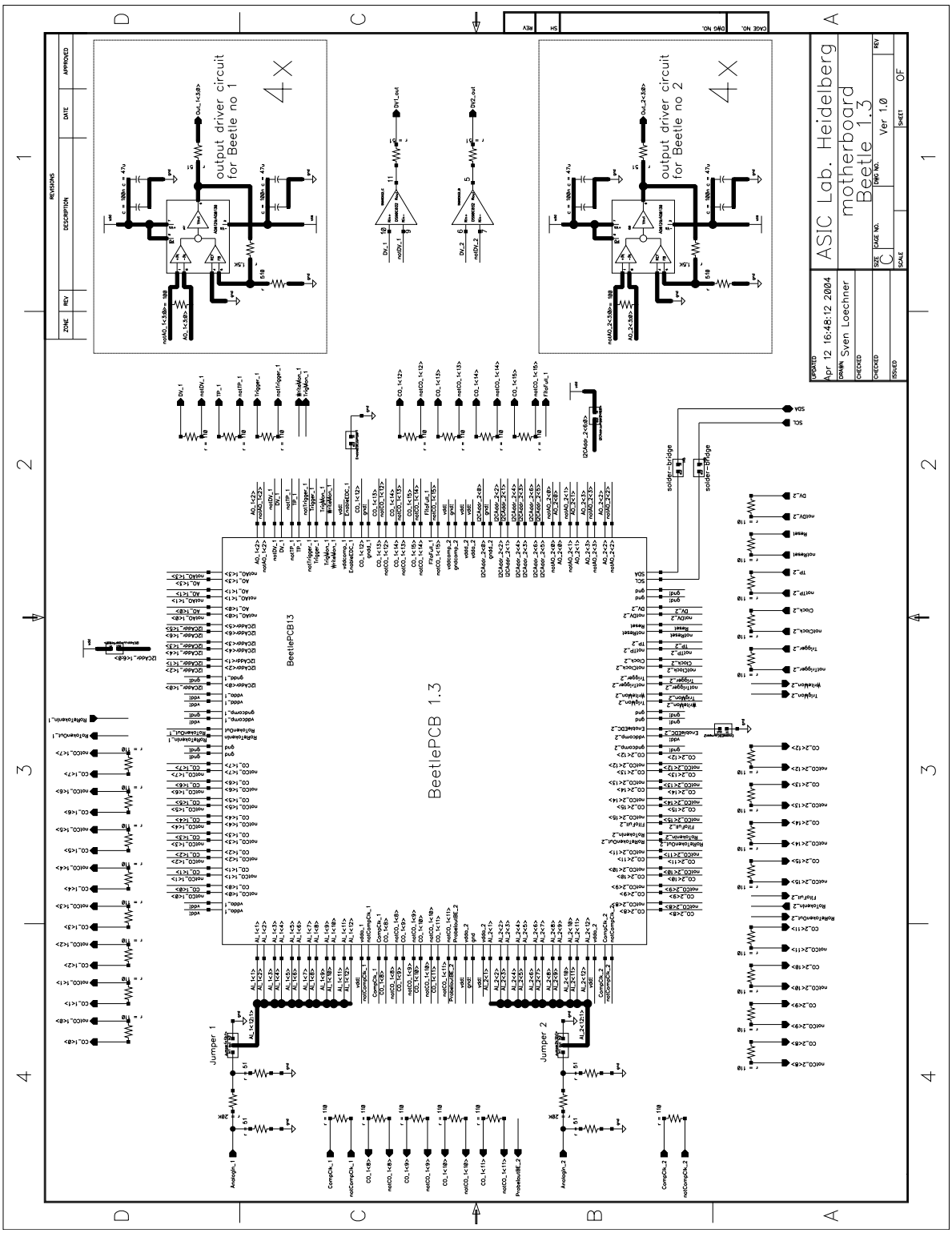


Figure 23: Schematic diagram of the mother board.

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