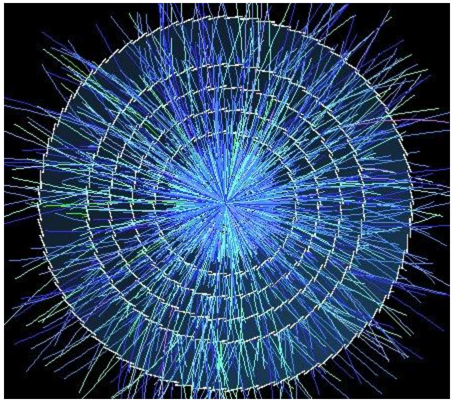
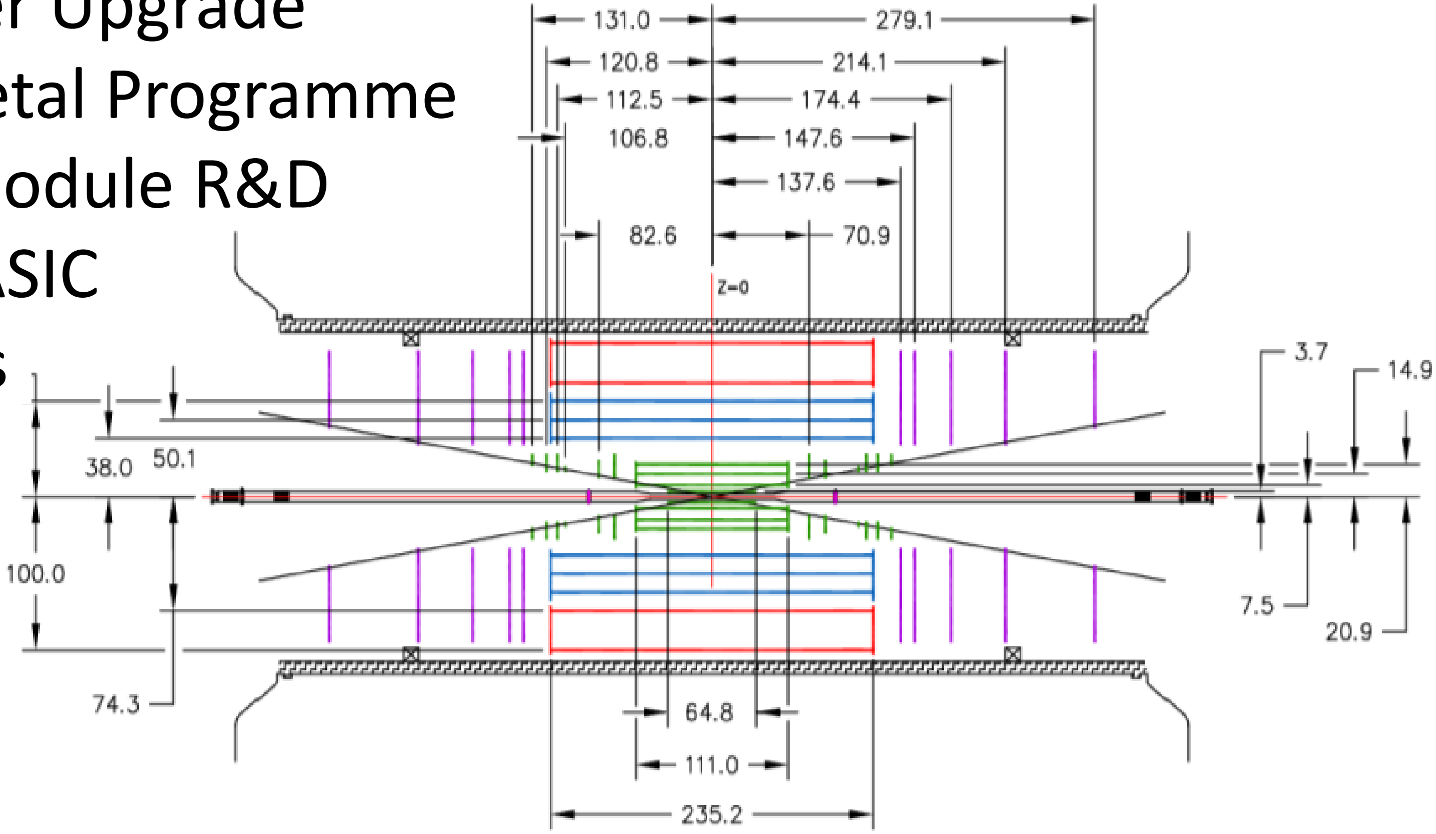
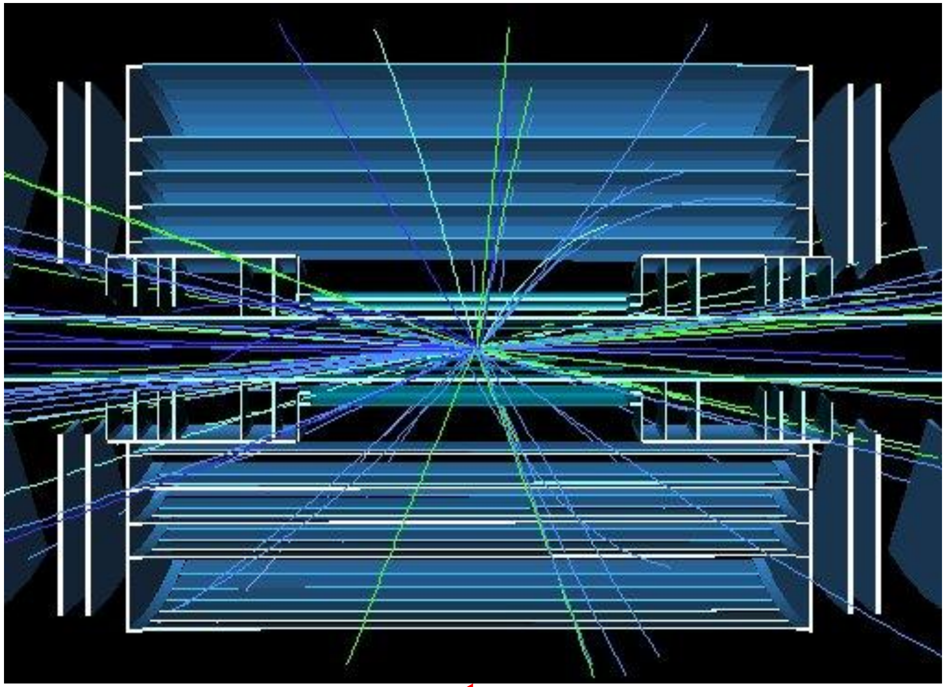
Tracker Upgrade for High Luminosity LHC (Phase-II)

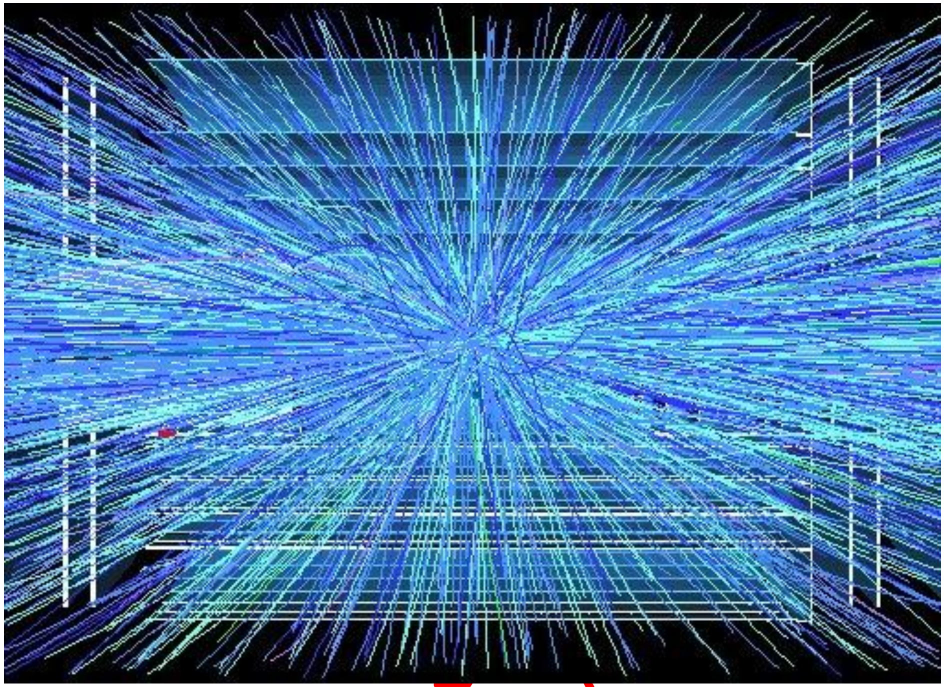


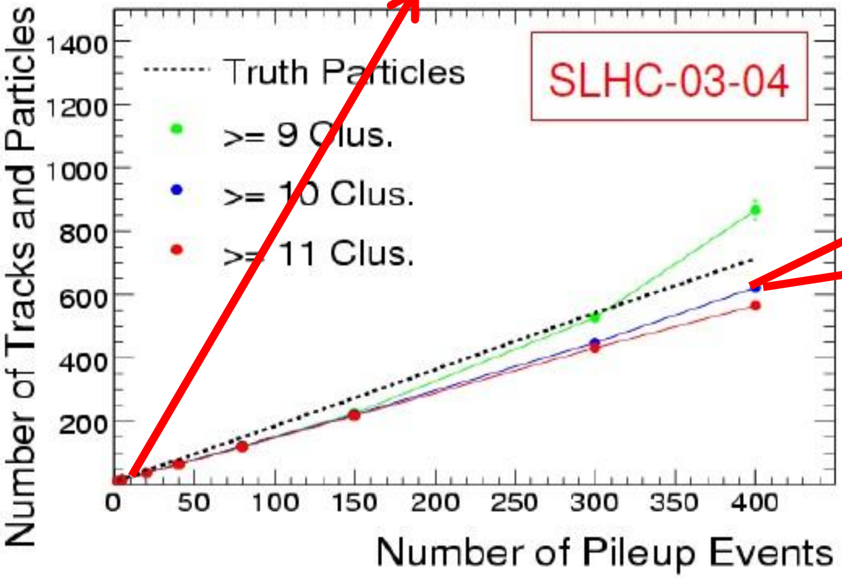
- Layout and Simulation
- Sensor Radiation Tolerance
- Pixel Detector at Phase-II
- Strip-Tracker Upgrade
  - Stave/Petal Programme
  - Super-module R&D
- New Strip ASIC
- Conclusions

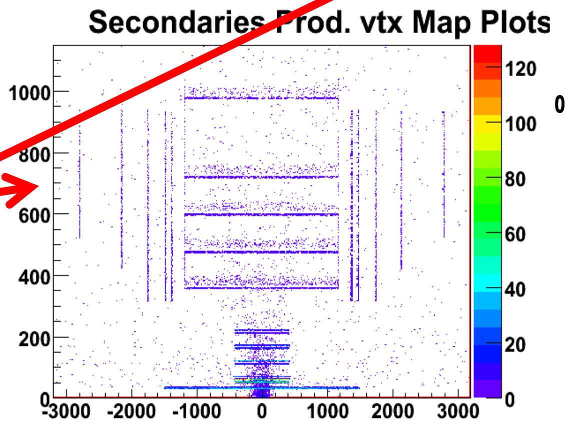


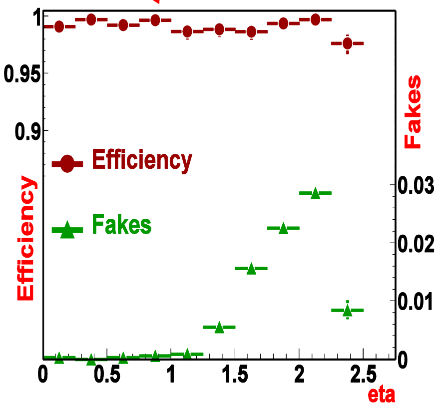
ATLAS Tracker Upgrade Simulation



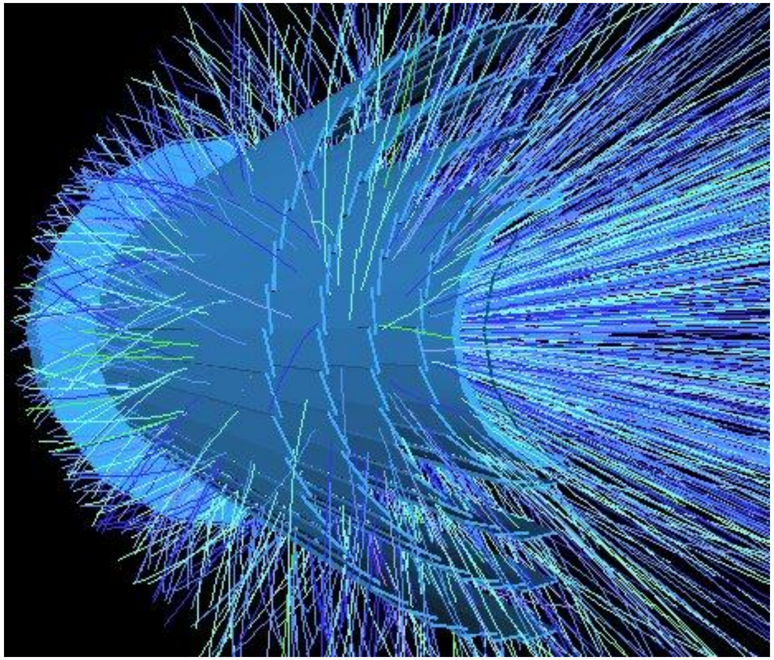


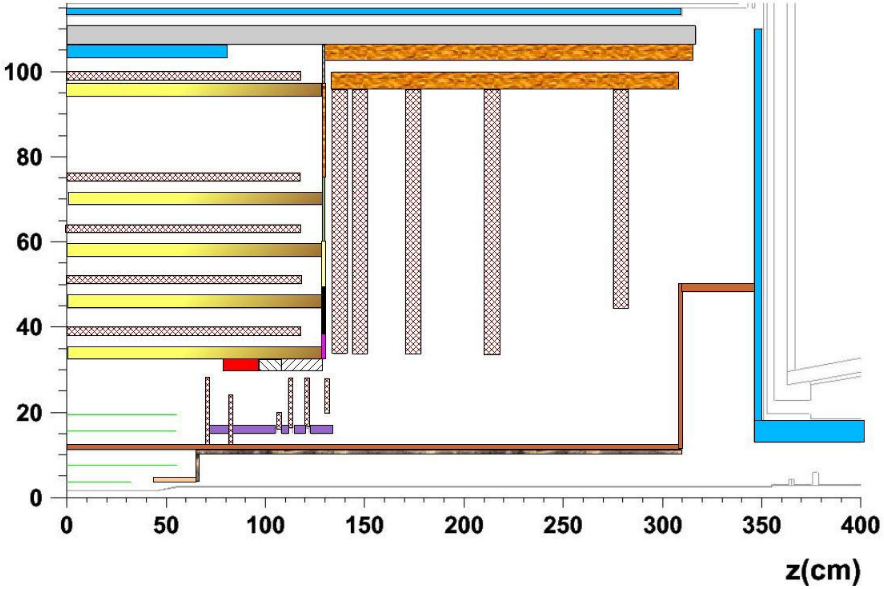




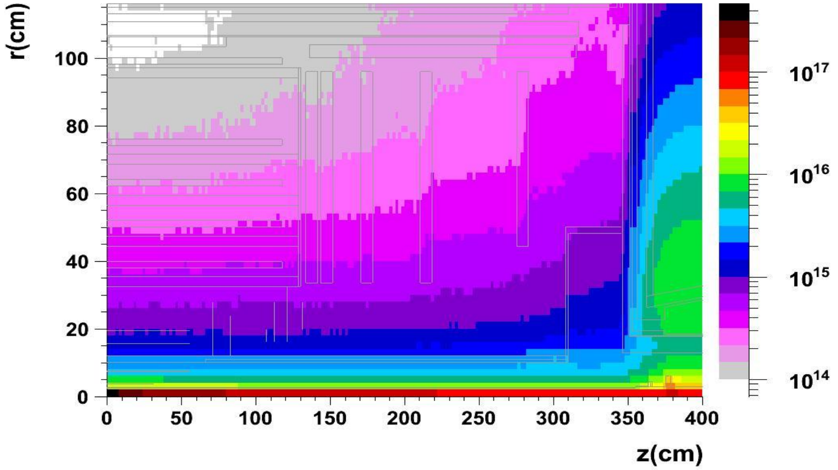


Radiation Background Simulation

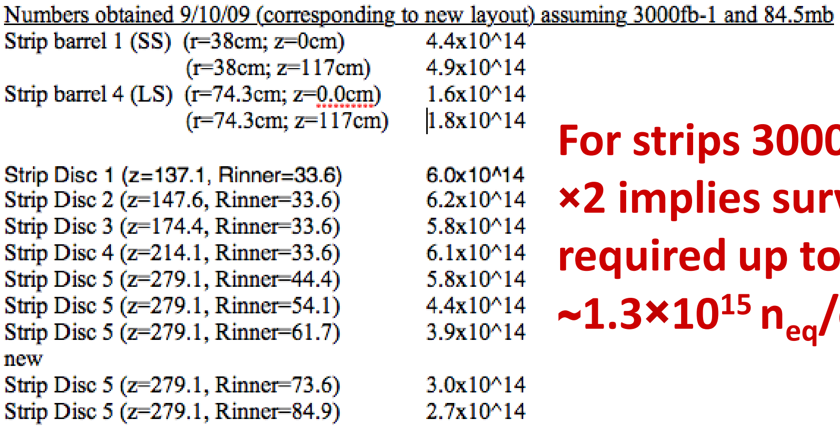




1 MeV neutron eq fluence



At inner pixel radii - target survival to 1-2×10^{16} n_{eq}/cm^2

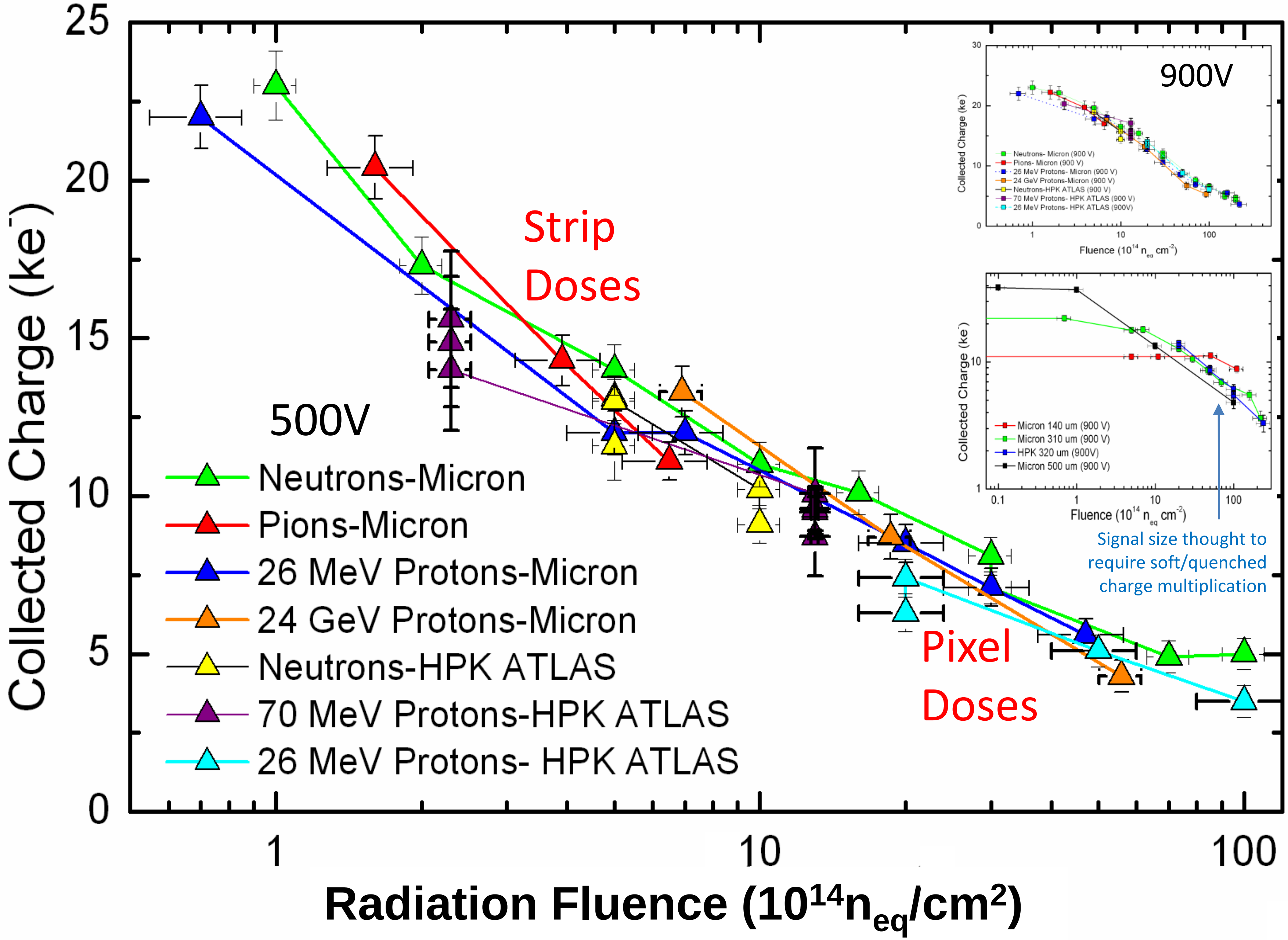


Numbers obtained 9/10/09 (corresponding to new layout) assuming 3000fb-1 and 84.5mb

Strip barrel 1 (SS)	(r=38cm; z=0cm)	4.4x10^14
	(r=38cm; z=117cm)	4.9x10^14
Strip barrel 4 (LS)	(r=74.3cm; z=0.0cm)	1.6x10^14
	(r=74.3cm; z=117cm)	1.8x10^14
Strip Disc 1 (z=137.1, Rinner=33.6)		6.0x10^14
Strip Disc 2 (z=147.6, Rinner=33.6)		6.2x10^14
Strip Disc 3 (z=174.4, Rinner=33.6)		5.8x10^14
Strip Disc 4 (z=214.1, Rinner=33.6)		6.1x10^14
Strip Disc 5 (z=279.1, Rinner=44.4)		5.8x10^14
Strip Disc 5 (z=279.1, Rinner=54.1)		4.4x10^14
Strip Disc 5 (z=279.1, Rinner=61.7)		3.9x10^14
new		
Strip Disc 5 (z=279.1, Rinner=73.6)		3.0x10^14
Strip Disc 5 (z=279.1, Rinner=84.9)		2.7x10^14

For strips 3000fb^{-1} ×2 implies survival required up to ~1.3×10^{15} n_{eq}/cm^2

n-in-p Planar FZ Irradiations

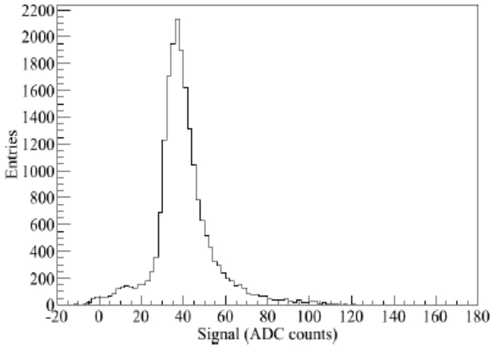


Signal size thought to require soft/quenched charge multiplication

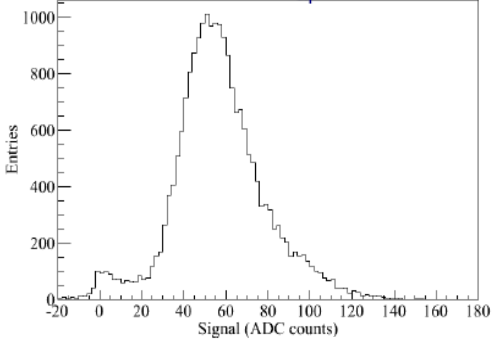
Irradiated 3D & Diamond Sensors Test Beam Results

- Signal of the channel closest to the track point of impact

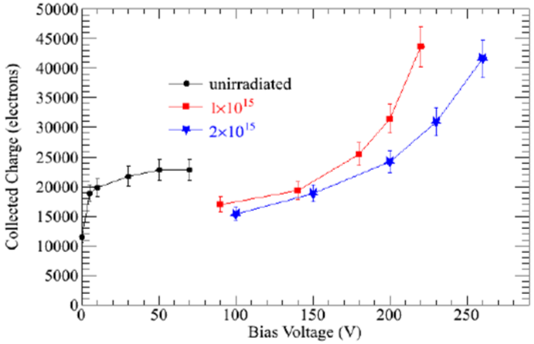
unirradiated, 70 V



irradiated (1x10^{15} n$_{eq}$/cm^2), 200 V



Landau Most Probable Value as a function of bias voltage



Irradiated device: increasing signal above ~150 V

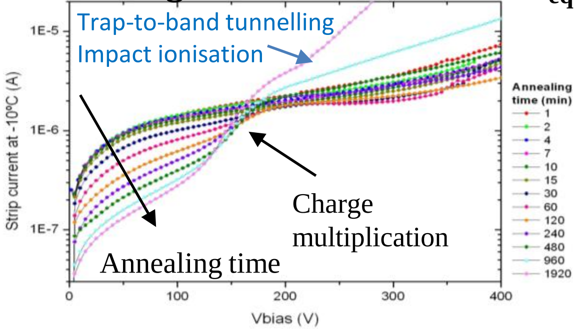
→ Charge Multiplication

- Higher signal after irradiation than before

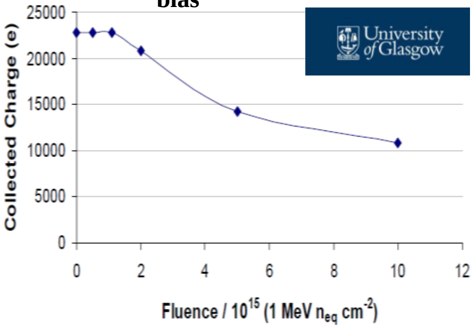
  → Charge multiplication!

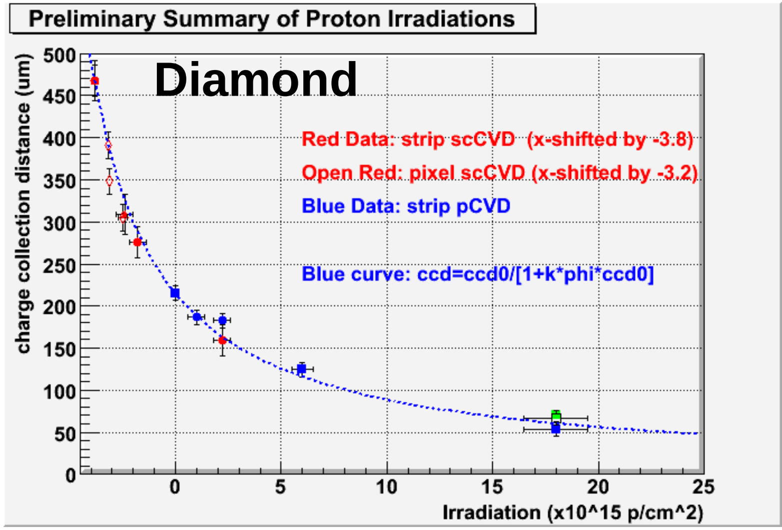
- Entries at low signal values: charge sharing, tracks going straight through columns

Leakage current, -10ºC, 10^{16} n$_{eq}$/cm^2



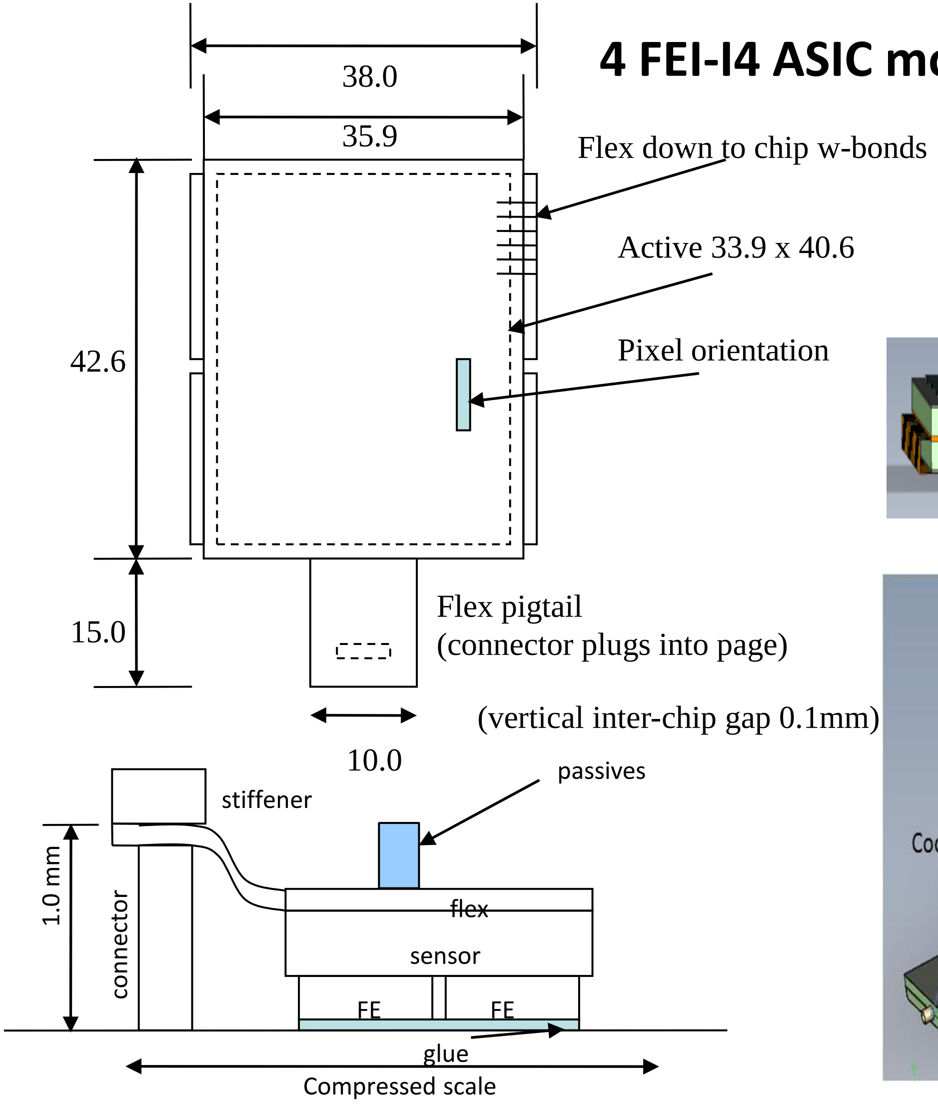
V$_{bias}$ fixed at 150V



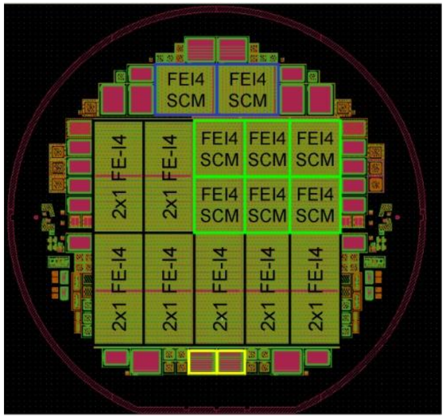


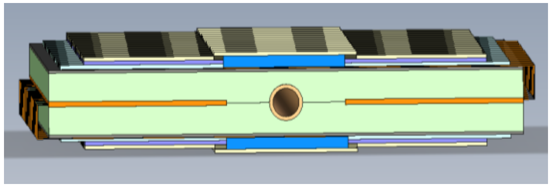
SLHC Phase-II Pixels Outer Layer Stave Concept

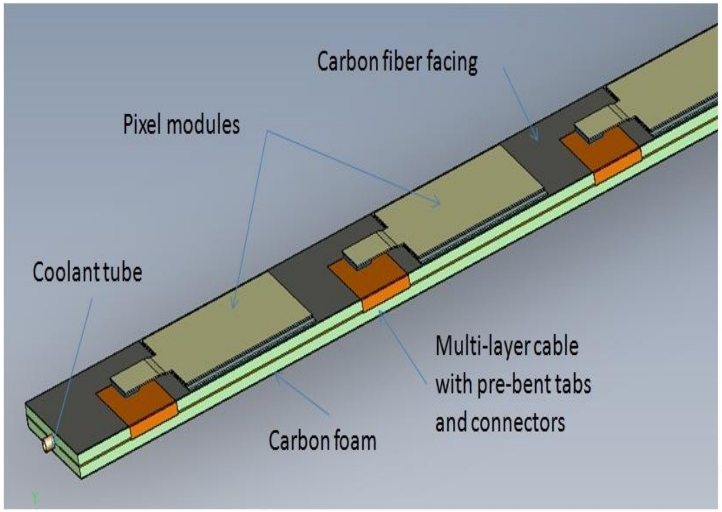
4 FEI-I4 ASIC module



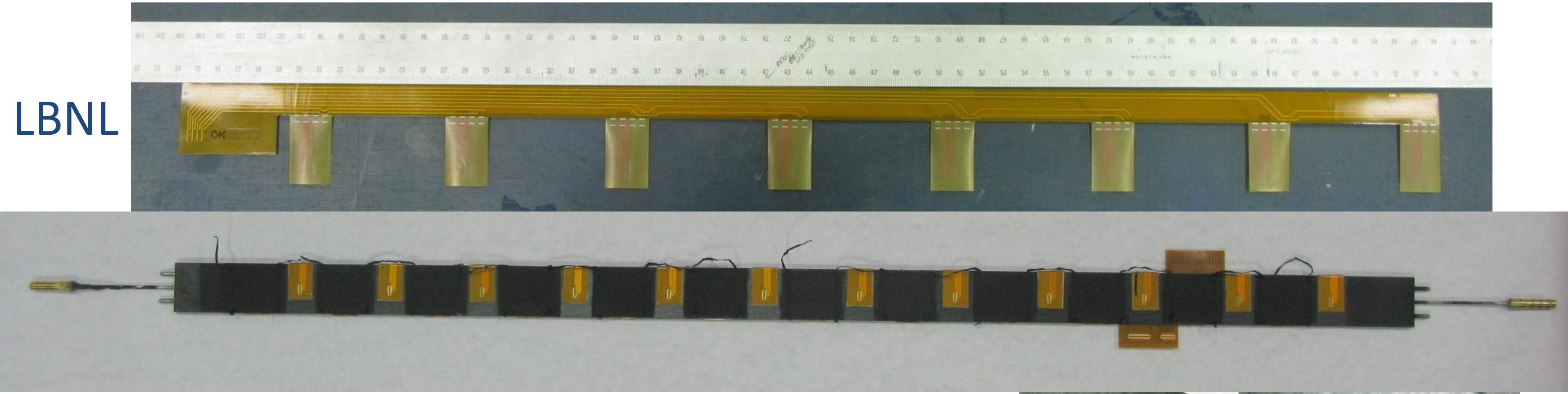
4 FEI-I4 compatible sensors from IBL project suitable for prototyping



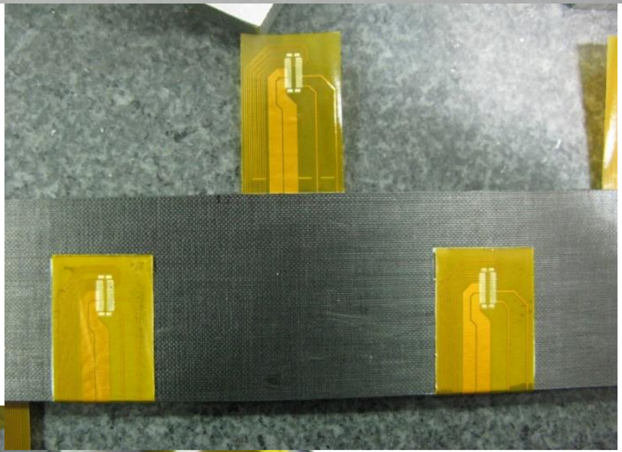


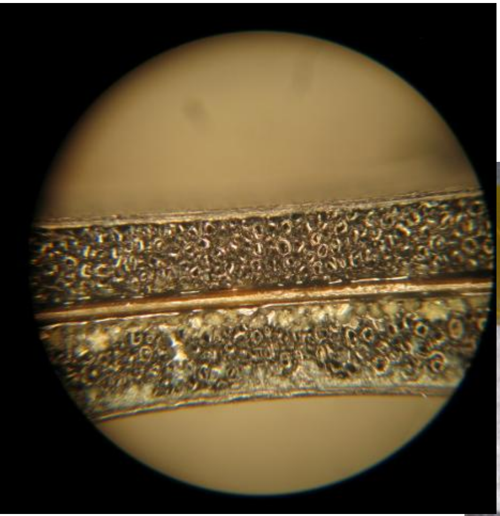


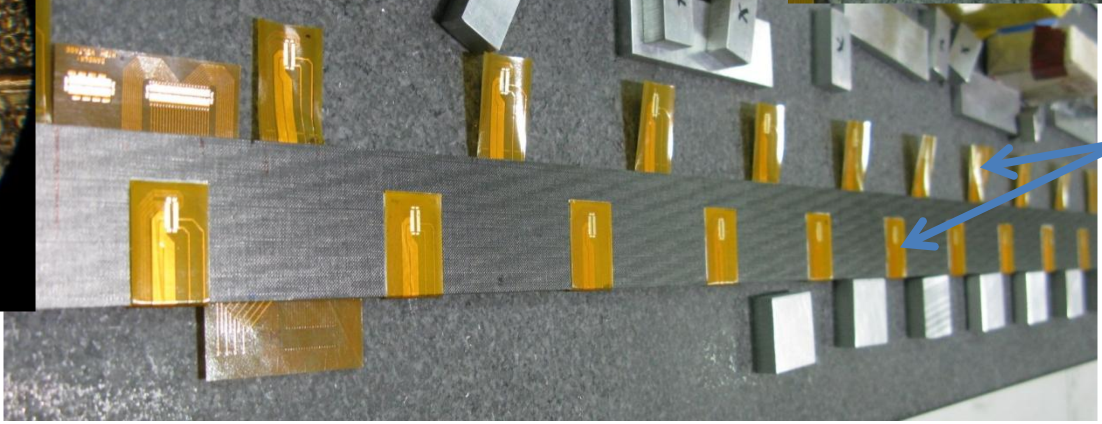
LBNL



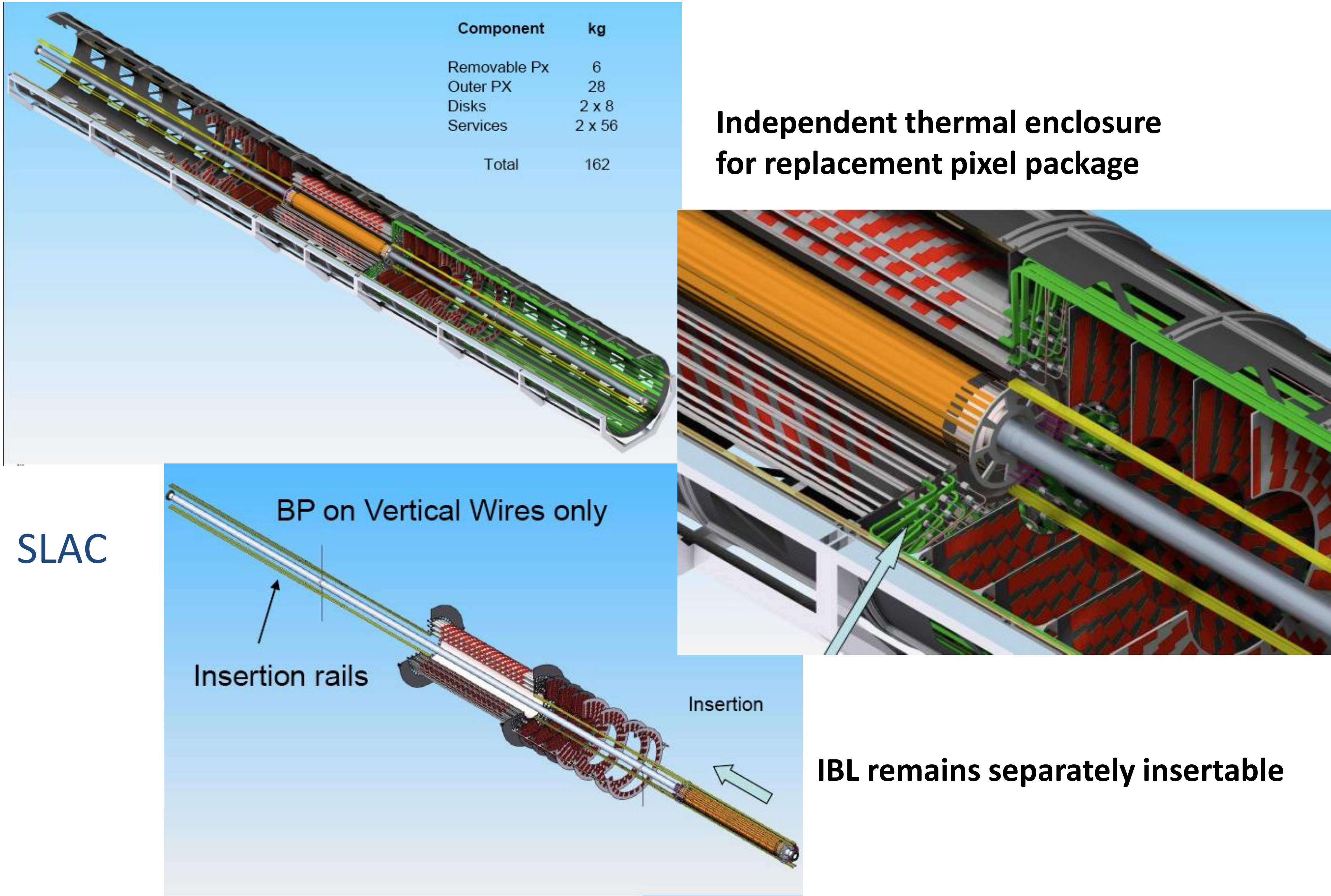
- Prototype cables made
- Embedded (glued) into 1m long stave
- Thermal, mechanical electrical testing just starting







Possible Phase-II Pixel Mechanics



Component	kg
Removable Px	6
Outer PX	28
Disks	2 x 8
Services	2 x 56
Total	162

Independent thermal enclosure
for replacement pixel package

SLAC

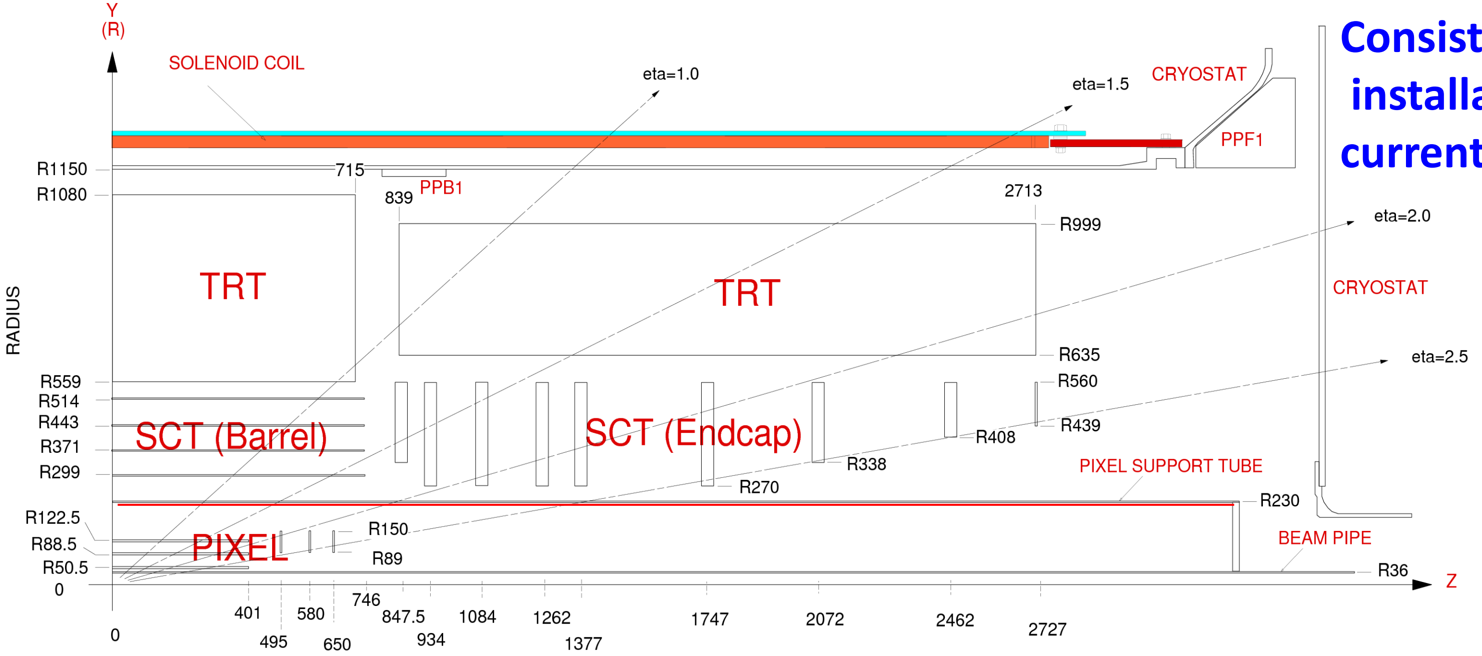
BP on Vertical Wires only

Insertion rails

Insertion

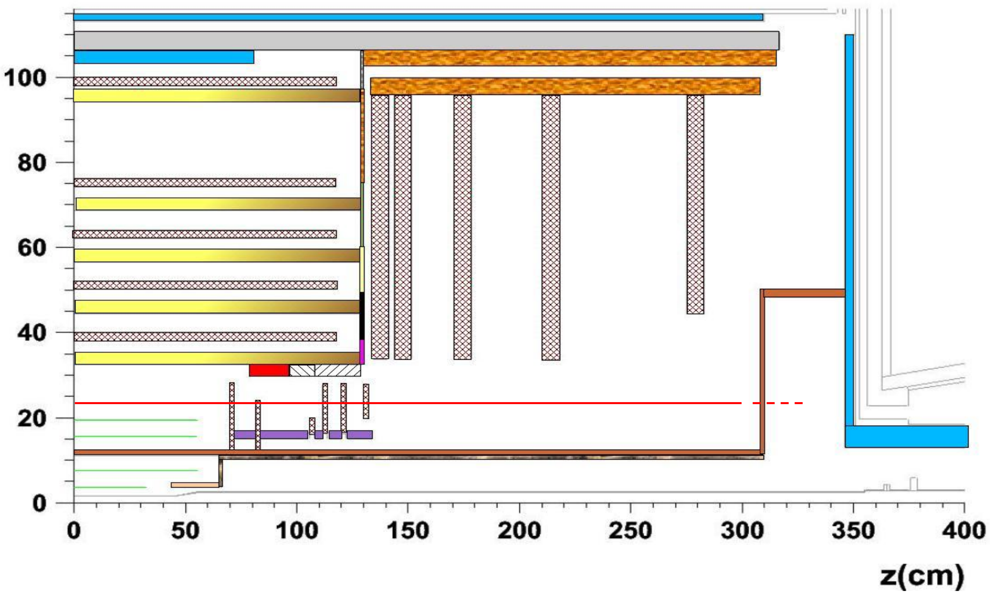
IBL remains separately insertable

Independently Installable Pixels



Consistent with installation within current pixel radii

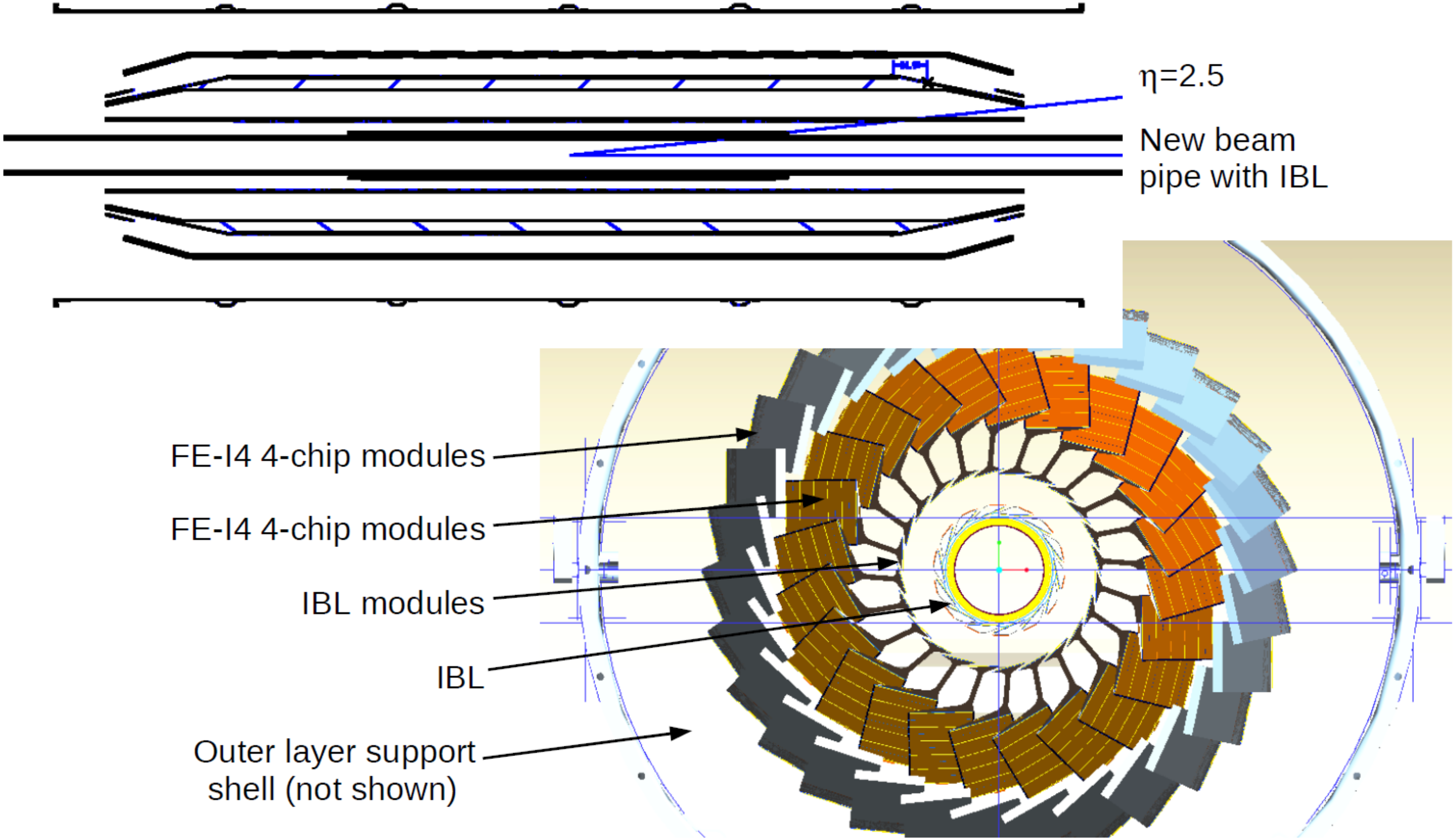
Current SCT quarter section layout showing pixel support tube at 23cm radius



Proposed All-silicon tracker layout showing radius of current pixel support tube.

Independently Installable Phase-II Pixel Design

LBNL



Existing pixel support tube

η=2.5

New beam pipe with IBL

FE-I4 4-chip modules

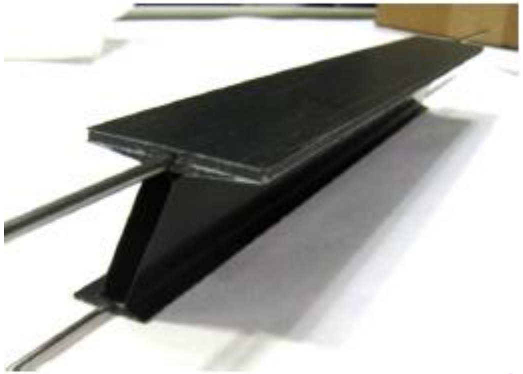
FE-I4 4-chip modules

IBL modules

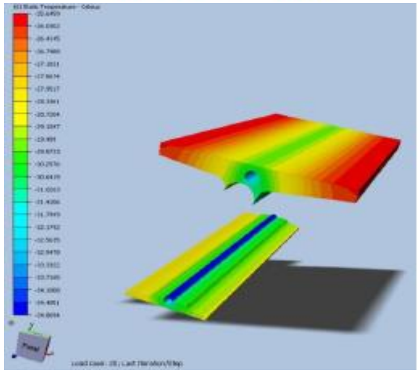
IBL

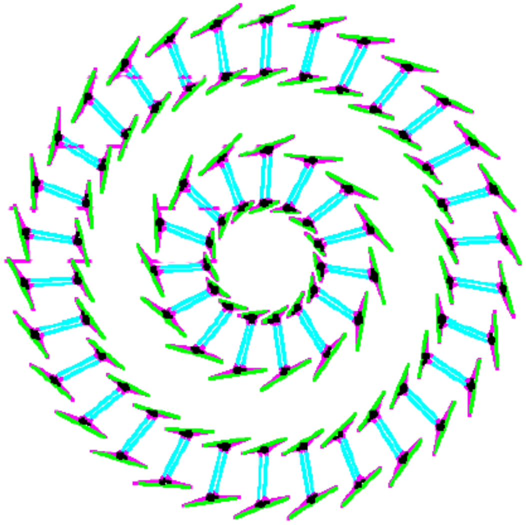
Outer layer support shell (not shown)

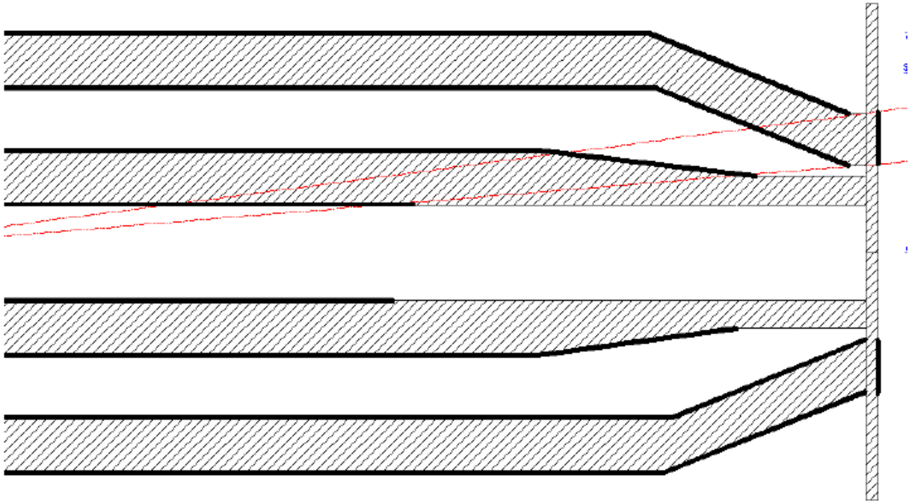
Material Reduction



I-beam prototype, LBNL 2010







LBNL

	Present detector + IBL	Double I-Beam
Number of channels	92 M	276 M
Global supports mass	8.3 kg	2.1 kg
Local supports mass	6.6 kg	5.6 kg (meas.)

Silicon mass equivalent of all mechanics	5.7 kg	2.8 kg
Sensor + chip mass	2.9 kg	4.4 kg (*)

Total silicon equivalent	8.7 kg	7.2 kg

Micro-Strips: Stave+Petal Programme

- **Designed to minimise material**
- **Requirements of automated assembly built in from the start**
- **Compatible with current services being reused or similar services cross-section**
- **Designs emphasises conservative assembly requirements assuming distributed production**
- **All component independently testable prior to construction**
- **Design aims to be low cost**

Spain: Valencia, Barcelona

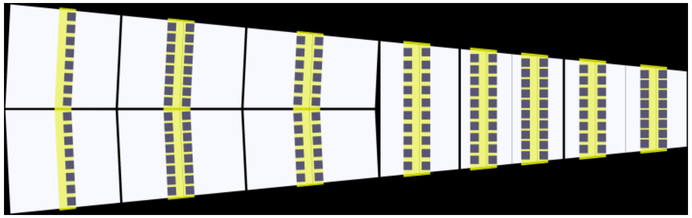
UK: Liverpool, RAL, Cambridge, Oxford, UCL, Sheffield, QMUL, Glasgow, ATC-Edinburgh, Lancaster

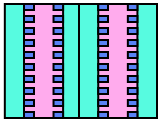
Germany: Freiburg, DESY, Berlin

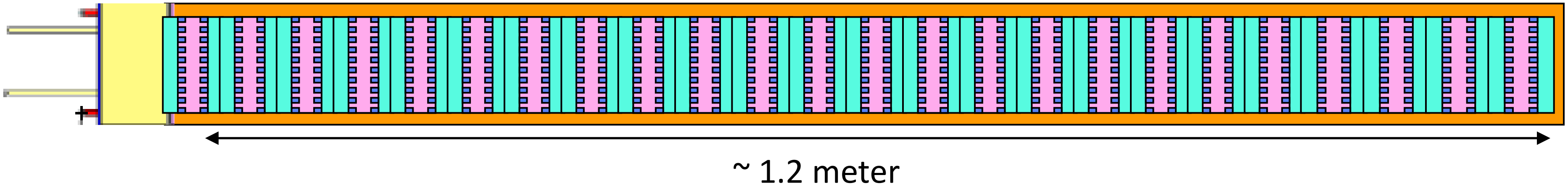
Netherlands: NIKHEF

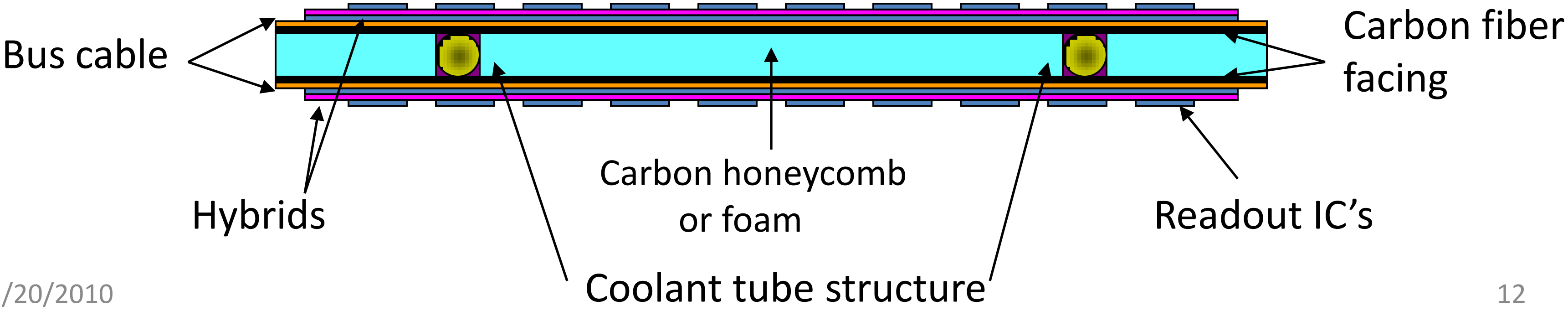
Czech Republic: Prague

USA: Brookhaven, Santa Cruz, SLAC, LBNL, Stonybrook, Yale, NYU, Duke

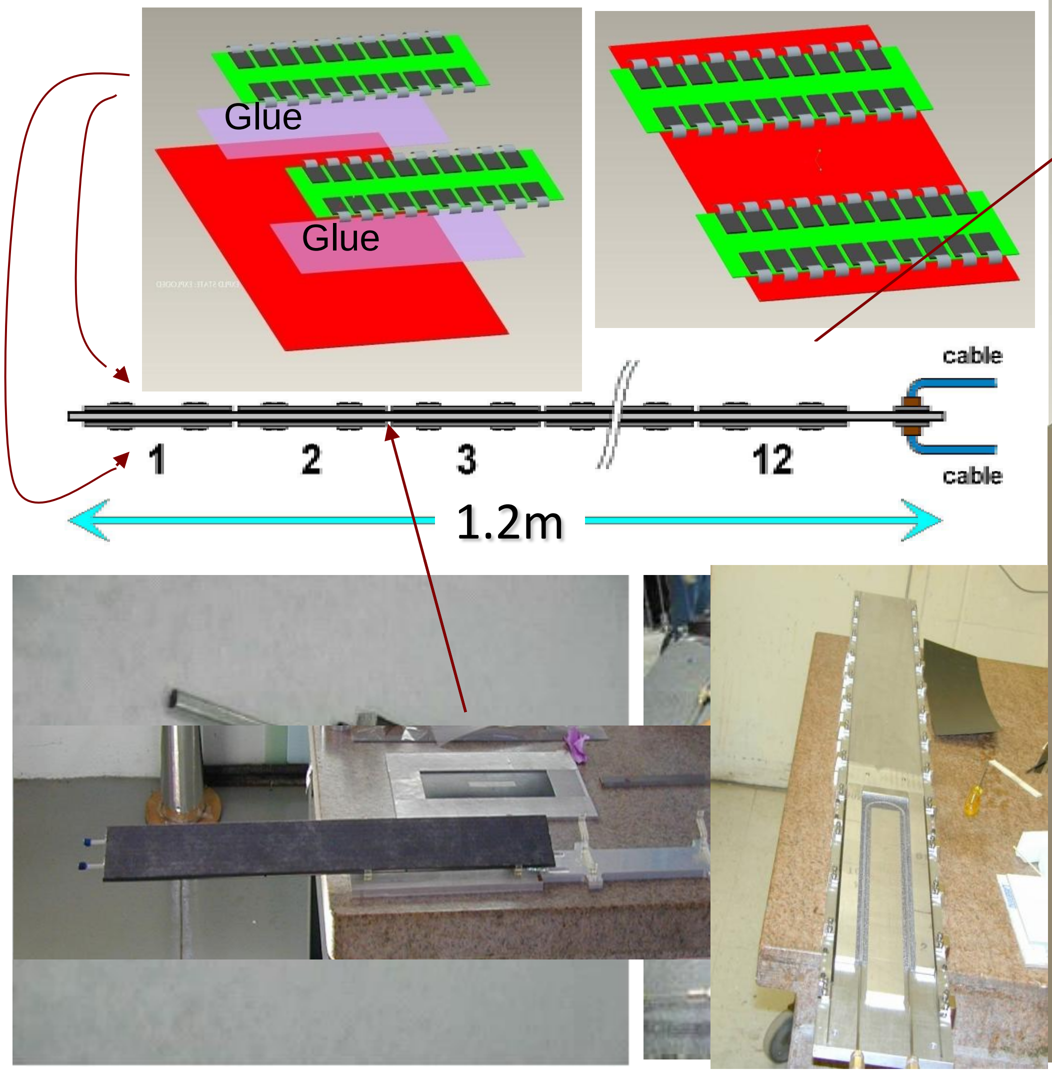


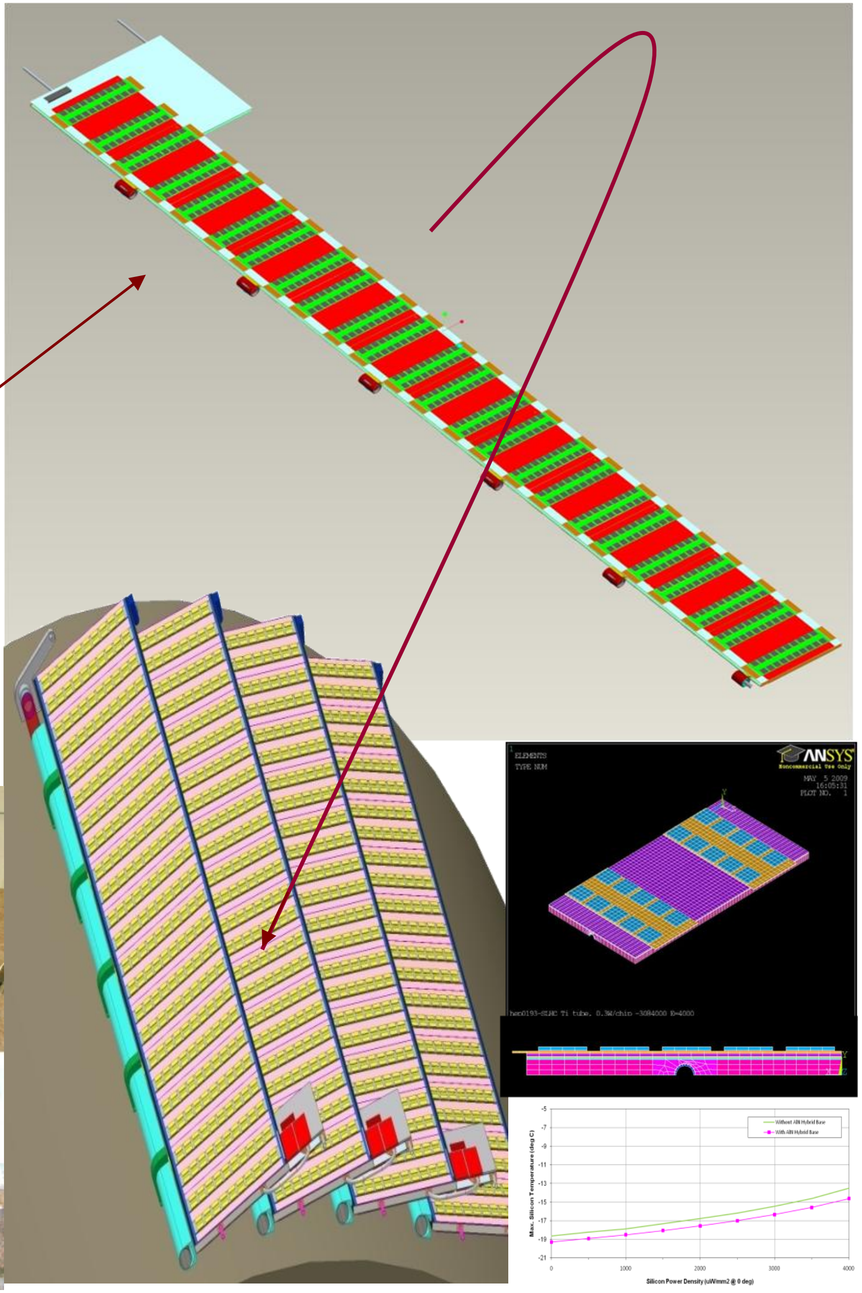






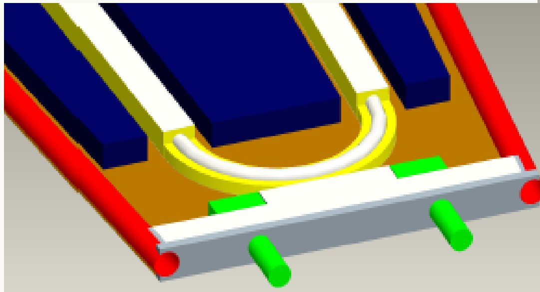
Stave: Hybrids glued to Sensors glued to Bus Tape glued to Cooling Substrate

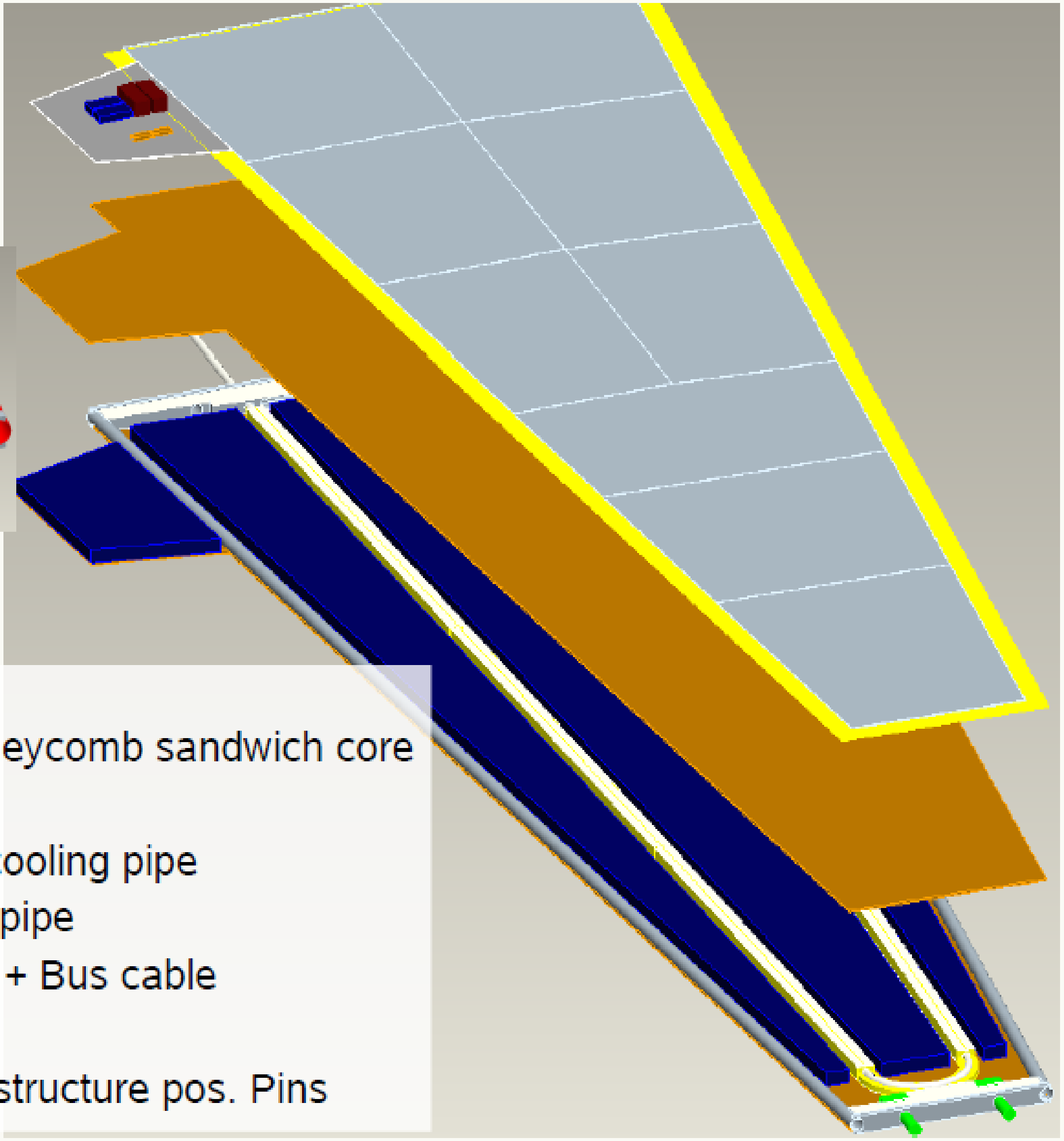




The Petal Concept

- ✓ Follows quite closely the barrel stave concept

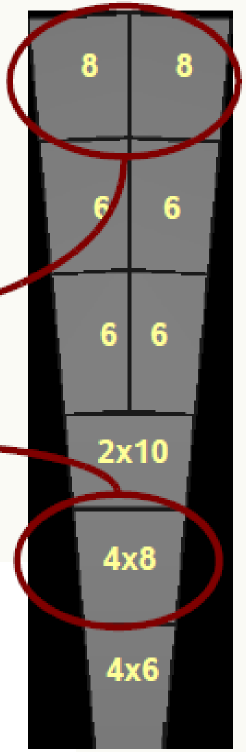


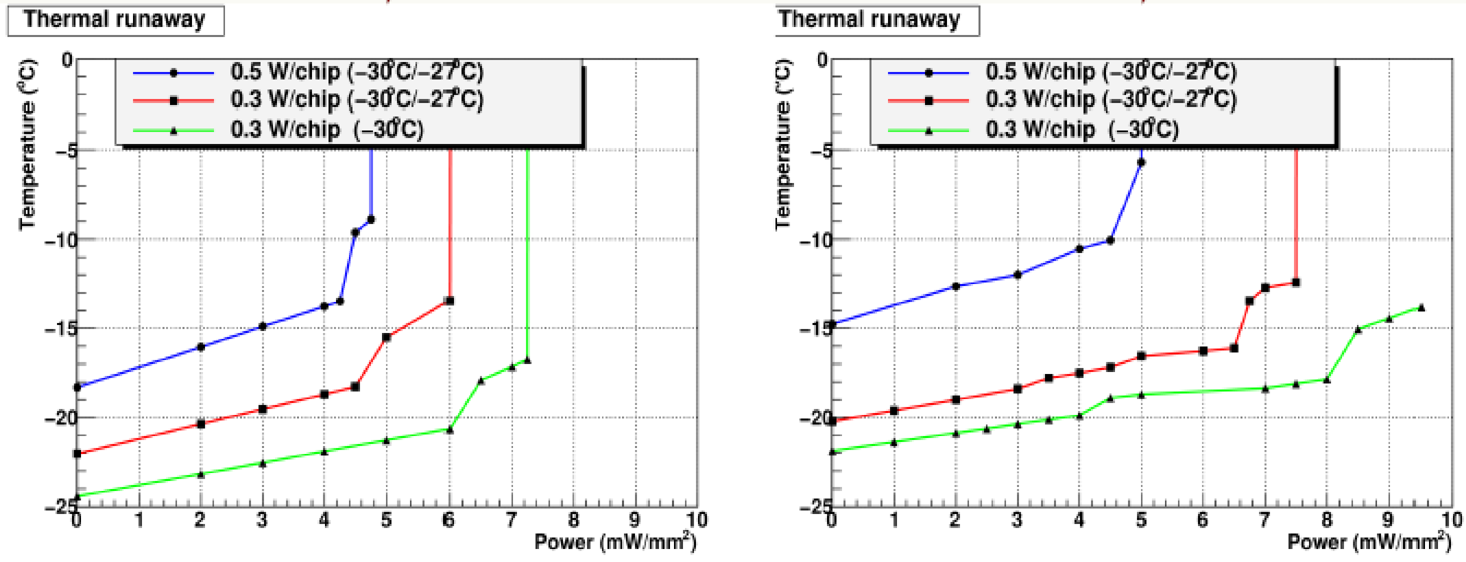


- ✓ 2 Carbon Facings + Honeycomb sandwich core
- ✓ CF tubes on sides
- ✓ Independent SS - CO2 cooling pipe
- ✓ POCOFoam around SS pipe
- ✓ Independent e- services + Bus cable
- ✓ Control card on side
- ✓ Top-bottom closeouts + structure pos. Pins

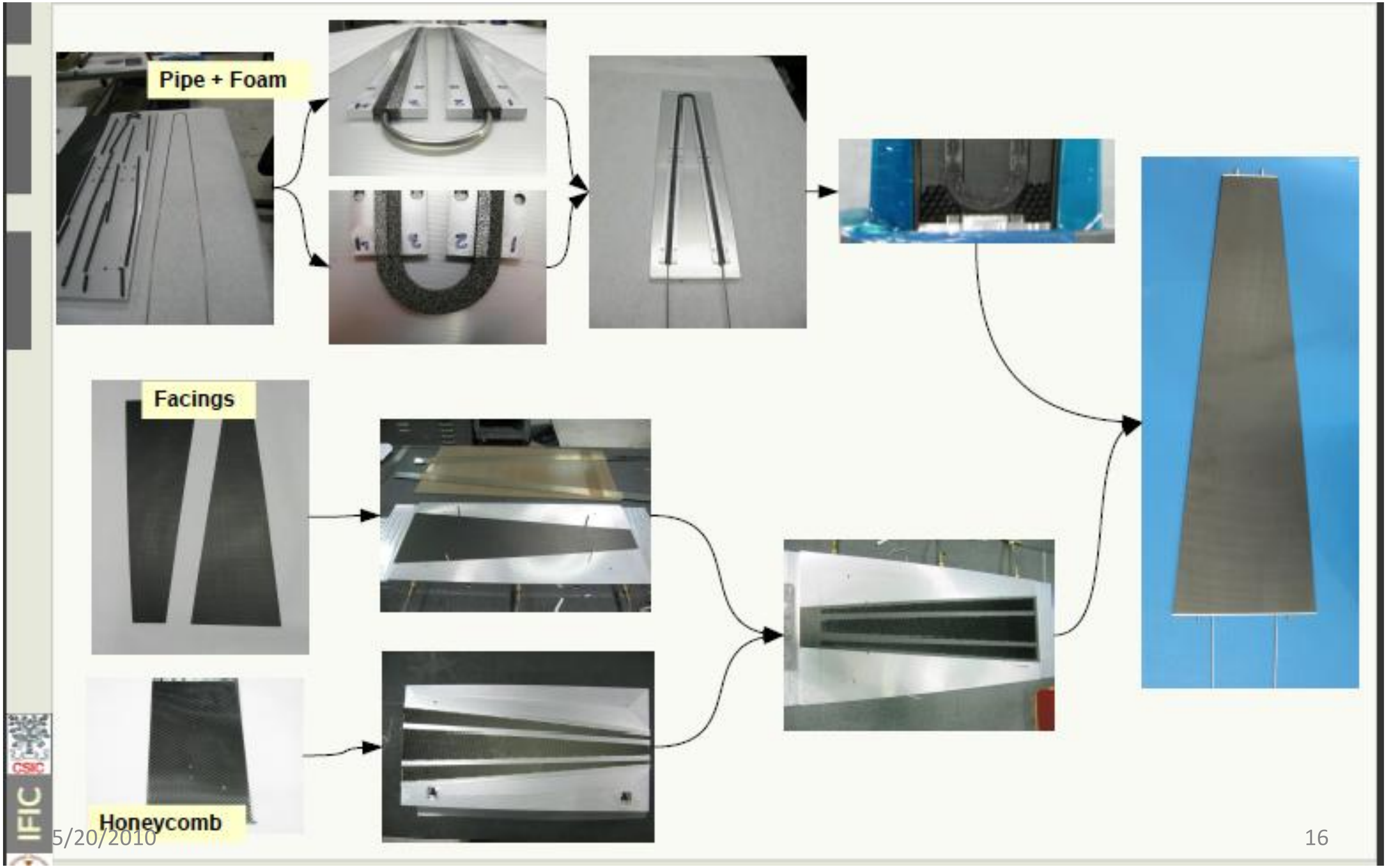
Thermal Runaway

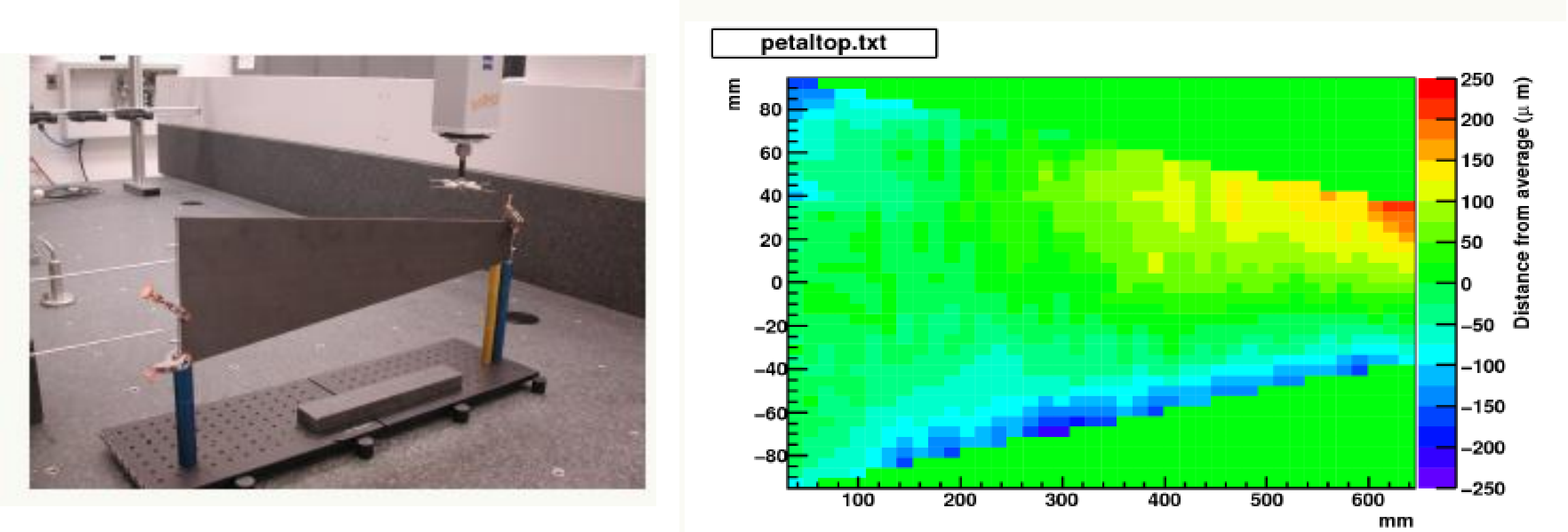
- ✔ Highest temperature on sensor as a function of the power
- ✔ Separation between pipes and chip density are coupled and compensate each other
- ✔ According to simulation we are within safety range
  - ➔ To be verified with prototypes



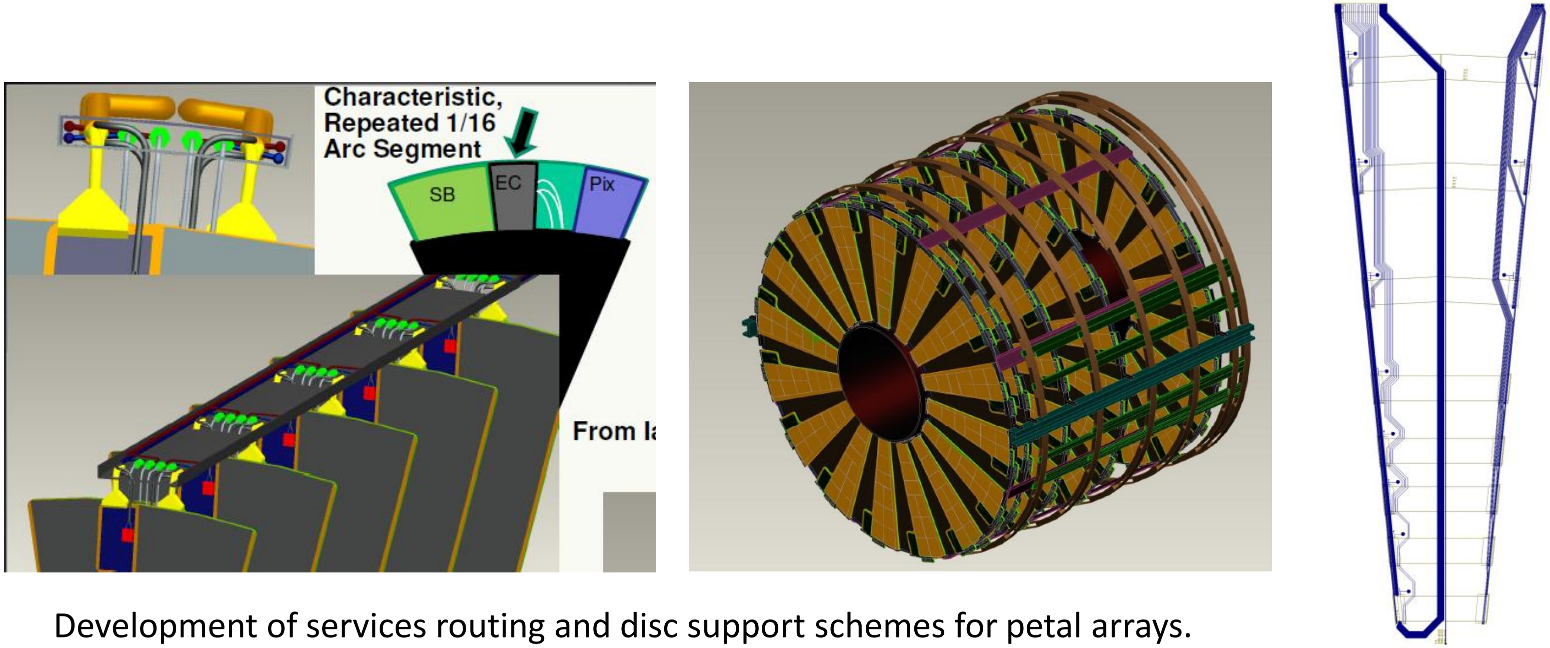


End-cap Petal Core Assembly





Metrology of first petal prototypes. Some twist observed which may be due to the use of 0-90-0 layup. Consider use of a quasi-isotropic layup to address this.



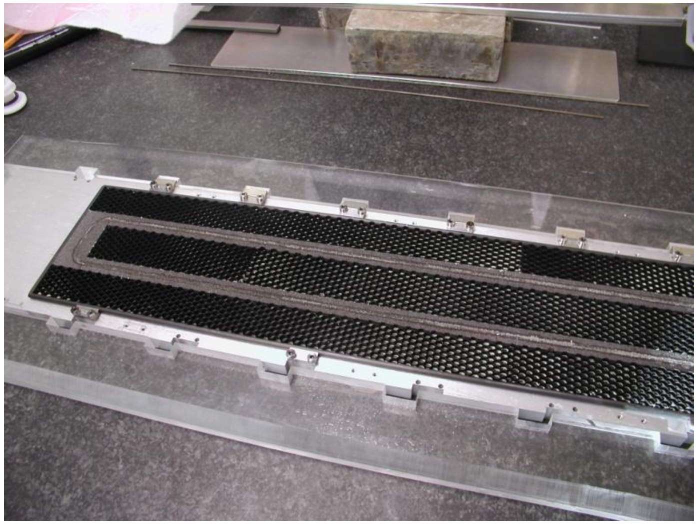
Development of services routing and disc support schemes for petal arrays.

Barrel Stave Core Assembly

Completed tube-foam subassy

Bottom facing with CF tubes, closeouts and BN loaded Hysol ready for tube-foam subassy.

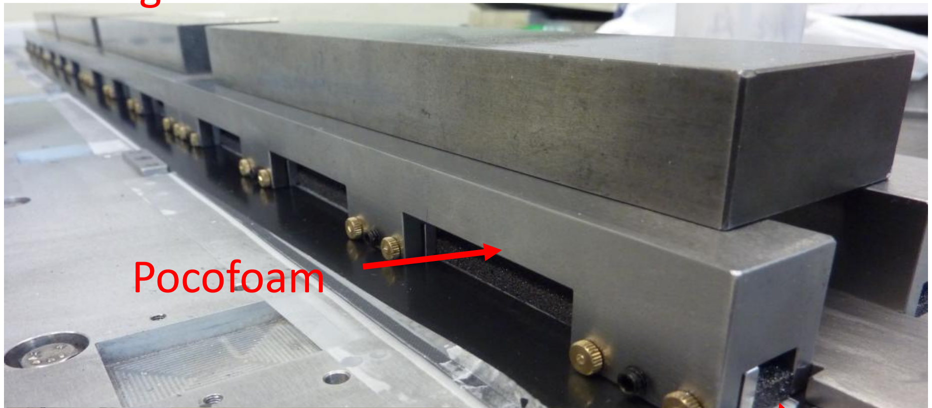
Bottom facing/tube-foam ready for vacuum bagging

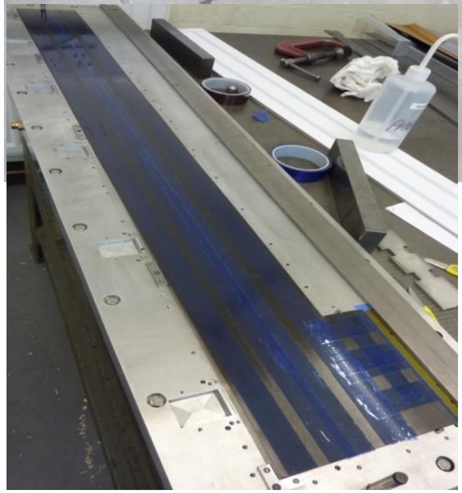


CF honeycomb placed; ready for next vac. bagging

Full-length Thermal Prototype

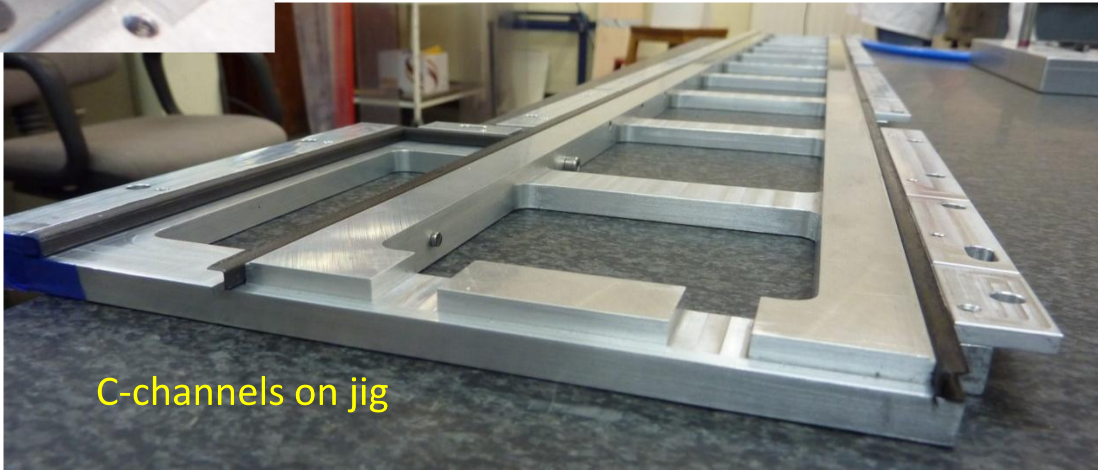
Gluing Pocofoam on Skin





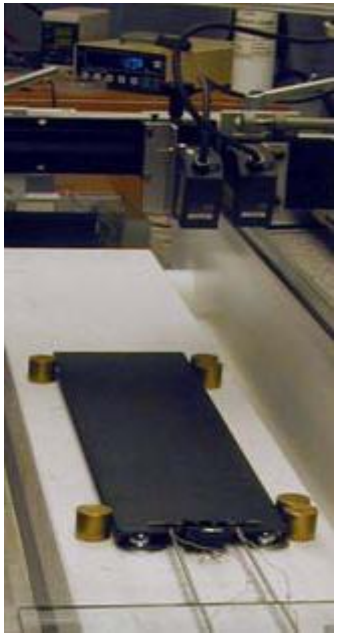
Masking for Pocofoam glue application

Grinding grooves for cooling pipe



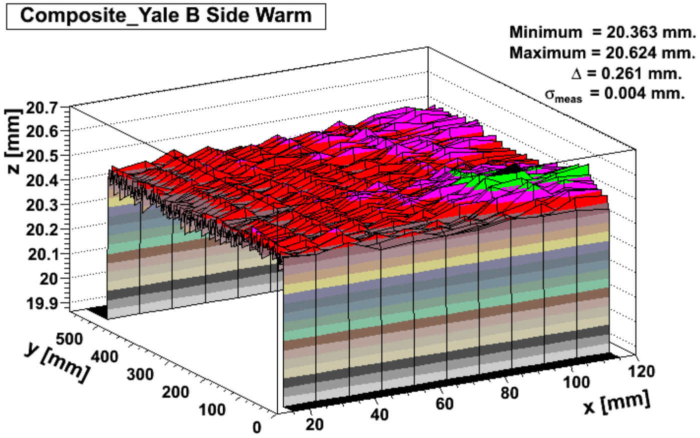
C-channels on jig

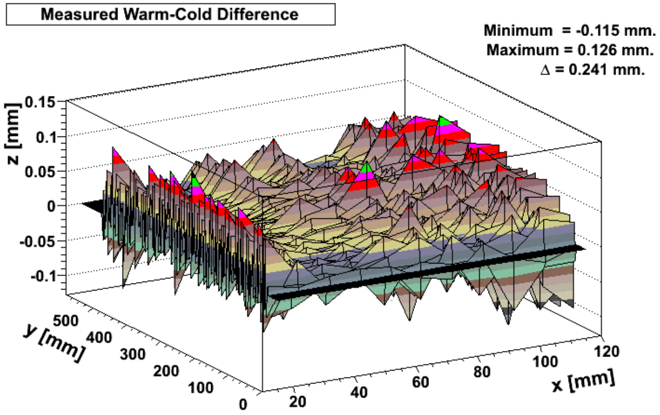
Stave Metrology

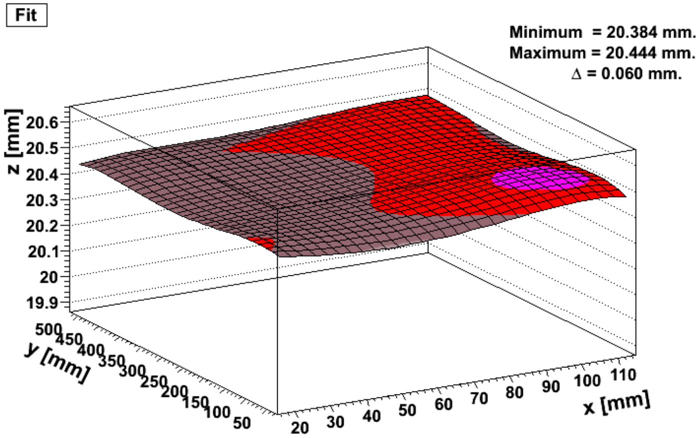


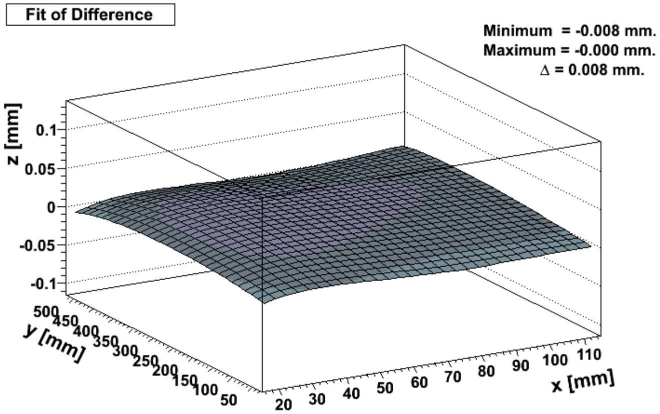
Warm/Cold
Laser scanner

Cold Inlet Temperature: -33^{o}C









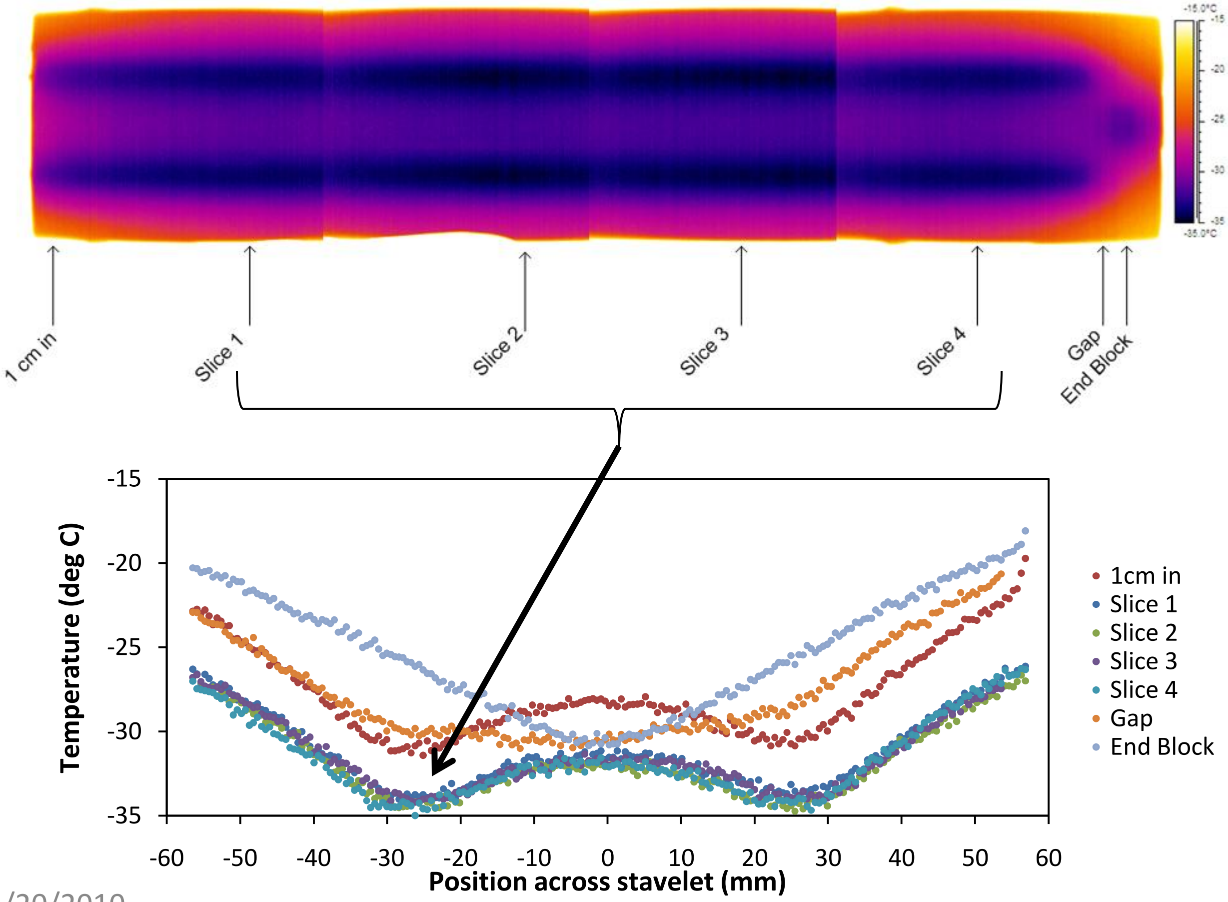
BNL-Yale

Warm: Inlet Temperature: 21^{o}C

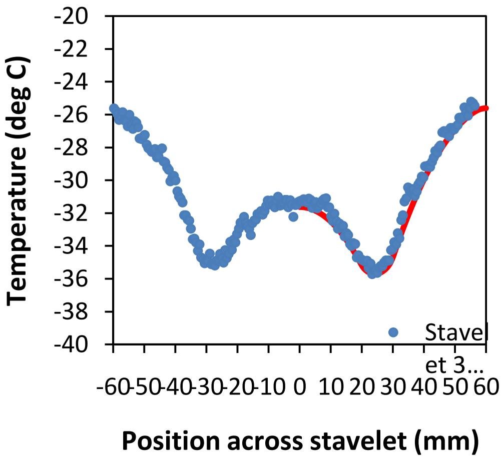
Warm – Cold ($\Delta T=54^{o}$C)
No significant distortion

Stavelet Thermal Performance

- 2 stavelets run for several hours with CO2, in test chamber held at +20C (~60W into stave)
- Thermal imaging camera used to check for temperature non-uniformity which could indicate core/facesheet adhesion failure.

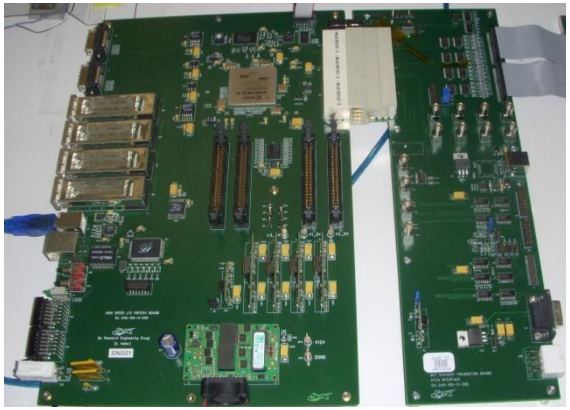


FEA see b/u

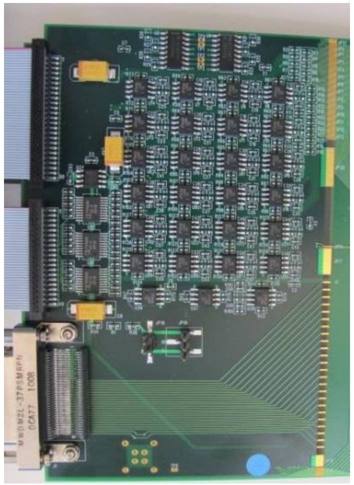


Full Stave Readout and Control Chain

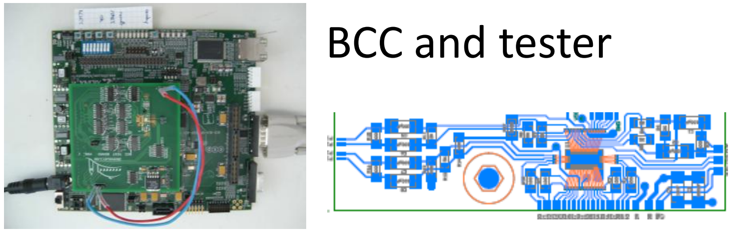
BNL
SLAC, LBNL
Oxford, RAL
UCL, Cambridge



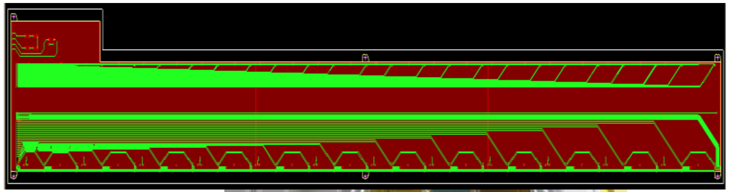
HSIO + interface



End of Stave



BCC and tester



Bus

Serial Power Protection

- A key goal of the stave programme is the development of a full scale readout and control chain, all components are delivered
- HSIO provides hard/firm/software for control, r/o, & analysis of the full stave load
- End-of-Stave provides interface, buffering, and temperature monitoring
- Bus Cable is a 1.3 m long low mass Cu-Kapton-Al fine pitch interconnection
- BCChip supports full multi-drop, parallel command, and multiplexed data out
- Serial Power Protection provides fast auto control and slow interface

SLAC-UCL-Cambridge
RAL-LBNL

HSIO/BCC Development

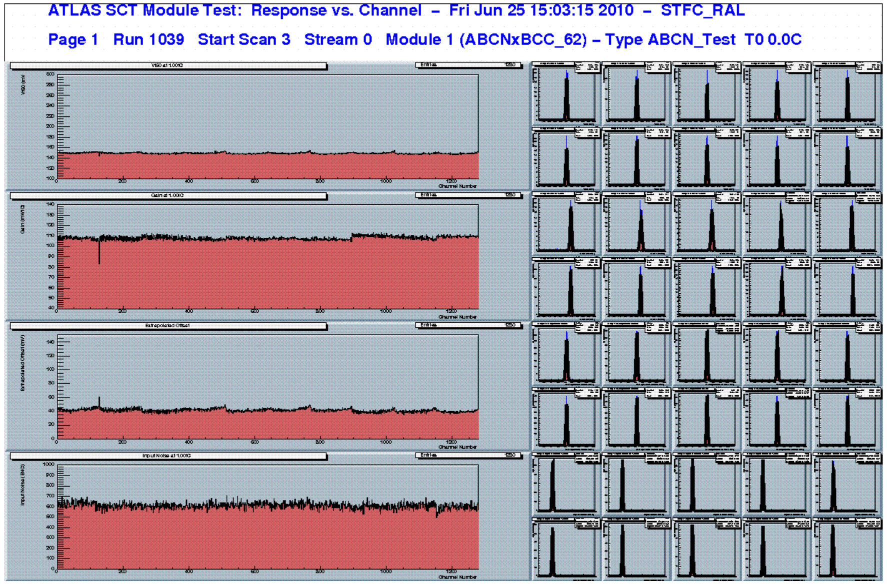
- HSIO Hardware +Firmware
  - Communication over fibre or copper Ethernet. Receives packets from host, sends to “module”. Receives data from “module”, demultiplex, can histogram, send to host
  - Programmed to run ABCn-25
- SCTDAQ Software = Scan control, histogramming and analysis
- 80 MHz data clock, generated from 40 MHz BCO by BCC, fully read out
- We were able not only to read out the module with BCC V2 using 80 MHz dclk, but also to set the strobe delay, to trim it, and to record good quality 3PG results.
- Module operating conditions:

  HV from SCTHV 100V 20uA (also ran up to 220V)

  LV from Jan Stastny’s (Prague) current source for serial powering operation

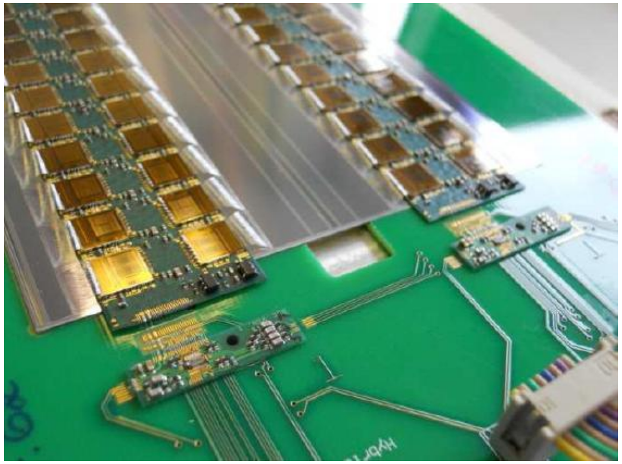
  I = 5A (also ran with 4.5 and 5.5A)

  Hybrid temperature 22C



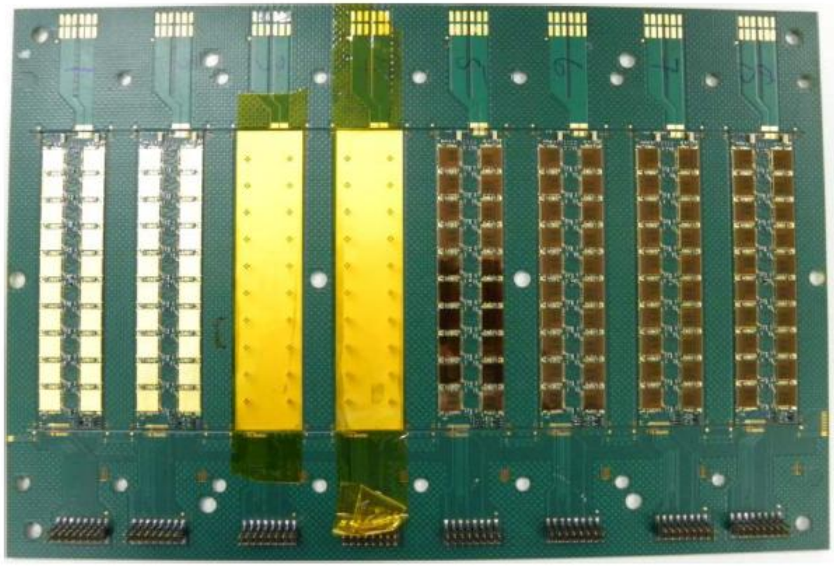
ATLAS SCT Module Test: Response vs. Channel – Fri Jun 25 15:03:15 2010 – STFC_RAL

Page 1 Run 1039 Start Scan 3 Stream 0 Module 1 (ABCNxBCC_62) – Type ABCN_Test T0 0.0C



Barrel Hybrids and their features

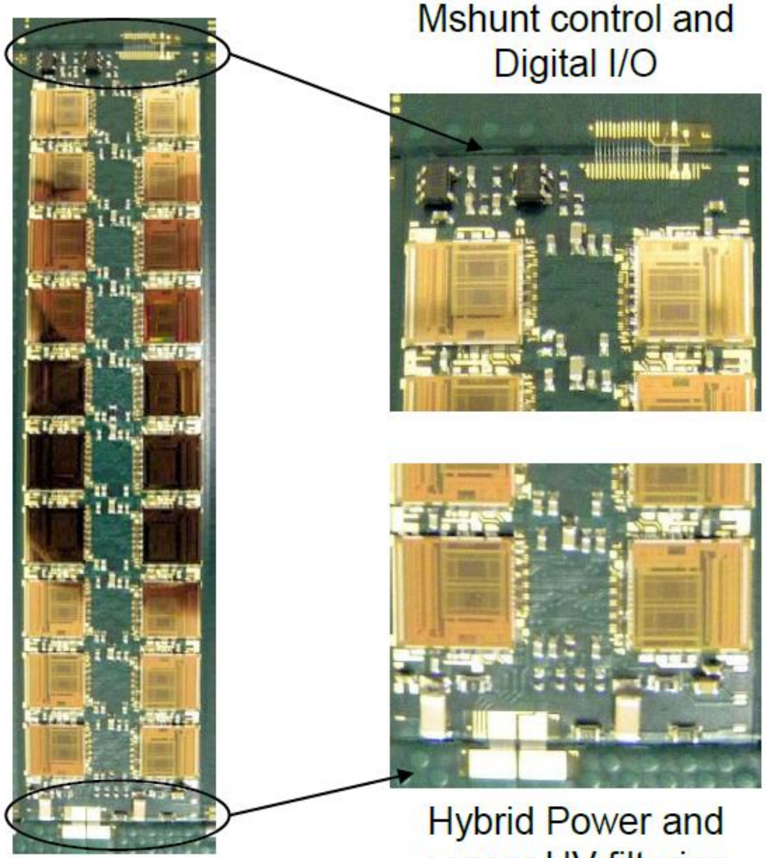
- Hybrids are designed to come on a panel (8 per panel) – first steps towards industrialisation
- Designed for machine placement and solder re-flow of passive components (capacitors, resistors, etc.)



- Panel dimensions: 300mm x 200mm
    - Hybrid dimensions: 24mm x 107.6mm

- Hybrids + ASICs are electrically tested on panel
    - With final ASIC set (ABCnext, MCC, power), we could test all hybrids in the panel with one connection for data I/O and two for SP power chain

- Finally, substrate-less hybrids are then picked out of panel with vacuum-jigging for module attachment



Mshunt control and Digital I/O

Hybrid Power and sensor HV filtering (spec'd to 500V)

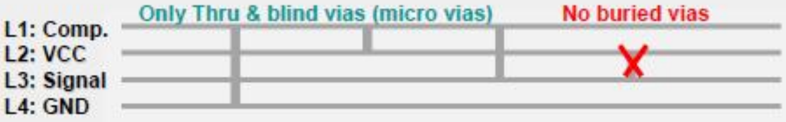
FR proto-type EndCap Hybrid

We Received a batch of 23 (E-tested good) Hybrids about 5 weeks ago from Würth Elektronik:

Overall Yield ~ 85% (still about 20 E-tested good Hybrids in the company)
First crude visual inspection (one PCB only) looks ok! No visible irregularities/defects or the like.

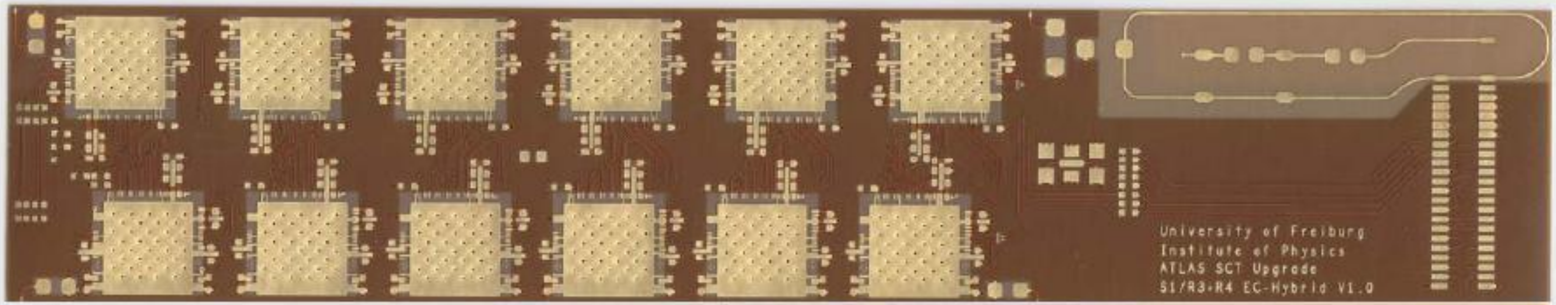
For Reference: PCB characteristics: 4-Layer Flex-PCB
Photosensitive dry film (brownish) Coverlay
adhesiveless single/double-sided ED Copper-Clad all-Polyimide Laminate
Sheet Adhesive: Acrylic
Surface finish: Electroless Nickel Immersion Gold (Ni/Au)

track width/separations	*95μ/95μ {nominal 100μ/100μ (4mil)}*
Microvia: Drill/Pad	*100μ/300μ (L1-L2)*
	125μ/350μ (L1-L3)
	250μ/500μ (L1-L4)

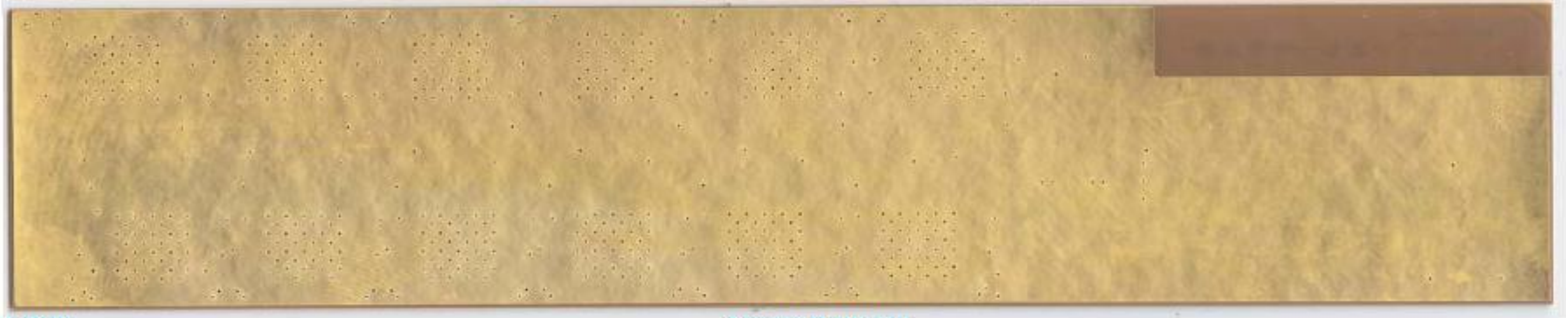


Hybrid Dimensions/Weight: 130mmx25.5mm, 2.5g

Top view

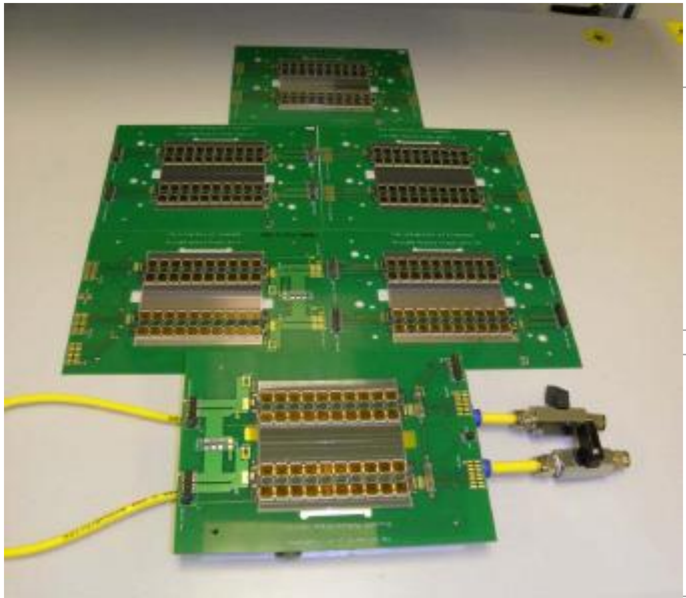


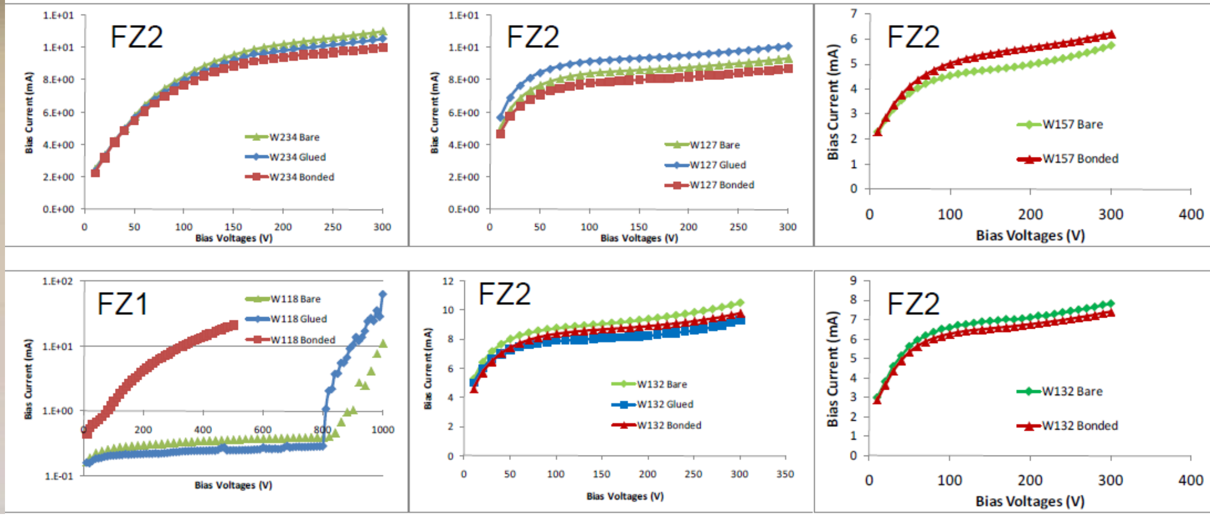
Bottom view



Single-sided Module Programme

(9 modules now assembled)

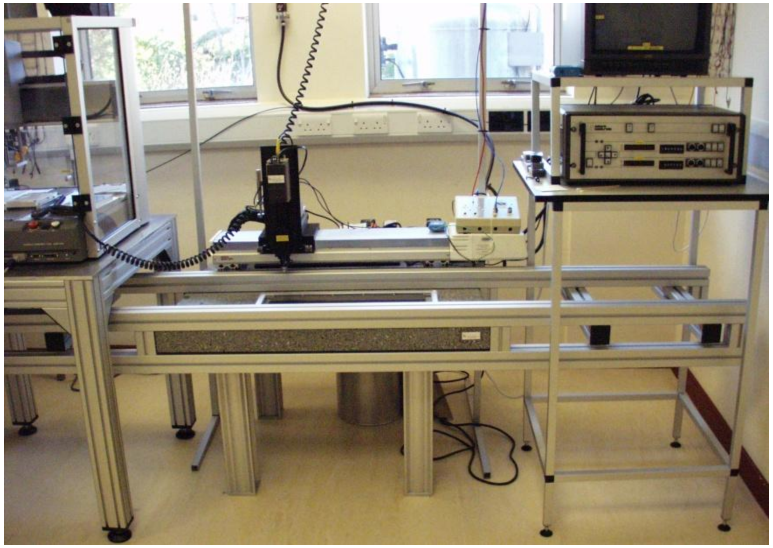


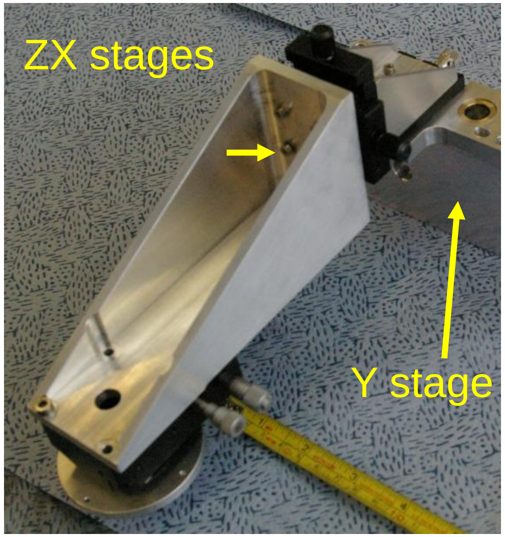


- Single-sided module programme with substrateless hybrids glued directly to sensors
- Hybrids produced with 100% yeild (2 runs)
- Large area sensor with bare hybrid under irradiation at PS (sensor strips wire bonded)
- Sensor behaviour does not show problems due to gluing although one module had sensor physically damaged during wire-bonding
- Tooling for mounting to staves at RAL undergoing final tests
- Expect to irradiate fully electrically working module with FZ1 sensor this Summer
- Expect to first construct two (4 module) stavelets
  - One with serial powering
  - One with DC-DC powering

  (Both powering schemes already demonstrated on bench with single-sided modules)
- **Main longer-term goal is to equip the 24 module double-sided stave**

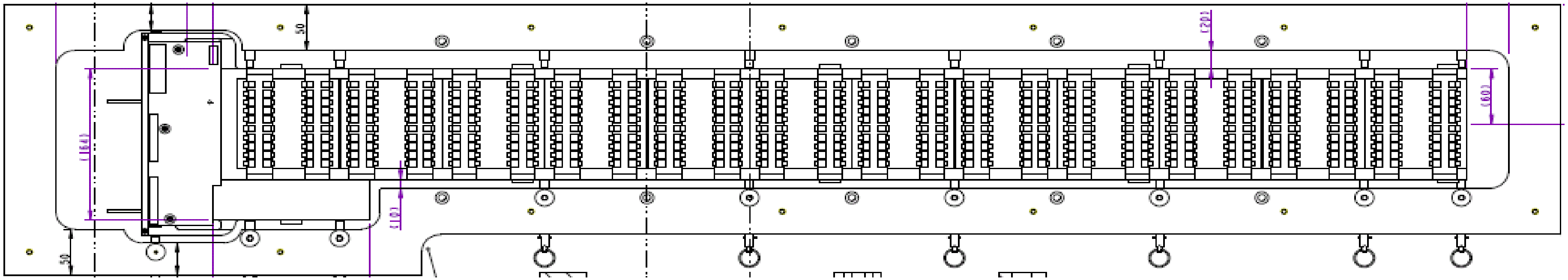
Module Mounting System





Rotate stage

Module mounting frame

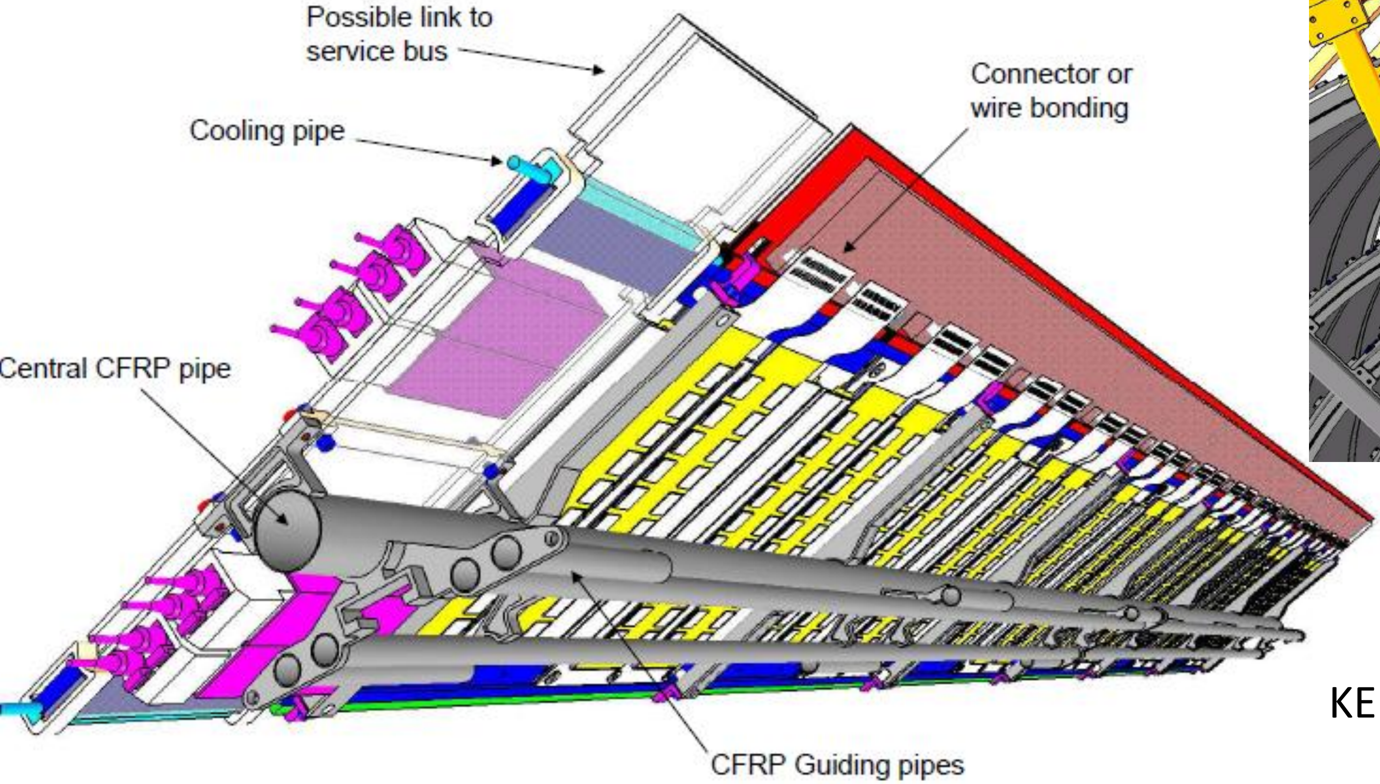


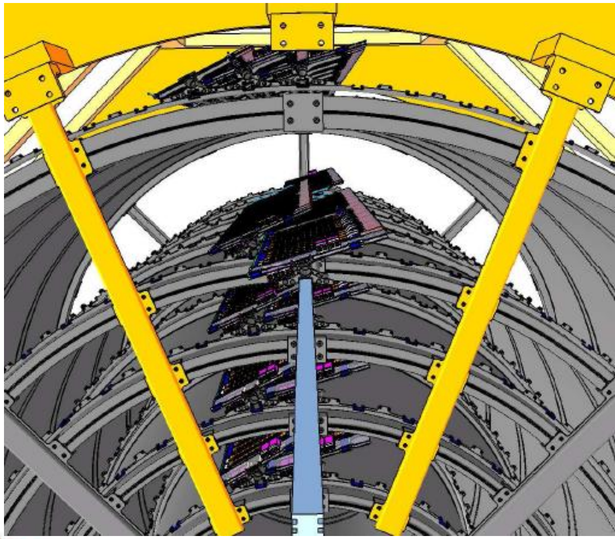
Features of the Strip Super-Module Concept

Key points:

- **Modular concept**. All the parts are decoupled from the module design and are modular. **Assembled and functional modules are built and tested in early stage and will remain as built.**
- **Full module coverage** in Z (shorter barrel structure)
- **Rework** is a strong point of the module concept –Possible up to the commissioning after integration
- **Design includes hybrid bridge** (which could be also glued as for stave modules)
- **Thermal performance show a large safety regarding the thermal runaway**
- End insertion give **flexibility for assembly & rework** - Allows less commissioning steps
- 1m20 or even longer stiff LS allows for **simpler support structure** (compared with SCT)

Super-Module – 12 modules mounted on a local support



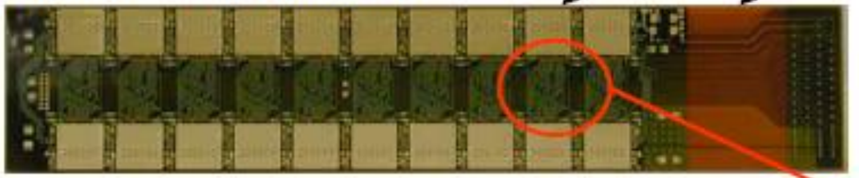


End-insertion illustration on pre-assembled barrel structure

KEK & University of Geneva

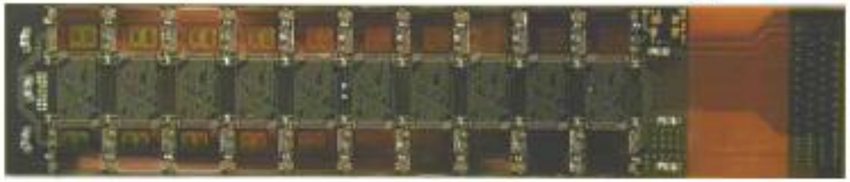
Hybrid Design and Fabrication from Japan

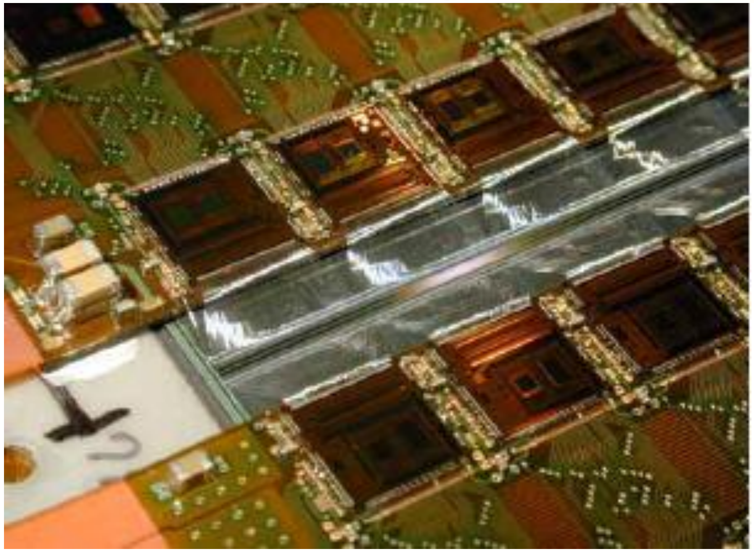
Front side 136mm x 28mm



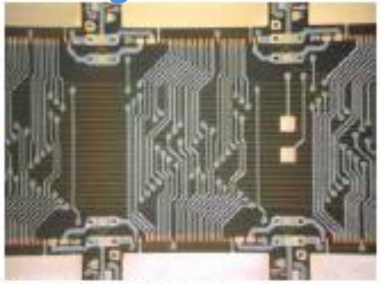
Back side

Hybrid after mounting FE chips, R C components and a 0.8mm pitch miniature connector at the right end.





Design from KEK



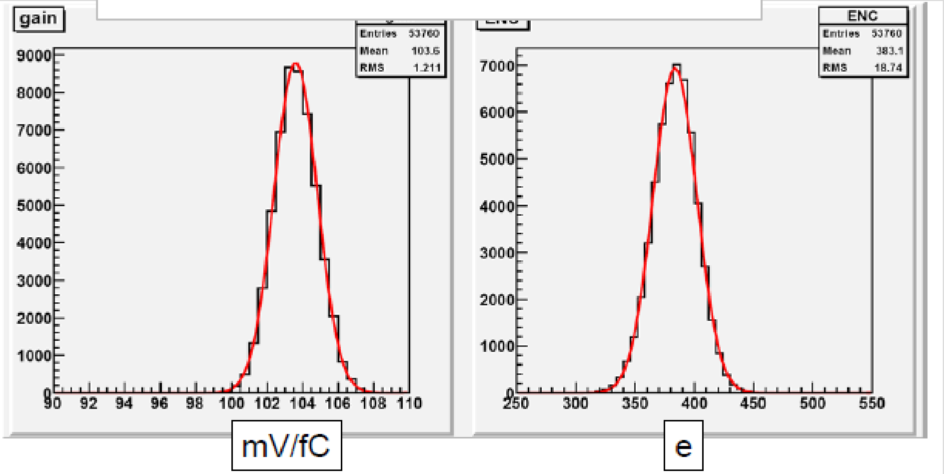
Min. Line Width	0.1mm
Min. Gap	0.09mm
Min. Via-hole	0.1mmΦ
Min. Thr.-hole	0.3mmΦ

Taiyo Industrial Co., LTD

Hybrid with a carbon bridge

FE chip performances as expected:

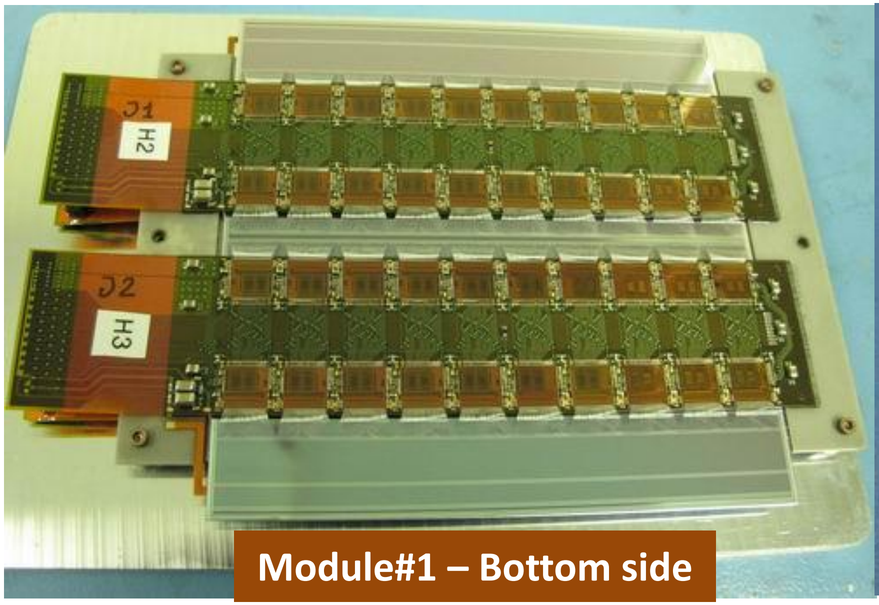
- Gain ~ 100 mV/fc
- Noise ~ 380 e-



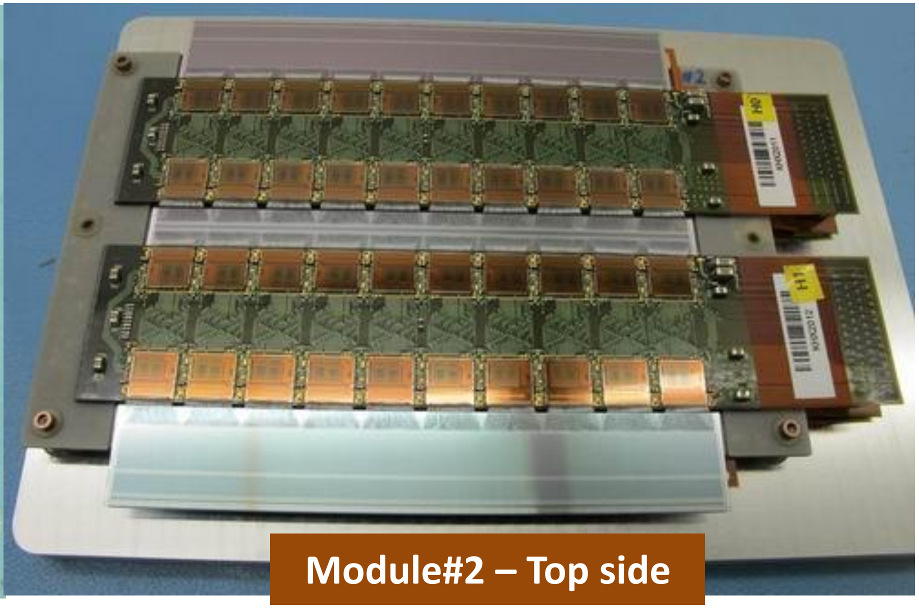
Double-sided Super-Module Assembly Status & Pictures

ID	Assembly & Bonding	Electrical Tests	Location
KEK #0	Completed in Sep 09 (half electrical)	Fully functional – Strip length tests	KEK lab in Japan
KEK #1	Completed in Feb 10	Fully functional – Vcc, Vdd independent	KEK lab in Japan
KEK #2	Completed in Apr 10	Fully functional – Vdd with FE regulator	KEK lab in Japan
UniGe #0	Completed in Oct 09 (half electrical)	Irradiated in Nov 09 Fully functional before & after irradiation	Stored cold in bld 161 lab at CERN
UniGe #1	Completed in Dec 09	Fully functional – Vcc, Vdd independent	Bld. 161 Lab at CERN
UniGe #2	Completed on Apr 10	Fully functional – Vdd with FE regulator	Bld. 161 Lab at CERN
UniGe #4	Completed on Apr 10	Fully functiona l– Vdd with FE regulator	Bld. 161 Lab at CERN

3 to 4 modules will be additionally made in July : 2 at KEK and up to 2 at UniGe



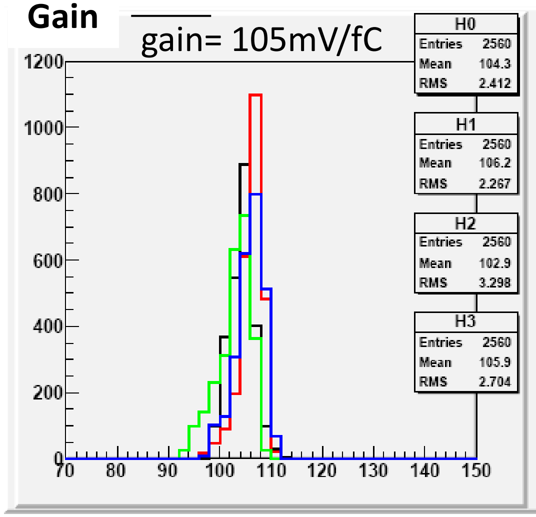
Module#1 – Bottom side

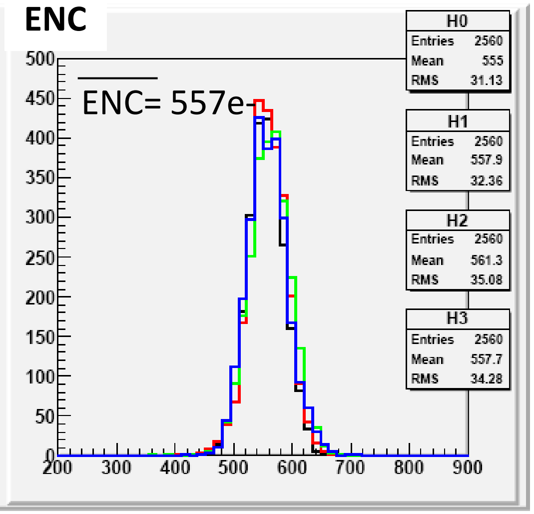


Module#2 – Top side

Double-sided Super-Module Test Results

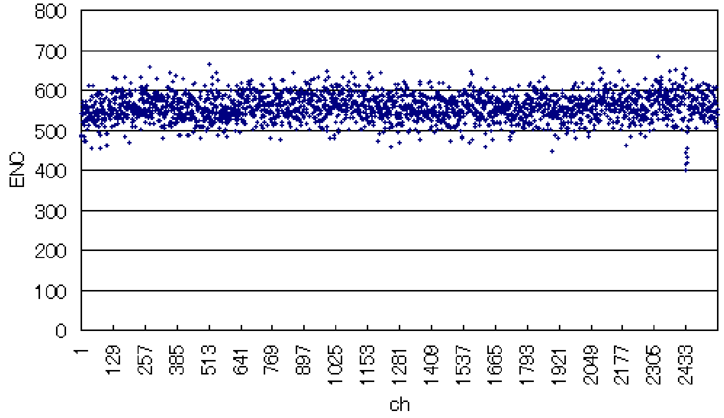
All modules produce so far either at KEK or at UniGe are working with consistent ENC noise of ~570e-
The noise occupancy is below 10^{-7} at 80mV while 1 fC threshold is at ~120mV



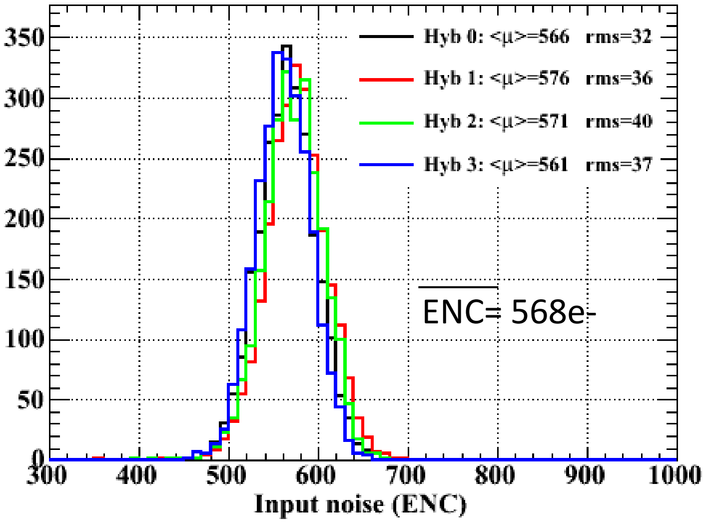


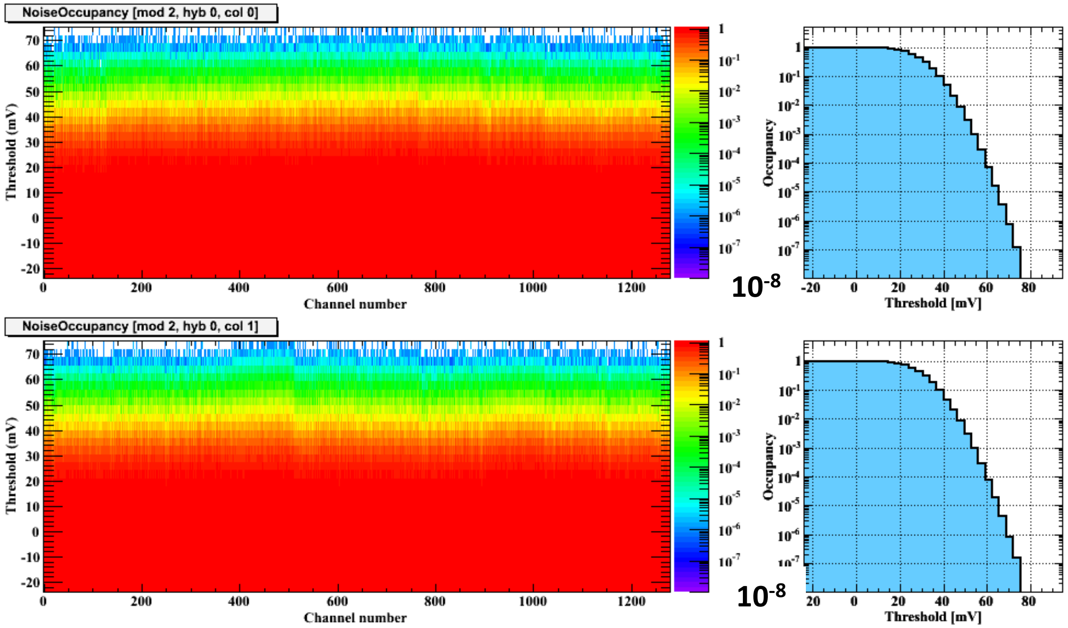
Results from KEK modules

ENC



Results from UniGe modules



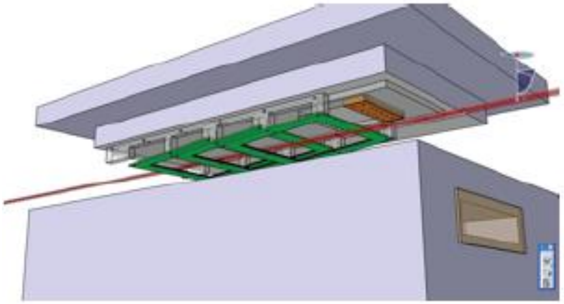


Investigation on the irradiated module

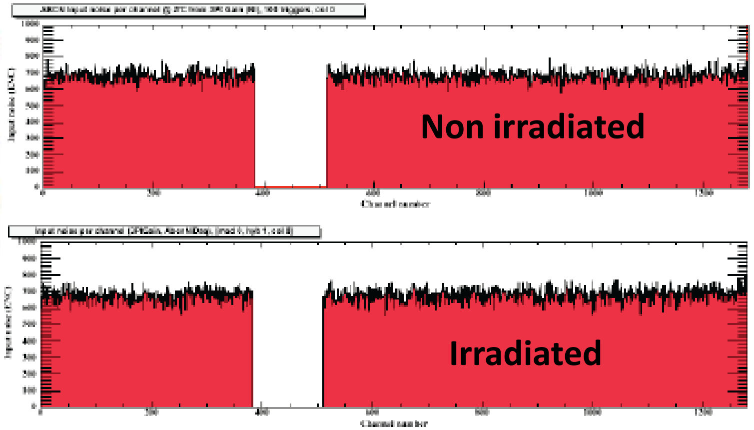
Module irradiated in CERN-PS irradiaton facility in November 2009

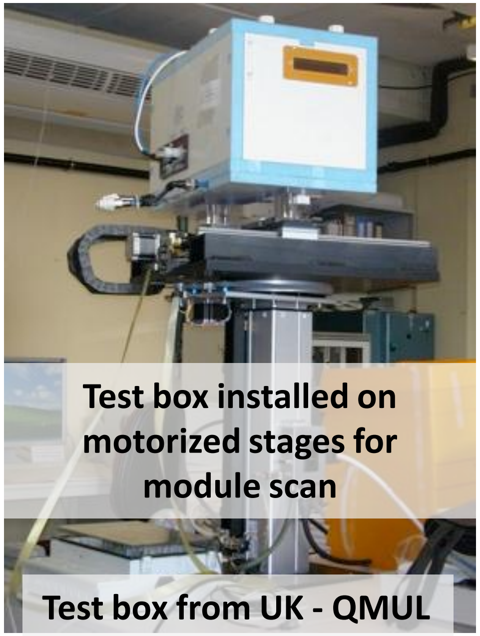
- PS-T7 24 GeV proton beam (~1x1 cm2), flux ~ 1-3x10^{13} p/h/cm2

Module received a fluence of ~5x10^{14} 1MeV n_{eq}



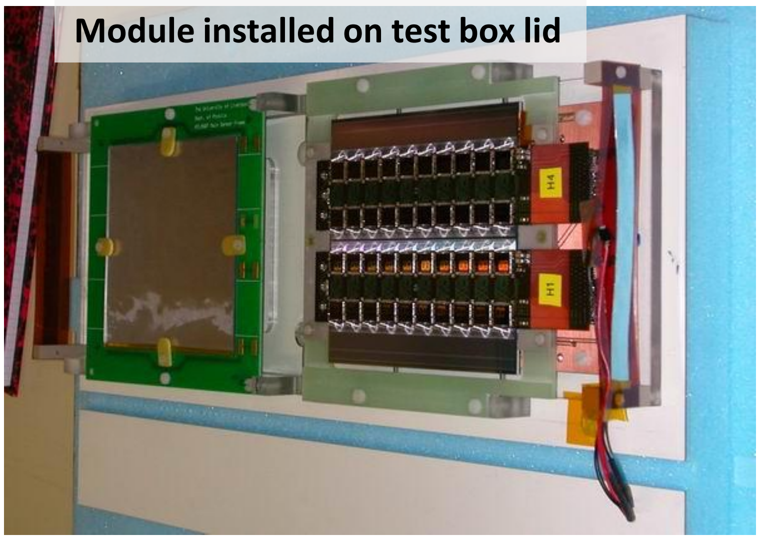
ENC noise invariant before and after irradiation





Test box installed on motorized stages for module scan

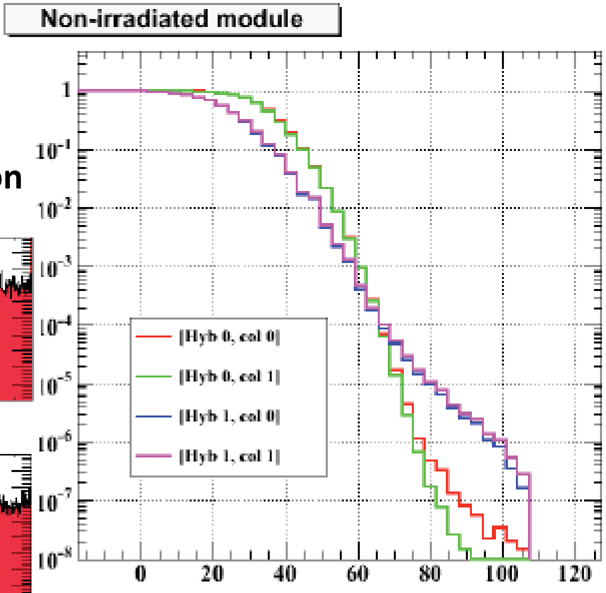
Test box from UK - QMUL

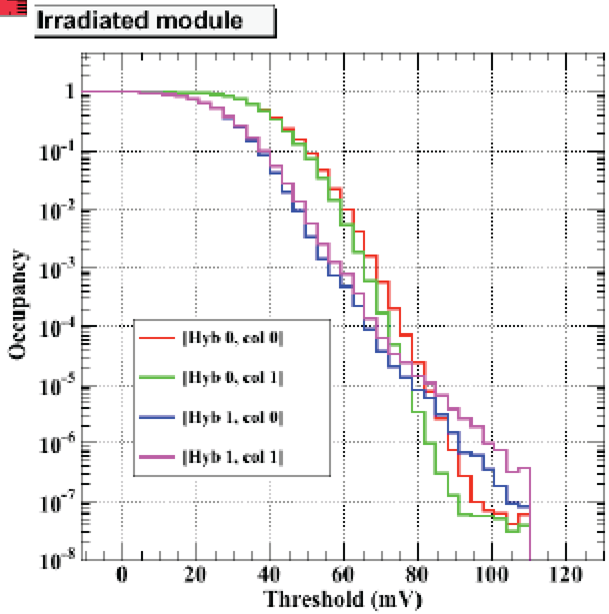


Module installed on test box lid

Noise Occupancy before & after irradiation

→ No significant degradation

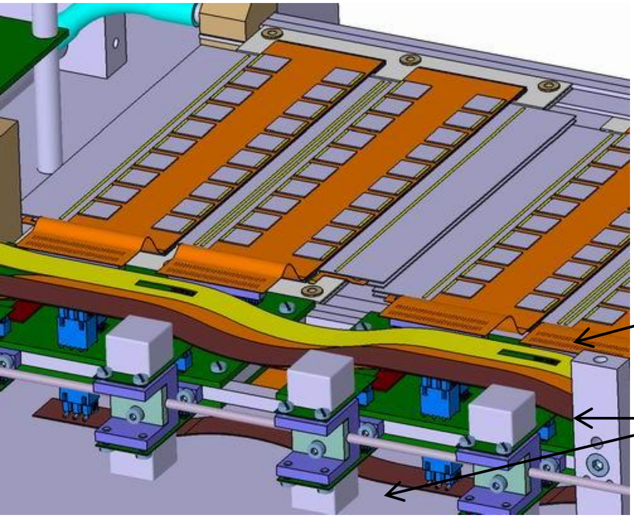




Super-Module Plans

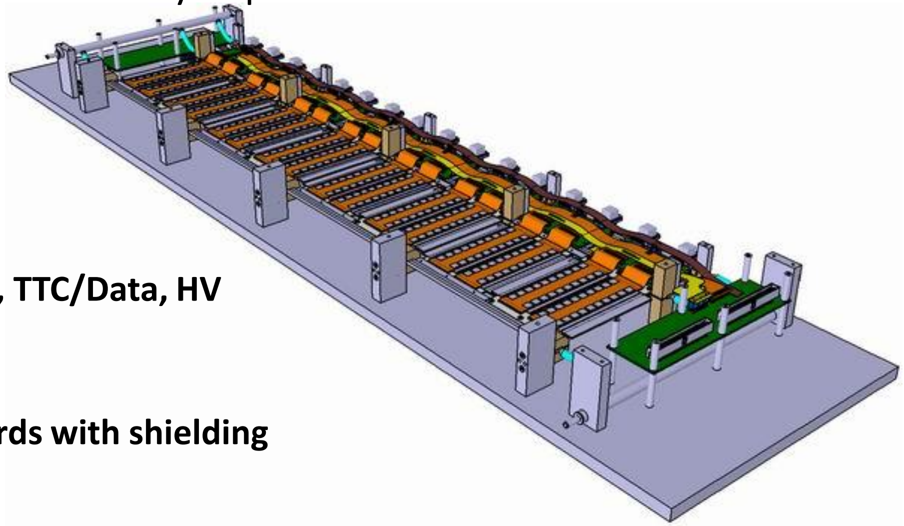
Target is to test the 8 modules together on a realistic support before end of 2010:

- Design and fabrication of **the service bus** that include connectivity for the BCC chips
- Include **adaptation of powering schemes** DC-DC plug and Serial Powering
- **DAQ** to be used and adapted **with the HSIO sets and BCC** (from US & UK) and still to be supplied
- **Cooling** to be used: **water, CO2 or C3F8**
- Ideally compatible for **stave and super-module DAQ readout** in a same testing place at CERN
- **A 12 module local support will be constructed** which will fully implement the mechanical features

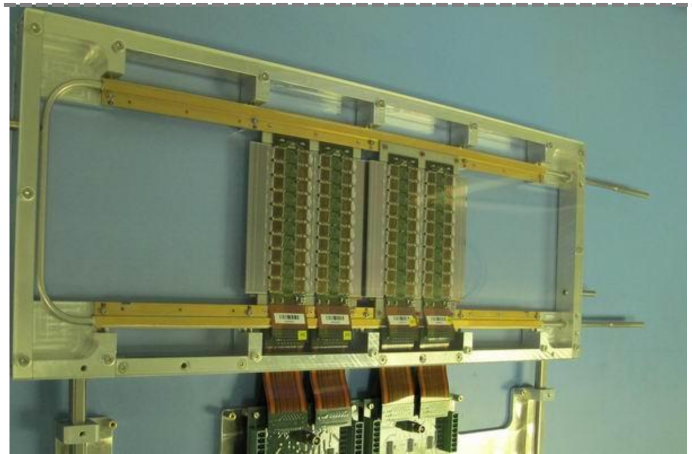


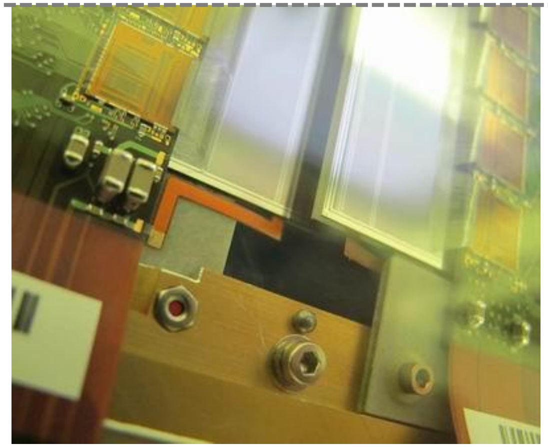
3 service buses: LV, TTC/Data, HV

DC-DC plug-in boards with shielding



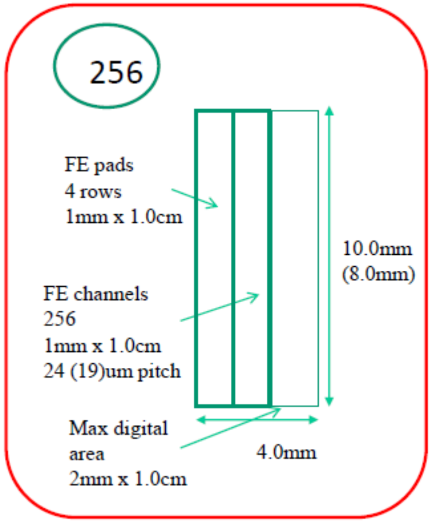
Meanwhile the 4 module test box should help for the combined test and noise configuration with DC-DC





New ASIC (ABCN130) Read-Out Design

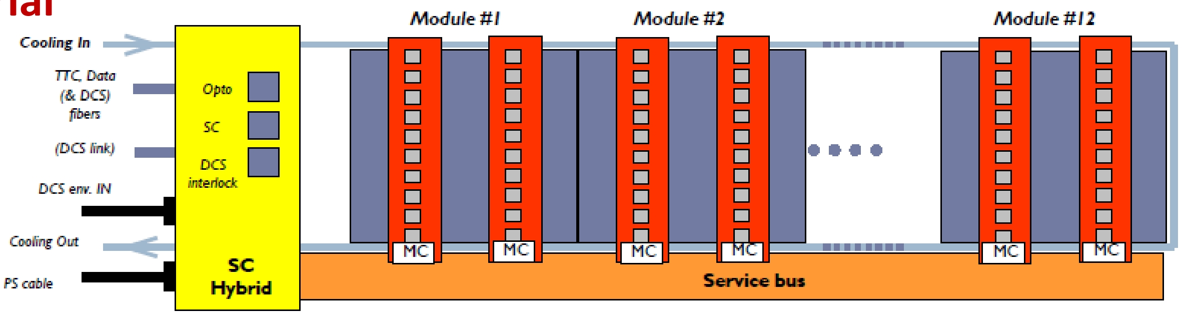
Major further reduction in material



- Gain 100mV/fC
- Peaking time 22ns (intrinsic)
- Detector capacitance 5 to 10pF
- ENC < 800e- at 5pF & 600nA leakage for 100µA input transistor current
- Input transistor bias; 80 to 160 µA
- Linear range 0 to 6fC
- Power consumption; Iinput + 80 µA (180 µA for nominal conditions)
- Power supply 1.2 to 1.5V
- Channel dimension 22µm x 700 µm

~140mW per 256 channel chip

Readout architecture with 256-channel FEIC



- Readout hybrids with 256-channel FEIC (ABCnext) and a module controller (MC)
- Assuming a binary readout as for the current SCT and a 100kHz L1A rate data volume requires extracting the data
  - @160Mbps from a readout hybrid (including a comfortable x2 safety factor)
  - @80Mbps on the hybrid if using two links from the FEICs to the MC
  - @3.8Gbps from a stave
- Includes some safety factor and depends on the data format used and is based on 10^{35}cm^{-2}.s^{-1}

Conclusions

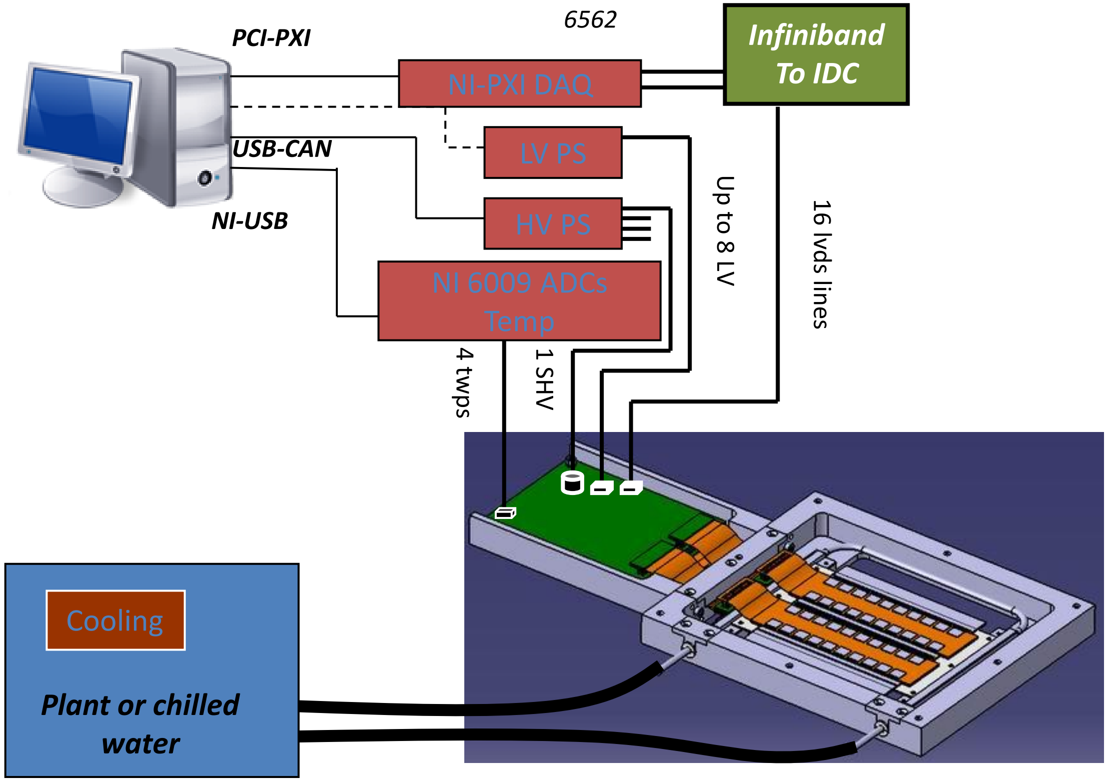
- Phase-II pixel programme benefitting from IBL activity but is now offering some very neat solutions for the full tracker upgrade
- Radiation issues at 3000fb^{-1} becoming close to manageable at all radii but work needed on understanding the (highly quenched) charge multiplication
- Good performance large area sensors being manufactured by Hamamatsu
- 40 chip modules demonstrated on both bridged and bare kapton that work well. Module being used for ASIC and DAQ studies and to check noise with different powering schemes.
- Tooling for first substrate-less hybrid modules developed successfully
- Corresponding hybrid for forward modules constructed and being evaluated
- Tooling for assembly of modules to first prototype short staves (stavelets) prepared and first stavelets substrates manufactured and being evaluated
- Programme of sensors for forward modules and forward prototyping needs further effort but DESY's participation is a big boost
- Good experience with super-module irradiation and complementary programme of hybrid, support and module development
- R&D programme is progressing well and is reasonably compatible with the latest machine schedules (but time is still really tight)

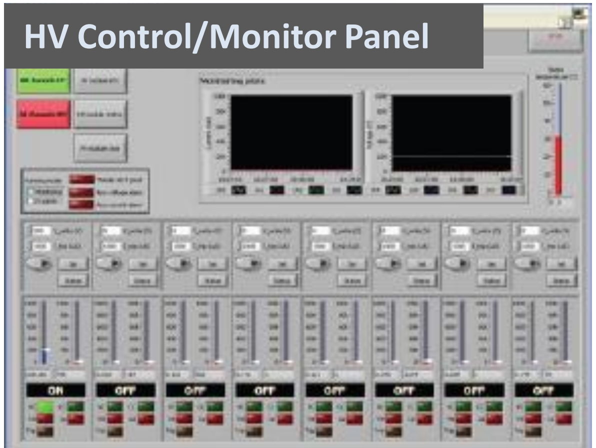
Backup

Module Test Set-up

Test System with NI-DAQ (Fully functional)

- **NI PXI-6562 X 4 cards**
  - 16 channel digital WF generator/analyzer
  - 200/400 Mbps per channel SDR/DDR
  - LVDS signals, per-channel direction controle
- **iSeg high-precision 6U PS card**
  - VME crate, USB CAN controller
  - 8 channels/card, V_{nom}=1000V, I_{nom}=8mA
  - Fully controlled and monitored
- **LV laboratory power supply**
- **Temperature readout with ADC NI-6009**
- **Software**
  - LabVIEW 8.6
  - configuration files through XML
  - Software on SVN repository




HV Control/Monitor Panel

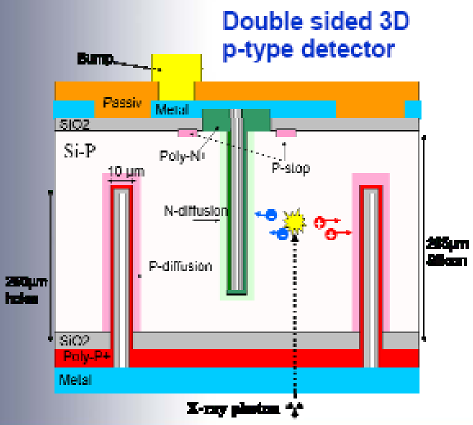
- ➢ **Working DAQ systems at KEK , CERN & Krakow**
- ➢ ***Can be used for single chip, single hybrid, module test and up to 4 combined module tests***

Tentative Schedule

Milestone	**Date**
Straw Man & options fixed	Dec 2006
R&D towards inner detector conceptual design	2007-2011
Letter of Intent	Dec 2010
Technical Proposal, Initial MoU and Costing	April 2013
New Insertable B-layer Installation	End 2014
Inner Tracker TDR	Dec 2014
Production readiness reviews and ramp up production	2015
Procure parts, Component assembly	2015 - 2017
Surface assembly	September 2017 - end 2018
Surface testing	2019
LHC stop for accelerator upgrade	Dec 2019
Remove old detectors, install new ones	Jan 2020 - Mar 2021
Commission new detectors	Apr 2021 - Jun 2021
Take data	July 2021

Table from: http://atlas.web.cern.ch/Atlas/GROUPS/UPGRADES/

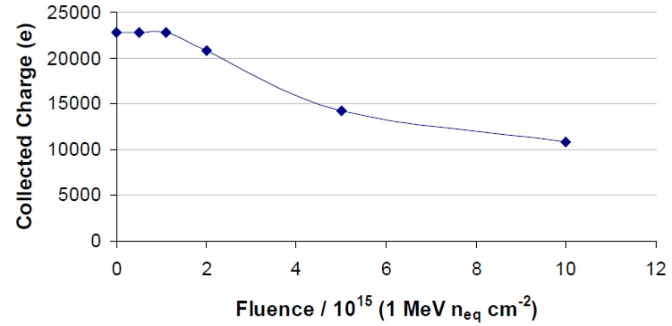
CNM double-sided 3D detectors



- Array of electrode columns passing through substrate
- Electrode spacing << wafer thickness (e.g. 30µm:300µm)
- Benefits:
  - Low full depletion voltage
  - Fast collection times → Reduced charge trapping
  - Reduced charge sharing due to E-field shape → Higher signal in one pixel
- More complicated fabrication - micromachining

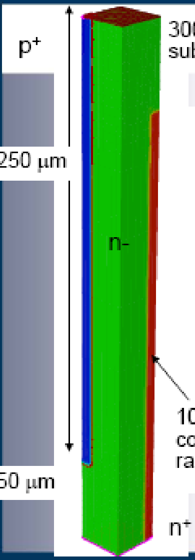
Collected charge for irradiated devices

Electron collecting strip detectors



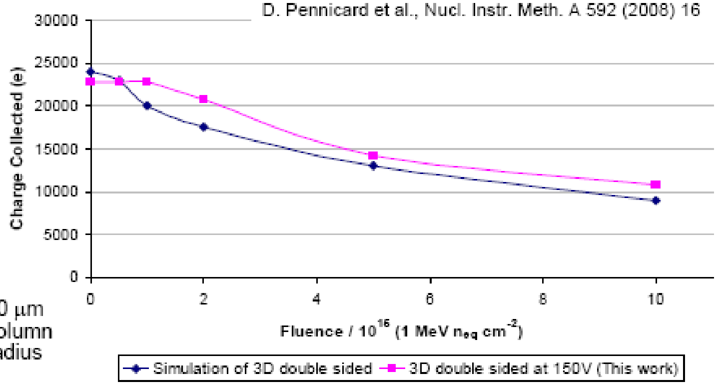
- Bias Voltage fixed at 150V for all irradiated samples
- Non-irradiated sample biased at 18V
- Detector's ceramic based board temperature between -10°C to -15°C

Simulation – ISE TCAD



Charge collection simulation

D. Pennicard et al., IEEE Trans. Nucl. Sci. 54, 4 (2007)
D. Pennicard et al., Nucl. Instr. Meth. A 592 (2008) 16



NB – simulation assumes n+ readout for detectors, and 55µm pixels, experimental results have n+ readout and 80µm pixels

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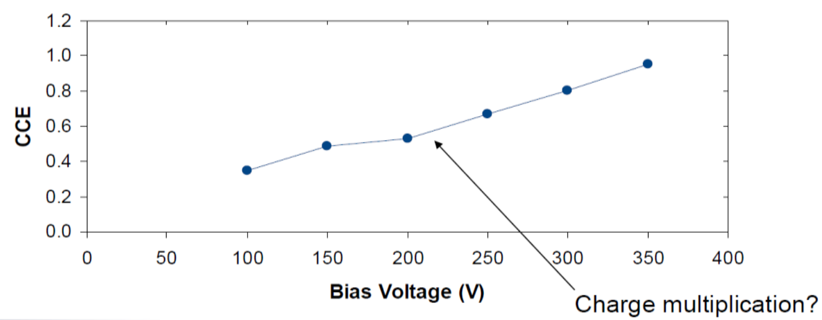
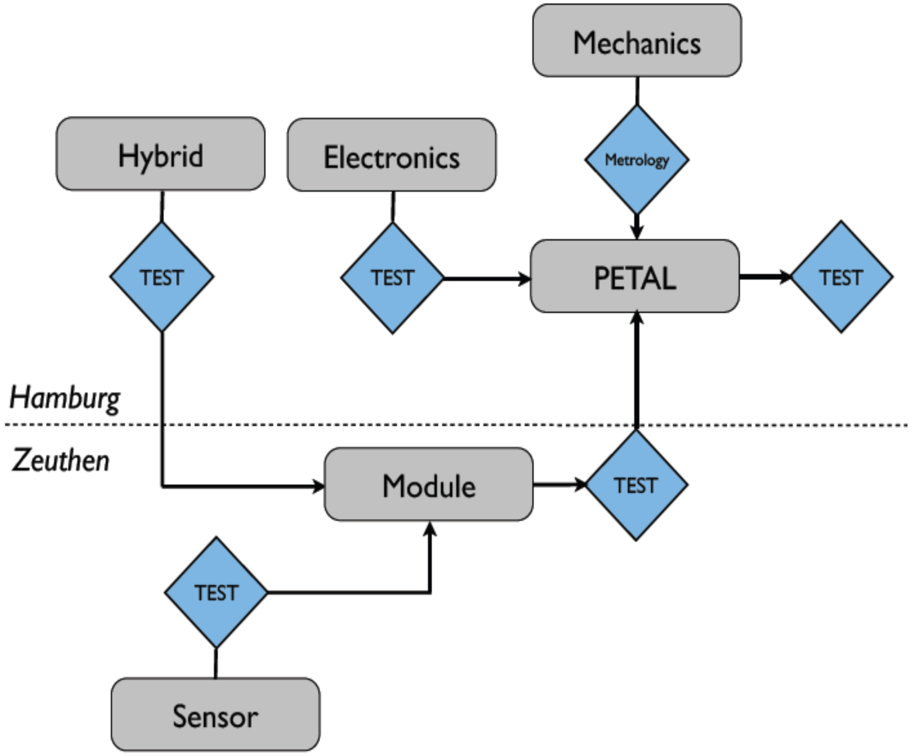
CCE with increasing bias voltage

Detector response after a fluence of 1 x 10^{16} 1 MeV n_{eq} cm^{-2}



Charge multiplication?

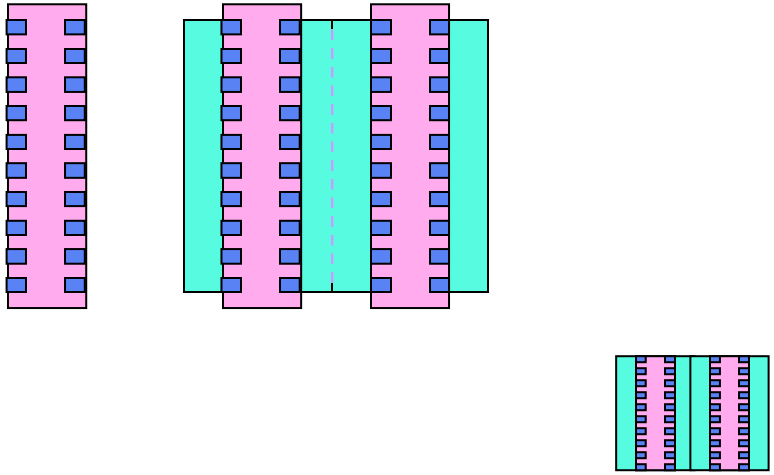
DESY: POSSIBLE INVOLVEMENT

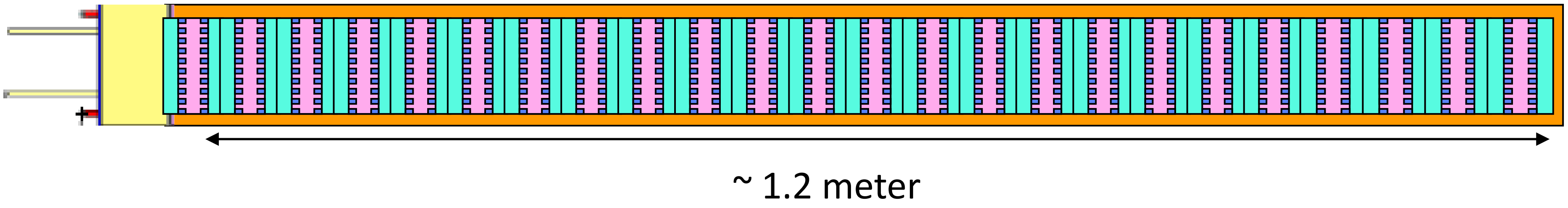


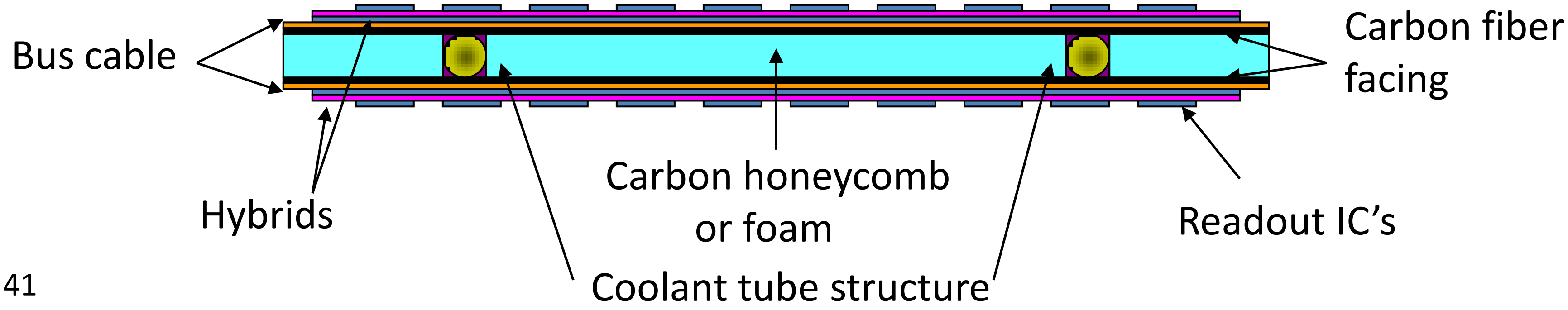
- Sensor testing
- Hybrid testing (maybe also production)
- Module production
- Development of petal electronics (e.g. SMC and/or bus tape)
- Petal mechanics: design and production support possible
- System aspects; testing

Engineering, Prototyping and Assembly

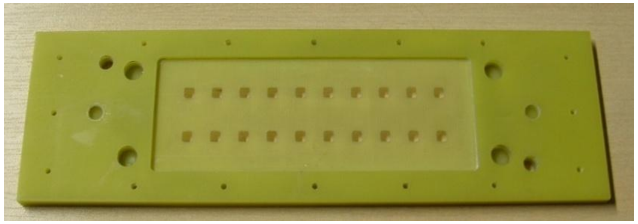
- P-type 4 segment crystals
- ABC-next
- Kapton hybrid
- Embedded bus cable
- End of stave card
- FPGA based DAQ system
- Stave mechanical core
- Assembly and measurement fixtures

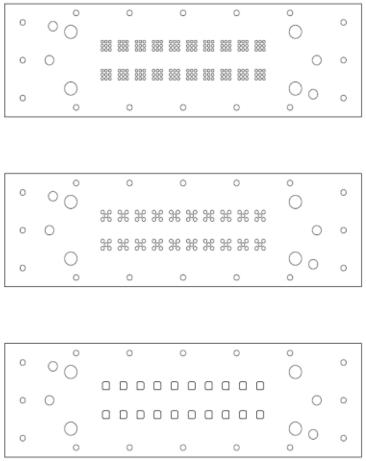




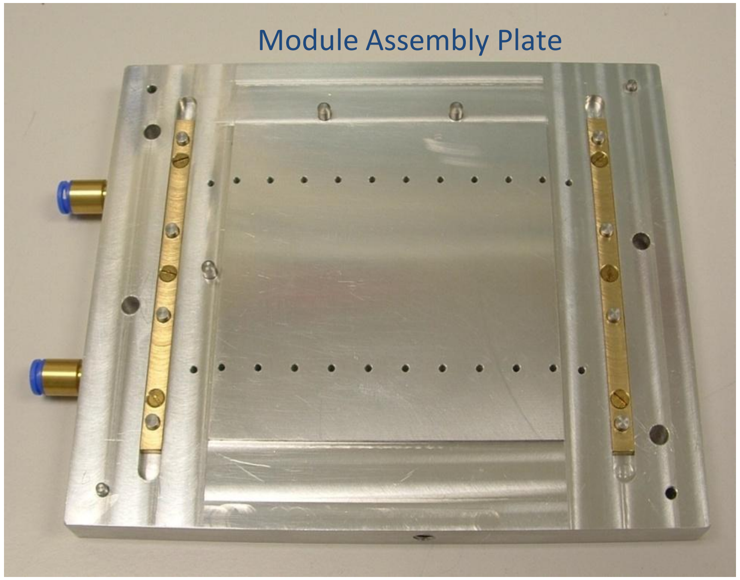


Module Construction Jigs

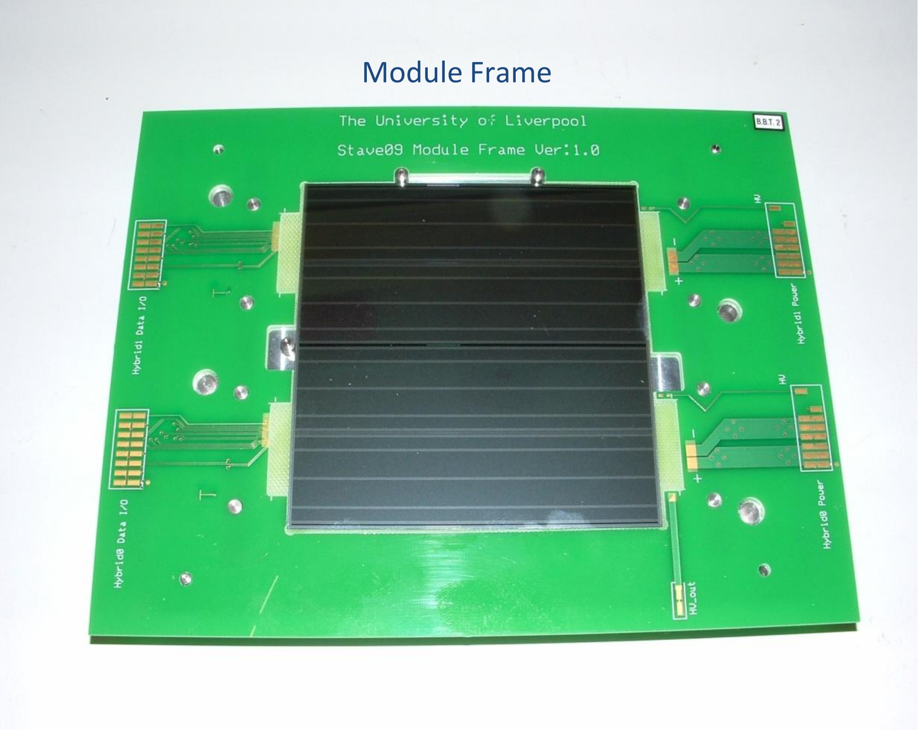




New Chip Gluing Jig



Module Assembly Plate



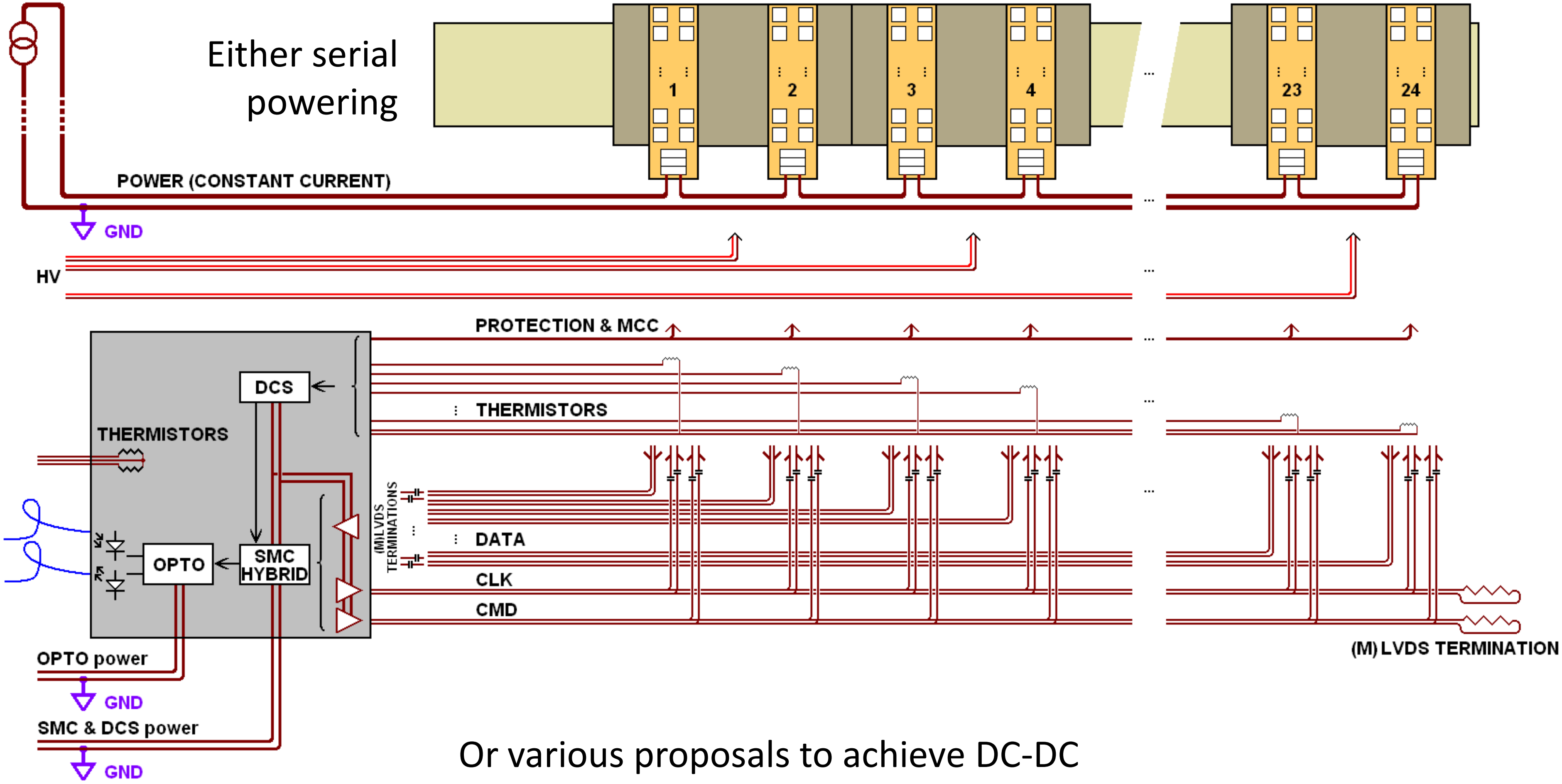
Module Frame

Module Testing Pedestal

Stave Electrical Concepts

Need to bring in power at low current and high voltage but deep sub-micron ASICs operate at lower and lower voltages

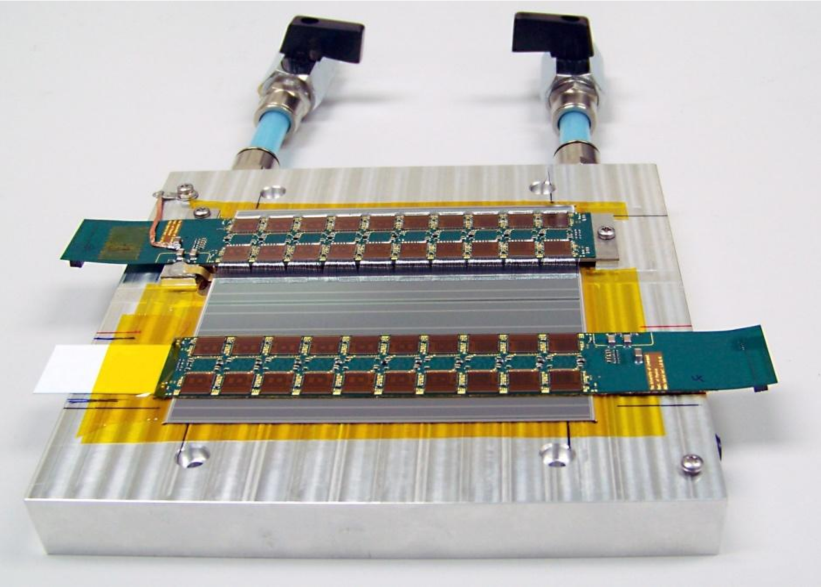
Either serial powering

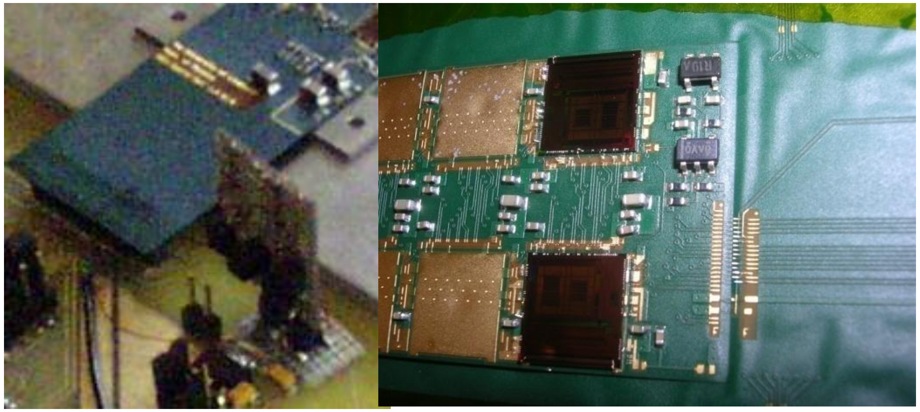


Or various proposals to achieve DC-DC conversion (Step down voltage at each module)

Studies Using Full Module

- Demonstrator used to test various international powering options
  - No show stoppers
  - New understanding in shielding needs



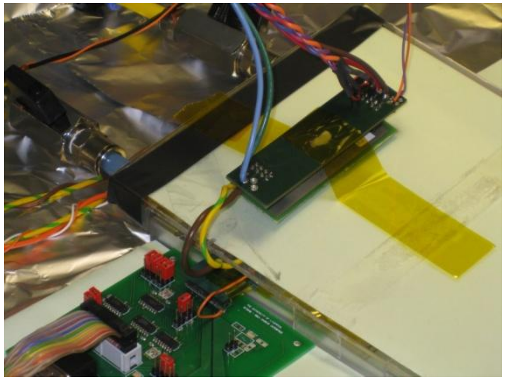


Serial Powering (RAL/BNL)

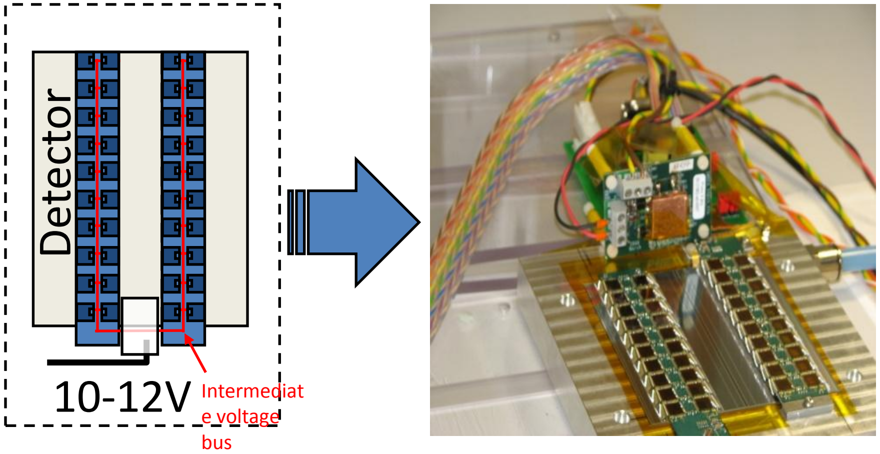
Shield 20 µm Al Foil

Sensor 1 cm from Coil

Noise
NO change with
Plug in card
on top



DC-DC (Yale)

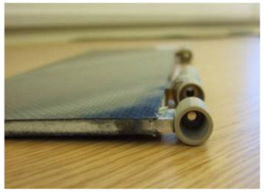


DC-DC (CERN)

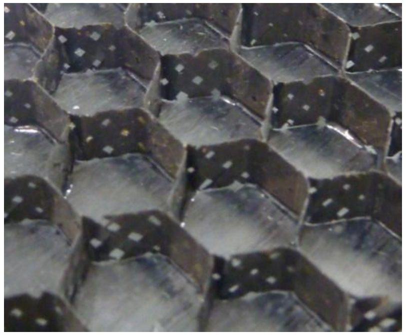
Stave Prototyping and Assembly Studies

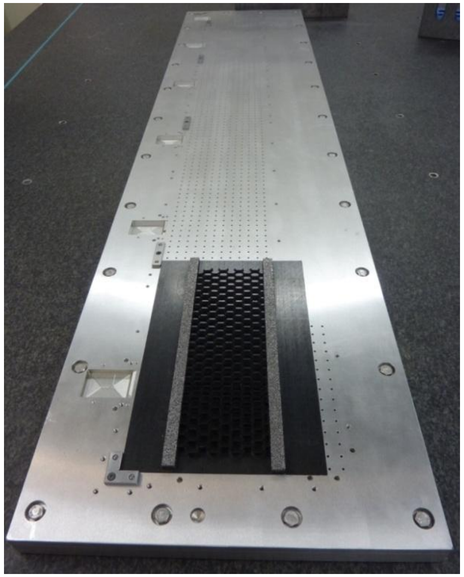
Insertion mechanism

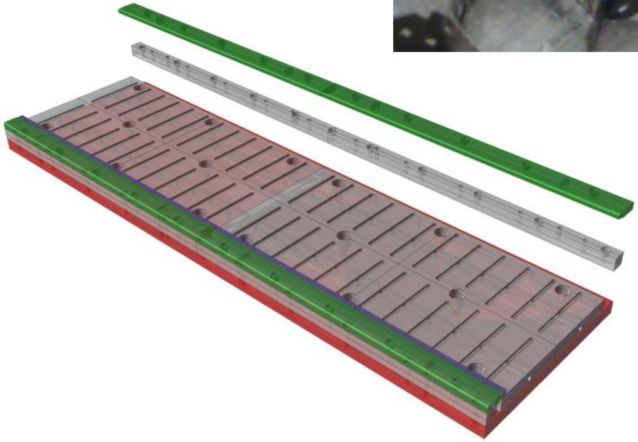
- Small section prototype complete
- Tested and fully working
- Efforts are underway to remove the long guide tube to drive down material (presently the largest constituent)



- A lot of work is underway understanding thermal performance of stave, specifically comparing hard bonded pipe to Pocofoam vs CGL
- This is being done with a CO2 cooling system and thermal imaging
- Naturally this requires a goods understanding of the build technique, so this is very well controlled
  - Glue layers are of particular interest in this as the performance is contingent upon this



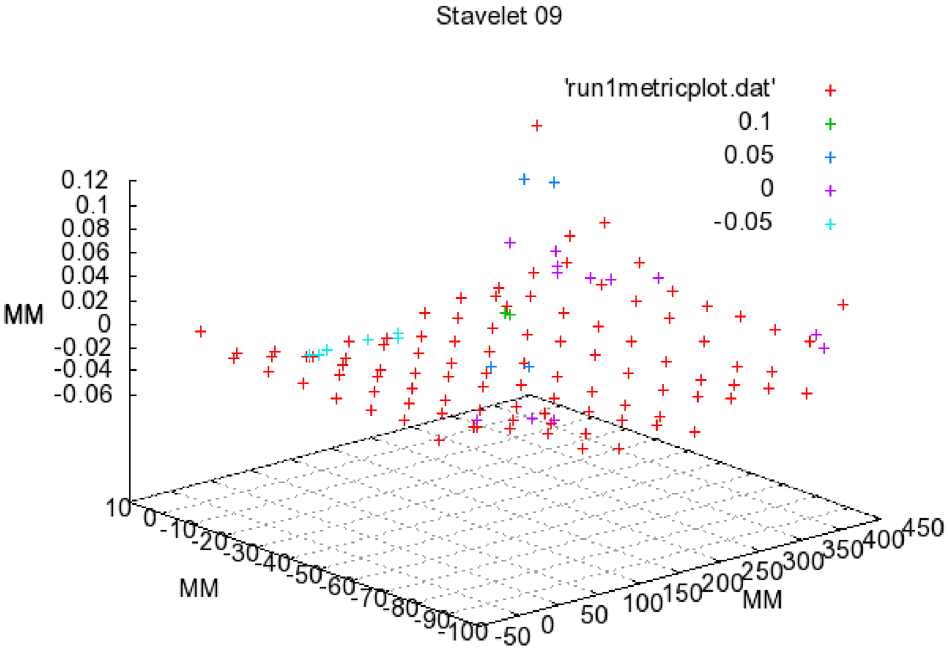




Stavelet09 Core Assembly

Core prior to 2nd facing

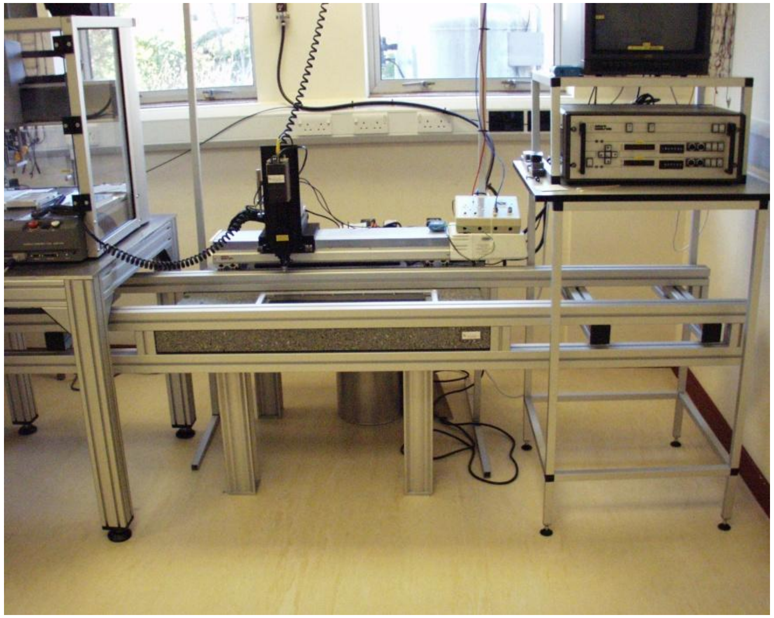
- Assembly of first core is complete.
- Deliver to BNL 19th January 2010

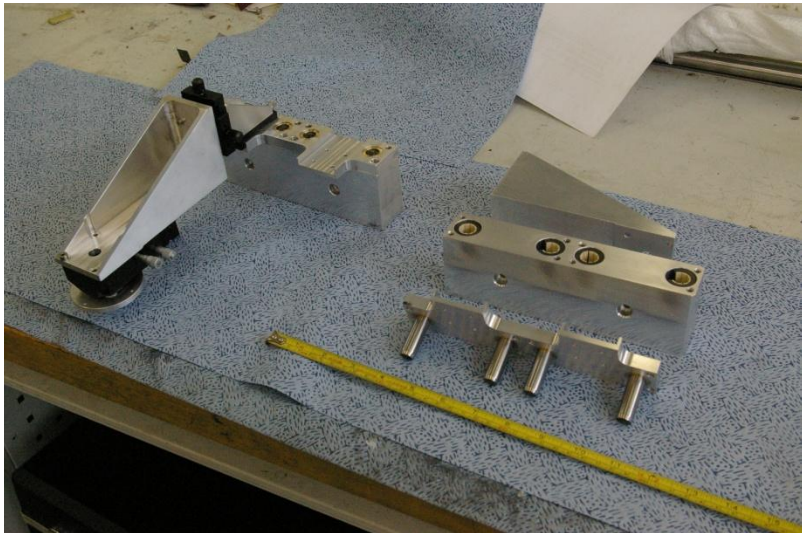


Completed core on OGP for survey

Module to Stave Assembly Hardware

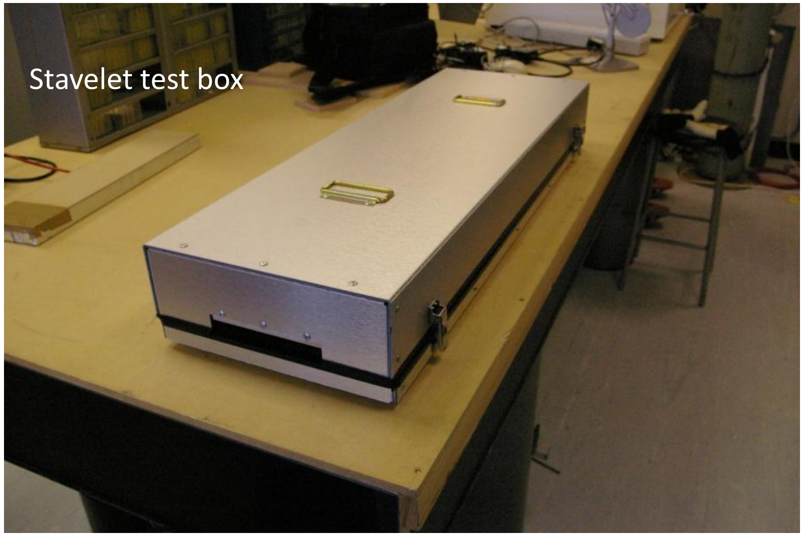
Frame mounted around the granite



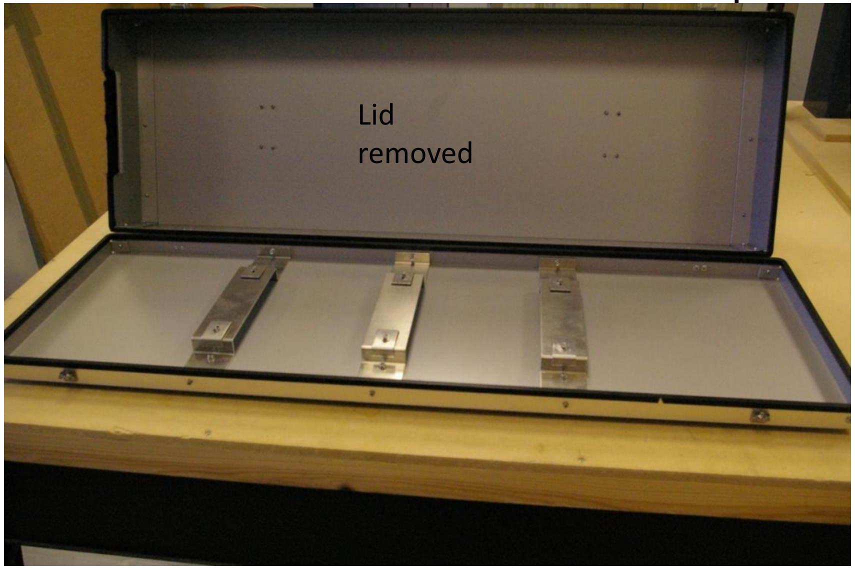


General shot of the positioning stages

2 compete kits made in case we need to work on a stave and a stavelet in parallel

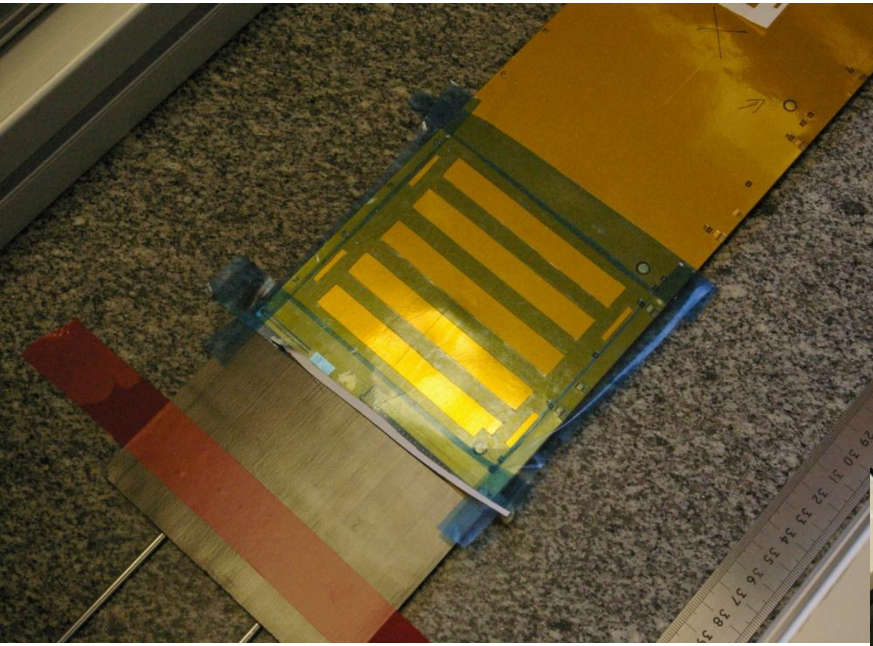


Stavelet test box



Lid removed

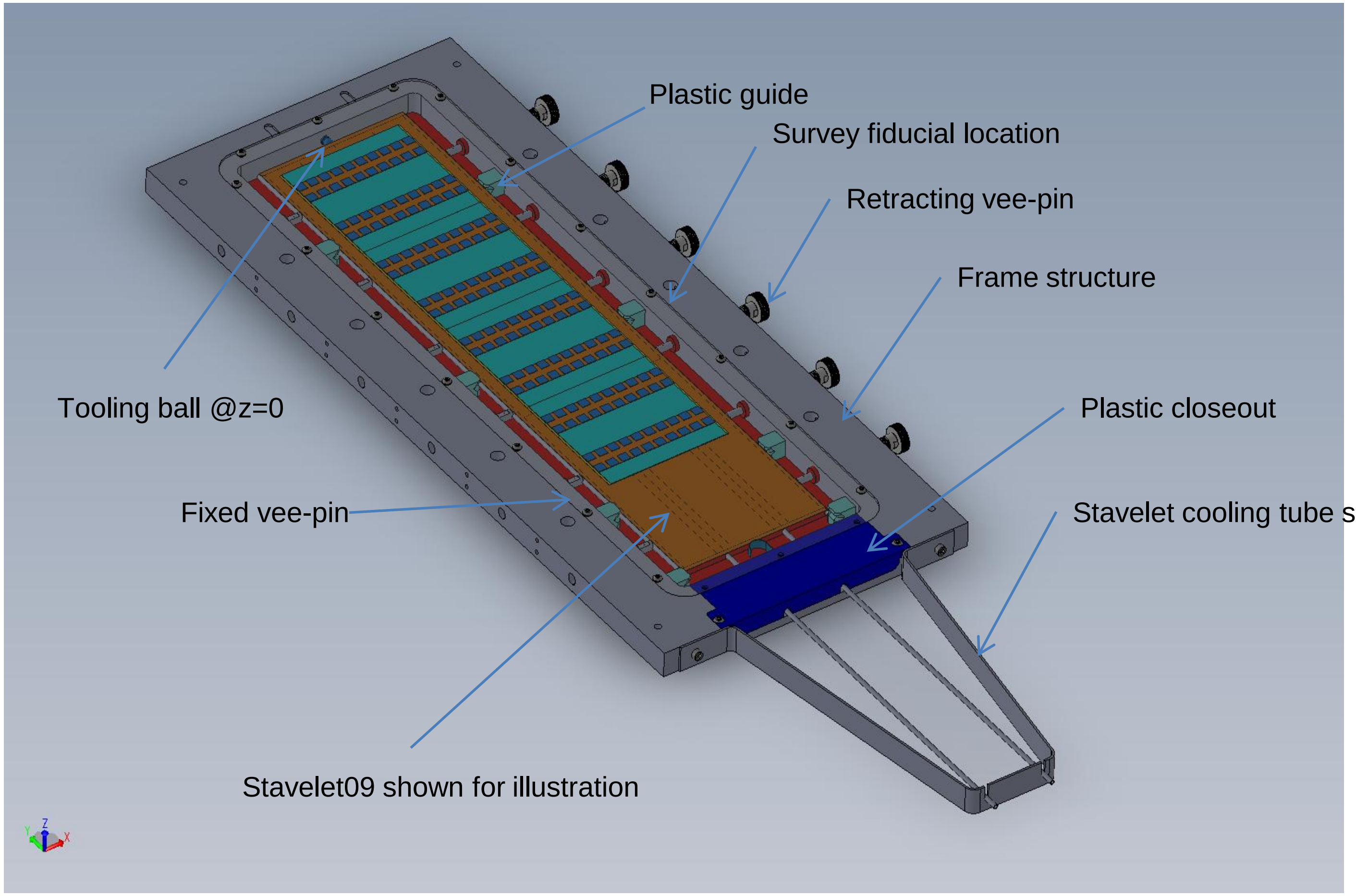
Module to Stave Gluing Trials



Now try on real stavelet with real kapton.
Kapton stuck with 3M photomount.
Mask also now includes areas for the
hybrid support spacer

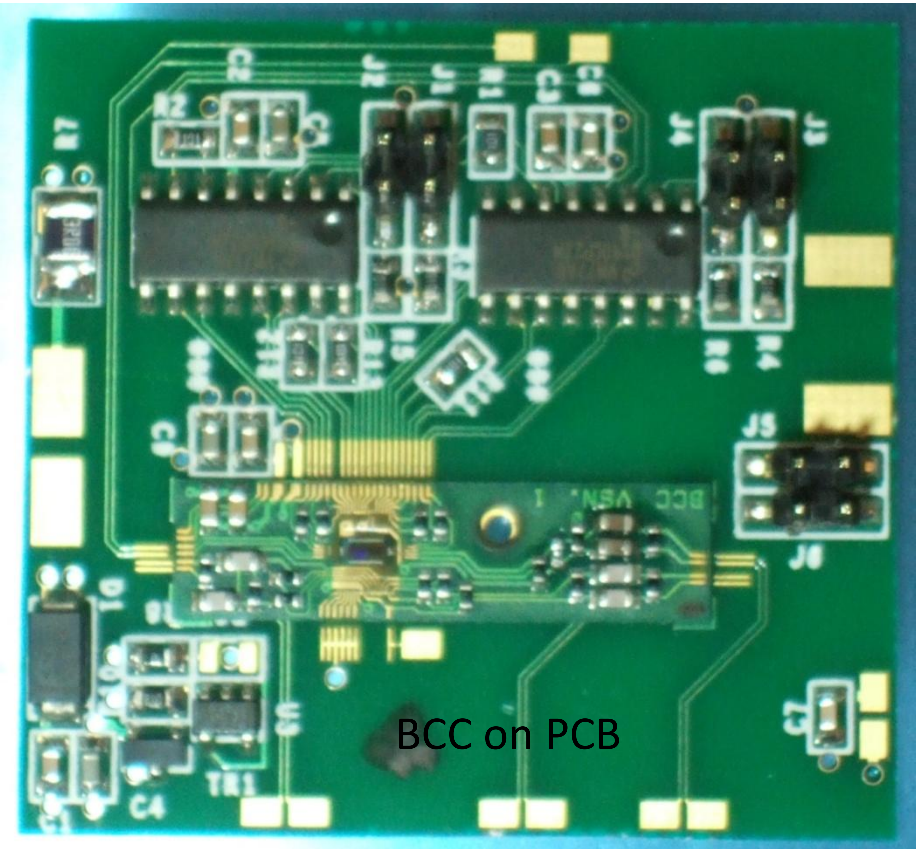
Adhesive being applied

Solid Model of Stavelet-09 Frame



Electrical Preparations for Full Length Stave

- Need to check data transmission for stave09 using BCC (prototype of Module Controller Chip, MCC).
  - Point to point data links
  - Multi-drop TTC: send TTC data to all 24 hybrids.
- BCC ASIC mounted on daughter/mother PCB bonded out to bus tape
- First bit error rate test (BERT) results encouraging BER $< 10^{-12}$.



BCC on PCB