Column-Parallel CCD Vertex Detector for TESLA: Driver Issues

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13 January 2000

I try in this note to summarise and update the back-of-envelope calculations that have so far had to substitute for real simulations.

We have set as a somewhat arbitrary goal a vertical clocking rate of 50 MHz. Since doing so, the inner CCDs have doubled in length, making the goal harder to reach in terms of driver requirements, and also less satisfactory as regards background suppression (readout time is doubled). Nevertheless, until we have some serious simulations, it seems reasonable to preserve this goal and see where it leads us.

1. Detector Background

For layer 1 we now have a CCD length of 10 cm, so a readout time (reading from both ends) of

$$\frac{100 \times 50 \times 20}{2} \text{ ns}$$

$$= 50\ \mu\text{s}$$

For the 500 GeV TESLA design this implies an accumulated background from 148 bunch crossings (bunch crossing interval 337 ns). For the X-band machine, we accumulate through the full train of 95 bunches (recently updated figure). TESLA produces bunches at an average frequency of 14.1 KHz, and the X-band at 11.4 KHz, so (other things being equal) we are still closely equivalent between the X-band and TESLA designs, as regards detector background.

2. Signal Processing

Assuming we can deposit the signals on the output node at 20 ns intervals, we can either (analogously to previous detectors) operate a reset on a once-per frame basis, or (as previously discussed) operate with a load resistance of ~ 100 MΩ and no resets. In either case, we need for each column an ADC operating at 50 MHz and digital logic (S_N - S_{N-1}) to recognise those pixels which contain signal charge. Further details of the clustering logic are being considered by Tony Gillman. The recent push by Instrumentation Division to extend their work to ASIC design at and below 0.25 μm CMOS makes the readout chip begin to look like a quite feasible concept.

3. Driver Requirements

See Fig 1. We assume driver FETs mounted at each end of the layer-1 ladder. These will themselves require high-current pre-driver pulses to their gates, but we assume these can be supplied from the local electronics outside the cryostat. This is one of many areas needing study.

For a 2- or 3-phase CCD, this circuit is repeated 2 or 3 times respectively. In either case, the low / high switching of one phase is always mirrored by a high / low switching of another (see Fig 2). Thus the local storage capacitor C_H requires a slow recharge averaging q per

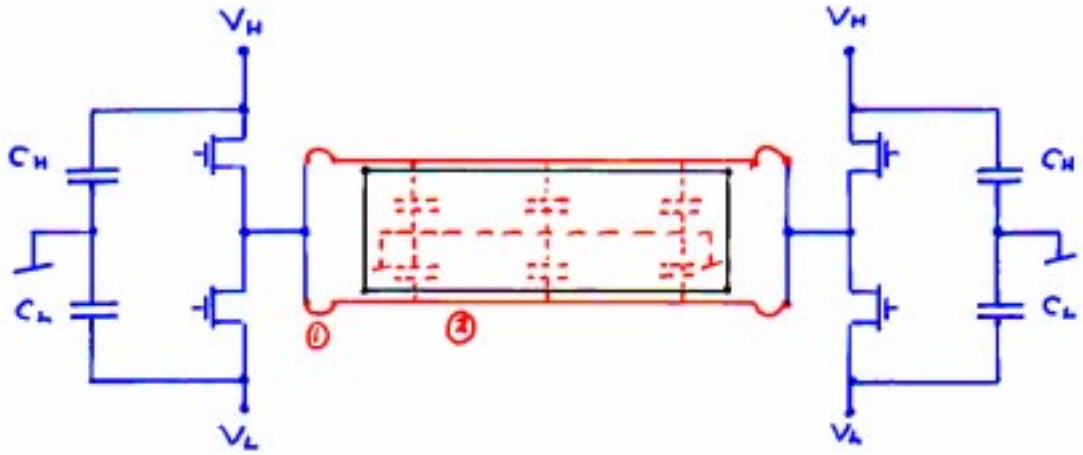

Fig 1 Inner Drivers For Layer-1 Ladders (1 Of 2 or 3 Phases)

cycle, while C_L requires a slow discharge averaging q per cycle. Very similar currents flow in at V_H and out at V_L to achieve this; the net current flow to ground is negligible.

The I gate capacitances simulated by Steve Bowring at EEV, which agreed closely with the experimental values for the CCD32 device used in the SLD detector, are as follows:

Active area 80×16 mm^2
Pixel size 20×20 μm^2

Capacitance to substrate 40 nF) per phase
Inter-gate capacitance 6 nF)

Nominal gate overlap = 0.5 μm

This implies 6.2 pF/cm to substrate
0.94 pF/cm interphase

Depletion depth ~ 4 μm with standard bias.

Given the possibility (following SONY) of removing the gate overlaps, and the possibility of using a greater depletion depth (say 40 μm) both these capacitance figures can surely be reduced. However, at some point the capacitance to substrate will be dominated by coupling to the channel stops. Until we have working simulations, it may be a reasonable guess to disregard the relatively small interphase capacitance but to provisionally leave the capacitance to substrate at the above value.

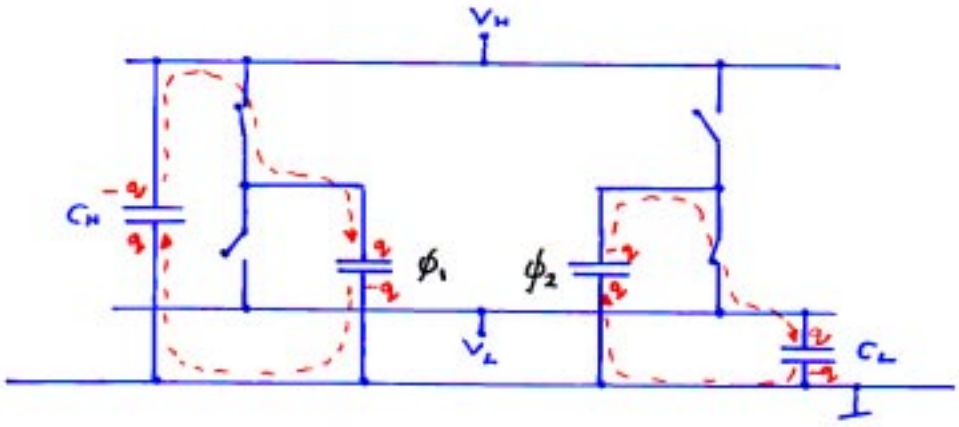

FIG 2 SYMMETRICAL SWITCHING OF 2 OR 3 PHASES, INDUCING EQUAL & OPPOSITE SUPPLY CURRENTS FROM V_H & V_L & NEGLIGIBLE CURRENT IN GROUND LINE.

For the TESLA layer-1 ladders, this leads to 38 nF / phase to substrate.

I hope that the drive pulse risetime may be limited by the FET channel resistance R_{CH}. This assumes that the bond inductances and on-CCD drive bus line resistances can be adequately reduced, which may be challenging.

For a 2-phase system running at 50 MHz, we need a drive pulse risetime (10-90%) of about 8 ns.

$$\text{So we need } RC = \frac{8 \text{ ns}}{2.2} = 3.6 \text{ ns}$$
$$\text{hence } R = 0.095\ \Omega$$

We can drive synchronously from both ends of the ladder, so need $R_{CH} = 0.19\ \Omega$. Whether this is feasible, or whether we can reduce the gate capacitance enough to make this risetime feasible, remains to be seen. Richard Stephenson found some very interesting specs for Motorola TMOS power FETs with drain-source on-resistence as low as 160 m Ω at room temperature (and 60 mΩ at 220 K). These would be even better than needed, but their input capacitance (1.2 nF) is too high for remote drive. There must be room here for a customised driver FET design. In the worst case, slower clocking results in higher background, but not necessarily unacceptable background, as seen from the SLD experience.

4. Power Dissipation

Assuming adequate in-cryostat storage capacitance C_H, C_L, the only power dissipation to be considered comes from the resistive FET channel and on-CCD bus lines. The drive voltages are restored on C_H and C_L via resistance external to the cryostat, during the period between bunch trains.

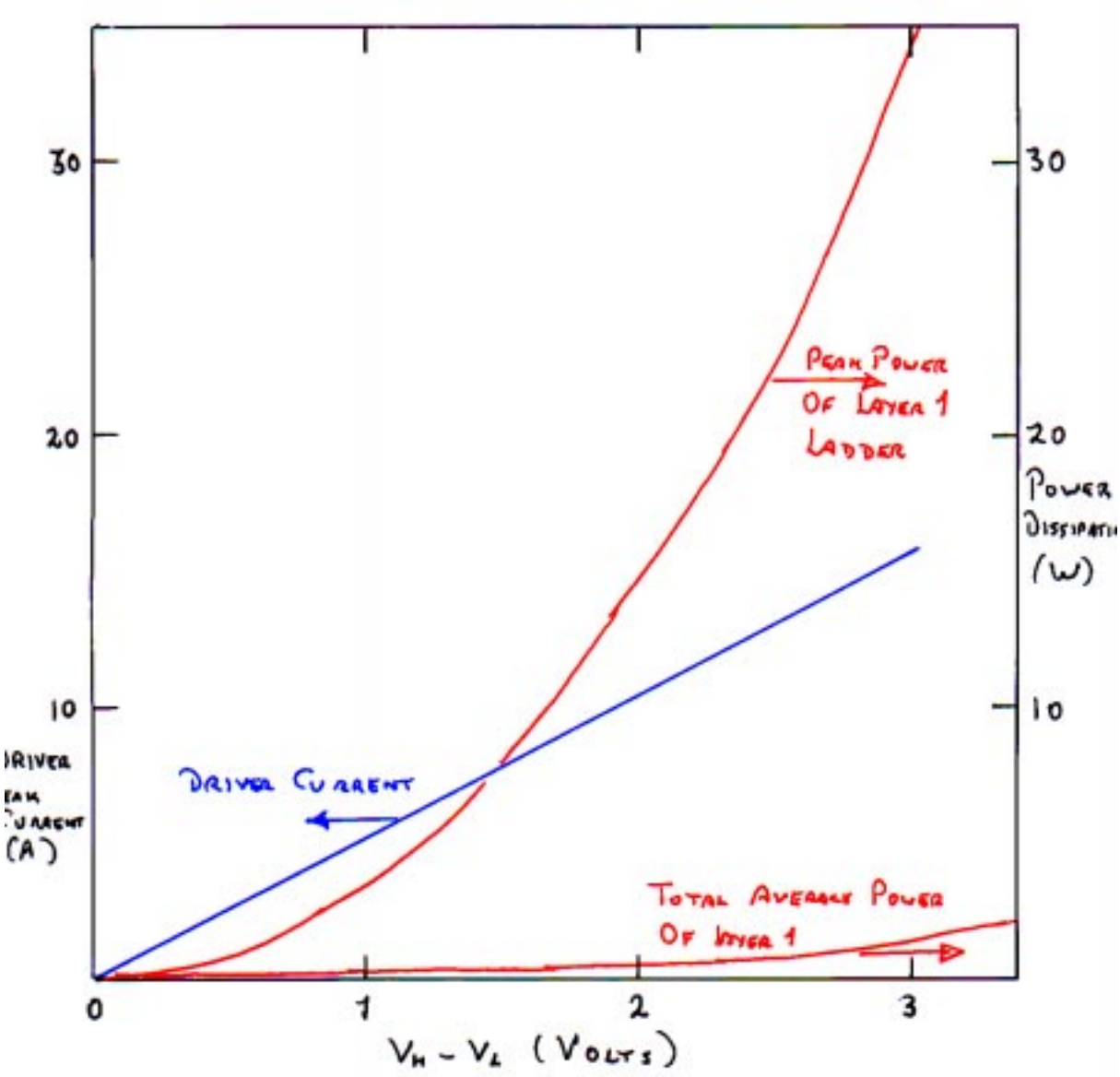

FIG 3: DRIVER CURRENT & POWER DISSIPATION IN LAYER 1 LADDERS

The energy dissipated when a single phase changes level

$$= \int I^2 R \, dt$$

where $I = I_0 e^{-t/RC}$

$$= \frac{I_0^2 R.RC}{2} = \tfrac{1}{2} C \left(V_H - V_L\right)^2$$

Per pixel shift, for a 2-phase register, we have overall energy dissipation

$$2C\left(V_H - V_L\right)^2$$

For a clocking frequency of f_{CL}, the in-cryostat power dissipation while clocking is thus

$$2C\left(V_H - V_L\right)^2 \times f_{CL} \text{ per CCD}$$

The peak current from any driver is $\left(\frac{V_H - V_L}{R_{CH}}\right)$

The average power is reduced by the TESLA duty cycle

$$\frac{950\mu\text{s}}{200\text{ ms}} = 4.75\times10^{-3}$$

The average power dissipated in layer 1 is 8 times higher (8 ladders or CCDs in layer 1).

These results are plotted in Fig 3. For a reasonable clock drive voltage of 2 V, we have quite high peak power on a ladder (15 W) but the average power on layer 1 is only 0.6 W.

For the outer layers, clocking rates can be substantially reduced, so they need not contribute more power dissipation than layer 1, despite the increased detector area.

Such a detector will be perfectly OK for gas cooled operation as in SLD.

5. Conclusions

One of the keys to the column-parallel operation, from the viewpoint of the CCD and driver, appears to be the achievement of a sufficiently low resistance driver circuit. This is needed in order to achieve the desired clocking rate, and it carries the advantage relative to the 'forced' drive considered previously of completely acceptable power dissipation.

[Forced drive meant switching between voltage $V_H' < V_H$ and $V_L' > V_L$, which could in principle permit clocking with period < RC. This could however lead to dangerously high in-cryostat power dissipation.]

While these conclusions are highly preliminary, it is hoped that they may at least encourage serious simulations of the overall CCD and driver system. Issues such as the inductances of bond connections or skin effect on bus lines could be very important, not to mention a serious understanding of the evolution in parameters of real driver FETs, and the evolution in gate design and voltage requirements of real CCDs.