A Fast CCD Vertex Detector for the Future e^+e^- Linear Collider: Some Recent Developments

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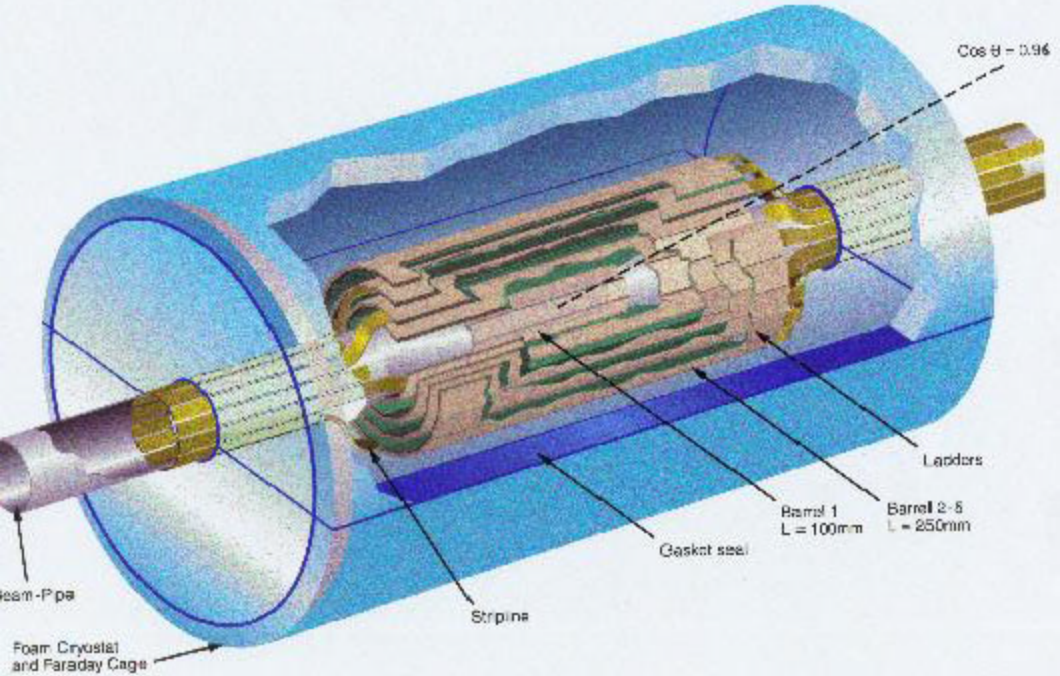
on behalf of
The LCFI Collaboration

Outline

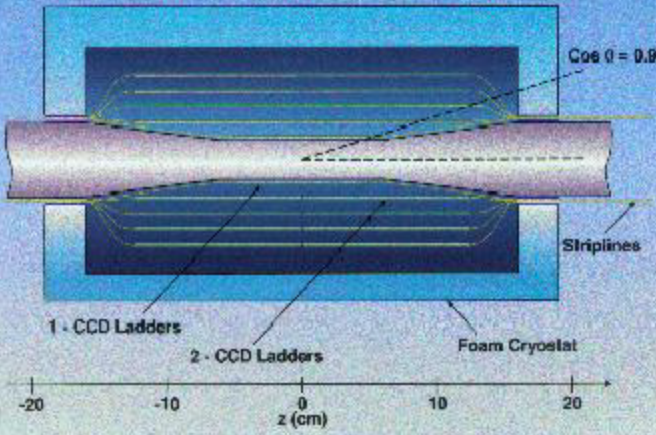
- *Introduction*
- *Overview of the NLC/TESLA vertex detector design*
- *Status of the current R&D programme*
- *The column-parallel CCD — a novel readout architecture to meet the TESLA challenge*
- *Conclusions*

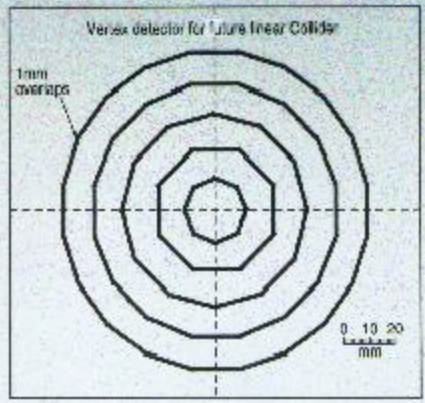
Introduction

- CCDs are ideal candidates for vertex detectors in the linear collider environment
- In SLD they have already demonstrated *(with 1990s technology)*:
  - Excellent 2-d space-point resolution ~3.5μm
  - Very small layer thickness (0.4% X_0 in SLD) → low multiple scattering
  - Serial readout multiplexes data by 200,000:1 → negligible signal cable plant
- Si-processing technology is still advancing rapidly:
  - → Faster clocking
  - → Improved signal/noise performance
  - → Larger area devices
- A conceptual design for a CCD-based VXD for the future linear collider has already been presented


Cos θ = 0.96
Ladders
Barrel 1
L = 100mm
Barrel 2-5
L = 250mm
Gasket seal
Stripline
Foam Cryostat
and Faraday Cage

CCD VXD for the Future Linear Collider





Detector performance targets

- 5-barrel construction to provide redundant stand-alone tracking
- Inner barrel (B1): radius 15 mm — length 100 mm
- 3-hit acceptance *(including B1)* to $\cos \Theta = 0.96$
- Individual layer thickness $0.06\% X_0$
- Dimensions of largest CCD $125 \times 22\ mm^2$
- Pixel readout rate 50 MHz

Current R&D programme

- *Initially (first 3 years) focussed on 3 main areas:*
  - High-speed CCD clocking — up to 50 MHz
  - Techniques for low-mass ladder assemblies
  - Neutron irradiation studies
- *At a later stage:*
  - Real-time signal processing *(min-I cluster-finding)* using fast FPGA-based algorithms
  - Customised CCD design:
    - column-parallel architectures
    - two-phase gate structures
    - low-noise output circuitry
  - Electronic system design:
    - clocking and signal processing electronics integrated with CCDs

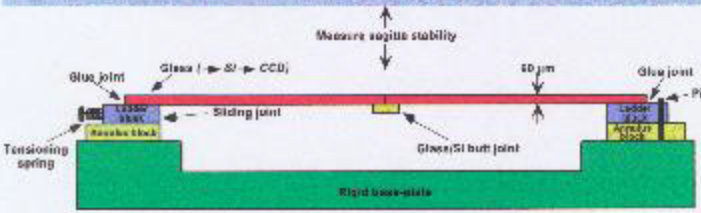
Mechanical studies

- Minimal layer thickness is crucial for precision vertexing *(multiple scattering)*
- Early studies assumed thin CCDs mounted *on one side only* of a thin Be substrate strengthened by Ω or V beam technique *(total thickness ~250 μm)*:

- The CCDs would be thinned to the edge of the epitaxial layer by lapping and etching — ~30 μm
- This would give ~0.12% X_0 per layer — of which the Be and associated adhesive contributes 0.09% X_0
- Could the Be support structure be eliminated?
- We are investigating an unsupported-Si technique

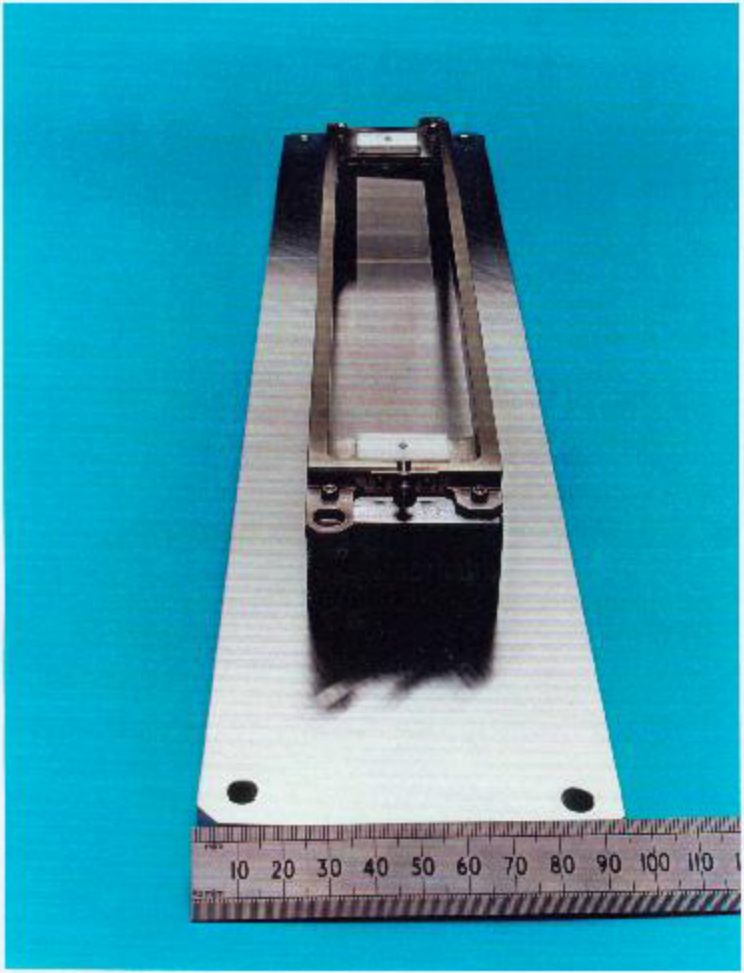
Substrate-free mechanics

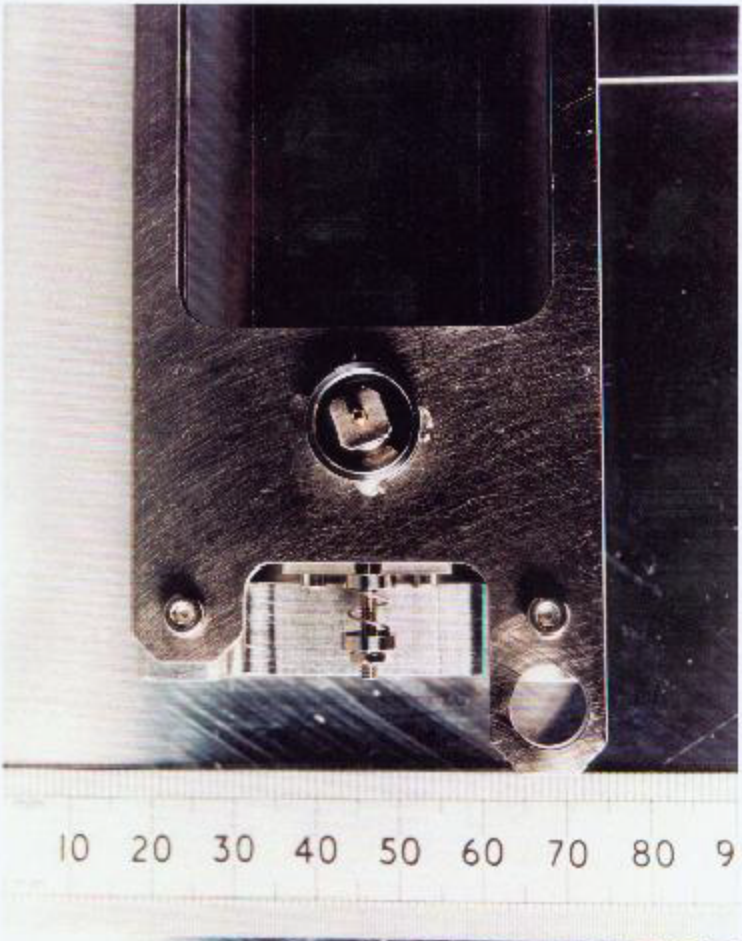
- Idea is to hold the thinned CCDs only at their ends and to give them rigidity by spring-tensioning them
- Use sliding V & flat ceramic block pairs *(spring-compressed)* for attachment — technique well-proven in SLD VXD3



Test-rig for substrate-free CCD structure

- *Potential problems:*
  - Profile repeatability under temperature-cycling
  - Electrical connections to CCDs
  - Back-face metallisation for ground-plane difficult
  - Handling!


10 20 30 40 50 60 70 80 90 100 110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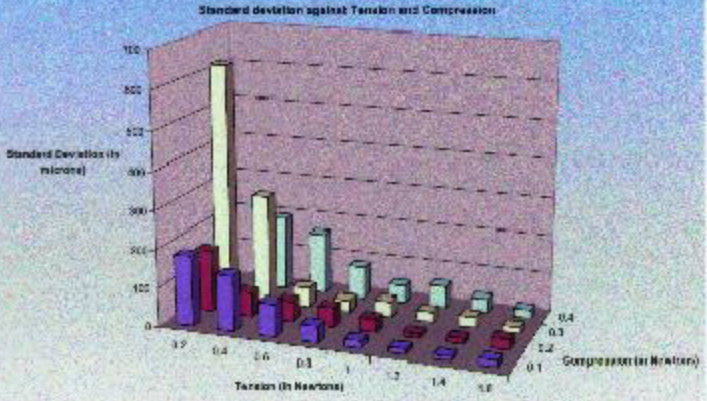
S/S-free mechanics — initial results ...

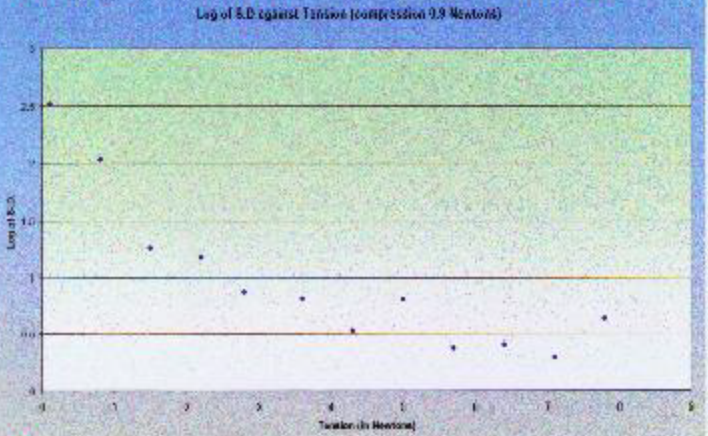
- Sagitta value measured 20 times for each combination of spring compression and tension, physically disturbing system between measurements



- *Comments:*
  - Tensioning spring too weak → σ ~few tens of μm

S/S-free mechanics — initial results ...

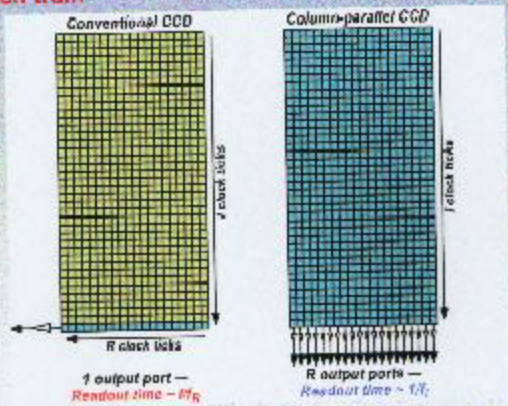
- Stronger tensioning spring reduces σ dramatically



- *(Tentative) conclusions:*
  - The technique appears to work — σ → ~3 μm for spring tension >5 N
  - The annulus blocks could be made from better surface-finish ceramic
  - More studies are needed, particularly at low-T ...
- Further idea — could the Be beam-pipe thickness be reduced locally ... to 250 μm?
  - use VXD support shell for strain relief

Column-parallel CCD architecture

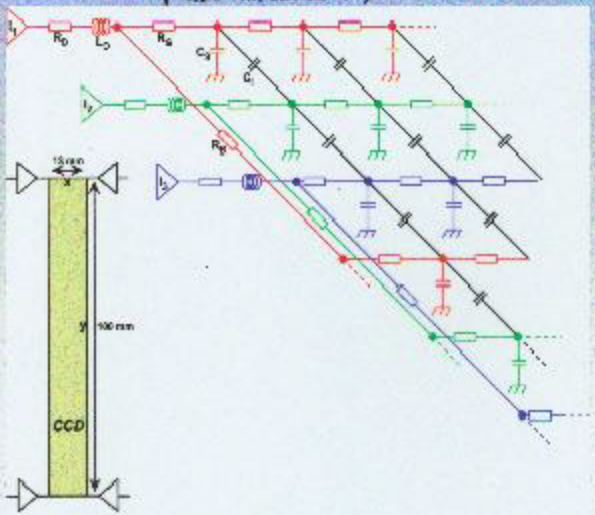
- In X-band LC, B1 CCDs *(r = 12 mm)* must be fully read out between bunch trains *(8.3 mS)* → 50 MHz clocking
- 100 bunches/train generates ~10 hits/mm^2 per CCD from e^+e^- pair background *(3T field)* → ~0.4% pixel occupancy
- In TESLA, read-out *between* bunch trains would integrate ~2800 bunches → ~20% pixel occupancy
- Solution — increase *effective* clocking rate to >1 GHz by eliminating CCD serial *(R)* register and read out *during* bunch train



- Consider area CCD as many linear CCDs reading out in parallel → 50 MHz clock rate for ~1% pixel occupancy
- This provides a few interesting technical challenges ...

Column-parallel CCD clocking

- Can the CCD I-gates be clocked at 50 MHz with good drive waveforms across entire imaging area — essential for good charge transfer efficiency?
- Is the resultant in-cryostat power dissipation too high to be managed with modest cold gas flow rates?
- We have modelled a realistic inner-layer CCD with SPICE, using "Marconi-approved" parameters:
  ("hot unreasonable")



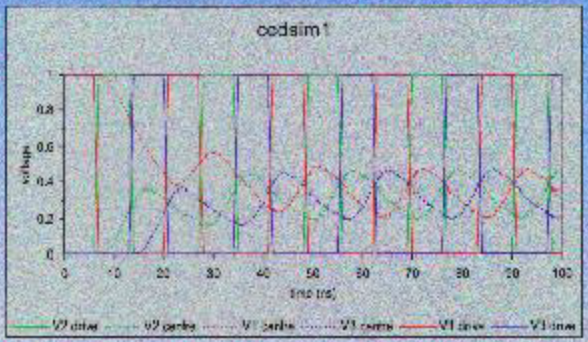
SPICE model of column-parallel CCD gate structure (VXD layer 1 dimensions)

Column-parallel CCD clocking

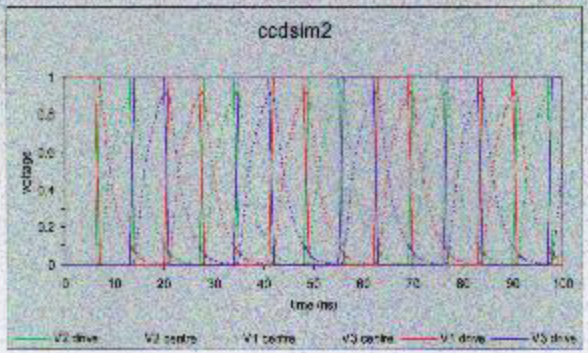
- We initially assumed the following parameters:
  - 1 V-swing square-wave clocks (t_{rf} = 1 nS) — 50 MHz
  - I-gate → substrate capacitance *(buried-channel and channel stop regions depleted)* — 3.3 pF/mm^2
  - Inter-gate capacitance — 2.5 pF/mm^2
  - Polysilicon gate resistance — 3 KΩ/mm
  - Al clock bus-line resistance *(200 K)* — 0.5 Ω /mm
  - Driver output impedance — *negligible*
  - Driver → clock bus-line inductance — *negligible*
- We later modified some of these parameters appropriately to attempt improvements to simulated waveforms
- Starting with these nominal parameters we monitor waveforms at extreme points on the gate structure

Column-parallel CCD clocking

a) **Drive waveform variation across the CCD in X:**



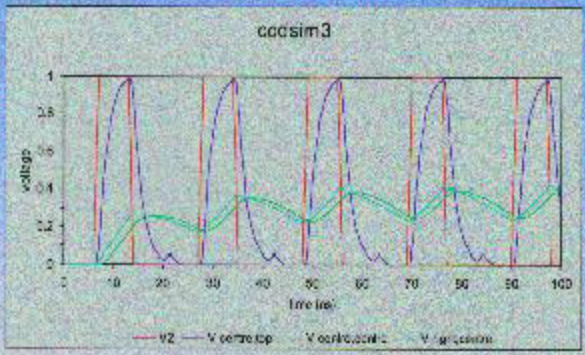
- **Add 3 μm wide Al overlay to the polysilicon gates —**



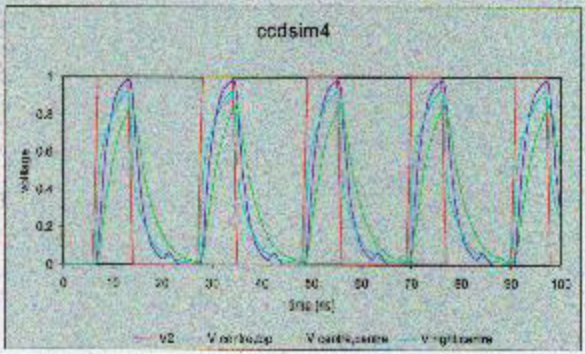
- **Waveform amplitudes attenuated by <10% in centre *(X)***

Column-parallel CCD clocking

b) Drive waveform variation along the CCD in Y:



- **Thicken the Al bus-lines from 1 μm → 10 μm —**



- **Waveform amplitudes attenuated by <15% in centre *(Y)***

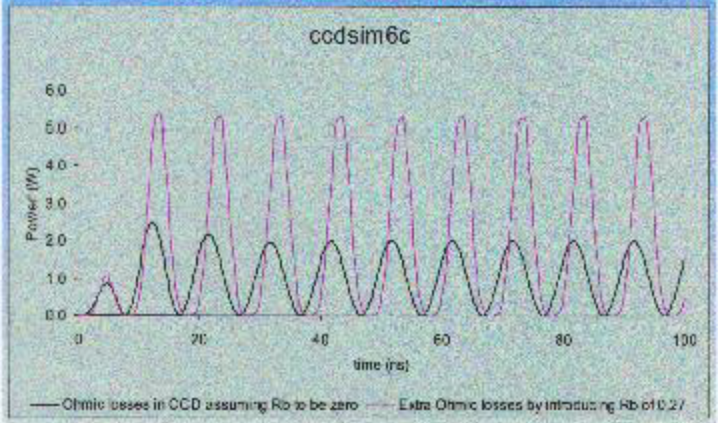
Column-parallel CCD clocking

c) Move to a 2-phase gate structure with sinusoidal drive waveforms *(scale all parameters accordingly and add inductance in the clock driver connection)*:

- *Advantages:*
  - Lowest possible driver frequency spectrum
  - Reduced peak current demands on drivers
  - Balanced anti-phase drive waveforms should produce minimal crosstalk to CCD output signals

Column-parallel CCD clocking

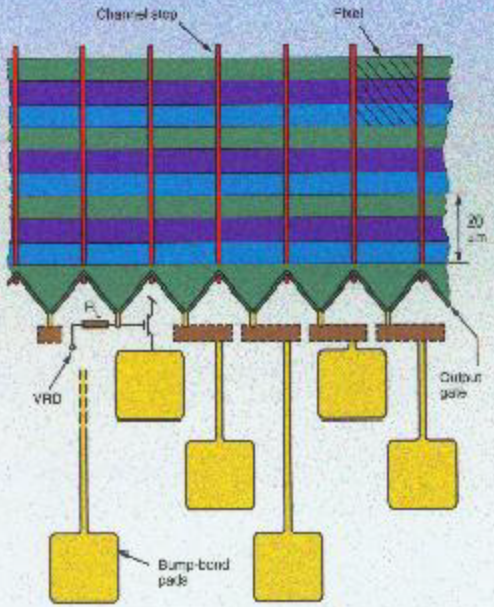
d) Clocking power dissipation *(resistive)* per CCD:



- **Total power dissipation/CCD ~3.6 W *(1 V p-p clocks)***
- ***N.B. Freezing clocking between TESLA bunch trains reduces power dissipation by a further factor of 200***
- **For layer 1 of the VXD — mean P_D <150 mW**
- **CCDs in outer layers can be clocked at a lower frequency (*much smaller backgrounds*) —**
  → Total VXD power dissipation ~few watts
- **Further simulation work needed *(ISE TCAD)***

Column-parallel CCD signal-handling

- Simplify reset circuit — passive with resistive load
- Signal-processing *(digitisation, real-time cluster-finding)* performed adjacent to CCD — in local readout chip
- 1-d row of staggered bump bonds *(industry-standard)* interconnects CCD and readout chip — 60 μm pitch
- Sparsified data transmitted off detector by optical fibre(s)



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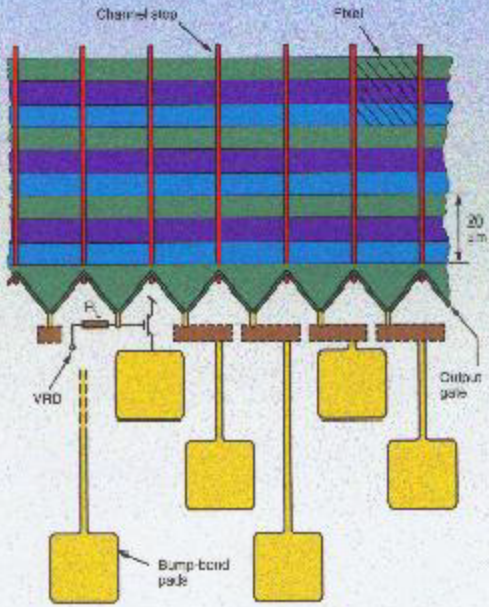
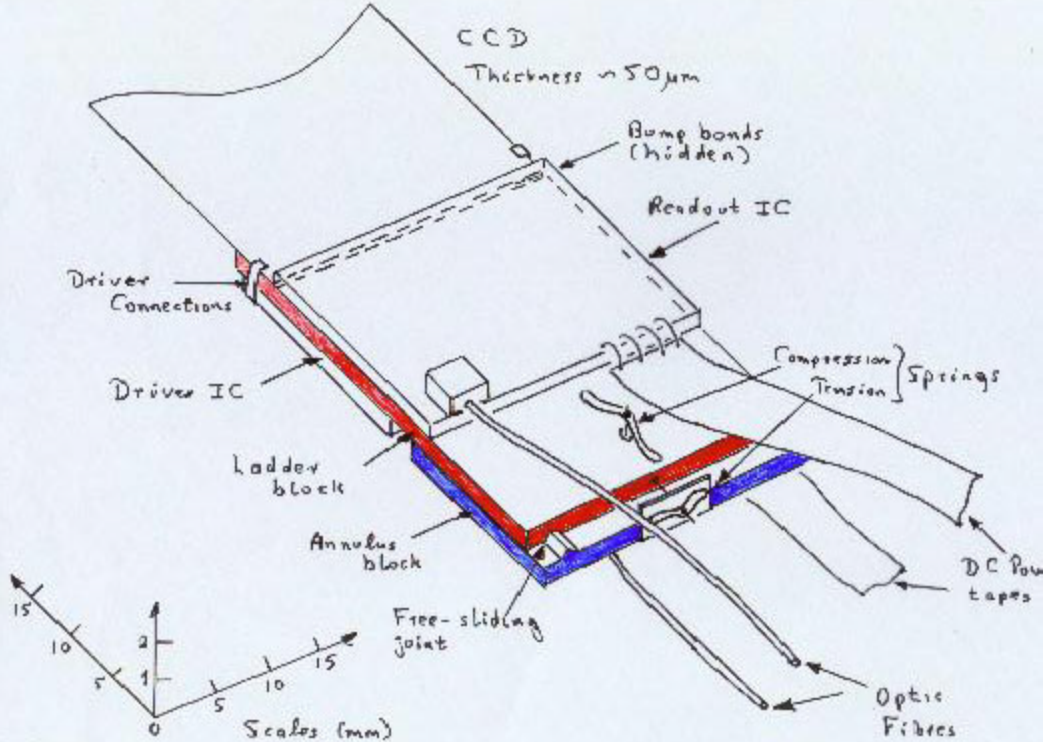
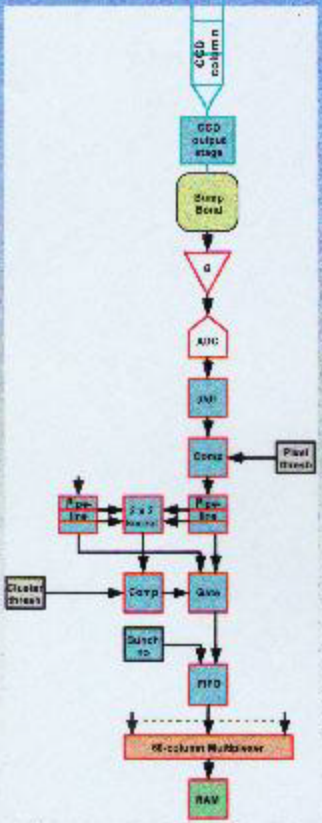



CCD
Thickness ~ 50μm
Bump bonds (hidden)
Readout IC
Driver Connections
Driver IC
Compression
Tension
Springs
Ladder block
Annulus block
Free-sliding joint
DC Power tapes
Optic Fibres
15
10
5
0
5
10
15
2
1
Scales (mm)

Column-parallel CCD signal-handling

- Functionality of readout chip *(n.b. very preliminary ideas — more study needed)*:



Column-parallel CCD data rates

- Proposal is to read out the CCDs throughout the 950 μs bunch train, storing *sparsified* cluster data in local RAM
- Based on current background rate estimates for TESLA, we would expect the following *(per bunch train)*:

Layer	CCD mm²	Ladders/CCDs	Clk/T_{BC}	Hits/mm²	Σ background
1	100x13	8/8	50MHz/50μs	5.9	1165 K
2	125x22	8/16	2.5MHz/250μs	2.9	484 K
3	125x22	12/24	2.5MHz/250μs	1.1	276 K
4	125x22	16/32	2.5MHz/250μs	0.9	301 K
5	125x22	20/40	2.5MHz/250μs	0.6	251 K

- Total no of hits to store during bunch-train ~2.5 x 10^6
- Each hit can contain up to 4 pixels *(2 x 2 clusters)* and must also be address-tagged → 6 bytes/hit
- Data volume to store during bunch-train ~15 Mbytes
- On receipt of a trigger, *only data corresponding to 1 subsequent frame* from each CCD need to be retained, so data volume to be transferred off the detector before next bunch-train is reduced to ~2.1 Mbytes *per event*
- For a trigger rate <50 Hz (!), data to transmit off detector ~21 Mbytes *per bunch-train* → 1 optical fibre per end!
- *N.B. If data storage cannot be on-detector, all sparsified data must be exported* → 1 – 4 optical fibres per CCD

Conclusions

- The LCFI collaboration is pursuing an active R&D programme across a broad range of topics aimed at a CCD VXD for NLC or TESLA
- Initial results just emerging are very encouraging:
  - Substrate-free mechanics appears viable
  - Simulations show that clocking a column-parallel structure at 50 MHz is feasible — waveform integrity and power are both acceptable
- The column-parallel architecture makes CCDs fully-compatible with the TESLA environment
- There are new ideas for in-detector signal processing, data sparsification and post-trigger processing
- CCD radiation damage studies are being prepared
- A close involvement with CCD designers/manufacturers is maintained, and is crucial